NCA6416-Q100

Low-voltage translating 16-bit I²C-bus/SMBus I/O expander

Rev. 1 — 20 August 2025 Product data sheet

1. General description

The NCA6416-Q100 is a versatile 16-bit general-purpose I/O expander designed for microcontrollers that need additional I/O pins. It communicates via an I²C-bus interface, making it ideal for applications with minimal space and wiring, such as battery-powered devices using sensors, keypads, push buttons or LED control for managing LED brightness.

Nexperia's I/O expanders feature a dual power supply architecture with two inputs: V_{CCI} and V_{CCP}. This design enables seamless level translation, supporting mixed-voltage environments. V_{CCI} powers the I²C interface and must be connected to the same voltage as the host microcontroller's I²C bus (SDA/SCL), which can range from 1.65 V to 5.5 V. V_{CCP} powers the internal core and the I/O pins on Port P, defining the voltage level for the connected peripherals. This allows a low-voltage microcontroller to interface with higher-voltage peripherals without additional external circuitry.

The NCA6416-Q100 contains four pairs of 8-bit registers: Configuration, Input, Output, and Polarity Inversion. By default, all I/O pins are configured as inputs at power-on. A system controller can dynamically reconfigure these pins as inputs or outputs by writing to the Configuration register. The Input and Output registers store the current state of each pin. The Polarity Inversion register allows to invert the polarity of the input pins, which can simplify logic in system by eliminating the need for external gates.

The device has an open-drain INT output that triggers when an input pin changes state. This interrupt can be connected to a microcontroller's interrupt pin, allowing the NCA6416-Q100 to notify the host of a change without the need for constant polling over the I²C bus. This feature makes the NCA6416-Q100 an efficient and passive I²C target device. To recover from errors like I²C time-outs, a system controller can drive the $\overline{\text{RESET}}$ input low. This resets all registers to their default state and reinitializes the I²C/SMBus interface without requiring a power cycle. A hardware ADDR pin allows to program the device's I²C address, making it possible to use up to two NCA6416-Q100 devices on a single bus. In addition, each output pin on Port P can sink up to 25 mA, making it suitable for directly driving low-current loads like LEDs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- I²C-bus to parallel port expander
- Supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- Low standby current consumption:
  - 1.5 µA typical at 5 V V_{CC}
  - 1.0 µA typical at 3.3 V V_{CC}
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.25 V (typical) at 2.5 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
  - V_{hys} = 0.5 V (typical) at 5 V
- 5 V tolerant I/O ports
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- 400 kHz Fast-mode I²C-bus
- Input/Output Configuration register
- Polarity Inversion register
- Internal power-on reset
- Glitch free power-up
- No power up sequence required
- Partial power down supported
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- Packages offered: TSSOP24, HWQFN24

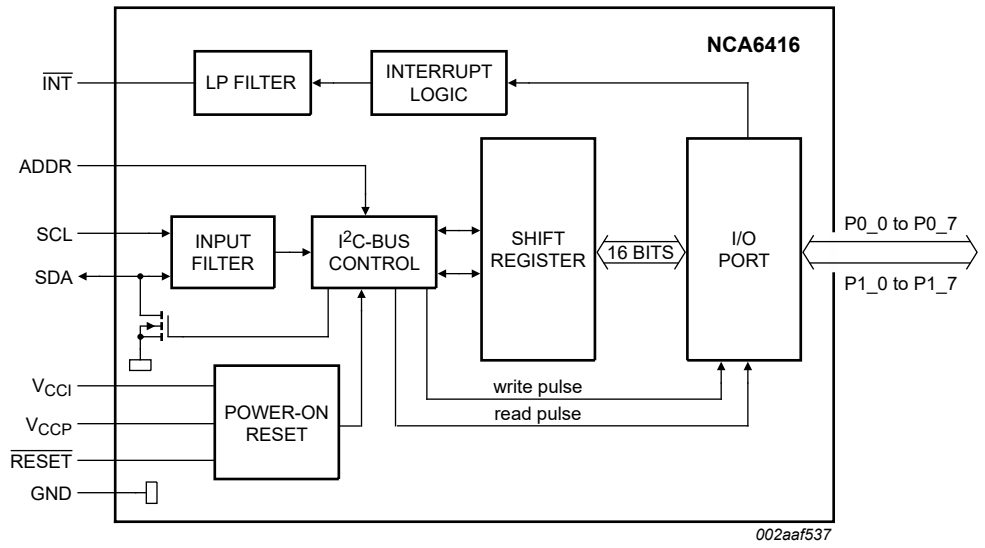
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NCA6416PW-Q100	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
NCA6416BY-Q100	-40 °C to +125 °C	HWQFN24	plastic thermal enhanced very very thin Quad Flat packages; no leads; 24 terminals; 0.5 mm pitch; 4 × 4 × 0.75 mm body	SOT8041-1

4. Block diagram



All I/Os are set to inputs at reset.

Fig. 1. Block diagram (positive logic)

5. Pinning information

5.1. Pinning

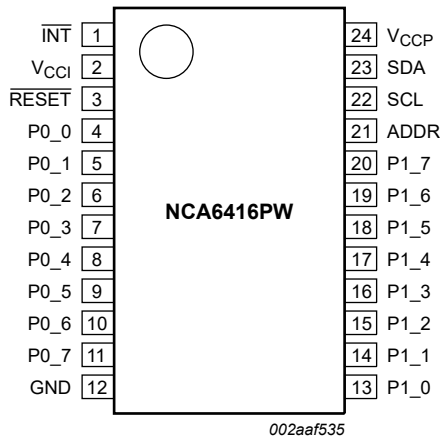
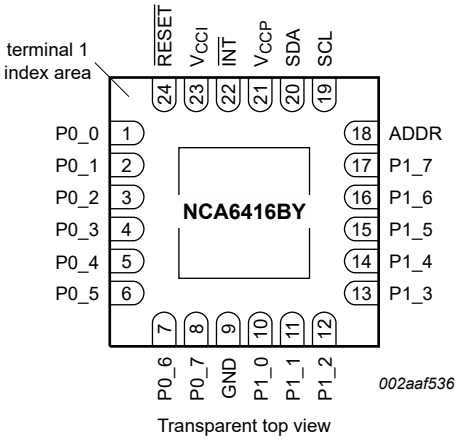


Fig. 2. Pin configuration SOT355-1 (TSSOP24)



The exposed center pad, if used, must be connected only as a secondary ground or must be left electrically open.

Fig. 3. Pin configuration SOT8041-1 (HWQFN24)

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	TSSOP24	HWQFN24	
$\overline{INT}$	1	22	Interrupt output. Connect to V_{CCI} or V_{CCP} through a pull-up resistor.
V_{CCI}	2	23	Supply voltage of I²C-bus. Connect directly to the V_{CC} of the external I²C controller. Provides voltage-level translation.
$\overline{RESET}$	3	24	Active LOW reset input. Connect to V_{CCI} through a pull-up resistor if no active connection is used.
P0_0 [1]	4	1	Port 0 input/output 0.
P0_1 [1]	5	2	Port 0 input/output 1.
P0_2 [1]	6	3	Port 0 input/output 2.
P0_3 [1]	7	4	Port 0 input/output 3.
P0_4 [1]	8	5	Port 0 input/output 4.
P0_5 [1]	9	6	Port 0 input/output 5.
P0_6 [1]	10	7	Port 0 input/output 6.
P0_7 [1]	11	8	Port 0 input/output 7.
GND	12	9	Ground.
P1_0 [2]	13	10	Port 1 input/output 0.
P1_1 [2]	14	11	Port 1 input/output 1.
P1_2 [2]	15	12	Port 1 input/output 2.
P1_3 [2]	16	13	Port 1 input/output 3.
P1_4 [2]	17	14	Port 1 input/output 4.
P1_5 [2]	18	15	Port 1 input/output 5.

Symbol	Pin		Description
	TSSOP24	HWQFN24	
P1_6 [2]	19	16	Port 1 input/output 6.
P1_7 [2]	20	17	Port 1 input/output 7.
ADDR	21	18	Address input. Connect directly to V_{CCP} or ground.
SCL	22	19	Serial clock bus. Connect to V_{CCI} through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to V_{CCI} through a pull-up resistor.
V_{CCP}	24	21	Supply voltage of NCA6416 for Port P.

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/O are configured as input.
[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-on, all I/O are configured as input.

6. Voltage translation

Table 3 shows how to set up V_{CC} levels for the necessary voltage translation between the I²C-bus and the NCA6416-Q100.

Table 3. Voltage translation

V_{CCI} (SDA and SCL of I²C controller)	V_{CCP} (Port P)
1.8 V	1.8 V
1.8 V	2.5 V
1.8 V	3.3 V
1.8 V	5 V
2.5 V	1.8 V
2.5 V	2.5 V
2.5 V	3.3 V
2.5 V	5 V
3.3 V	1.8 V
3.3 V	2.5 V
3.3 V	3.3 V
3.3 V	5 V
5 V	1.8 V
5 V	2.5 V
5 V	3.3 V
5 V	5 V

7. Functional description

Refer to Fig. 1 (Block diagram (positive logic)).

7.1. Device address

The address of the NCA6416-Q100 is shown in Fig. 4.

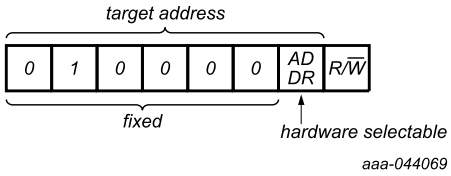


Fig. 4. NCA6416-Q100 address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible target addresses. The last bit of the target address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

7.2. Interface definition

Table 4. Interface definition

Byte	Bit							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
I²C-bus target address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

7.3. Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus controller sends a command byte, which is stored in the Pointer register in the NCA6416-Q100. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

Once a new command has been sent, the register that was last addressed continues to be accessed by reads until a new command byte is sent.

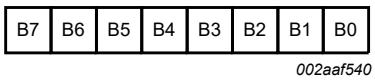


Fig. 5. Pointer register bits

Table 5. Command byte

Pointer register bits								Command byte	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx [1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx [1]
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111

[1] Undefined.

7.4. Register descriptions

7.4.1. Input port registers (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 8.2.

Table 6. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 7. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

7.4.2. Output port registers (02h, 03h)

The Output port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in Section 8.1 and a register pair read is described in Section 8.2.

Table 8. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 9. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

7.4.3. Polarity inversion registers (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write is described in Section 8.1 and a register pair read is described in Section 8.2.

Table 10. Polarity inversion port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 11. Polarity inversion port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

7.4.4. Configuration registers (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in Section 8.1 and a register pair read is described in Section 8.2.

Table 12. Configuration port 0 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

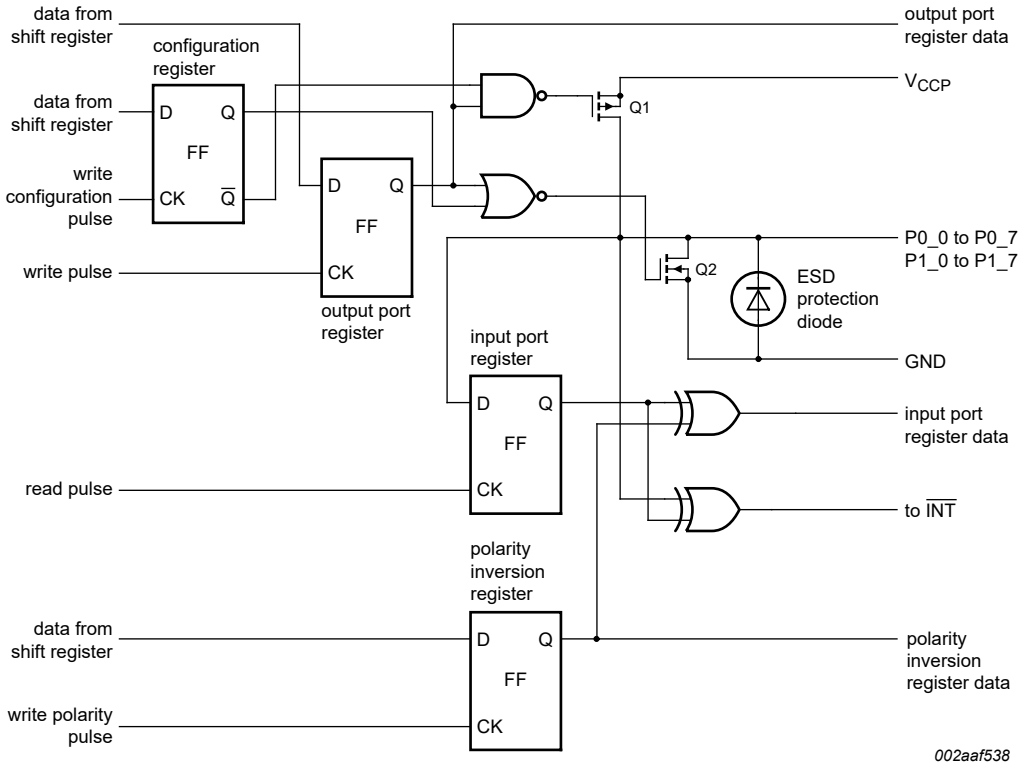
Table 13. Configuration port 1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

7.5. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CCP} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CCP} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig. 6. Simplified schematic of P0_0 to P1_7

7.6. Power-on reset

When power (from 0 V) is applied to V_{CCP}, an internal power-on reset holds the NCA6416-Q100 in a reset condition until V_{CCP} has reached V_{POR}. At that time, the reset condition is released and the NCA6416-Q100 registers and I²C-bus/SMBus state machine initializes to their default states. After that, V_{CCP} must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. See Section 9.2 requirements".

7.7. Reset input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The NCA6416-Q100 registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to V_{CCI} if no active connection is used.

7.8. Interrupt output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{\text{INT}}$ is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see Fig. 10). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The $\overline{\text{INT}}$ output has an open-drain structure and requires pull-up resistor to V_{CCP} or V_{CCI} depending on the application. $\overline{\text{INT}}$ should be connected to the voltage source of the device that requires the interrupt information.

8. Bus transactions

The NCA6416-Q100 is an I²C-bus target device. Data is exchanged between the controller and NCA6416-Q100 through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1. Write commands

Data is transmitted to the NCA6416-Q100 by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Fig. 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the NCA6416-Q100 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion and configuration registers. After sending data to one register, the next data byte is sent to the other register in the pair (see Fig. 7 and Fig. 8). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers or the host can simply update a single register.

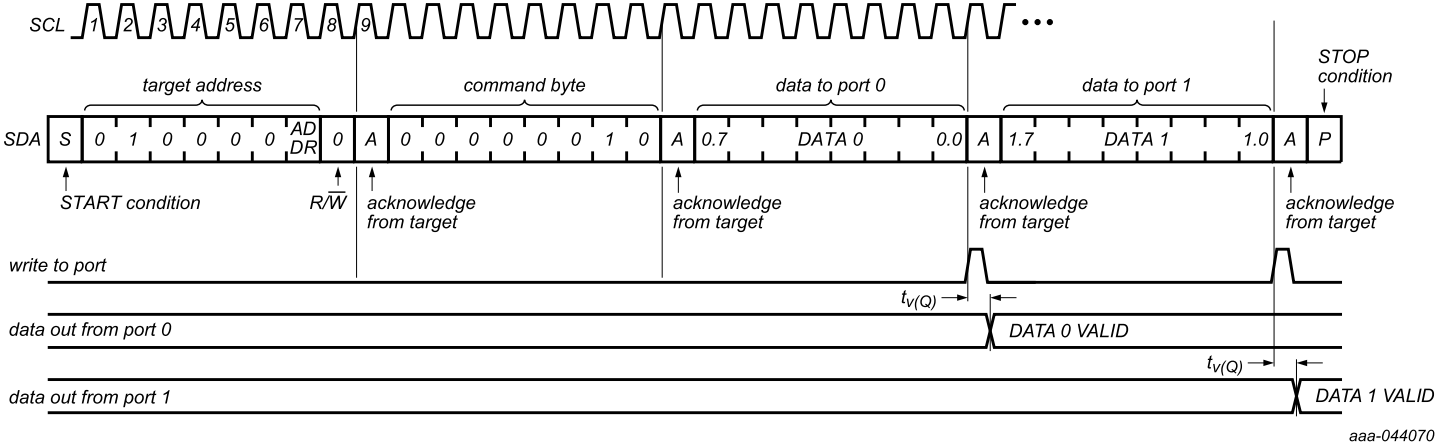


Fig. 7. Write to output port register

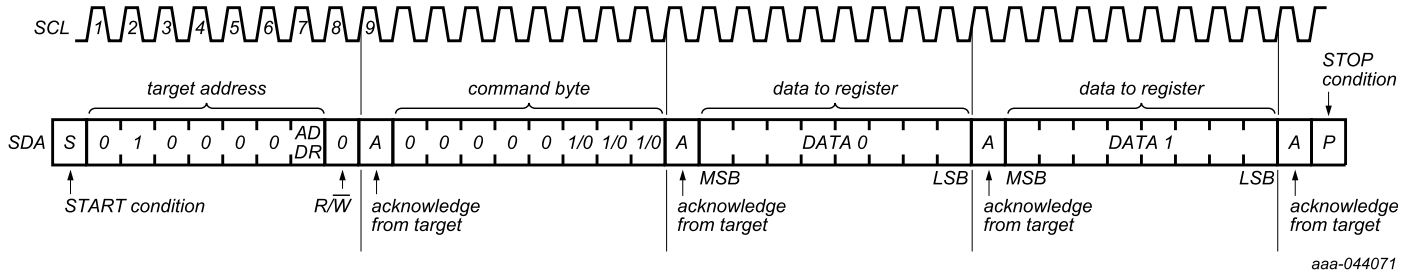


Fig. 8. Write to device registers

8.2. Read commands

To read data from the NCA6416-Q100, the bus controller must first send the NCA6416-Q100 address with the least significant bit set to a logic 0 (see Fig. 4 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the NCA6416-Q100 (see Fig. 9 and Fig. 10). Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus controller must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.

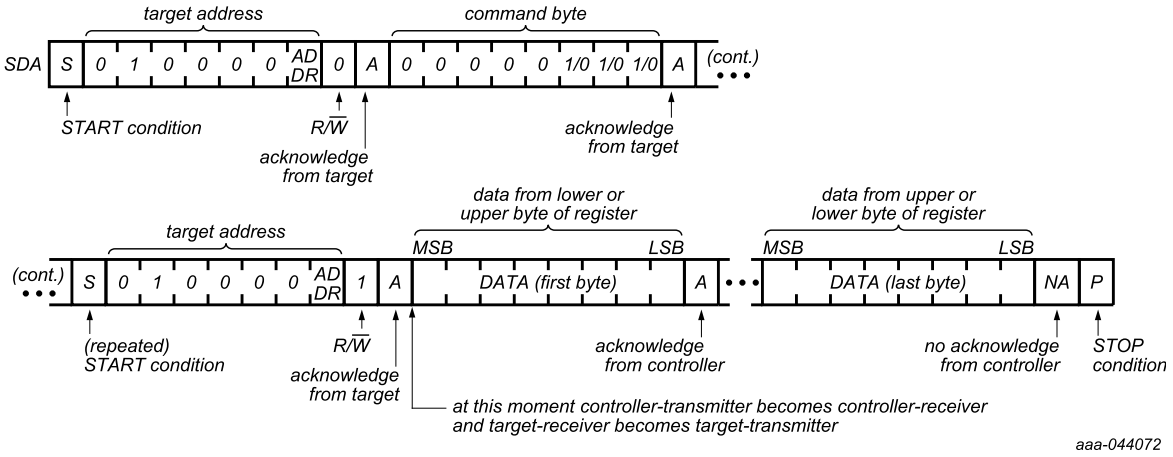
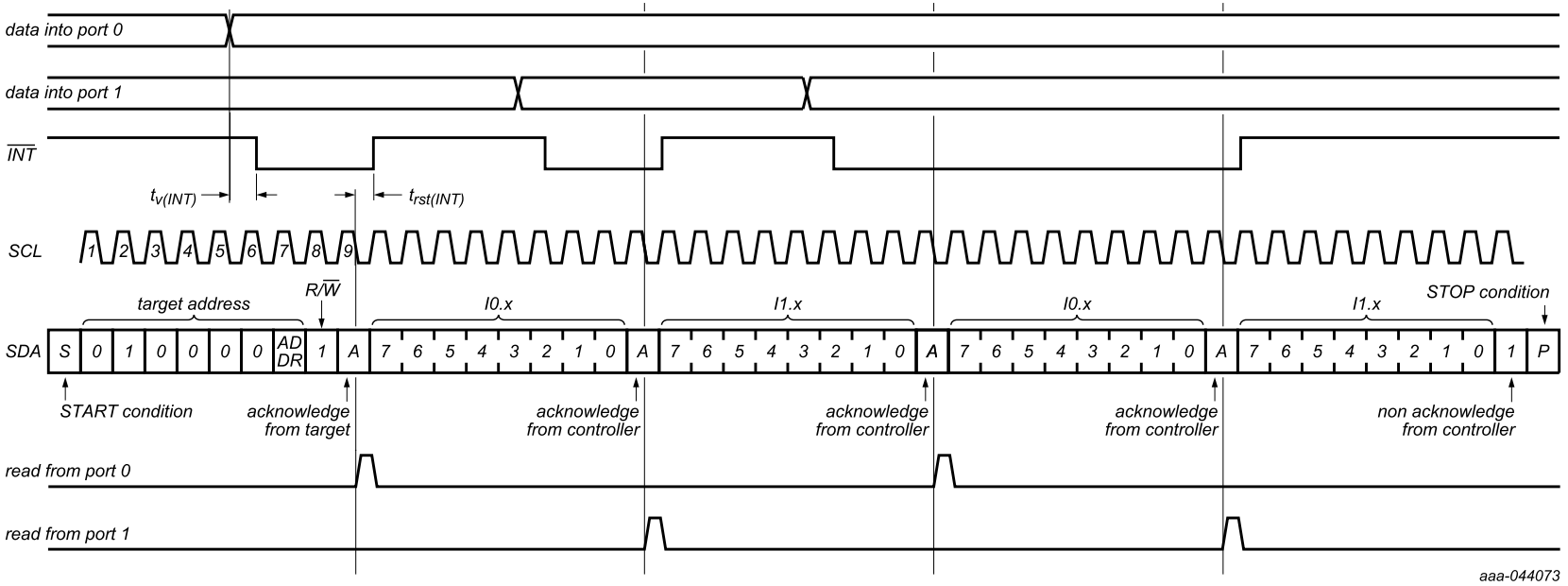


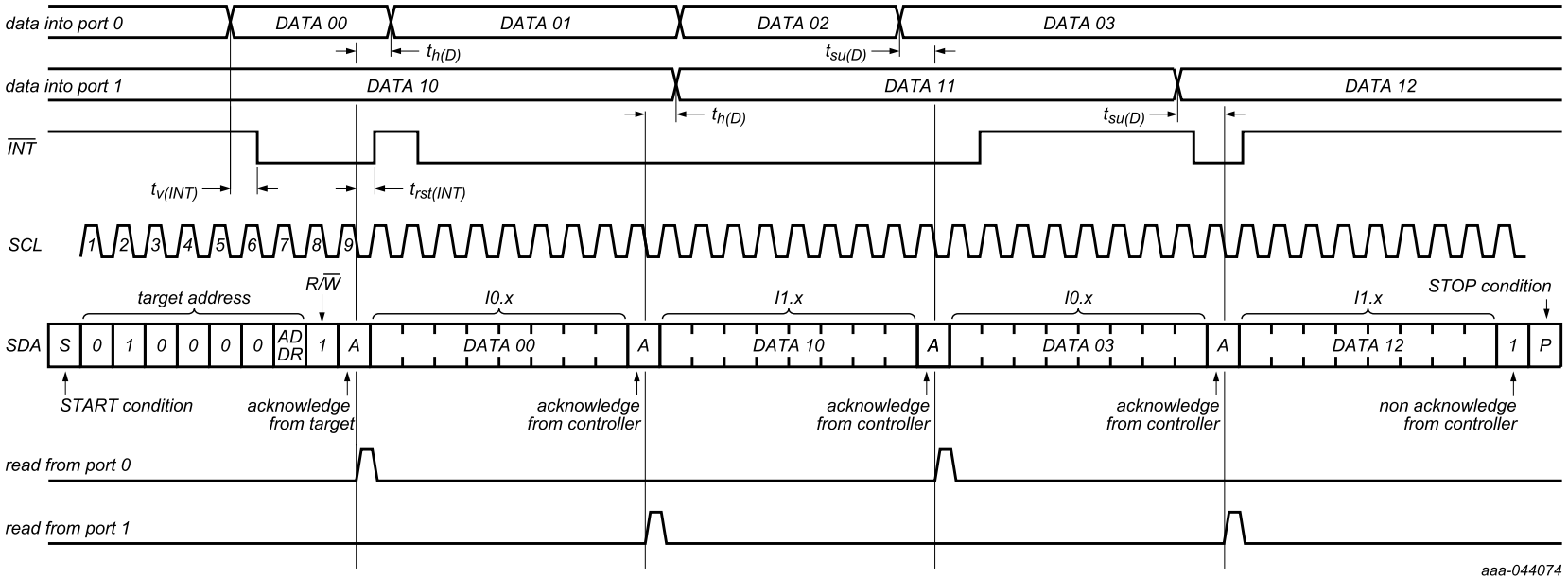
Fig. 9. Read from device registers



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode).It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial target address call and actual data transfer from P port (see Fig. 9).

Fig. 10. Read input port register, scenario 1

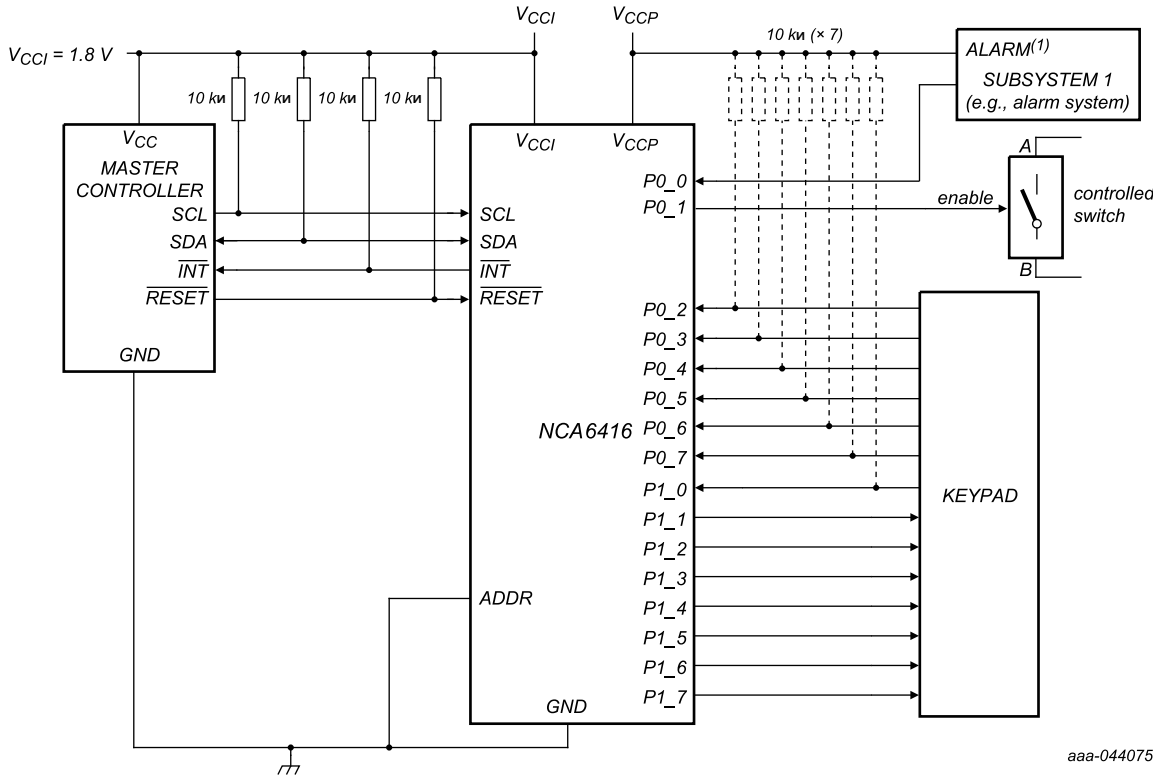


Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode).It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial target address call and actual data transfer from P port (see Fig. 9).

Fig. 11. Read input port register, scenario 2

9. Application design-in information



Device address configured as 0100 0000 for this example.

P0_0 and P0_2 through P1_0 are configured as inputs.

P0_1 and P1_1 through P1_7 are configured as outputs.

(1) External resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. If an output in the P port is configured as a push-pull output there is no need for external pull-up resistors. If an output in the P port is configured as an open-drain output, external pull-up resistors are required.

Fig. 12. Typical application

9.1. Minimizing I_{CC} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CCP} through a resistor as shown in Fig. 12. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{CCP}. The supply current, I_{CCP}, increases as V_I becomes lower than V_{CCP}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CCP} when the LED is off. Fig. 13 shows a high value resistor in parallel with the LED. Fig. 14 shows V_{CCP} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{CCP} and prevents additional supply current consumption when the LED is off.

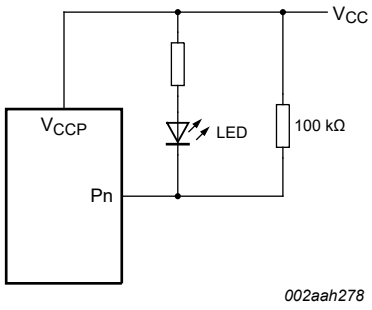


Fig. 13. High value resistor in parallel with the LED

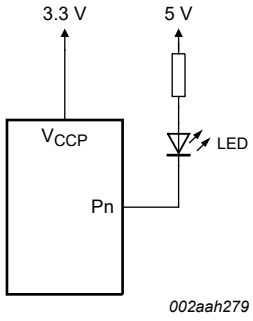


Fig. 14. Device supplied by a lower voltage

9.2. Power-on reset requirements

In the event of a glitch or data corruption, NCA6416-Q100 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The power-on reset is shown in Fig. 15.

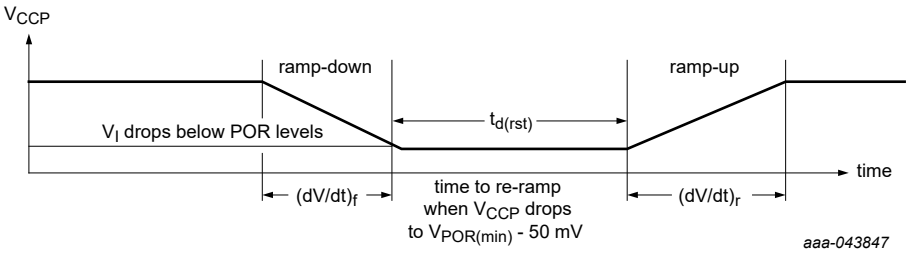


Fig. 15. V_{CCP} is lowered below the POR threshold, then ramped back up to V_{CCP}

Table 14 specifies the performance of the power-on reset feature for NCA6416-Q100.

Table 14. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	see Fig. 15	0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	see Fig. 15	0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Fig. 15; re-ramp time when V_{CCP} drops to $V_{POR(min)}$ - 50 mV	1	-	-	µs
$\Delta V_{CC(gl)}$	glitch supply voltage difference	see Fig. 16 [1]	-	-	1.0	V
$t_{w(gl)VCC}$	supply voltage glitch pulse width	Fig. 17 [2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling V_{CCP}	0.8	-	-	V
		rising V_{CCP}	-	-	1.6	V

[1] Level that V_{CCP} can glitch down to with a ramp rate at 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VCC}$ < 1 µs.
[2] Glitch width that will not cause a functional disruption when $\Delta V_{CC(gl)} = 0.5 \times V_{CCP}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VCC}$) and glitch height ($\Delta V_{CC(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Fig. 16 and Table 14 provide more information on how to measure these specifications.

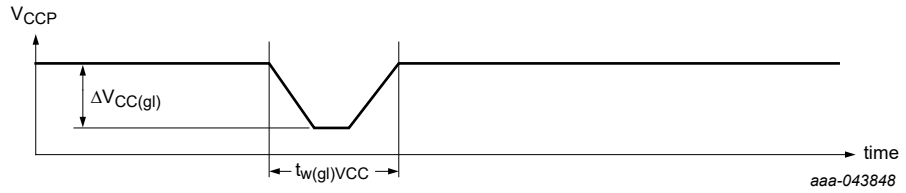


Fig. 16. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0 V. Fig. 17 and Table 14 provide more details on this specification.

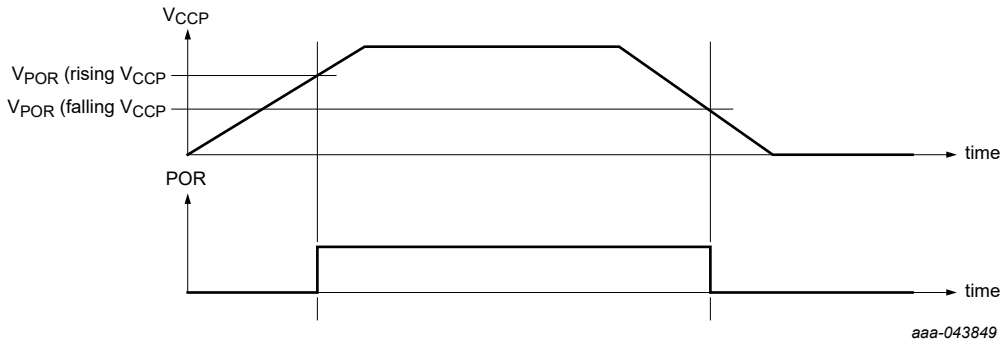


Fig. 17. Power-on reset voltage (V_{POR})

9.3. Partial power-down and power-up sequence

The NCA6416-Q100 has two supplies and a voltage translation function, translating between the I²C bus and the P-PORTs. Fig. 1 shows the block diagram that features a POWER-ON RESET block that senses both VCCI and VCCP. This is part of the implementation of the feature allowing partial power-down. Table 15 gives an overview of supply and reset condition combinations.

Table 15. NCA6416-Q100 modes based on combinations of V_{CCI}, V_{CCP} and $\overline{RESET}$

H = HIGH voltage level; L = LOW voltage level; X = don't care.

V_{CCI}	V_{CCP}	$\overline{RESET}$	Mode
L	L	X	Not functional
H	H	L	Reset
H	H	H	Functional
L	H	X	Partial power-down / Reset
H	L	X	Partial power-down / Reset

In the absence of both power supplies (V_{CCP} and V_{CCI}), the product is non-functional. However, overvoltage protection on the P-PORTs remains permissible, consistent with other operational modes. The overvoltage protection ensures that when a P-PORT is biased with an input voltage (V_i) exceeding V_{CCP}, input current is prevented. This protection is disabled only when a P-PORT is configured as an output in functional mode. When both V_{CCP} and V_{CCI} are present, the $\overline{RESET}$ signal determines the product's operational state, toggling between functional mode and reset mode. If V_{CCP} is present but V_{CCI} is absent, the product enters reset mode. In this state, configuration registers are initialized to their default values, configuring all P-PORTs as input ports, with their output drivers disabled. When V_{CCI} is present but V_{CCP} absent, the SDA and $\overline{INT}$ open drain drivers are off. In partial power-down scenarios, where only one supply is active, there is no risk of excessive current draw on the active supply. Section 13 provides I_{CC} specifications for both normal operation and partial power-down modes. The power supplies, V_{CCP} and V_{CCI}, can be sequenced (ramped-up or -down) in any order while output glitches are prevented. Regardless of the power-up sequence, the product initializes in its default state. Section 9.2 specifies a V_{CCP} power cycle procedure that ensures the product resets upon V_{CCP} power-up, initiating in the default state. During power-up, the $\overline{RESET}$ signal can be pulled HIGH to enable functional mode at startup. Alternatively, if $\overline{RESET}$ is pulled LOW during power-up, the product remains in reset (disabled) mode. De-asserting $\overline{RESET}$ subsequently transitions the product to functional mode. Section 7.2 provides a detailed description of the $\overline{RESET}$ function.

10. Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCI}	I²C-bus supply voltage		-0.5	+6.5	V
V_{CCP}	supply voltage port P		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
V_O	output voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	ADDR, $\overline{RESET}$, SCL; $V_I < 0$ V	-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V	-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{CCP}$	-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{CCI}$	-	±20	mA
I_{OL}	LOW-level output current	continuous; P port; V_O = 0 V to V_{CCP}	-	50	mA
		continuous; SDA, $\overline{INT}$; V_O = 0 V to V_{CCI}	-	25	mA
I_{OH}	HIGH-level output current	continuous; P port; V_O = 0 V to V_{CCP}	-	25	mA
I_{CC}	supply current	continuous through GND	-	200	mA
I_{CCP}	supply current port P	continuous through V_{CCP}	-	160	mA
I_{CCI}	I²C-bus supply current	continuous through V_{CCI}	-	10	mA
T_{stg}	storage temperature		-65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

11. Recommended operating conditions

Table 17. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCI}	I²C-bus supply voltage		1.65	5.5	V
V_{CCP}	supply voltage port P		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$	0.7 × V_{CCI}	5.5	V
		ADDR, P1_7 to P0_0	0.7 × V_{CCP}	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$	-0.5	0.3 × V_{CCI}	V
		ADDR, P1_7 to P0_0	-0.5	0.3 × V_{CCP}	V
I_{OH}	HIGH-level output current	P1_7 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P1_7 to P0_0	-	25	mA
T_{amb}	ambient temperature	operating in free air	-40	+125	°C

12. Thermal characteristics

Table 18. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP24 package	[1]	88	K/W
		HWQFN24 package	[1]	66	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

13. Static characteristics

Table 19. Static characteristics

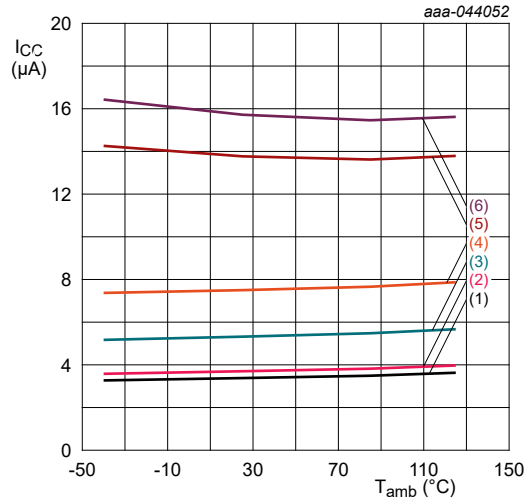
V_{CCI} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IK}	input clamping voltage	I_I = -18 mA	-1.2	-	-	-1.2	-	V
V_{POR}	power-on reset voltage	$V_I = V_{CCP}$ or GND; I_O = 0 mA						
		Falling V_{CCP}	0.8	1.1	-	0.8	-	V
		Rising V_{CCP}	-	1.25	1.55	-	1.6	V
V_{OH}	HIGH-level output voltage	P port						
		I_{OH} = -8 mA; V_{CCP} = 1.65 V [2]	1.2	-	-	1.2	-	V
		I_{OH} = -10 mA; V_{CCP} = 1.65 V [2]	1.1	-	-	1.1	-	V
		I_{OH} = -8 mA; V_{CCP} = 2.3 V [2]	1.8	-	-	1.8	-	V
		I_{OH} = -10 mA; V_{CCP} = 2.3 V [2]	1.7	-	-	1.7	-	V
		I_{OH} = -8 mA; V_{CCP} = 3.0 V [2]	2.6	-	-	2.6	-	V
		I_{OH} = -10 mA; V_{CCP} = 3.0 V [2]	2.5	-	-	2.5	-	V
		I_{OH} = -8 mA; V_{CCP} = 4.5 V [2]	4.1	-	-	4.1	-	V
		I_{OH} = -10 mA; V_{CCP} = 4.5 V [2]	4.0	-	-	4.0	-	V
V_{OL}	LOW-level output voltage	P port; I_{OL} = 8 mA						
		V_{CCP} = 1.65 V [2]	-	-	0.45	-	0.45	V
		V_{CCP} = 2.3 V [2]	-	-	0.25	-	0.25	V
		V_{CCP} = 3 V [2]	-	-	0.25	-	0.25	V
		V_{CCP} = 4.5 V [2]	-	-	0.2	-	0.2	V
		P port; I_{OL} = 10 mA						
		V_{CCP} = 1.65 V [2]	-	-	0.6	-	0.6	V
		V_{CCP} = 2.3 V [2]	-	-	0.3	-	0.3	V
		V_{CCP} = 3 V [2]	-	-	0.25	-	0.25	V
		V_{CCP} = 4.5 V [2]	-	-	0.2	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{CCP} = 1.65 V to 5.5 V						
		SDA [3]	3	-	-	3	-	mA
		$\overline{INT}$ [3]	3	15 [4]	-	3	-	mA
		P port						
		V_{OL} = 0.5 V; V_{CCP} = 1.65 V [3]	8	-	-	8	-	mA
		V_{OL} = 0.7 V; V_{CCP} = 1.65 V [3]	10	-	-	10	-	mA
		V_{OL} = 0.5 V; V_{CCP} = 2.3 V [3]	8	-	-	8	-	mA
		V_{OL} = 0.7 V; V_{CCP} = 2.3 V [3]	10	-	-	10	-	mA
		V_{OL} = 0.5 V; V_{CCP} = 3.0 V [3]	8	-	-	8	-	mA
		V_{OL} = 0.7 V; V_{CCP} = 3.0 V [3]	10	-	-	10	-	mA
		V_{OL} = 0.5 V; V_{CCP} = 4.5 V [3]	8	-	-	8	-	mA
		V_{OL} = 0.7 V; V_{CCP} = 4.5 V [3]	10	-	-	10	-	mA
I_I	input current	V_{CCP} = 1.65 V to 5.5 V						
		SCL, SDA, $\overline{RESET}$; $V_I = V_{CCI}$ or GND	-	-	±1	-	±1	µA
		ADDR; $V_I = V_{CCP}$ or GND	-	-	±1	-	±1	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{IH}	HIGH-level input current	P port; $V_I = V_{CCP}$; V_{CCP} = 1.65 V to 5.5 V	-	-	1	-	1	µA
I_{IL}	LOW-level input current	P port; V_I = GND; V_{CCP} = 1.65 V to 5.5 V	-	-	1	-	1	µA
I_{CC}	supply current	$I_{CCI} + I_{CCP}$; SDA, P port, ADDR, $\overline{RESET}$; V_I on SDA and $\overline{RESET}$ = V_{CCI} or GND; V_I on P port and ADDR = V_{CCP}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz						
		V_{CCP} = 3.6 V to 5.5 V	-	10	25	-	27	µA
		V_{CCP} = 2.3 V to 3.6 V	-	6.5	15	-	17	µA
		V_{CCP} = 1.65 V to 2.3 V	-	4	11	-	13	µA
		$I_{CCI} + I_{CCP}$; SCL, SDA, P port, ADDR, $\overline{RESET}$; V_I on SCL, SDA and $\overline{RESET}$ = V_{CCI} or GND; V_I on P port and ADDR = V_{CCP}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz						
		V_{CCP} = 3.6 V to 5.5 V	-	1.5	3.5	-	8	µA
		V_{CCP} = 2.3 V to 3.6 V	-	1	2.0	-	5	µA
		V_{CCP} = 1.65 V to 2.3 V	-	0.5	1.5	-	2.5	µA
		Active mode; $I_{CCI} + I_{CCP}$; P port, ADDR, $\overline{RESET}$; V_I on $\overline{RESET}$ = V_{CCI}; V_I on P port and ADDR = V_{CCP}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz, continuous register read						
		V_{CCP} = 3.6 V to 5.5 V	-	21	40	-	40	µA
		V_{CCP} = 2.3 V to 3.6 V	-	12	22	-	25	µA
		V_{CCP} = 1.65 V to 2.3 V	-	8	16	-	18	µA
I_{CCI}	supply current	Partial power-down V_{CCP} = 3.6 V; V_{CCI} = 1.65 V to 5.5 V	-	-	1	-	1	µA
I_{CCP}	supply current	Partial power-down V_{CCI} = 3.6 V; V_{CCP} = 1.65 V to 5.5 V	-	-	1	-	3	µA
ΔI_{CC}	additional quiescent supply current	SCL, SDA, $\overline{RESET}$; one input at V_{CCI} - 0.6 V, other inputs at V_{CCI} or GND; V_{CCP} = 1.65 V to 5.5 V	-	-	5	-	10	µA
		P port, ADDR; one input at V_{CCP} - 0.6 V, other inputs at V_{CCP} or GND; V_{CCP} = 1.65 V to 5.5 V	-	-	5	-	10	µA
C_i	input capacitance	$V_I = V_{CCI}$ or GND; V_{CCP} = 1.65 V to 5.5 V	-	2	2.5	-	3.5	pF
C_{io}	input/output capacitance	SDA; $V_{I/O} = V_{CCI}$ or GND; V_{CCP} = 1.65 V to 5.5 V	-	2	3	-	4	pF
		P port; $V_{I/O} = V_{CCP}$ or GND; V_{CCP} = 1.65 V to 5.5 V	-	4.5	5.5	-	6	pF

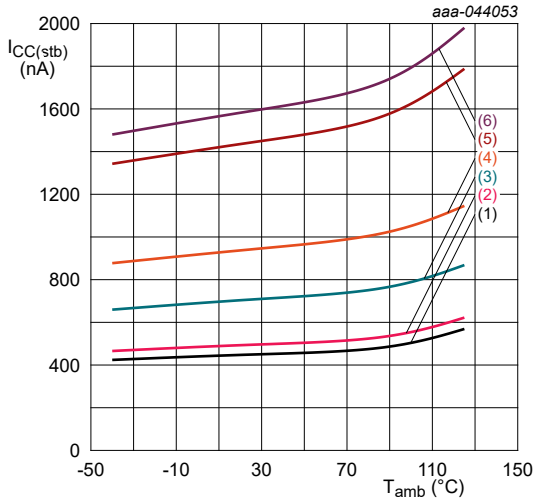
[1] For I_{CC}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V_{CC}) and T_{amb} = 25 °C. Except for I_{CC}, the typical values are at $V_{CCP} = V_{CCI}$ = 3.3 V and T_{amb} = 25 °C.
[2] The total current sourced by all I/Os must be limited to 160 mA.
[3] Each I/O must be externally limited to a maximum of 25 mA, for a device total of 200 mA.
[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{CC} = 3.3 V. Typical value for V_{CC} < 2.5 V, V_{OL} = 0.6 V.

13.1. Typical characteristics



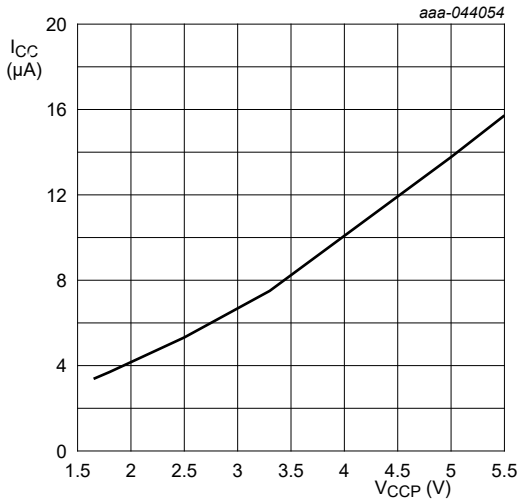
$I_{CC} = I_{CCI} + I_{CCP}$
(1) V_{CCP} = 1.65 V; (2) V_{CCP} = 1.8 V
(3) V_{CCP} = 2.5 V; (4) V_{CCP} = 3.3 V
(5) V_{CCP} = 5.0 V; (6) V_{CCP} = 5.5 V

Fig. 18. Supply current versus ambient temperature



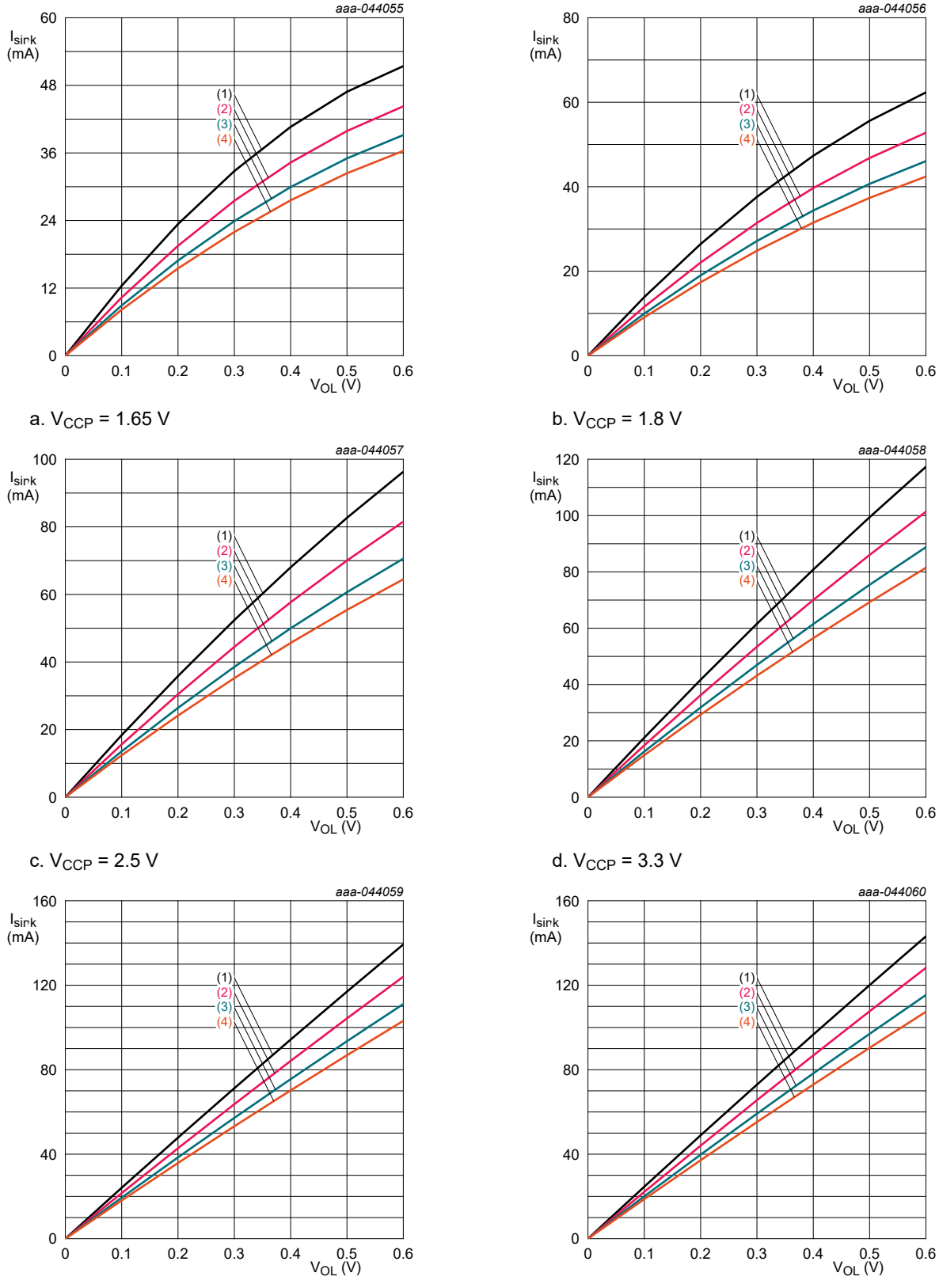
(1) V_{CCP} = 1.65 V; (2) V_{CCP} = 1.8 V
(3) V_{CCP} = 2.5 V; (4) V_{CCP} = 3.3 V
(5) V_{CCP} = 5.0 V; (6) V_{CCP} = 5.5 V

Fig. 19. Standby supply current versus ambient temperature



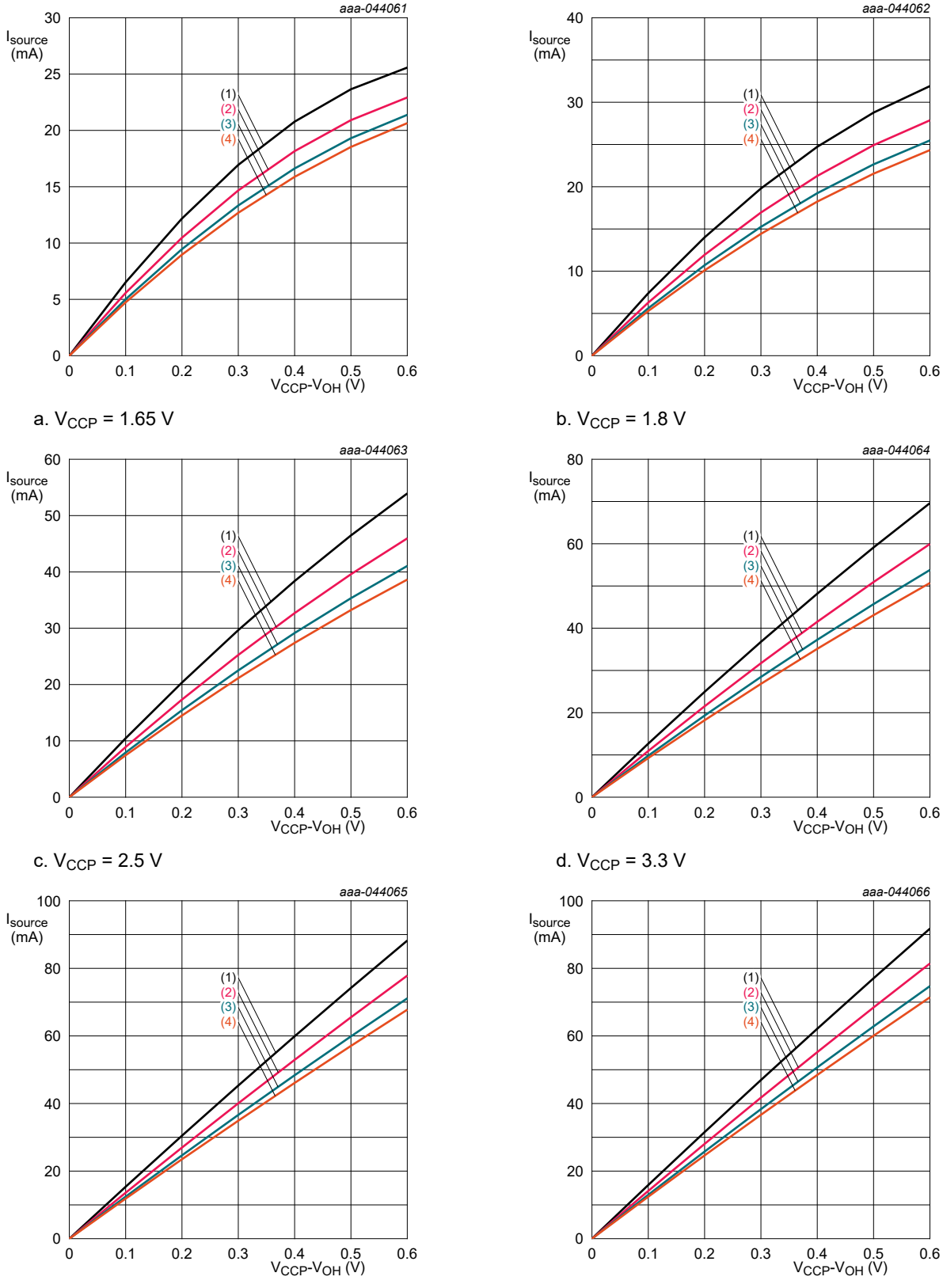
T_{amb} = 25 °C
$I_{CC} = I_{CCI} + I_{CCP}$

Fig. 20. Supply current versus supply voltage



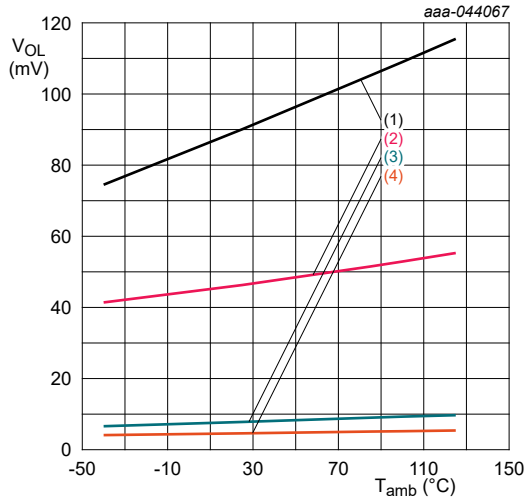
(1) T_{amb} = -40 °C, (2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C, (4) T_{amb} = 125 °C

Fig. 21. I/O sink current versus LOW-level output voltage



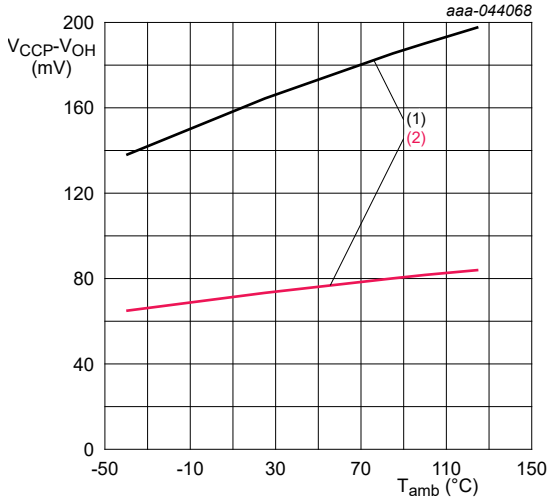
(1) T_{amb} = -40 °C, (2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C, (4) T_{amb} = 125 °C

Fig. 22. I/O source current versus HIGH-level output voltage



(1) V_{CCP} = 1.8 V; I_{sink} = 10 mA
(2) V_{CCP} = 5 V; I_{sink} = 10 mA
(3) V_{CCP} = 1.8 V; I_{sink} = 1 mA
(4) V_{CCP} = 5 V; I_{sink} = 1 mA

Fig. 23. LOW-level output voltage versus temperature



I_{source} = -10 mA
(1) V_{CCP} = 1.8 V
(2) V_{CCP} = 5 V

Fig. 24. I/O high voltage versus temperature

14. Dynamic characteristics

Table 20. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Fig. 26.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals		-	300	20 × (V_{CC} / 5.5 V)	300	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	µs

Table 21. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Fig. 28.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{w(rst)}$	reset pulse width		6	-	6	-	ns
$t_{rec(rst)}$	reset recovery time		0	-	0	-	ns
t_{rst}	reset time	[1]	600	-	600	-	ns

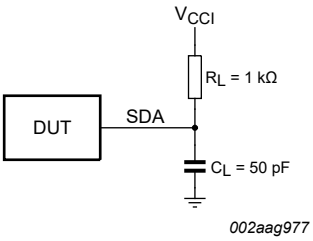
[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

Table 22. Switching characteristics

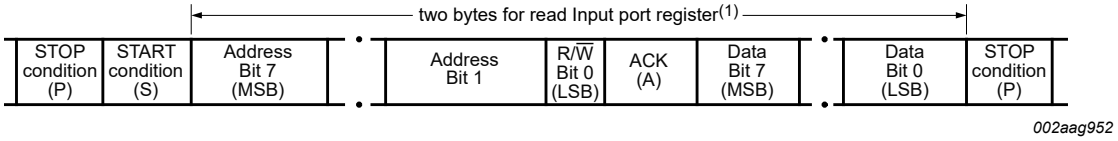
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Fig. 27.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	µs
$t_{v(Q)}$	data output valid time	from SCL to P port	-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	300	-	300	-	ns

15. Parameter measurement information

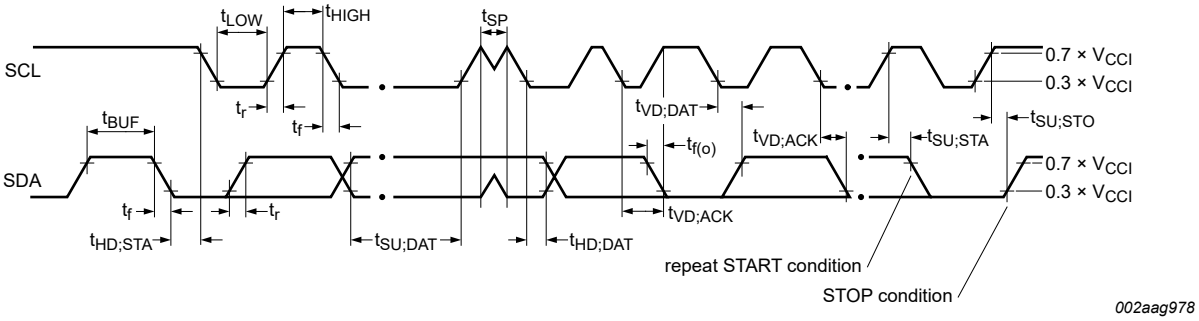


a. SDA load configuration



b. Transaction format

(1) See Fig. 10.



c. Voltage waveforms

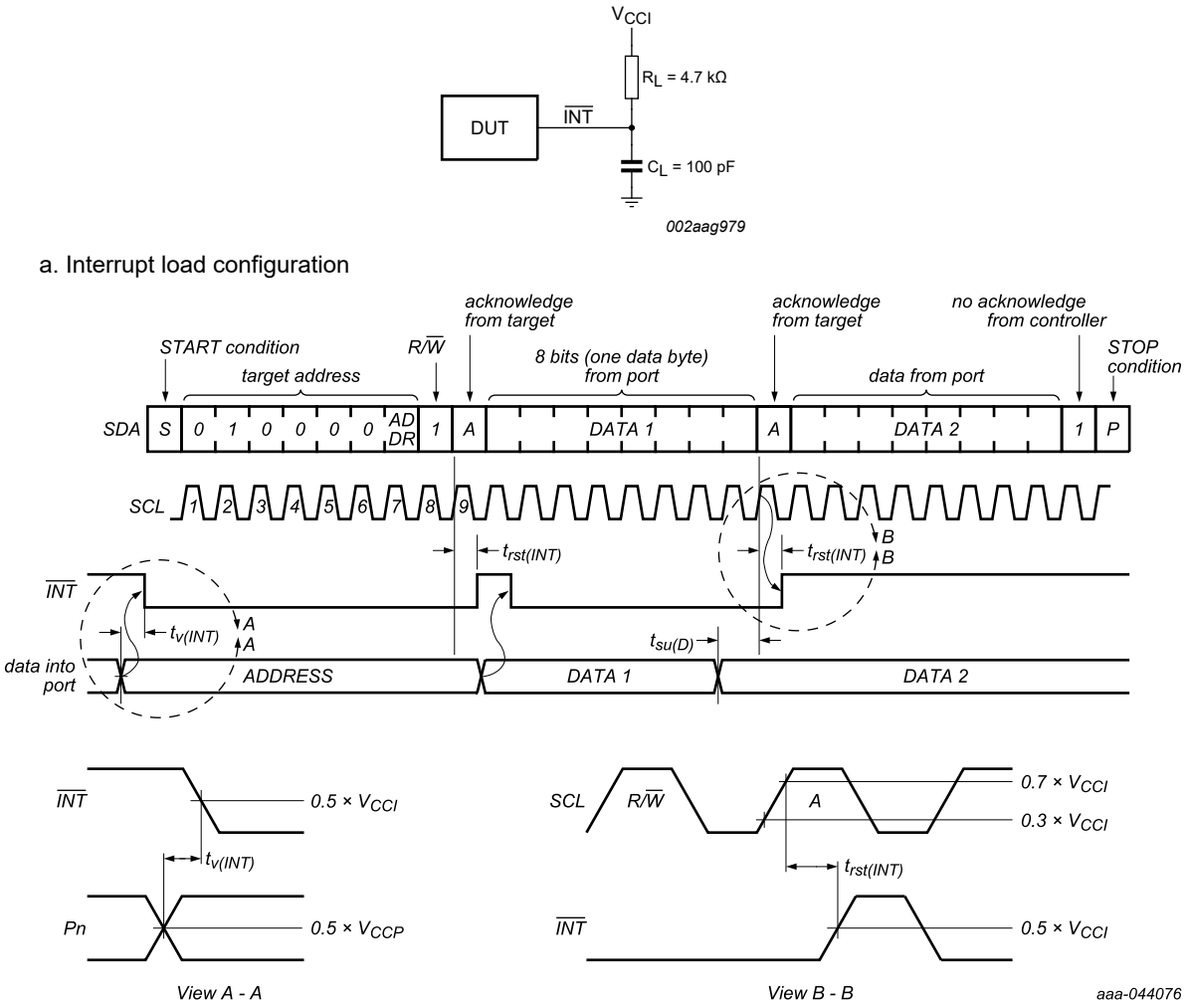
C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

Byte 1 = I²C-bus address; Byte 2, byte 3 = P port data.

Fig. 25. I²C-bus interface load circuit and voltage waveforms



a. Interrupt load configuration

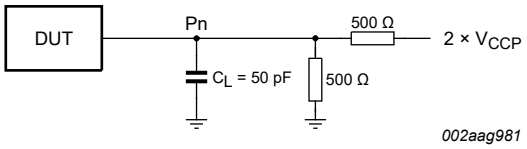
b. Voltage waveforms

C_L includes probe and jig capacitance.

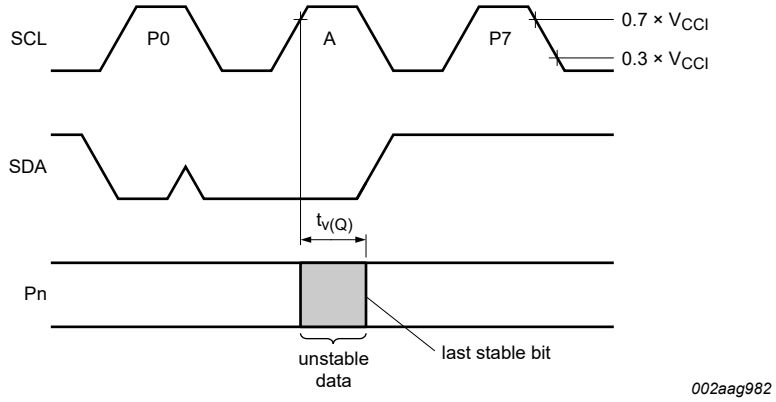
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

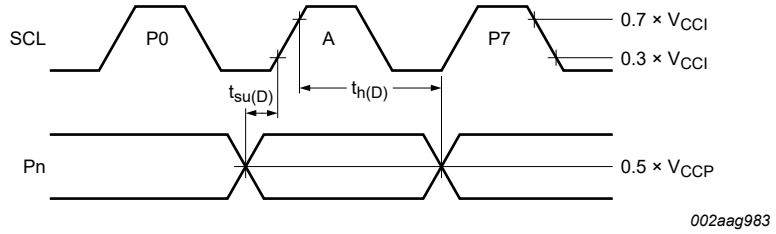
Fig. 26. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

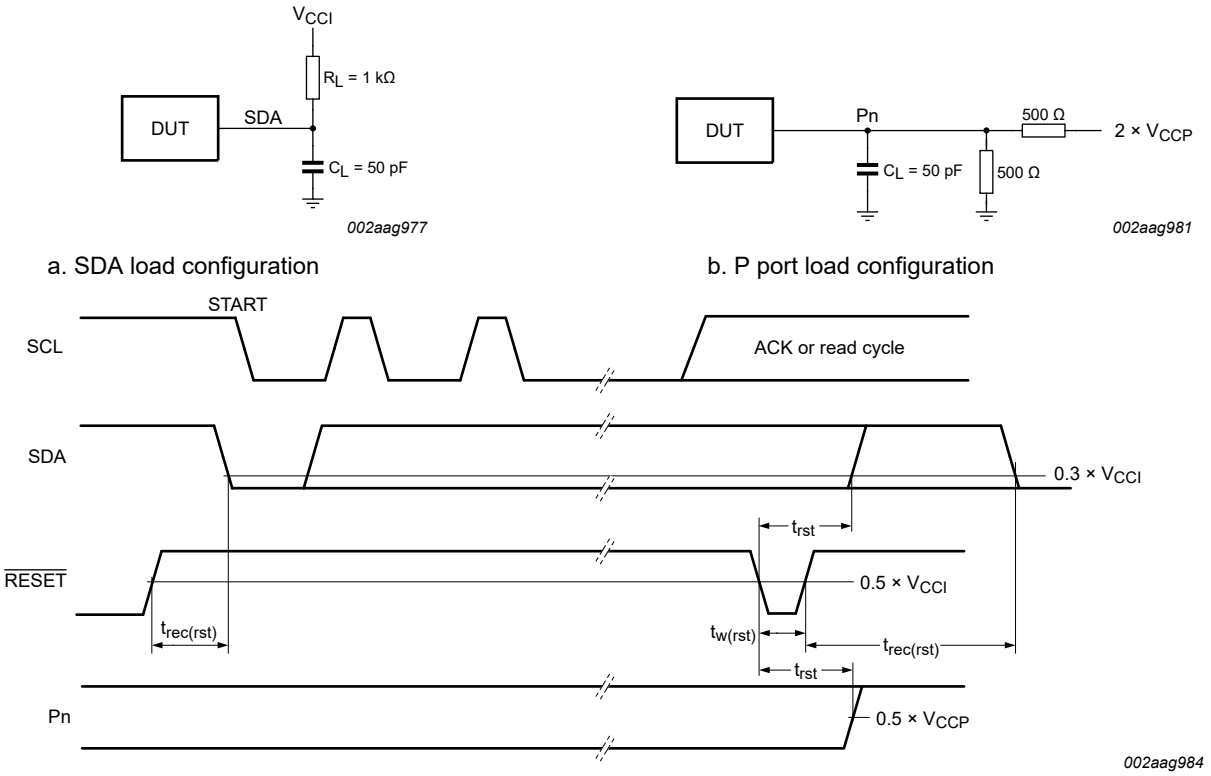
$t_{v(Q)}$ is measured from 0.7 × V_{CCI} on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig. 27. P port load circuit and voltage waveforms



c. $\overline{\text{RESET}}$ timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

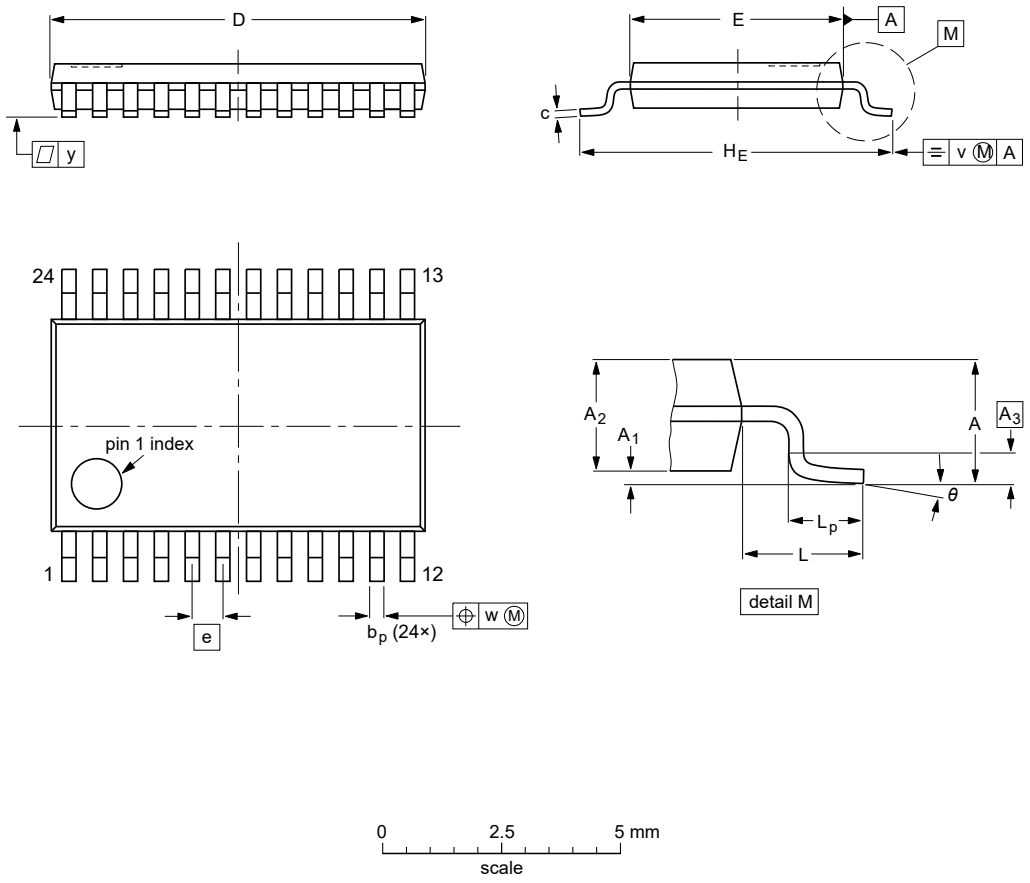
I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

Fig. 28. Reset load circuits and voltage waveforms

16. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05	0.25 BSC	0.30	0.20	7.90	4.50	0.65 BSC	6.60	1.00 REF	0.75	0.2	0.1	0.1	8°
	nom																
	min		0.05	0.80		0.19	0.09	7.70	4.30		6.20		0.45				0°

Notes

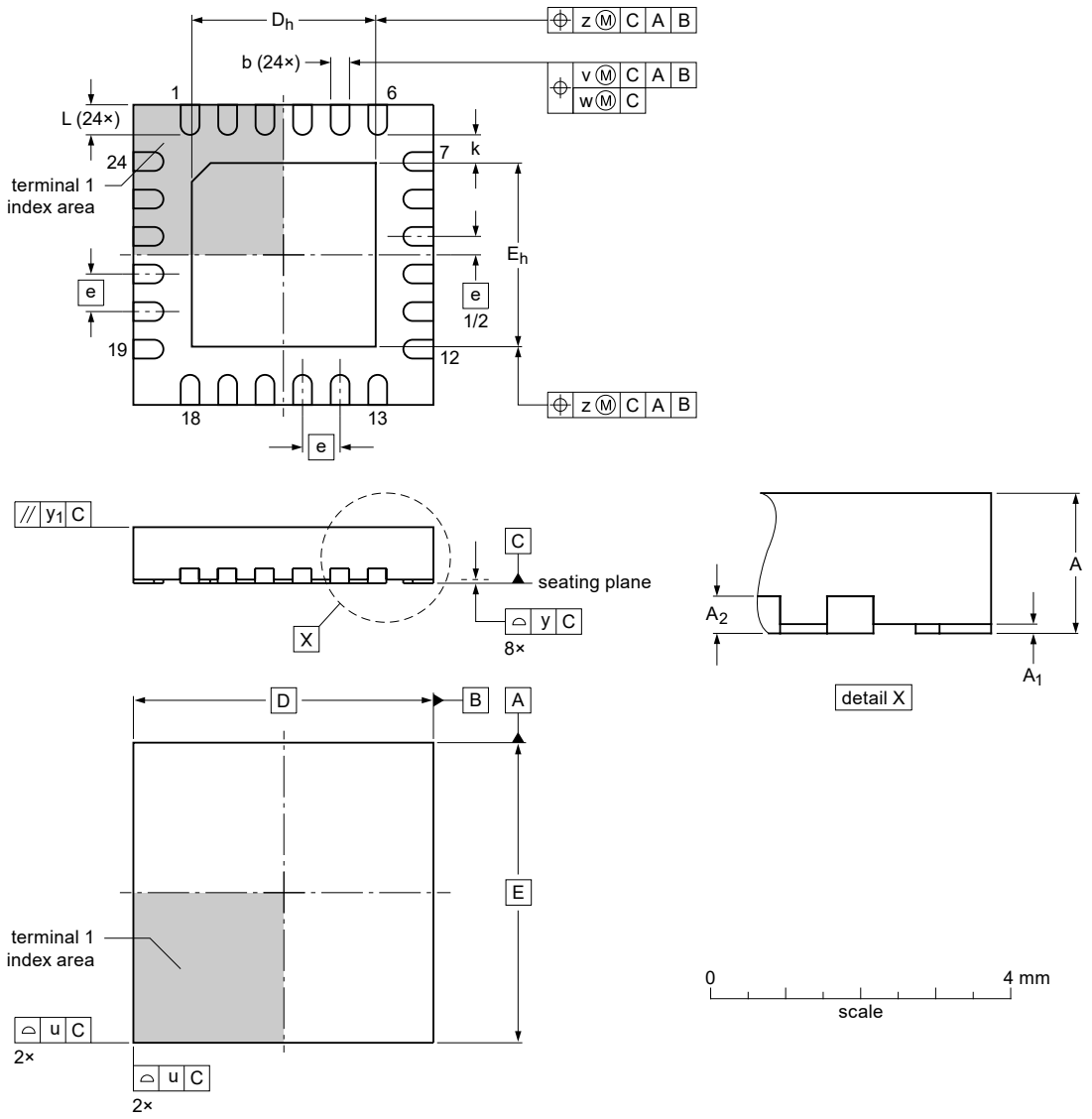
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot355-1_po

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~03-02-19~~ 24-11-07

Fig. 29. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin Quad Flat packages, no leads; 24 terminals; 0.5 mm pitch; 4 x 4 x 0.75 mm body **SOT8041-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_h	E	E_h	e	k	L	u	v	w	y	y_1	z
mm	max	0.80	0.05	0.2 Ref.	0.30	4 BSC	2.55	4 BSC	2.55	0.5 BSC	0.375 Ref.	0.50	0.10	0.10	0.05	0.08	0.10	0.10
	nom	0.75			0.25		2.45		2.45			0.40						
	min	0.70	0.00		0.20		2.35		2.35			0.30						

sot8041-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8041-1		MO-220 (WGGD-8)				~~22-04-01~~ 22-04-25

Fig. 30. Package outline SOT8041-1 (HWQFN24)

17. Abbreviations

Table 23. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	Not ACKnowledge
PCB	Printed-Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SMBus	System Management Bus

18. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA6416_Q100 v.1	20250820	Product data sheet	-	-

19. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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