



# NCA6416

Low-voltage translating 16-bit I<sup>2</sup>C-bus/SMBus I/O expander

Rev. 1 — 20 August 2025

Product data sheet

## 1. General description

The NCA6416 is a versatile 16-bit general-purpose I/O expander designed for microcontrollers that need additional I/O pins. It communicates via an I<sup>2</sup>C-bus interface, making it ideal for applications with minimal space and wiring, such as battery-powered devices using sensors, keypads, push buttons or LED control for managing LED brightness.

Nexperia's I/O expanders feature a dual power supply architecture with two inputs:  $V_{CCI}$  and  $V_{CCP}$ . This design enables seamless level translation, supporting mixed-voltage environments.  $V_{CCI}$  powers the I<sup>2</sup>C interface and must be connected to the same voltage as the host microcontroller's I<sup>2</sup>C bus (SDA/SCL), which can range from 1.65 V to 5.5 V.  $V_{CCP}$  powers the internal core and the I/O pins on Port P, defining the voltage level for the connected peripherals. This allows a low-voltage microcontroller to interface with higher-voltage peripherals without additional external circuitry.

The NCA6416 contains four pairs of 8-bit registers: Configuration, Input, Output, and Polarity Inversion. By default, all I/O pins are configured as inputs at power-on. A system controller can dynamically reconfigure these pins as inputs or outputs by writing to the Configuration register. The Input and Output registers store the current state of each pin. The Polarity Inversion register allows to invert the polarity of the input pins, which can simplify logic in system by eliminating the need for external gates.

The device has an open-drain INT output that triggers when an input pin changes state. This interrupt can be connected to a microcontroller's interrupt pin, allowing the NCA6416 to notify the host of a change without the need for constant polling over the I<sup>2</sup>C bus. This feature makes the NCA6416 an efficient and passive I<sup>2</sup>C target device.

To recover from errors like I<sup>2</sup>C time-outs, a system controller can drive the RESET input low. This resets all registers to their default state and reinitializes the I<sup>2</sup>C/SMBus interface without requiring a power cycle.

A hardware ADDR pin allows to program the device's I<sup>2</sup>C address, making it possible to use up to two NCA6416 devices on a single bus.

In addition, each output pin on Port P can sink up to 25 mA, making it suitable for directly driving low-current loads like LEDs.

## 2. Features and benefits

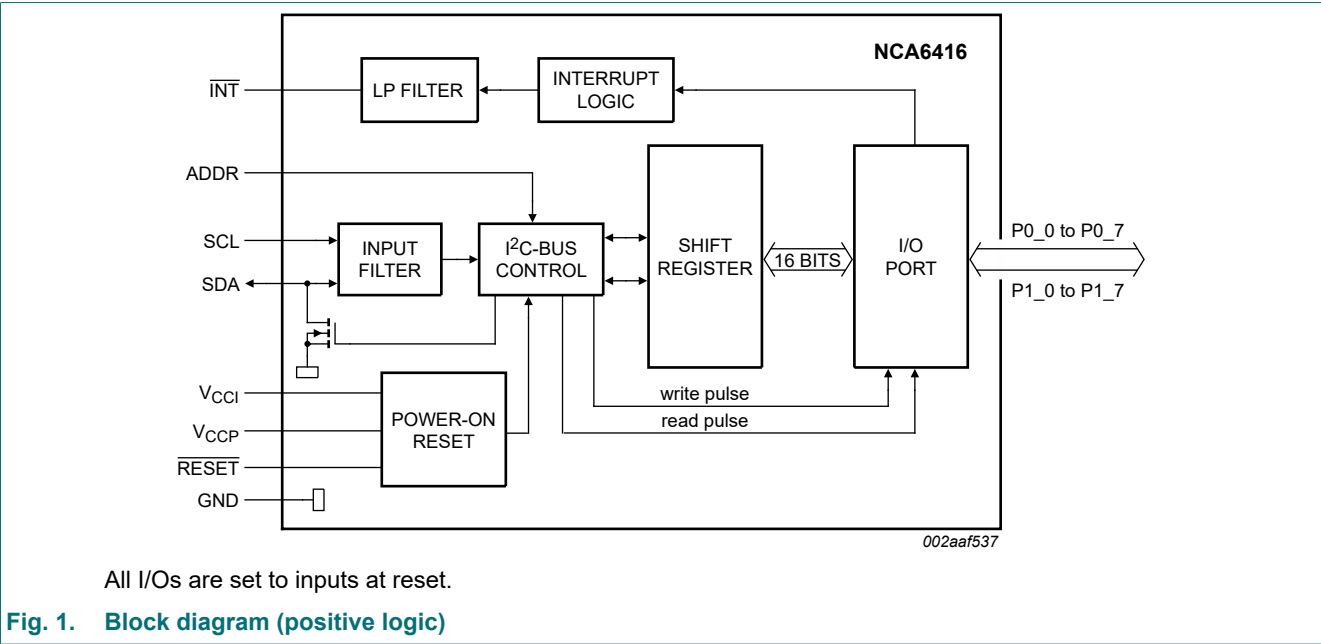
- I<sup>2</sup>C-bus to parallel port expander
- Supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- Low standby current consumption:
  - 1.5  $\mu$ A typical at 5 V  $V_{CC}$
  - 1.0  $\mu$ A typical at 3.3 V  $V_{CC}$
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - $V_{hys} = 0.18$  V (typical) at 1.8 V
  - $V_{hys} = 0.25$  V (typical) at 2.5 V
  - $V_{hys} = 0.33$  V (typical) at 3.3 V
  - $V_{hys} = 0.5$  V (typical) at 5 V
- 5 V tolerant I/O ports
- Active LOW reset input (RESET)
- Open-drain active LOW interrupt output (INT)
- 400 kHz Fast-mode I<sup>2</sup>C-bus
- Input/Output Configuration register
- Polarity Inversion register
- Internal power-on reset
- Glitch free power-up
- No power up sequence required
- Partial power down supported
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Packages offered: TSSOP24, HWQFN24
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">NCA6416PW</a>	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	<a href="#">SOT355-1</a>
<a href="#">NCA6416BY</a>	-40 °C to +125 °C	HWQFN24	plastic thermal enhanced very very thin Quad Flat packages; no leads; 24 terminals; 0.5 mm pitch; 4 × 4 × 0.75 mm body	<a href="#">SOT8041-1</a>

4. Block diagram



5. Pinning information

5.1. Pinning

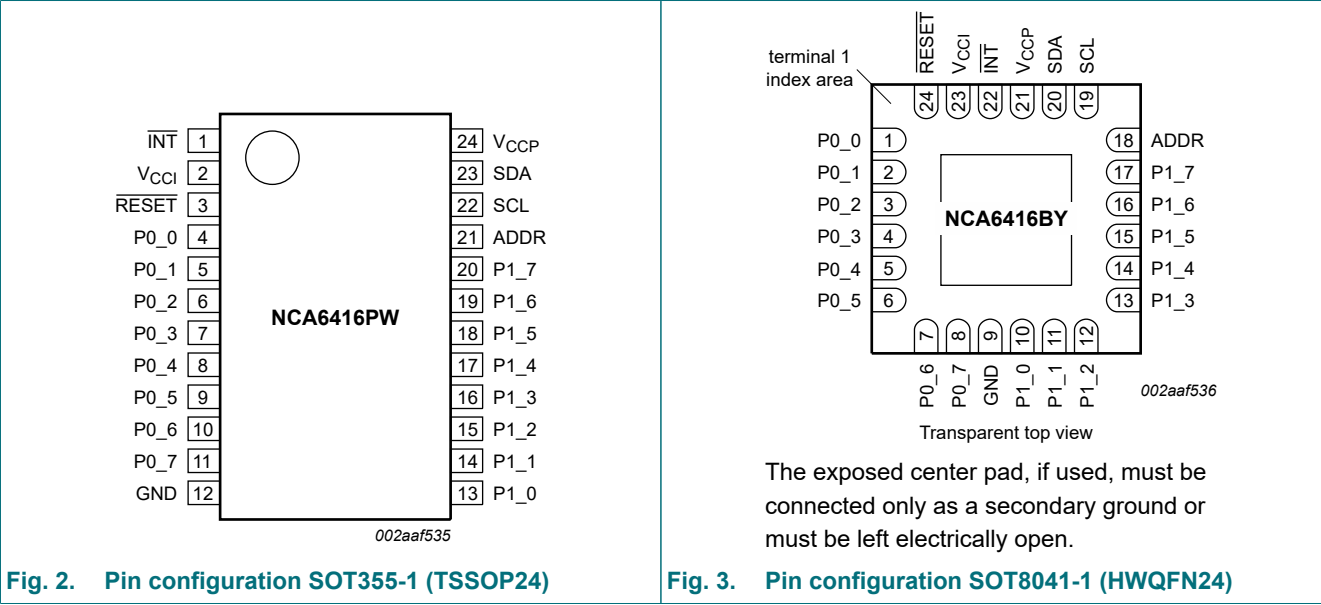


Fig. 2. Pin configuration SOT355-1 (TSSOP24)

Fig. 3. Pin configuration SOT8041-1 (HWQFN24)

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	TSSOP24	HWQFN24	
INT	1	22	Interrupt output. Connect to V <sub>CCI</sub> or V <sub>CCP</sub> through a pull-up resistor.
V <sub>CCI</sub>	2	23	Supply voltage of I <sup>2</sup> C-bus. Connect directly to the V <sub>CC</sub> of the external I <sup>2</sup> C controller. Provides voltage-level translation.
RESET	3	24	Active LOW reset input. Connect to V <sub>CCI</sub> through a pull-up resistor if no active connection is used.
P0_0 [1]	4	1	Port 0 input/output 0.
P0_1 [1]	5	2	Port 0 input/output 1.
P0_2 [1]	6	3	Port 0 input/output 2.
P0_3 [1]	7	4	Port 0 input/output 3.
P0_4 [1]	8	5	Port 0 input/output 4.
P0_5 [1]	9	6	Port 0 input/output 5.
P0_6 [1]	10	7	Port 0 input/output 6.
P0_7 [1]	11	8	Port 0 input/output 7.
GND	12	9	Ground.
P1_0 [2]	13	10	Port 1 input/output 0.
P1_1 [2]	14	11	Port 1 input/output 1.
P1_2 [2]	15	12	Port 1 input/output 2.
P1_3 [2]	16	13	Port 1 input/output 3.
P1_4 [2]	17	14	Port 1 input/output 4.
P1_5 [2]	18	15	Port 1 input/output 5.

Symbol	Pin		Description
	TSSOP24	HWQFN24	
P1_6 <a href="#">[2]</a>	19	16	Port 1 input/output 6.
P1_7 <a href="#">[2]</a>	20	17	Port 1 input/output 7.
ADDR	21	18	Address input. Connect directly to V <sub>CCP</sub> or ground.
SCL	22	19	Serial clock bus. Connect to V <sub>CCI</sub> through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to V <sub>CCI</sub> through a pull-up resistor.
V <sub>CCP</sub>	24	21	Supply voltage of NCA6416 for Port P.

[1] Pins P0\_0 to P0\_7 correspond to bits P0.0 to P0.7. At power-on, all I/O are configured as input.  
[2] Pins P1\_0 to P1\_7 correspond to bits P1.0 to P1.7. At power-on, all I/O are configured as input.

## 6. Voltage translation

[Table 3](#) shows how to set up V<sub>CC</sub> levels for the necessary voltage translation between the I<sup>2</sup>C-bus and the NCA6416.

Table 3. Voltage translation

V <sub>CCI</sub> (SDA and SCL of I <sup>2</sup> C controller)	V <sub>CCP</sub> (Port P)
1.8 V	1.8 V
1.8 V	2.5 V
1.8 V	3.3 V
1.8 V	5 V
2.5 V	1.8 V
2.5 V	2.5 V
2.5 V	3.3 V
2.5 V	5 V
3.3 V	1.8 V
3.3 V	2.5 V
3.3 V	3.3 V
3.3 V	5 V
5 V	1.8 V
5 V	2.5 V
5 V	3.3 V
5 V	5 V

## 7. Functional description

Refer to [Fig. 1](#) (Block diagram (positive logic)).

### 7.1. Device address

The address of the NCA6416 is shown in [Fig. 4](#).

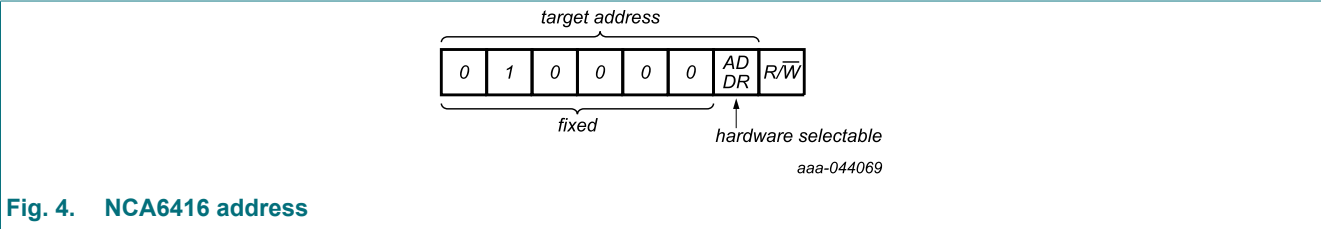


Fig. 4. NCA6416 address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible target addresses. The last bit of the target address ( $R/\overline{W}$ ) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

### 7.2. Interface definition

Table 4. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C-bus target address	L	H	L	L	L	L	ADDR	$R/\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

### 7.3. Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus controller sends a command byte, which is stored in the Pointer register in the NCA6416. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

Once a new command has been sent, the register that was last addressed continues to be accessed by reads until a new command byte is sent.

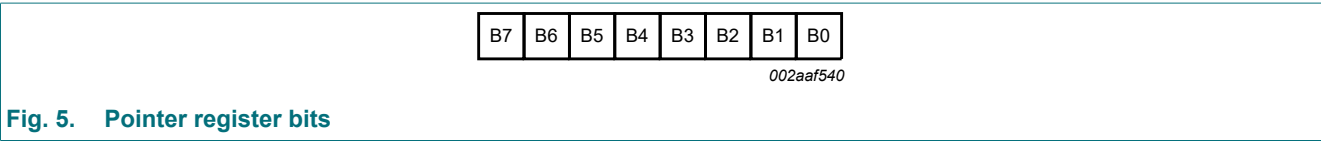


Fig. 5. Pointer register bits

Table 5. Command byte

Pointer register bits								Command byte	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx [1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx [1]
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111

[1] Undefined.

7.4. Register descriptions

7.4.1. Input port registers (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in [Section 8.2](#).

Table 6. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 7. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

7.4.2. Output port registers (02h, 03h)

The Output port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in [Section 8.1](#) and a register pair read is described in [Section 8.2](#).

Table 8. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 9. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

### 7.4.3. Polarity inversion registers (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write is described in [Section 8.1](#) and a register pair read is described in [Section 8.2](#).

**Table 10. Polarity inversion port 0 register (address 04h)**

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

**Table 11. Polarity inversion port 1 register (address 05h)**

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

### 7.4.4. Configuration registers (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in [Section 8.1](#) and a register pair read is described in [Section 8.2](#).

**Table 12. Configuration port 0 register (address 06h)**

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

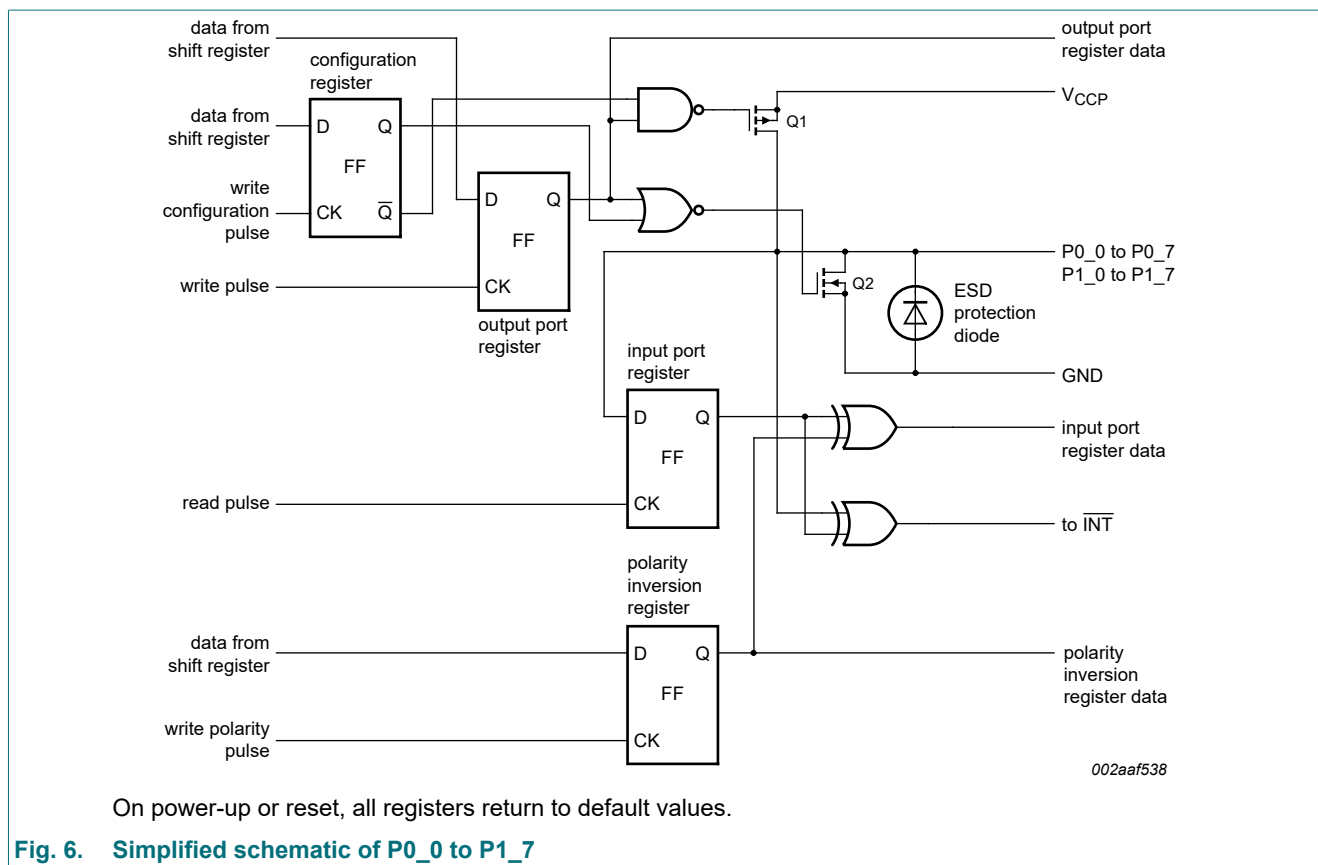
**Table 13. Configuration port 1 register (address 07h)**

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

## 7.5. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above  $V_{CCP}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{CCP}$  or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



**Fig. 6. Simplified schematic of P0\_0 to P1\_7**

## 7.6. Power-on reset

When power (from 0 V) is applied to  $V_{CCP}$ , an internal power-on reset holds the NCA6416 in a reset condition until  $V_{CCP}$  has reached  $V_{POR}$ . At that time, the reset condition is released and the NCA6416 registers and I<sup>2</sup>C-bus/SMBus state machine initializes to their default states. After that,  $V_{CCP}$  must be lowered to below  $V_{POR}$  and back up to the operating voltage for a power-reset cycle. See [Section 9.2](#) requirements".

## 7.7. Reset input ( $\overline{\text{RESET}}$ )

The  $\overline{\text{RESET}}$  input can be asserted to initialize the system while keeping the  $V_{CCP}$  at its operating level. A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of  $t_{w(\text{rst})}$ . The NCA6416 registers and I<sup>2</sup>C-bus/SMBus state machine are changed to their default state once  $\overline{\text{RESET}}$  is LOW (0). When  $\overline{\text{RESET}}$  is HIGH (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to  $V_{CCI}$  if no active connection is used.

## 7.8. Interrupt output ( $\overline{\text{INT}}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time  $t_{v(\text{INT})}$ , the signal  $\overline{\text{INT}}$  is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see [Fig. 10](#)). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ .

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The  $\overline{\text{INT}}$  output has an open-drain structure and requires pull-up resistor to  $V_{CCP}$  or  $V_{CCI}$  depending on the application.  $\overline{\text{INT}}$  should be connected to the voltage source of the device that requires the interrupt information.



## 8. Bus transactions

The NCA6416 is an I<sup>2</sup>C-bus target device. Data is exchanged between the controller and NCA6416 through write and read commands using I<sup>2</sup>C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 8.1. Write commands

Data is transmitted to the NCA6416 by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see [Fig. 4](#) for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the NCA6416 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion and configuration registers. After sending data to one register, the next data byte is sent to the other register in the pair (see [Fig. 7](#) and [Fig. 8](#)). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers or the host can simply update a single register.

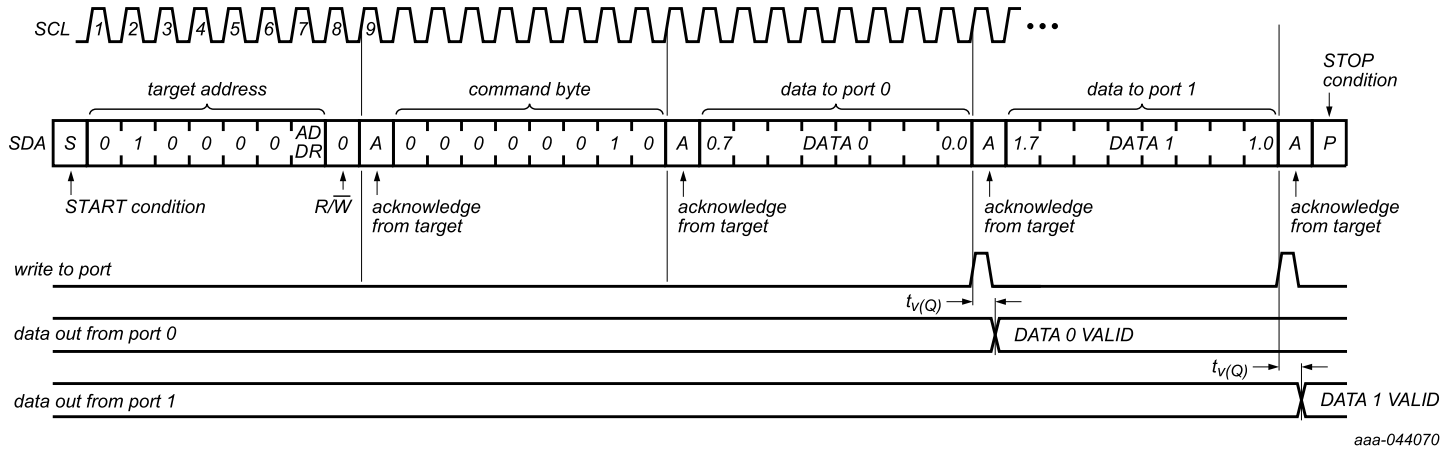


Fig. 7. Write to output port register

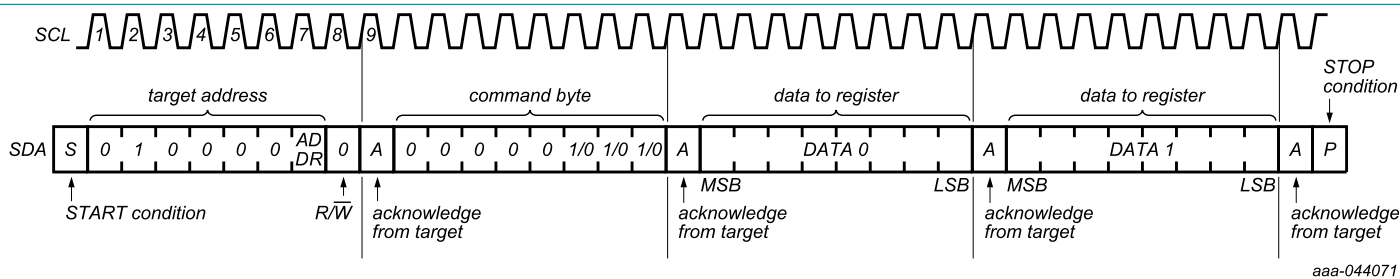


Fig. 8. Write to device registers

8.2. Read commands

To read data from the NCA6416, the bus controller must first send the NCA6416 address with the least significant bit set to a logic 0 (see Fig. 4 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the NCA6416 (see Fig. 9 and Fig. 10). Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus controller must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.

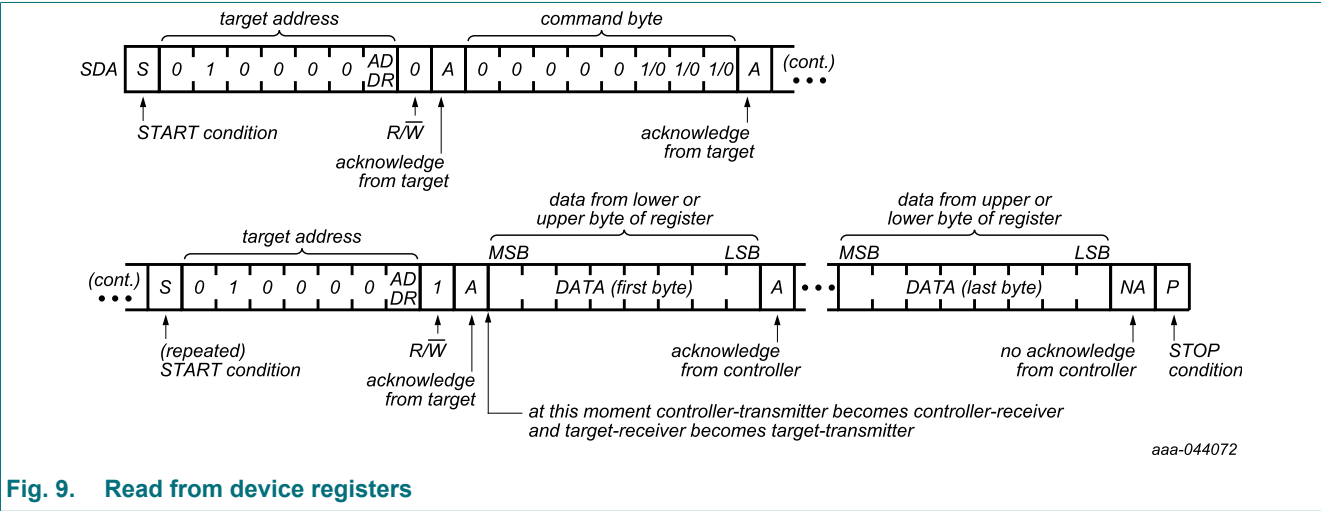
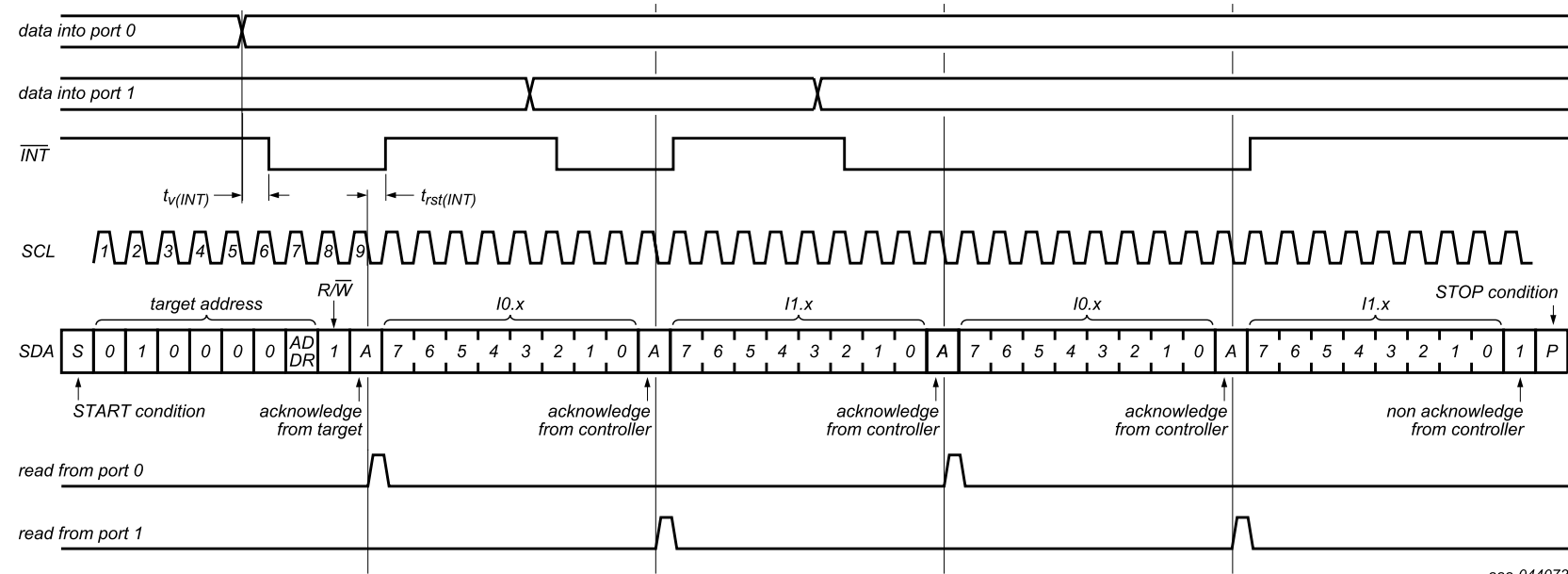
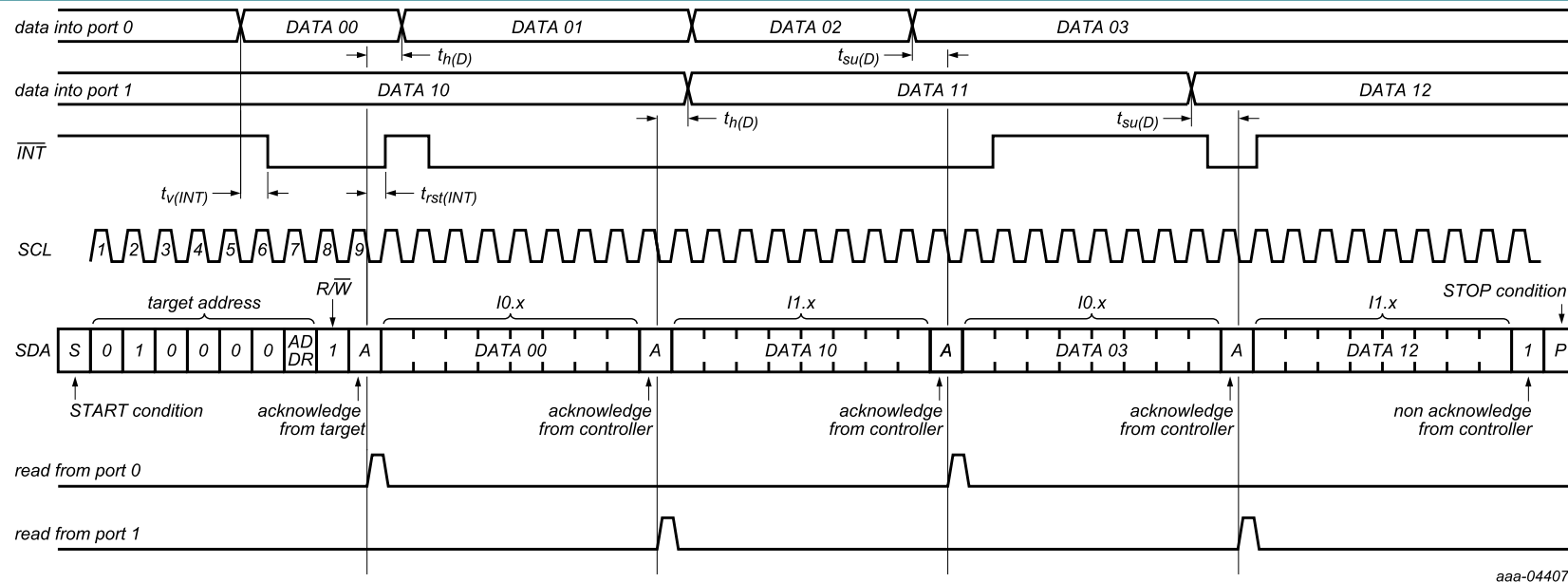


Fig. 9. Read from device registers



**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register). This figure eliminates the command byte transfer and a restart between the initial target address call and actual data transfer from P port (see Fig. 9).

Fig. 10. Read input port register, scenario 1



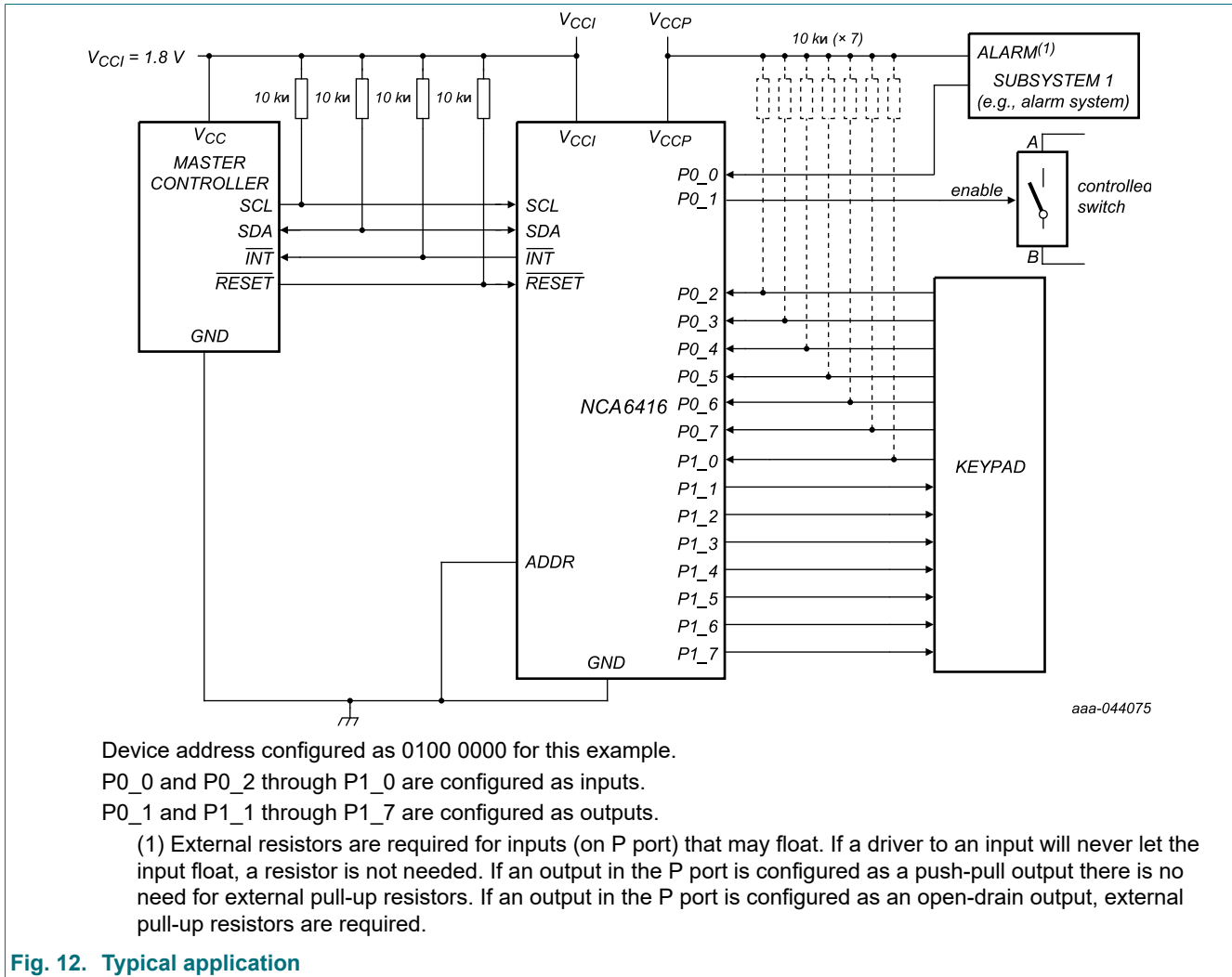
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**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial target address call and actual data transfer from P port (see [Fig. 9](#)).

**Fig. 11. Read input port register, scenario 2**

## 9. Application design-in information



**Fig. 12. Typical application**

### 9.1. Minimizing I<sub>CC</sub> when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>CCP</sub> through a resistor as shown in Fig. 12. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>CCP</sub>. The supply current, I<sub>CCP</sub>, increases as V<sub>I</sub> becomes lower than V<sub>CCP</sub>.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>CCP</sub> when the LED is off. Fig. 13 shows a high value resistor in parallel with the LED. Fig. 14 shows V<sub>CCP</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above V<sub>CCP</sub> and prevents additional supply current consumption when the LED is off.

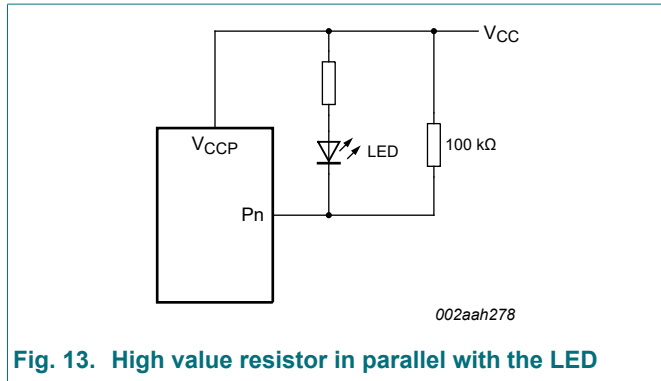


Fig. 13. High value resistor in parallel with the LED

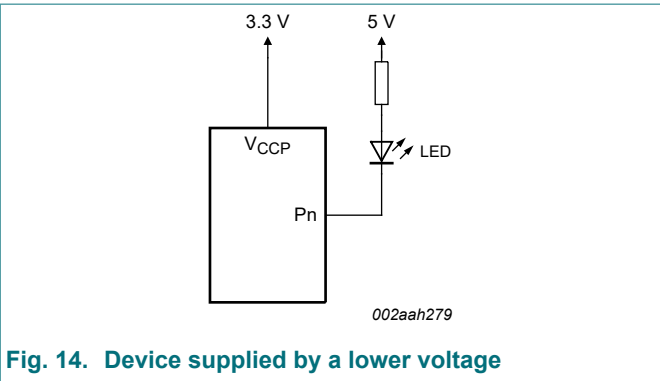


Fig. 14. Device supplied by a lower voltage

## 9.2. Power-on reset requirements

In the event of a glitch or data corruption, NCA6416 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The power-on reset is shown in Fig. 15.

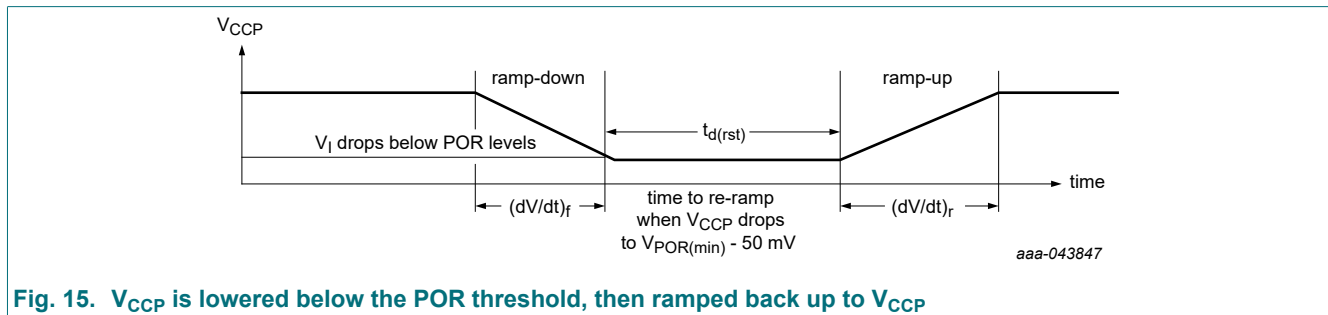
Fig. 15.  $V_{CCP}$  is lowered below the POR threshold, then ramped back up to  $V_{CCP}$ 

Table 14 specifies the performance of the power-on reset feature for NCA6416.

**Table 14. Recommended supply sequencing and ramp rates**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	see Fig. 15	0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	see Fig. 15	0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Fig. 15; re-ramp time when $V_{CCP}$ drops to $V_{POR(min)} - 50\text{ mV}$	1	-	-	$\mu\text{s}$
$\Delta V_{CC(gl)}$	glitch supply voltage difference	see Fig. 16 [1]	-	-	1.0	V
$t_{w(gl)VCC}$	supply voltage glitch pulse width	Fig. 17 [2]	-	-	10	$\mu\text{s}$
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{CCP}$	0.8	-	-	V
		rising $V_{CCP}$	-	-	1.6	V

[1] Level that  $V_{CCP}$  can glitch down to with a ramp rate at  $0.4\text{ }\mu\text{s/V}$ , but not cause a functional disruption when  $t_{w(gl)VCC} < 1\text{ }\mu\text{s}$ .

[2] Glitch width that will not cause a functional disruption when  $\Delta V_{CC(gl)} = 0.5 \times V_{CCP}$ .

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $t_{w(gl)VCC}$ ) and glitch height ( $\Delta V_{CC(gl)}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Fig. 16 and Table 14 provide more information on how to measure these specifications.

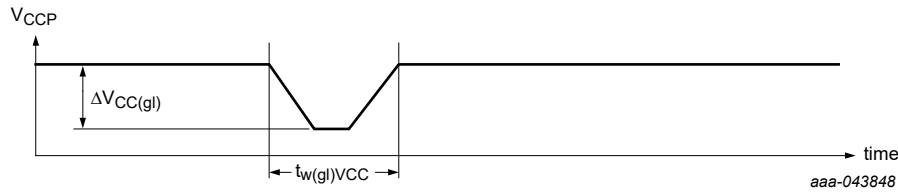
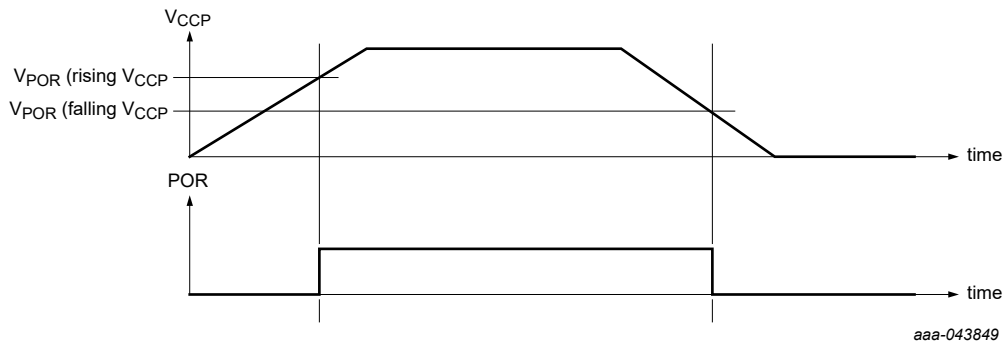


Fig. 16. Glitch width and glitch height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0 V. Fig. 17 and Table 14 provide more details on this specification.

Fig. 17. Power-on reset voltage ( $V_{POR}$ )

### 9.3. Partial power-down and power-up sequence

The NCA6416 has two supplies and a voltage translation function, translating between the I<sup>2</sup>C bus and the P-PORTs. Fig. 1 shows the block diagram that features a POWER-ON RESET block that senses both  $V_{CCI}$  and  $V_{CCP}$ . This is part of the implementation of the feature allowing partial power-down. Table 15 gives an overview of supply and reset condition combinations.

**Table 15. NCA6416 modes based on combinations of  $V_{CCI}$ ,  $V_{CCP}$  and RESET**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

$V_{CCI}$	$V_{CCP}$	RESET	Mode
L	L	X	Not functional
H	H	L	Reset
H	H	H	Functional
L	H	X	Partial power-down / Reset
H	L	X	Partial power-down / Reset

In the absence of both power supplies ( $V_{CCP}$  and  $V_{CCI}$ ), the product is non-functional. However, overvoltage protection on the P-PORTs remains permissible, consistent with other operational modes. The overvoltage protection ensures that when a P-PORT is biased with an input voltage ( $V_i$ ) exceeding  $V_{CCP}$ , input current is prevented. This protection is disabled only when a P-PORT is configured as an output in functional mode. When both  $V_{CCP}$  and  $V_{CCI}$  are present, the RESET signal determines the product's operational state, toggling between functional mode and reset mode. If  $V_{CCP}$  is present but  $V_{CCI}$  is absent, the product enters reset mode. In this state, configuration registers are initialized to their default values, configuring all P-PORTs as input ports, with their output drivers disabled. When  $V_{CCI}$  is present but  $V_{CCP}$  absent, the SDA and INT open drain drivers are off. In partial power-down scenarios, where only one supply is active, there is no risk of excessive current draw on the active supply. Section 13 provides  $I_{CC}$  specifications for both normal operation and partial power-down modes. The power supplies,  $V_{CCP}$  and  $V_{CCI}$ , can be sequenced (ramped-up or -down) in any order while output glitches are prevented. Regardless of the power-up sequence, the product initializes in its default state. Section 9.2 specifies a  $V_{CCP}$  power cycle procedure that ensures the product resets upon  $V_{CCP}$  power-up, initiating in the default state. During power-up, the RESET signal can be pulled HIGH to enable functional mode at startup. Alternatively, if RESET is pulled LOW during power-up, the product remains in reset (disabled) mode. De-asserting RESET subsequently transitions the product to functional mode. Section 7.2 provides a detailed description of the RESET function.



## 10. Limiting values

**Table 16. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCI</sub>	I <sup>2</sup> C-bus supply voltage		-0.5	+6.5	V
V <sub>CCP</sub>	supply voltage port P		-0.5	+6.5	V
V <sub>I</sub>	input voltage	[1]	-0.5	+6.5	V
V <sub>O</sub>	output voltage	[1]	-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	ADDR, RESET, SCL; V <sub>I</sub> < 0 V	-	±20	mA
I <sub>OK</sub>	output clamping current	INT; V <sub>O</sub> < 0 V	-	±20	mA
I <sub>IOK</sub>	input/output clamping current	P port; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CCP</sub>	-	±20	mA
		SDA; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CCI</sub>	-	±20	mA
I <sub>OL</sub>	LOW-level output current	continuous; P port; V <sub>O</sub> = 0 V to V <sub>CCP</sub>	-	50	mA
		continuous; SDA, INT; V <sub>O</sub> = 0 V to V <sub>CCI</sub>	-	25	mA
I <sub>OH</sub>	HIGH-level output current	continuous; P port; V <sub>O</sub> = 0 V to V <sub>CCP</sub>	-	25	mA
I <sub>CC</sub>	supply current	continuous through GND	-	200	mA
I <sub>CCP</sub>	supply current port P	continuous through V <sub>CCP</sub>	-	160	mA
I <sub>CCI</sub>	I <sup>2</sup> C-bus supply current	continuous through V <sub>CCI</sub>	-	10	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j(max)</sub>	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 11. Recommended operating conditions

**Table 17. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCI</sub>	I <sup>2</sup> C-bus supply voltage		1.65	5.5	V
V <sub>CCP</sub>	supply voltage port P		1.65	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	SCL, SDA, RESET	0.7 × V <sub>CCI</sub>	5.5	V
		ADDR, P1_7 to P0_0	0.7 × V <sub>CCP</sub>	5.5	V
V <sub>IL</sub>	LOW-level input voltage	SCL, SDA, RESET	-0.5	0.3 × V <sub>CCI</sub>	V
		ADDR, P1_7 to P0_0	-0.5	0.3 × V <sub>CCP</sub>	V
I <sub>OH</sub>	HIGH-level output current	P1_7 to P0_0	-	10	mA
I <sub>OL</sub>	LOW-level output current	P1_7 to P0_0	-	25	mA
T <sub>amb</sub>	ambient temperature	operating in free air	-40	+125	°C

## 12. Thermal characteristics

**Table 18. Thermal characteristics**

Symbol	Parameter	Conditions	Max	Unit
Z <sub>th(j-a)</sub>	transient thermal impedance from junction to ambient	TSSOP24 package [1]	88	K/W
		HWQFN24 package [1]	66	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

## 13. Static characteristics

**Table 19. Static characteristics**
 $V_{CCI} = 1.65\text{ V to }5.5\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IK}$	input clamping voltage	$I_I = -18\text{ mA}$	-1.2	-	-	-1.2	-	V
$V_{POR}$	power-on reset voltage	$V_I = V_{CCP}$ or GND; $I_O = 0\text{ mA}$						
		Falling $V_{CCP}$	0.8	1.1	-	0.8	-	V
		Rising $V_{CCP}$	-	1.25	1.55	-	1.6	V
$V_{OH}$	HIGH-level output voltage	P port						
		$I_{OH} = -8\text{ mA}$ ; $V_{CCP} = 1.65\text{ V}$ [2]	1.2	-	-	1.2	-	V
		$I_{OH} = -10\text{ mA}$ ; $V_{CCP} = 1.65\text{ V}$ [2]	1.1	-	-	1.1	-	V
		$I_{OH} = -8\text{ mA}$ ; $V_{CCP} = 2.3\text{ V}$ [2]	1.8	-	-	1.8	-	V
		$I_{OH} = -10\text{ mA}$ ; $V_{CCP} = 2.3\text{ V}$ [2]	1.7	-	-	1.7	-	V
		$I_{OH} = -8\text{ mA}$ ; $V_{CCP} = 3.0\text{ V}$ [2]	2.6	-	-	2.6	-	V
		$I_{OH} = -10\text{ mA}$ ; $V_{CCP} = 3.0\text{ V}$ [2]	2.5	-	-	2.5	-	V
		$I_{OH} = -8\text{ mA}$ ; $V_{CCP} = 4.5\text{ V}$ [2]	4.1	-	-	4.1	-	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 8\text{ mA}$						
		$V_{CCP} = 1.65\text{ V}$ [2]	-	-	0.45	-	0.45	V
		$V_{CCP} = 2.3\text{ V}$ [2]	-	-	0.25	-	0.25	V
		$V_{CCP} = 3\text{ V}$ [2]	-	-	0.25	-	0.25	V
		$V_{CCP} = 4.5\text{ V}$ [2]	-	-	0.2	-	0.2	V
		P port; $I_{OL} = 10\text{ mA}$						
		$V_{CCP} = 1.65\text{ V}$ [2]	-	-	0.6	-	0.6	V
		$V_{CCP} = 2.3\text{ V}$ [2]	-	-	0.3	-	0.3	V
		$V_{CCP} = 3\text{ V}$ [2]	-	-	0.25	-	0.25	V
		$V_{CCP} = 4.5\text{ V}$ [2]	-	-	0.2	-	0.2	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$ ; $V_{CCP} = 1.65\text{ V to }5.5\text{ V}$						
		SDA [3]	3	-	-	3	-	mA
		INT [3]	3	15 [4]	-	3	-	mA
		P port						
		$V_{OL} = 0.5\text{ V}$ ; $V_{CCP} = 1.65\text{ V}$ [3]	8	-	-	8	-	mA
		$V_{OL} = 0.7\text{ V}$ ; $V_{CCP} = 1.65\text{ V}$ [3]	10	-	-	10	-	mA
		$V_{OL} = 0.5\text{ V}$ ; $V_{CCP} = 2.3\text{ V}$ [3]	8	-	-	8	-	mA
		$V_{OL} = 0.7\text{ V}$ ; $V_{CCP} = 2.3\text{ V}$ [3]	10	-	-	10	-	mA
		$V_{OL} = 0.5\text{ V}$ ; $V_{CCP} = 3.0\text{ V}$ [3]	8	-	-	8	-	mA
		$V_{OL} = 0.7\text{ V}$ ; $V_{CCP} = 3.0\text{ V}$ [3]	10	-	-	10	-	mA
		$V_{OL} = 0.5\text{ V}$ ; $V_{CCP} = 4.5\text{ V}$ [3]	8	-	-	8	-	mA
		$V_{OL} = 0.7\text{ V}$ ; $V_{CCP} = 4.5\text{ V}$ [3]	10	-	-	10	-	mA
$I_I$	input current	$V_{CCP} = 1.65\text{ V to }5.5\text{ V}$						
		SCL, SDA, RESET; $V_I = V_{CCI}$ or GND	-	-	±1	-	±1	µA
		ADDR; $V_I = V_{CCP}$ or GND	-	-	±1	-	±1	µA

Low-voltage translating 16-bit I<sup>2</sup>C-bus/SMBus I/O expander

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I <sub>IH</sub>	HIGH-level input current	P port; V <sub>I</sub> = V <sub>CCP</sub> ; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	-	1	-	1	μA
I <sub>IL</sub>	LOW-level input current	P port; V <sub>I</sub> = GND; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	-	1	-	1	μA
I <sub>CC</sub>	supply current	I <sub>CCI</sub> + I <sub>CCP</sub> ; SDA, P port, ADDR, RESET; V <sub>I</sub> on SDA and RESET = V <sub>CCI</sub> or GND; V <sub>I</sub> on P port and ADDR = V <sub>CCP</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 400 kHz						
		V <sub>CCP</sub> = 3.6 V to 5.5 V	-	10	25	-	27	μA
		V <sub>CCP</sub> = 2.3 V to 3.6 V	-	6.5	15	-	17	μA
		V <sub>CCP</sub> = 1.65 V to 2.3 V	-	4	11	-	13	μA
		I <sub>CCI</sub> + I <sub>CCP</sub> ; SCL, SDA, P port, ADDR, RESET; V <sub>I</sub> on SCL, SDA and RESET = V <sub>CCI</sub> or GND; V <sub>I</sub> on P port and ADDR = V <sub>CCP</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 0 kHz						
		V <sub>CCP</sub> = 3.6 V to 5.5 V	-	1.5	3.5	-	8	μA
		V <sub>CCP</sub> = 2.3 V to 3.6 V	-	1	2.0	-	5	μA
		V <sub>CCP</sub> = 1.65 V to 2.3 V	-	0.5	1.5	-	2.5	μA
		Active mode; I <sub>CCI</sub> + I <sub>CCP</sub> ; P port, ADDR, RESET; V <sub>I</sub> on RESET = V <sub>CCI</sub> ; V <sub>I</sub> on P port and ADDR = V <sub>CCP</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 400 kHz, continuous register read						
		V <sub>CCP</sub> = 3.6 V to 5.5 V	-	21	40	-	40	μA
		V <sub>CCP</sub> = 2.3 V to 3.6 V	-	12	22	-	25	μA
		V <sub>CCP</sub> = 1.65 V to 2.3 V	-	8	16	-	18	μA
I <sub>CCI</sub>	supply current	Partial power-down V <sub>CCP</sub> = 3.6 V; V <sub>CCI</sub> = 1.65 V to 5.5 V	-	-	1	-	1	μA
I <sub>CCP</sub>	supply current	Partial power-down V <sub>CCI</sub> = 3.6 V; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	-	1	-	3	μA
ΔI <sub>CC</sub>	additional quiescent supply current	SCL, SDA, RESET; one input at V <sub>CCI</sub> - 0.6 V, other inputs at V <sub>CCI</sub> or GND; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	-	5	-	10	μA
		P port, ADDR; one input at V <sub>CCP</sub> - 0.6 V, other inputs at V <sub>CCP</sub> or GND; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	-	5	-	10	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>CCI</sub> or GND; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	2	2.5	-	3.5	pF
C <sub>io</sub>	input/output capacitance	SDA; V <sub>I/O</sub> = V <sub>CCI</sub> or GND; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	2	3	-	4	pF
		P port; V <sub>I/O</sub> = V <sub>CCP</sub> or GND; V <sub>CCP</sub> = 1.65 V to 5.5 V	-	4.5	5.5	-	6	pF

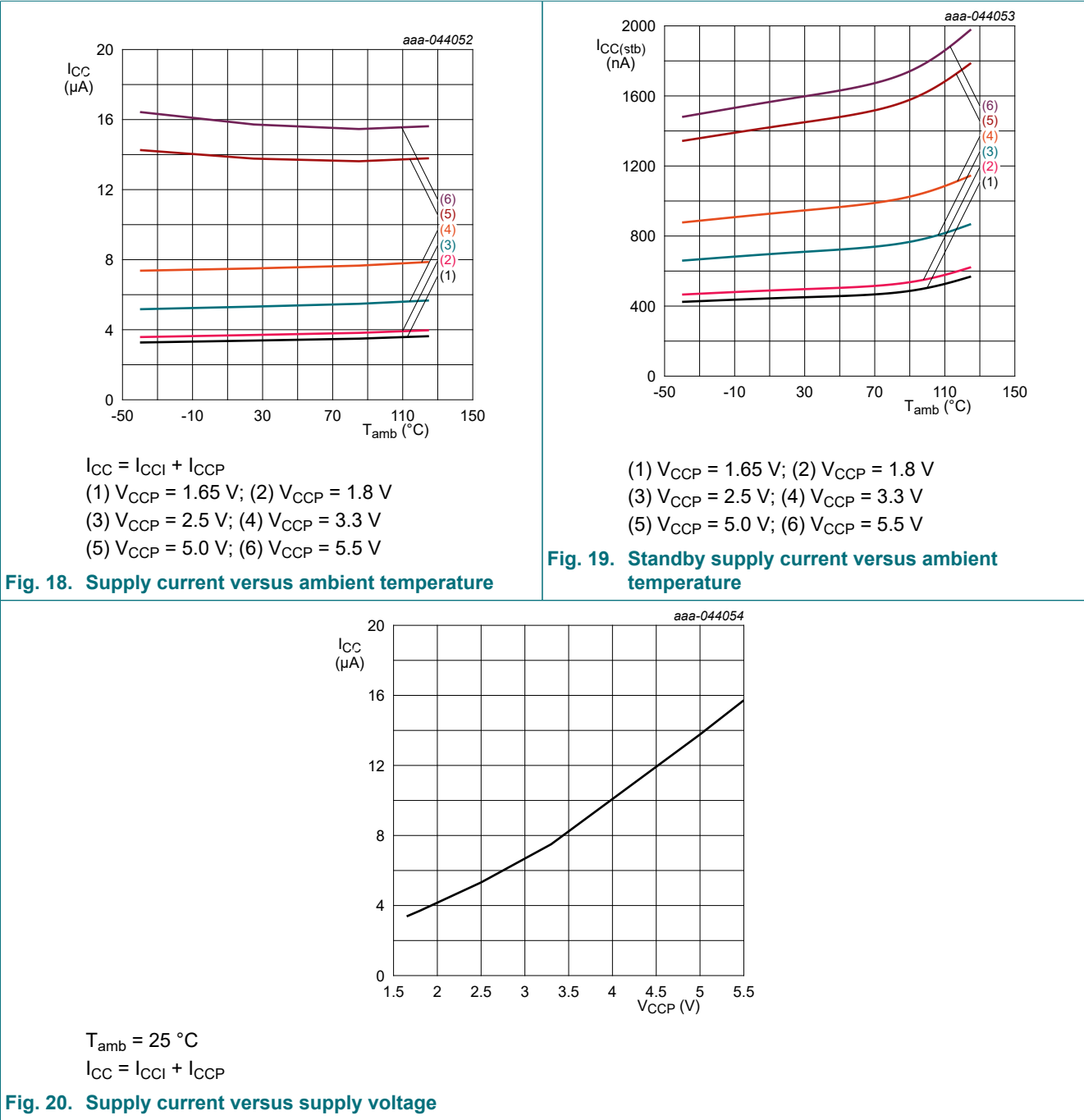
[1] For I<sub>CC</sub>, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V<sub>CC</sub>) and T<sub>amb</sub> = 25 °C. Except for I<sub>CC</sub>, the typical values are at V<sub>CCP</sub> = V<sub>CCI</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

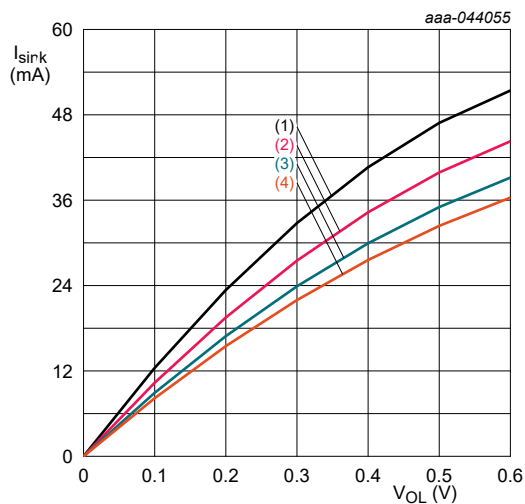
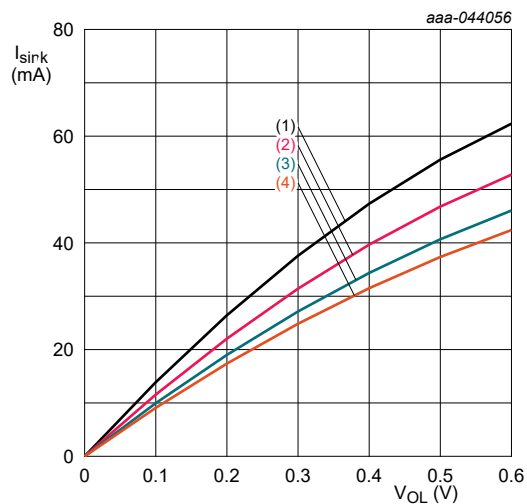
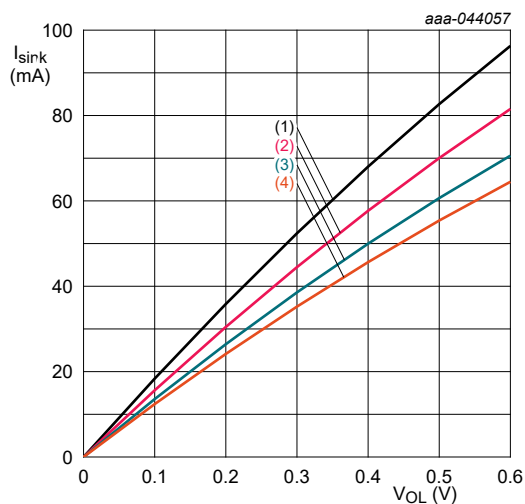
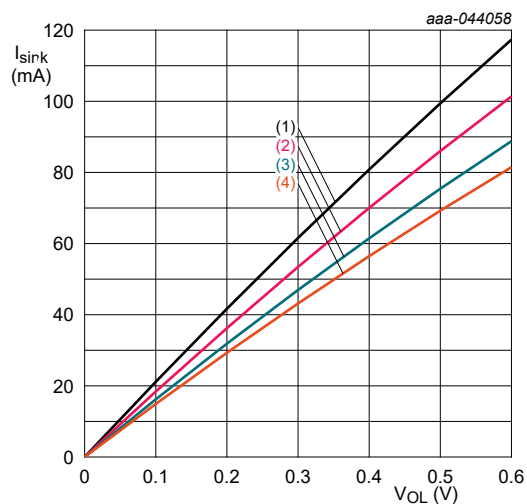
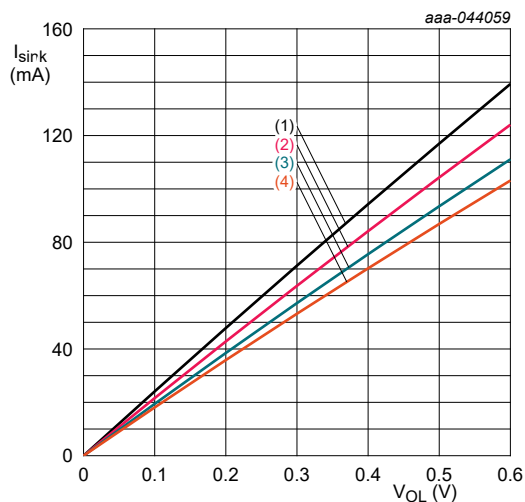
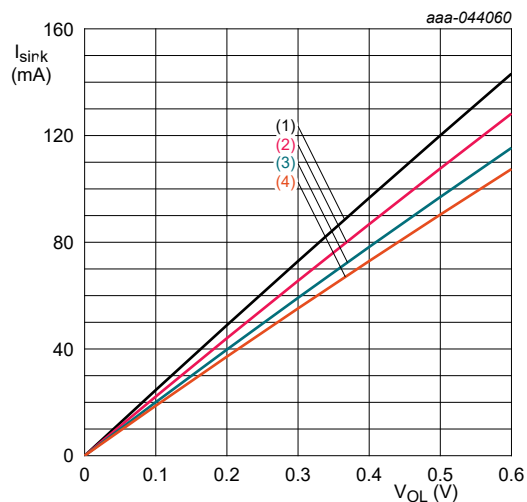
[2] The total current sourced by all I/Os must be limited to 160 mA.

[3] Each I/O must be externally limited to a maximum of 25 mA, for a device total of 200 mA.

[4] Typical value for T<sub>amb</sub> = 25 °C. V<sub>OL</sub> = 0.4 V and V<sub>CC</sub> = 3.3 V. Typical value for V<sub>CC</sub> < 2.5 V, V<sub>OL</sub> = 0.6 V.

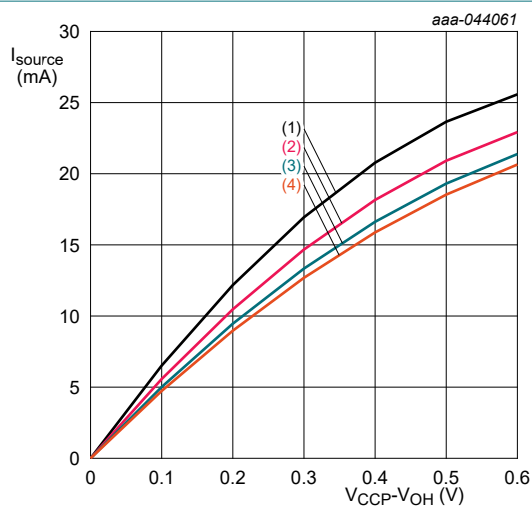
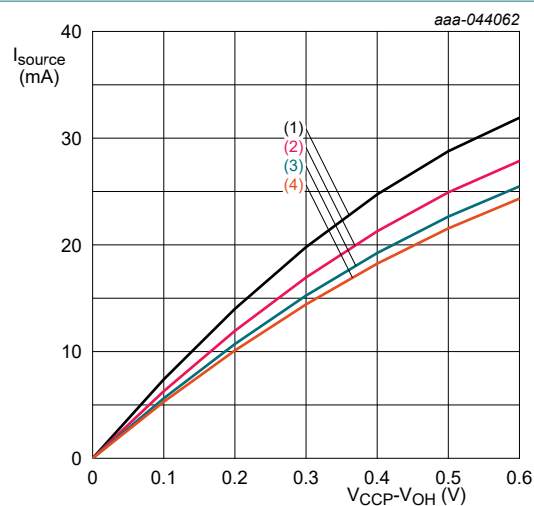
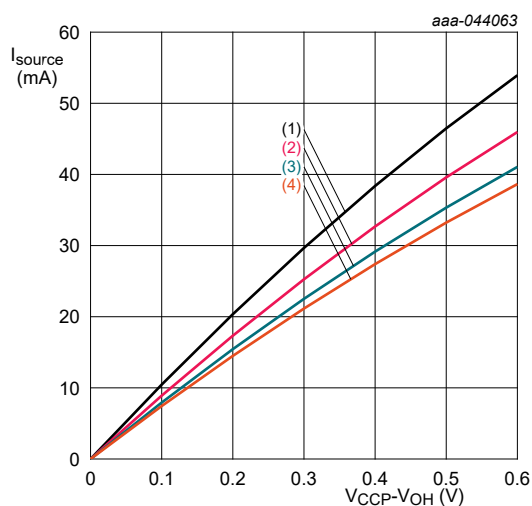
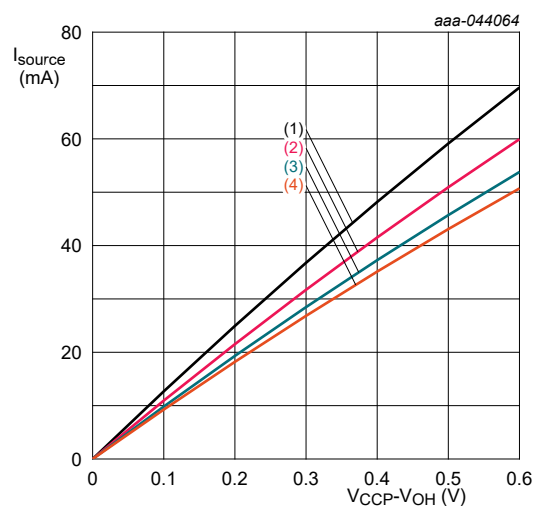
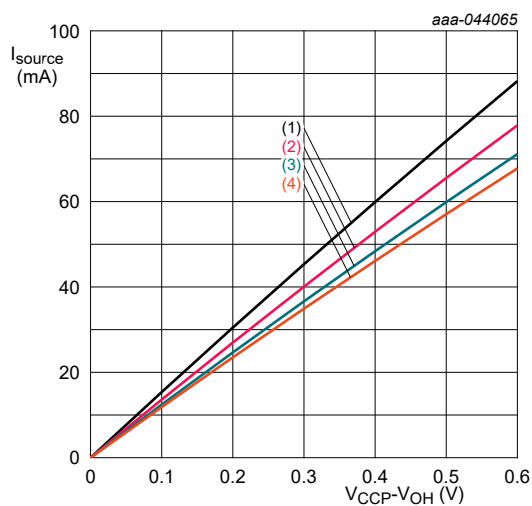
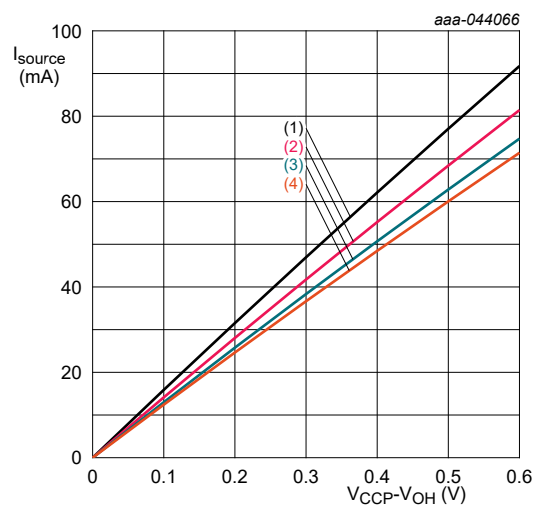
13.1. Typical characteristics



a.  $V_{CCP} = 1.65 \text{ V}$ b.  $V_{CCP} = 1.8 \text{ V}$ c.  $V_{CCP} = 2.5 \text{ V}$ d.  $V_{CCP} = 3.3 \text{ V}$ e.  $V_{CCP} = 5.0 \text{ V}$ f.  $V_{CCP} = 5.5 \text{ V}$ 

(1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$ , (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 85 \text{ }^{\circ}\text{C}$ , (4)  $T_{amb} = 125 \text{ }^{\circ}\text{C}$

Fig. 21. I/O sink current versus LOW-level output voltage

a.  $V_{CCP} = 1.65 \text{ V}$ b.  $V_{CCP} = 1.8 \text{ V}$ c.  $V_{CCP} = 2.5 \text{ V}$ d.  $V_{CCP} = 3.3 \text{ V}$ e.  $V_{CCP} = 5.0 \text{ V}$ f.  $V_{CCP} = 5.5 \text{ V}$ 

(1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$ , (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 85 \text{ }^{\circ}\text{C}$ , (4)  $T_{amb} = 125 \text{ }^{\circ}\text{C}$

Fig. 22. I/O source current versus HIGH-level output voltage

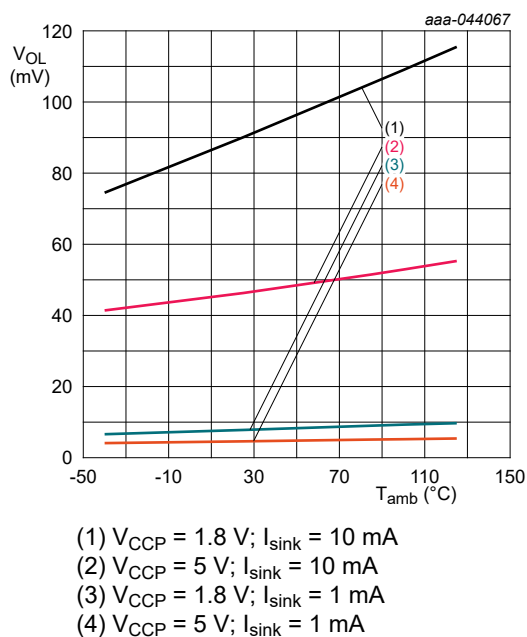


Fig. 23. LOW-level output voltage versus temperature

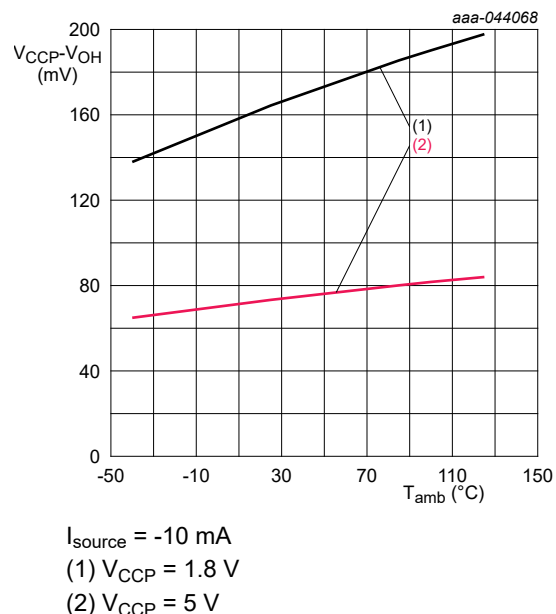


Fig. 24. I/O high voltage versus temperature

## 14. Dynamic characteristics

Table 20. I<sup>2</sup>C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Fig. 26.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$f_{\text{SCL}}$	SCL clock frequency		0	100	0	400	kHz
$t_{\text{HIGH}}$	HIGH period of the SCL clock		4	-	0.6	-	$\mu\text{s}$
$t_{\text{LOW}}$	LOW period of the SCL clock		4.7	-	1.3	-	$\mu\text{s}$
$t_{\text{SP}}$	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{\text{SU,DAT}}$	data set-up time		250	-	100	-	ns
$t_{\text{HD,DAT}}$	data hold time		0	-	0	-	ns
$t_{\text{r}}$	rise time of both SDA and SCL signals		-	1000	20	300	ns
$t_{\text{f}}$	fall time of both SDA and SCL signals		-	300	$20 \times (V_{\text{CC}} / 5.5\text{ V})$	300	ns
$t_{\text{BUF}}$	bus free time between a STOP and START condition		4.7	-	1.3	-	$\mu\text{s}$
$t_{\text{SU,STA}}$	set-up time for a repeated START condition		4.7	-	0.6	-	$\mu\text{s}$
$t_{\text{HD,STA}}$	hold time (repeated) START condition		4	-	0.6	-	$\mu\text{s}$
$t_{\text{SU,STO}}$	set-up time for STOP condition		4	-	0.6	-	$\mu\text{s}$
$t_{\text{VD,DAT}}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	$\mu\text{s}$
$t_{\text{VD,ACK}}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	$\mu\text{s}$

Table 21. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Fig. 28.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
t <sub>w(rst)</sub>	reset pulse width		6	-	6	-	ns
t <sub>rec(rst)</sub>	reset recovery time		0	-	0	-	ns
t <sub>rst</sub>	reset time	[1]	600	-	600	-	ns

[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

Table 22. Switching characteristics

Over recommended operating free air temperature range; C<sub>L</sub> ≤ 100 pF; unless otherwise specified. See Fig. 27.

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
t <sub>v(INT)</sub>	valid time on pin INT	from P port to INT	-	1	-	1	μs
t <sub>rst(INT)</sub>	reset time on pin INT	from SCL to INT	-	1	-	1	μs
t <sub>v(Q)</sub>	data output valid time	from SCL to P port	-	400	-	400	ns
t <sub>su(D)</sub>	data input set-up time	from P port to SCL	0	-	0	-	ns
t <sub>h(D)</sub>	data input hold time	from P port to SCL	300	-	300	-	ns



15. Parameter measurement information

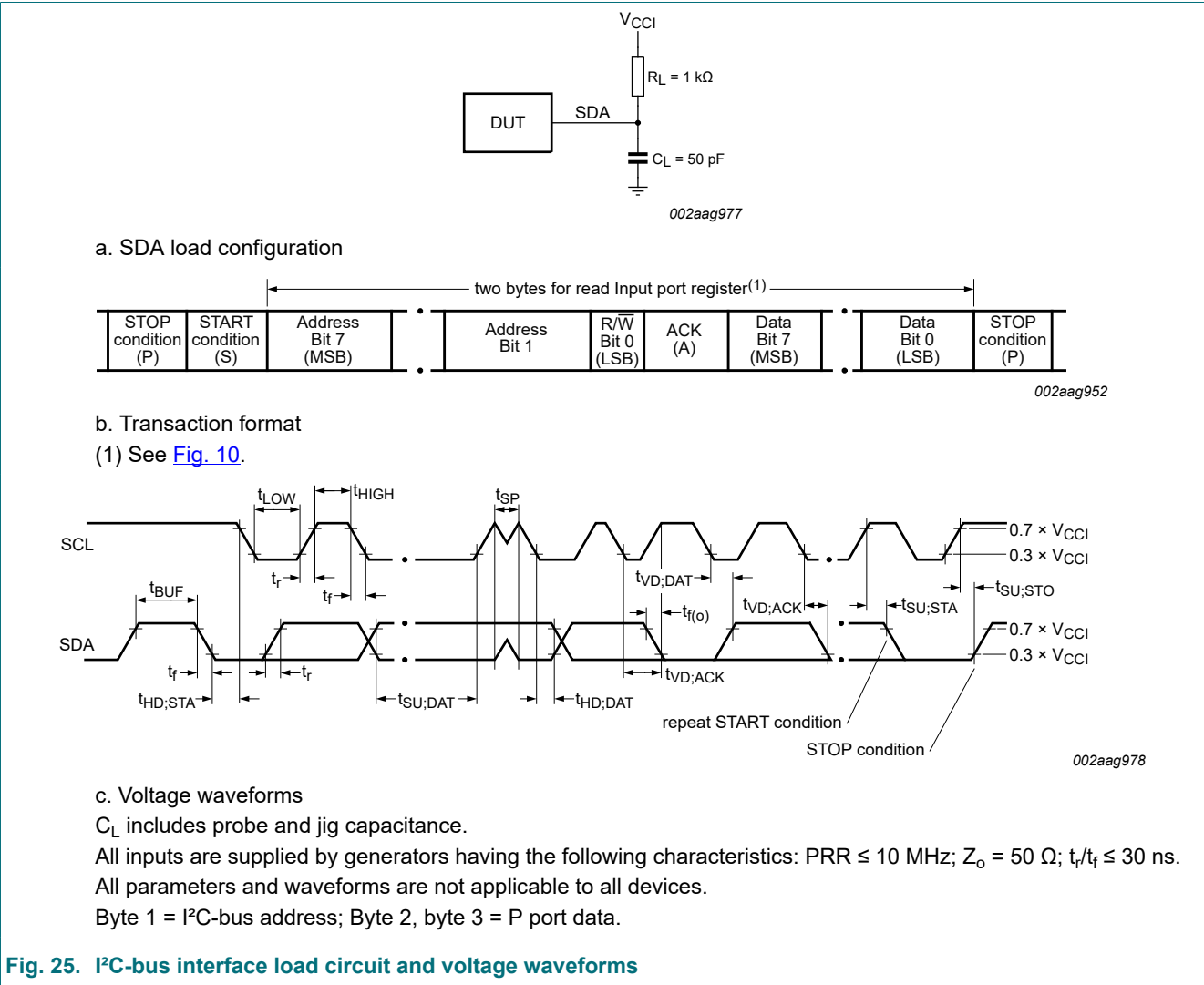
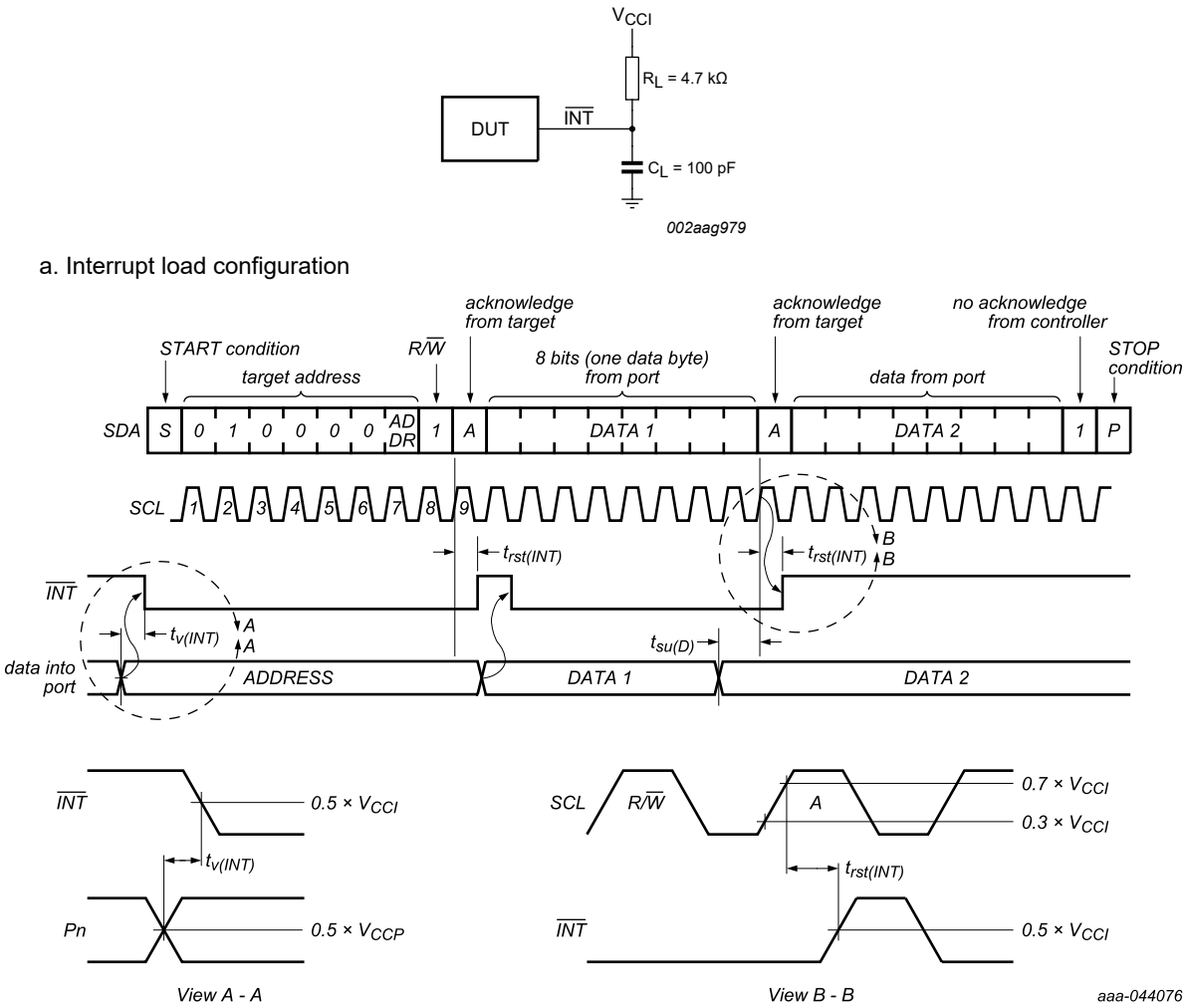


Fig. 25. I<sup>2</sup>C-bus interface load circuit and voltage waveforms



b. Voltage waveforms

$C_L$  includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30$  ns.

All parameters and waveforms are not applicable to all devices.

Fig. 26. Interrupt load circuit and voltage waveforms

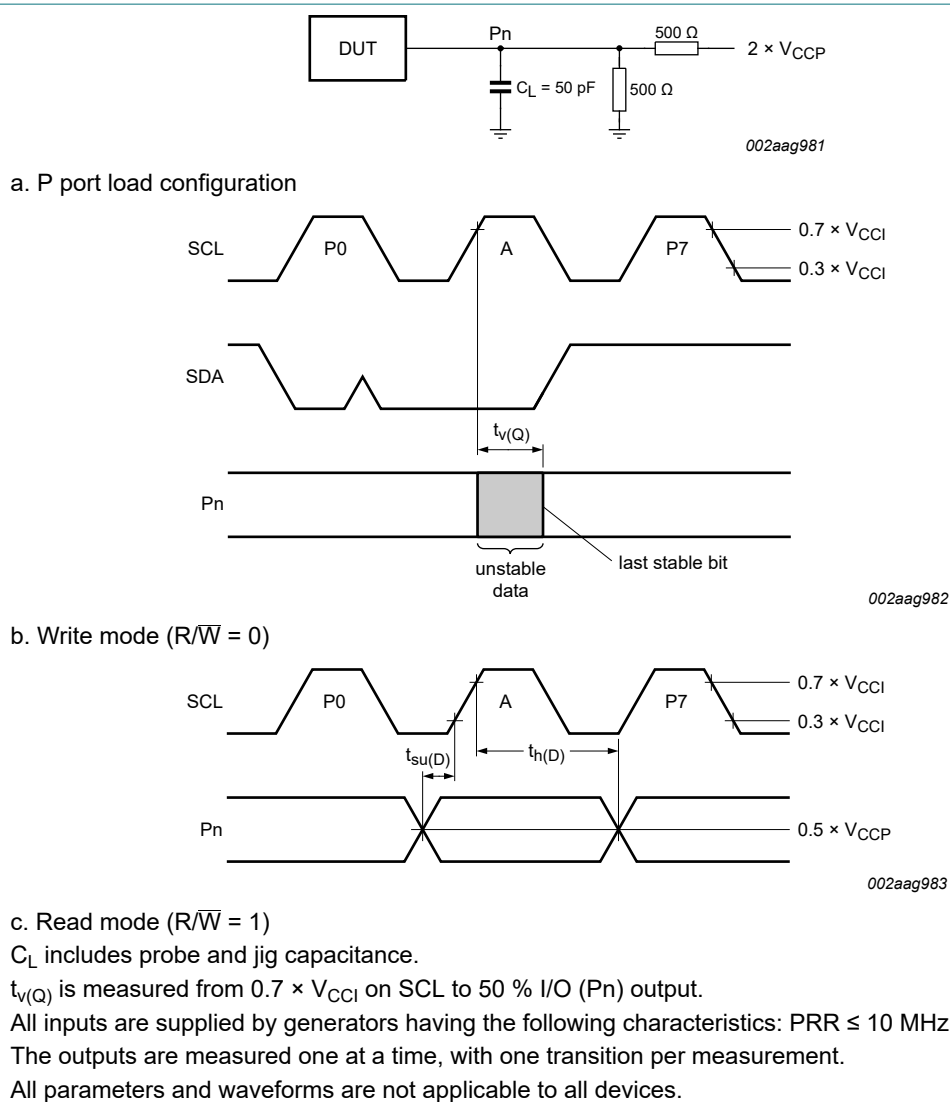
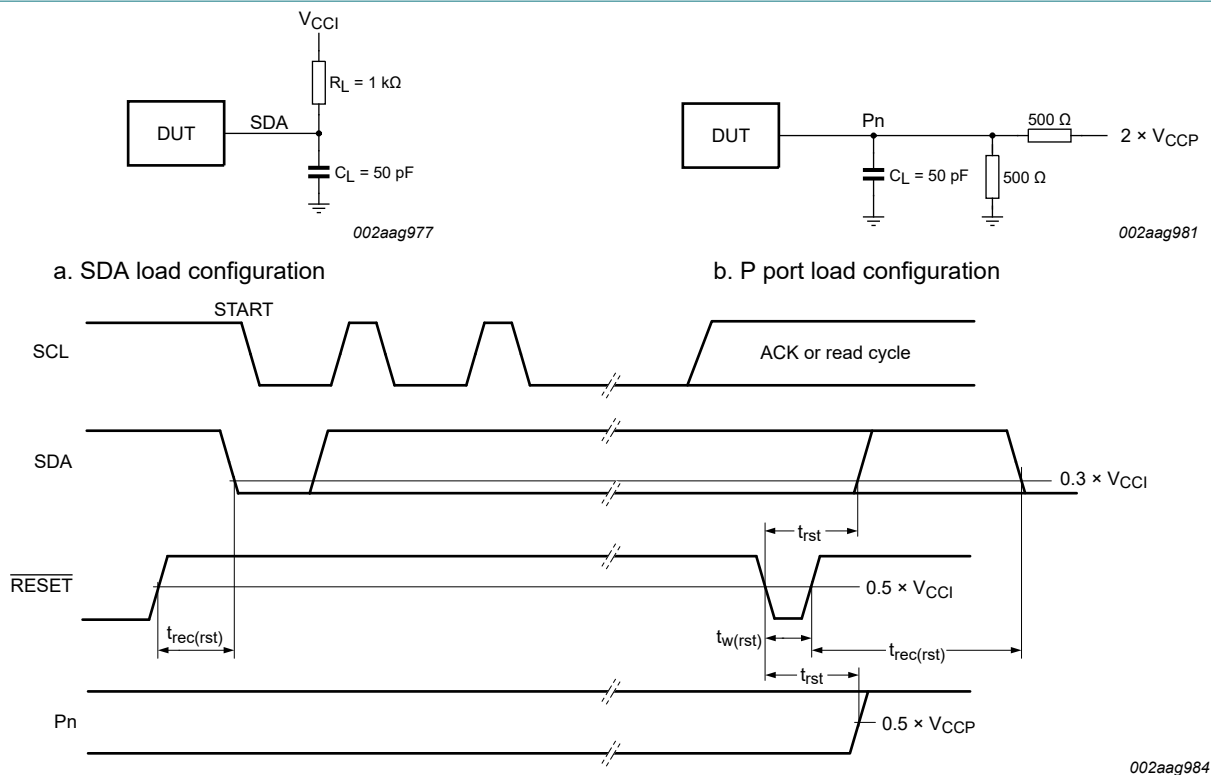


Fig. 27. P port load circuit and voltage waveforms



#### c. RESET timing

$C_L$  includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30$  ns.

The outputs are measured one at a time, with one transition per measurement.

I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

**Fig. 28. Reset load circuits and voltage waveforms**

16. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

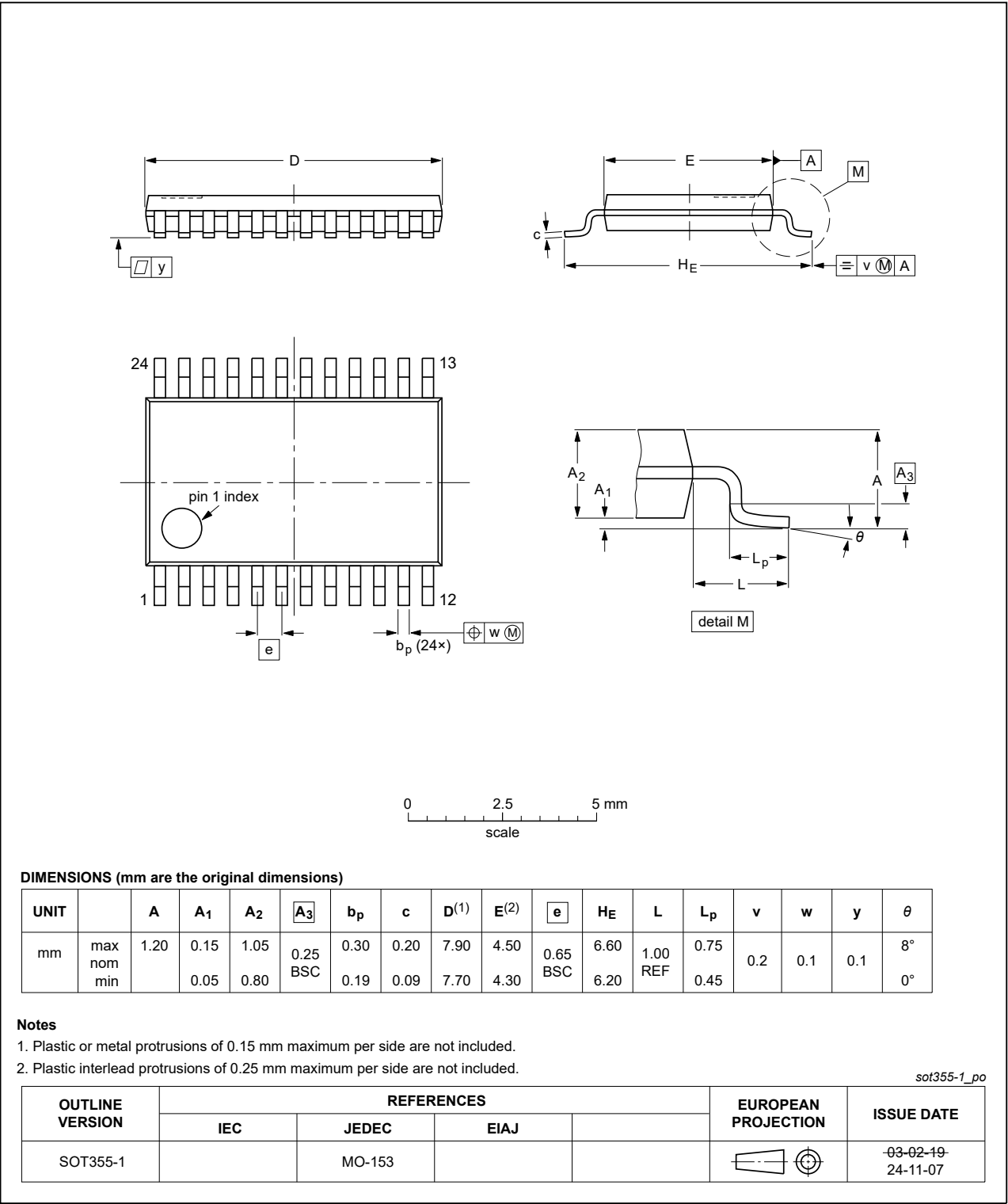


Fig. 29. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin Quad Flat packages, no leads;  
24 terminals; 0.5 mm pitch; 4 x 4 x 0.75 mm body

SOT8041-1

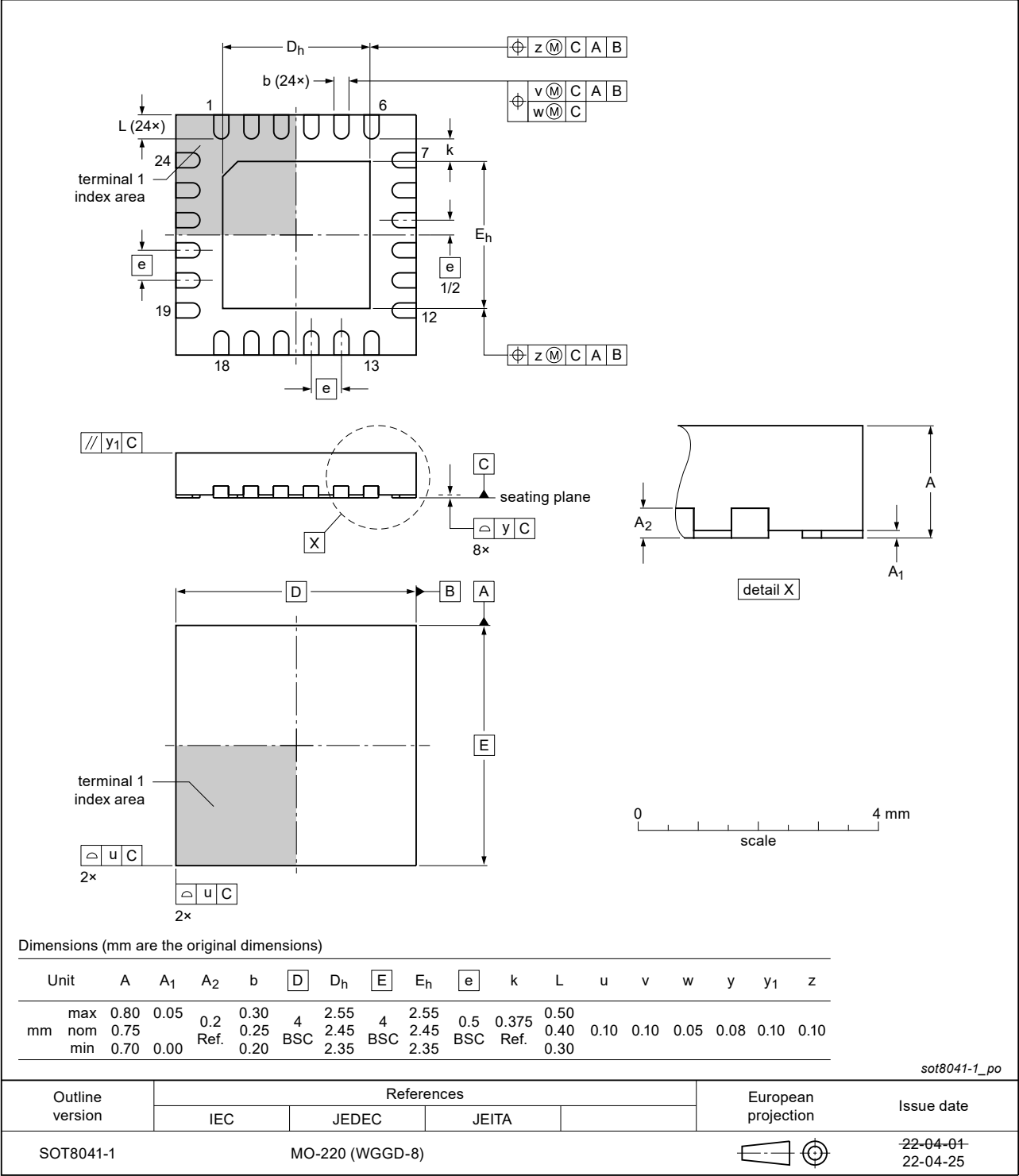


Fig. 30. Package outline SOT8041-1 (HWQFN24)

## 17. Abbreviations

Table 23. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	Not ACKnowledge
PCB	Printed-Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SMBus	System Management Bus

## 18. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA6416 v.1	20250820	Product data sheet	-	-

## 19. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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