NOVOSENSE
纳芯微电子

NCA9544

4-channel I²C-bus multiplexer with interrupt logic

Datasheet (EN) 1.0

Product Overview

The NCA9544 is a 1-of-4 bidirectional translating multiplexer controlled via the I²C bus. The SCL/SDA upstream pair fans out to one of the four downstream pairs, or channels. Only one SCn/SDn channel is selected at a time, determined by the contents of the programmable control register. Four interrupt inputs (/INT3–/INT0), one for each of the downstream pairs, are provided. One interrupt (/INT) output acts as an AND of the four interrupt inputs.

A power-on reset function returns the registers to their default state and initializes the I²C state machine, with all channels deselected.

The pass gates of the multiplexer are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the NCA9544. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

Key Features

- 1-of-4 Bidirectional Translating multiplexer
- I²C Bus and SMBus Compatible
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Three Address Terminals, Allowing up to eight Devices on the I²C Bus
- Channel Selection via I²C Bus
- Power-Up with All Switch Channels Deselected
- Low RON Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD 78
- RoHS & REACH compliant
- ESD Protection Exceeds JESD 22
  - – 2000-V Human-Body Model (A114-A)
  - – 1000-V Charged-Device Model (C101)

Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

Device Information

Part Number	*Package*	*Body Size*
NCA9544-DQNTR	QFN20	5.0mm*5.0mm

Pin Configuration

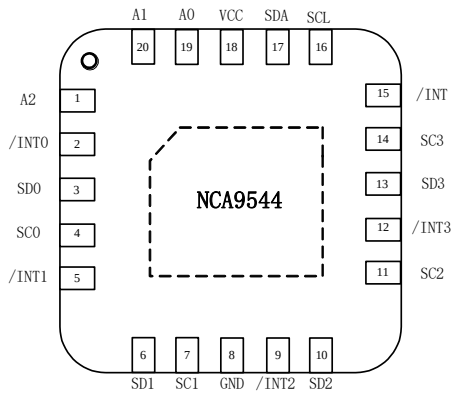

Figure 1. NCA9544 Pin Configuration

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1. Pin Configuration and Functions

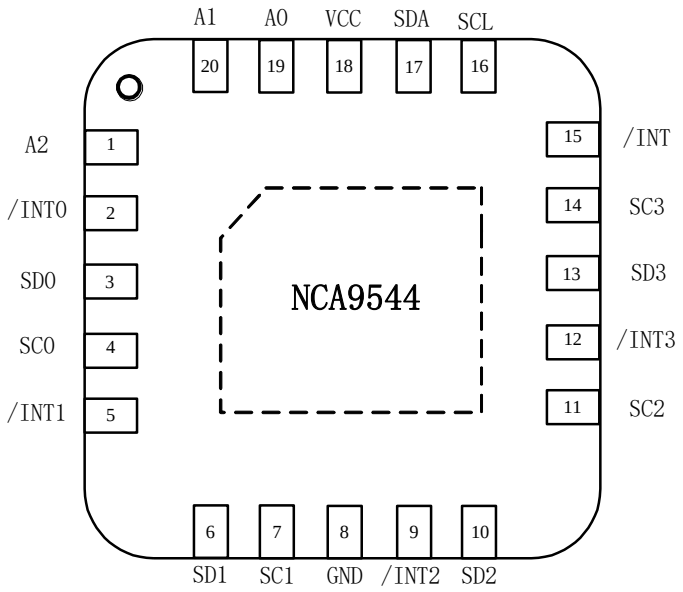


Figure 1.1 NCA9544 Package

Table 1.1 NCA9544 Pin Configuration and Description

NCA9544 PIN NO.	*SYMBOL*	*FUNCTION*
1	A2	Address input 2. Connect directly to VCC or ground.
2	/INT0	Active-low interrupt input 0. Connect to VDPU01 through a pull-up resistor.
3	SD0	Serial data 0. Connect to VDPU01 through a pul-up resistor.
4	SC0	Serial clock 0. Connect to VDPU01 through a pull-up resistor.
5	/INT1	Active-low interrupt input 1. Connect to VDPU11 through a pull-up resistor.
6	SD1	Serial data 1. Connect to VDPU11 through a pull-up resistor.
7	SC1	Serial clock 1. Connect to VDPU11 through a pull-up resistor.
8	GND	Ground
9	/INT2	Active-low interrupt input 2. Connect to VDPU21 through a pull-up resistor.
10	SD2	Serial data 2. Connect to VDPU21 through a pull-up resistor.
11	SC2	Serial clock 2. Connect to VDPU21 through a pull-up resistor.
12	/INT3	Active-low interrupt input 3. Connect to VDPU31 through a pull-up resistor.
13	SD3	Serial data 3. Connect to VDPU31 through a pull-up resistor.
14	SC3	Serial clock 3. Connect to VDPU31 through a pull-up resistor.
15	/INT	Active-low interrupt output. Connect to VDPUM1 through a pull-up resistor.
16	SCL	Serial clock line. Connect to VDPUM1 through a pull-up resistor.

17	SDA	Serial data line. Connect to VDPUM1 through a pull-up resistor.
18	VCC	Supply power
19	A0	Address input 0. Connect directly to VCC or ground.
20	A1	Address input 1. Connect directly to VCC or ground.

[1] V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C master reference voltage and V_{DPU0}–V_{DPU3} are the slave channel reference voltages.

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Comments*
Supply Voltage	V_{CC}	-0.5	7	V	
Input/output Voltage	V_I/V_O	-0.5	7	V	
Input current	I_I		±25	mA	
Output current	I_O		±25	mA	V_O<0V
Continuous current through VCC or GND	I_{CC}		±100	mA	
Storage Temperature	Tstg	-65	150	°C	

3. ESD Ratings

	Ratings	*Value*	*Unit*
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1000	V

4. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	V_{CC}	1.65		5.5	V	
High-level Input Voltage	V_{IH}	0.7*V_{CC}		6	V	SCL, SDA, A2, A1, A0, /INT3–/INT0
Low-level Input Voltage	V_{IL}	-0.5		0.3*V_{CC}	V	SCL, SDA, A2, A1, A0, /INT3–/INT0,
Ambient Temperature	Ta	-40		105	°C	

5. Thermal Information

Parameters	Symbol	QFN20	Unit
Junction-to-ambient thermal resistance	θ_{JA}	32	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC\ (top)}$	28.7	°C/W
Junction-to-board thermal resistance	θ_{JB}	26.4	°C/W

6. Specifications

6.1. Electrical Characteristics

VCC = 1.65V to 5.5V; Tamb = -40℃ to +105℃; unless otherwise noted. Typical specification are at TA=25℃,VCC=3.3V

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Supply						
Supply voltage Range	V_{CC}	1.65	-	5.5	V	
Power On Reset rising	V_{PORR}	-	1.15	1.4	V	no load; $V_I = V_{CC}$ or GND
Power On Reset falling	V_{PORF}	0.9	1.08		V	no load; VI = V_{CC} or GND
Supply current	I_{CC}	-	-	10	μA	Operating mode; V_{CC} = 5.5 V; V_I=V_{CC} or GND; no load; f_{SCL} = 100 kHz
Standby current	I_{stb}	-	0.3	5	μA	Standby mode; V_{CC} = 5.5 V; V_I=V_{CC} or GND; no load
Input SCL; Input/Output SDA						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{CC}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{CC}	-	6	V	
LOW-level output current	I_{OL}	2.5	15	-	mA	V_{OL}= 0.4 V
		4	20		mA	V_{OL}=0.6V
Input leakage current	I_L	-1	-	+1	μA	$V_I = V_{CC}$ or GND
Input capacitance	C_i	-	15		pF	V_I = GND
Select inputs A0, A1, A2, /INT0, /INT1, /INT2, /INT3						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{CC}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{CC}	-	6	V	
Leakage current	I_L	-1	-	1	μA	$V_I = V_{CC}$ or GND
Input capacitance	C_i	-	1.6	3	pF	V_I = GND
/INT output						
HIGH-level output current	I_{OH}	-	-	±1	μA	

LOW-level output current	I_{OL}	3	12	-	mA	V_{CC} =3.6V, V_{OL} = 0.4V[2]
		4	17	-	mA	V_{CC} =3.6V, V_{OL} = 0.6 V[2]
Pass gate						
On-state resistance	R_{on}	4	14	20	Ω	Vo=0.4 V, I_O = 15 mA, V_{CC} = 4.5V
		5	16	25	Ω	Vo=0.4 V, I_O = 15 mA, V_{CC} = 3V
		6	19	30		Vo=0.4 V, I_O = 10 mA, V_{CC} = 2.3V
		10	28	40		Vo=0.4 V, I_O = 10 mA, V_{CC} = 1.65V
Switch output voltage	$V_{O(SW)}$		3.64		V	V_{CC} = 5 V, $I_{O(SW)}$ = -100μA
		2.6		4.5		V_{CC} = 4.5V to 5.5 V, $I_{O(SW)}$ = -100μA
			2.15			V_{CC} = 3.3 V, $I_{O(SW)}$ = -100μA
		1.6		2.8	V	V_{CC} = 3 V to 3.6 V, $I_{O(SW)}$ = -100μA
			1.46			V_{CC} = 2.5 V, $I_{O(SW)}$ = -100μA
		1		1.9		V_{CC} = 2.3 V to 2.7 V, $I_{O(SW)}$ = -100μA
			0.99		V	V_{CC} = 1.8 V, $I_{O(SW)}$ = -100μA
		0.5		1.2		V_{CC} = 1.65 V to 1.95 V, $I_{O(SW)}$ = -100μA
Leakage current	I_L	-1	-	+1	μA	V_I = V_{CC} or GND
C_{io}	Input/output capacitance	-	-	6	pF	V_I=GND

6.2. Dynamic Characteristics

Parameters	*Symbol*	*Standard-mode I²C-bus*		*Fast-mode I²C-bus*		*Unit*
		Min	*Max*	*Min*	*Max*	
propagation delay	t_{PD}[1]		0.3		0.3	ns
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
hold time (repeated) START condition	$t_{HD;STA}$[2]	4.0	-	0.6	-	μs
set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	μs
set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	μs
data valid acknowledge time	$t_{VD;ACK}$		1		1	μs
data hold time	$t_{HD;DAT}$[3]	0	3.45	0	0.9	μs
data valid time(high to low)	$t_{VD;DAT}$[4]		1		1	μs
data valid time(low to high)			0.6		0.6	μs
data set-up time	$t_{SU;DAT}$	250	-	100	-	ns

LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
fall time of both SDA and SCL signals	t_f	-	300	20 + 0.1C_b[5]	300	ns
rise time of both SDA and SCL signals	t_r	-	1000	20 + 0.1C_b[5]	300	ns
pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	50	-	50	ns
/INT						
Valid time from /INTn to /INT singal	$t_{iv(INTnN-INT)}$	-	4	-	4	µs
Delay time from /INTn to /INT inactive	$t_{ir(INTnN-INT)}$	-	2	-	2	µs
Low-level rejection time	$T_{w(rej)L}$	1	-	1	-	µs
High-level rejection time	$T_{w(rej)H}$	0.5	-	0.5	-	µs

[1]Pass gate propagation delay is calculated from the 20 Ω typical Ron and the 15 pF load capacitance.

[2]After this period, the first clock pulse is generated.

[3]A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4]Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

[5]C_b = total capacitance of one bus line in pF.

6.3. Parameter Measurement Information

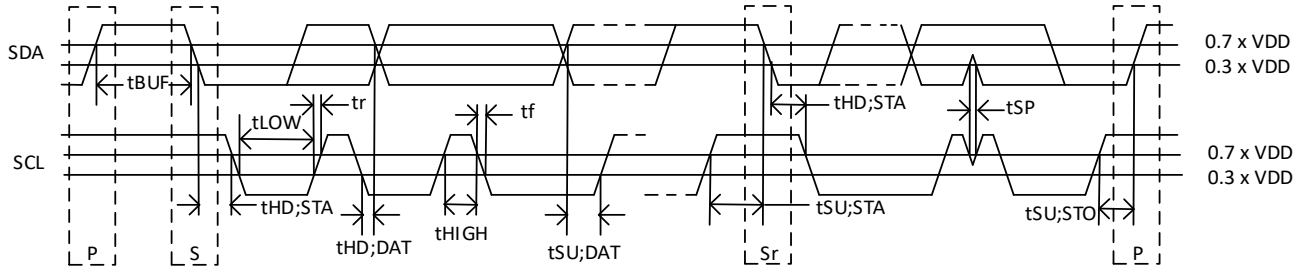


Figure 6.1 Definition of timing on I²C-bus

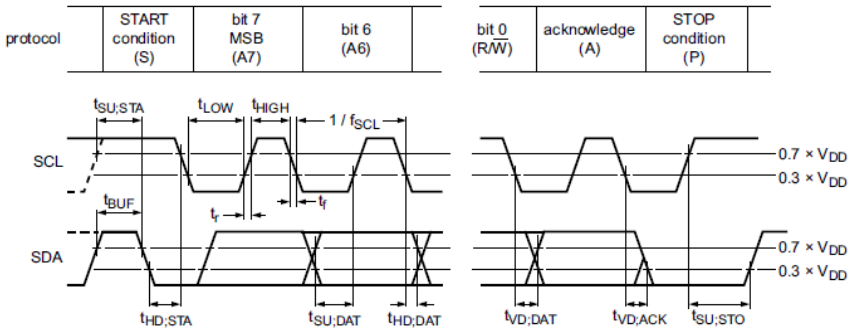


Figure 6.2 I²C-bus timing diagram

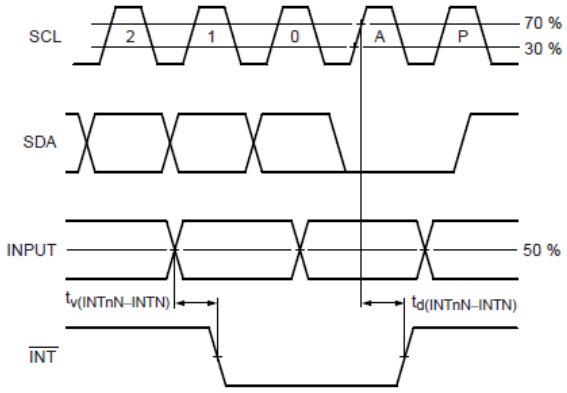
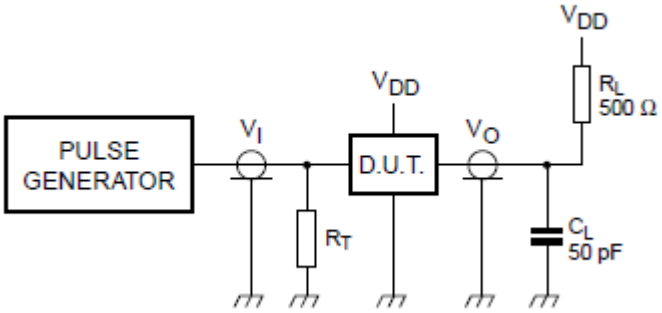


Figure 6.3 Expanded view of read input port register



Definitions test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Zo of the pulse generator.

Figure 6.4 Test circuitry for switching times

7. Detailed Description

7.1. Overview

The NCA9544 is a 4-channel, bidirectional translating I²C multiplexer. The master SCL/SDA signal pair is directed to one of four channels of slave devices, SC0&SD0-SC3&SD3.Only one individual downstream channel can be selected of the four channels at a time. The NCA9544 also supports interrupt signals in order for the master to detect an interrupt on the /INT output terminal that can result from any of the slave devices connected to the /INT3-/INT0 input terminals.

The device can be reset by cycling the power supply, VCC, also known as a power-on reset (POR), which resets the state machine and allows the NCA9544 to recover should one of the downstream I²C buses get stuck in a low state. A POR event causes all channels to be deselected.

The connections of the I²C data path are controlled by the same I²C master device that is switched to communicate with I²C slave. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channel and state of the interrupts.

The NCA9544 may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

7.2. Functional Block Diagram

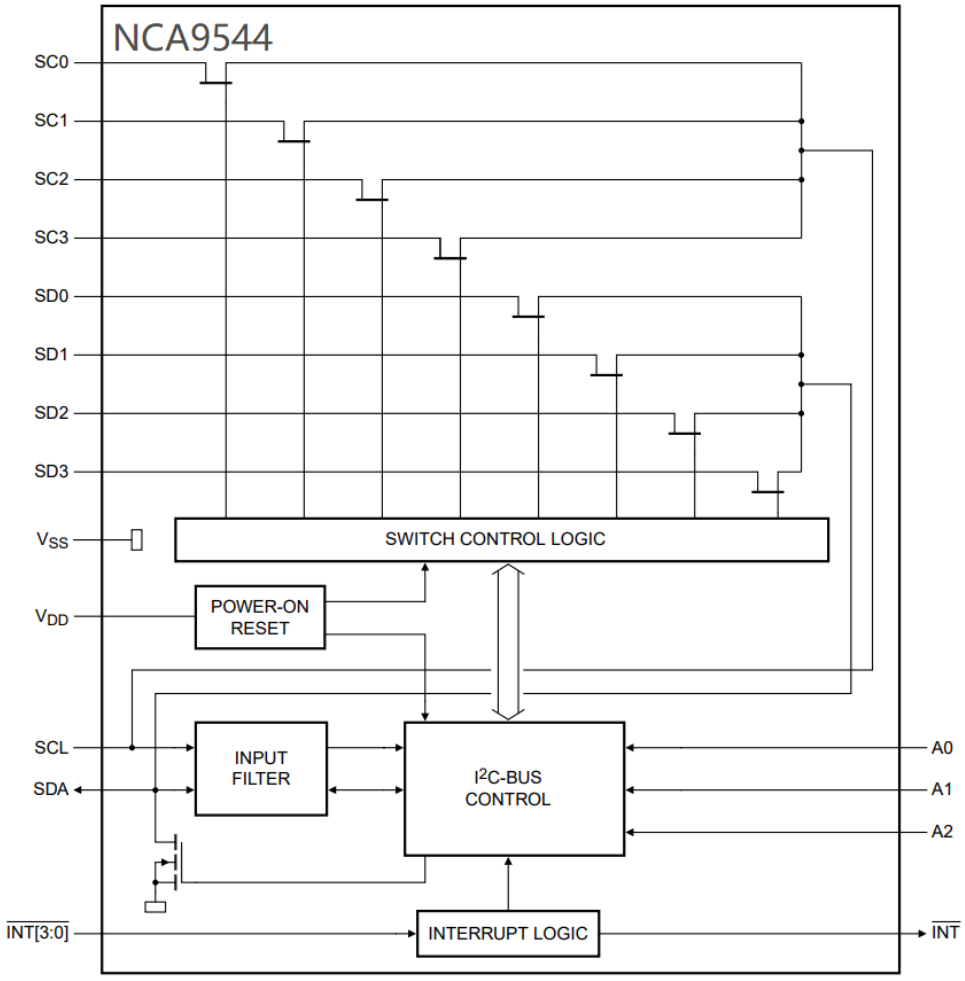


Figure 7.1 NCA9544 Functional block

7.3. Power-On Reset

When power is applied to VCC, an internal power-on reset holds the NCA9544 in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the NCA9544 registers and I²C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below at least V_{PORF} to reset the device.

7.4. I²C Interface

The I²C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 7.2)

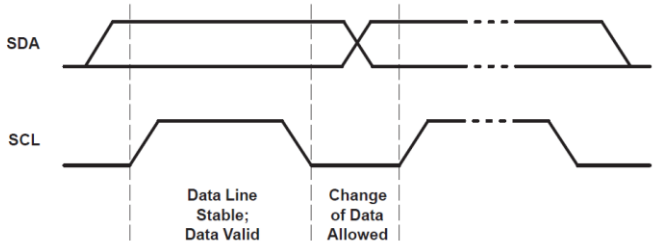


Figure 7.2 Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 7.3).

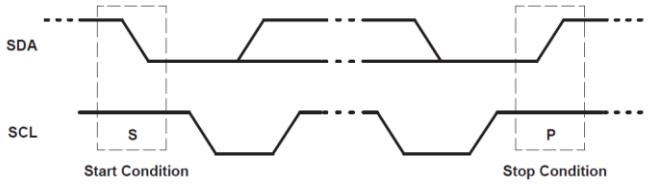


Figure 7.3 Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 7.4).

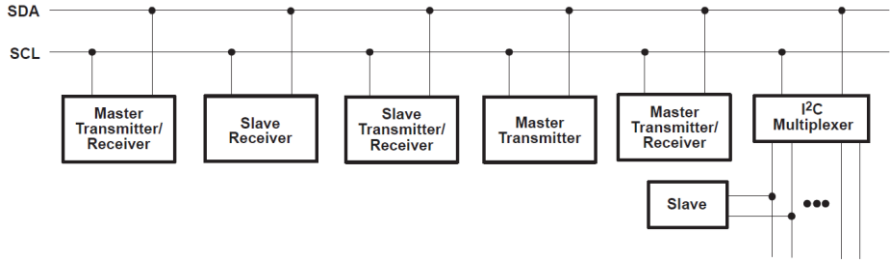


Figure 7.4 System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7.5). Setup and hold times must be taken into account.

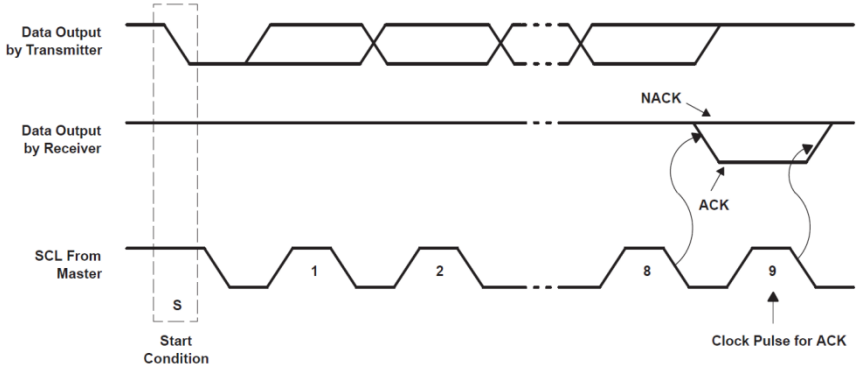


Figure 7.5 Acknowledgment on the I²C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition. Data is transmitted to the NCA9544 control register using the write mode shown in Figure 7.6.

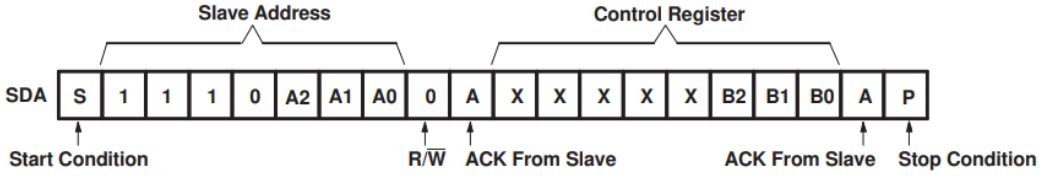


Figure 7.6 Write Control Register

Data is read from the NCA9544 control register using the read mode shown in Figure 7.7.

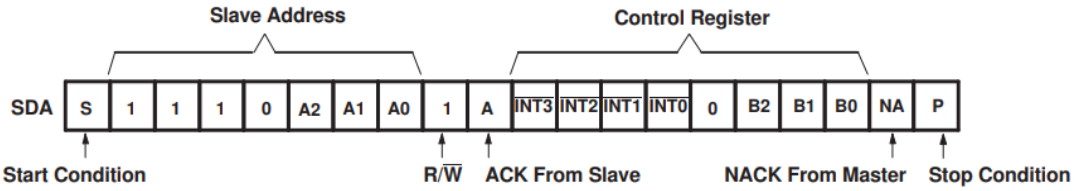


Figure 7.7 Read Control Register

7.5. Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the NCA9544 is shown in Figure 7.8. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

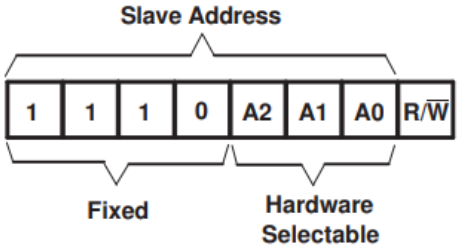


Figure 7.8 NCA9544 Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

7.6. Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the NCA9544, which is stored in the control register (see Figure 7.9). If multiple bytes are received by the NCA9544, it saves the last byte received. This register can be written and read via the I²C bus.

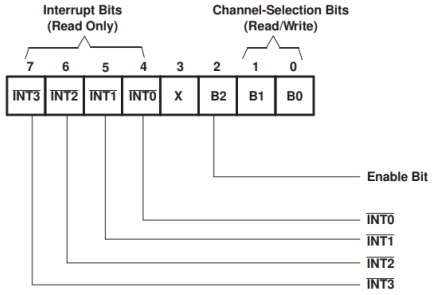


Figure 7.9 Control Register

7.7. Control Register Definition

Only one SCn/SDn downstream pair, or channel, can be selected by the contents of the control register (see Table 7.1). After the NCA9544 has been addressed, the control register is written. The three LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 7.1. Control Register Write (Channel Selection), Control Register Read (Channel Status)

/INT3	/INT2	/INT1	/INT0	D3	B2	B1	B0	COMMAND

X	X	X	X	X	0	X	X	No channel selected
X	X	X	X	X	1	0	0	Channel 0 enabled
X	X	X	X	X	1	0	1	Channel 1 enabled
X	X	X	X	X	1	1	0	Channel 2 enabled
X	X	X	X	X	1	1	1	Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power up/reset default state

[1] Only one channel can be enabled at the same time.

7.8. Interrupt Handling

The NCA9544 provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 7.2). When an interrupt is generated by any device, it is detected by the NCA9544 and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register. Bits 4–7 of the control register correspond to channels 0–3 of the NCA9544, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the NCA9544 and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the NCA9544 to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to VCC.

Table 7.2. Control Register Read (Interrupt)[1]

/INT3	/INT2	/INT1	/INT0	D3	B2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

[1] Several interrupts can be active at the same time. For example, /INT3 = 0, /INT2 = 1, /INT1 = 1, /INT0 = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

8. Application and Implementation

Applications of the NCA9544 will contain an I²C (or SMBus) master device and up to eight I²C slave devices. The downstream channels are ideally used to resolve I²C slave address conflicts. For example, if four identical digital temperature sensors are needed in the

application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I²C master can move on and read the next channel.

In an application where the I²C bus will contain many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels.

8.1. Typical Application

A typical application of the NCA9544 will contain anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU3}). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, V_{pass} = V_{DPUX}. Once the maximum Vpass is known, Vcc can be selected easily using Figure 8.2. In an application where voltage translation is necessary, additional design requirements must be considered (See Design Requirements).

Figure 8.1 shows an application in which the NCA9544 can be used.

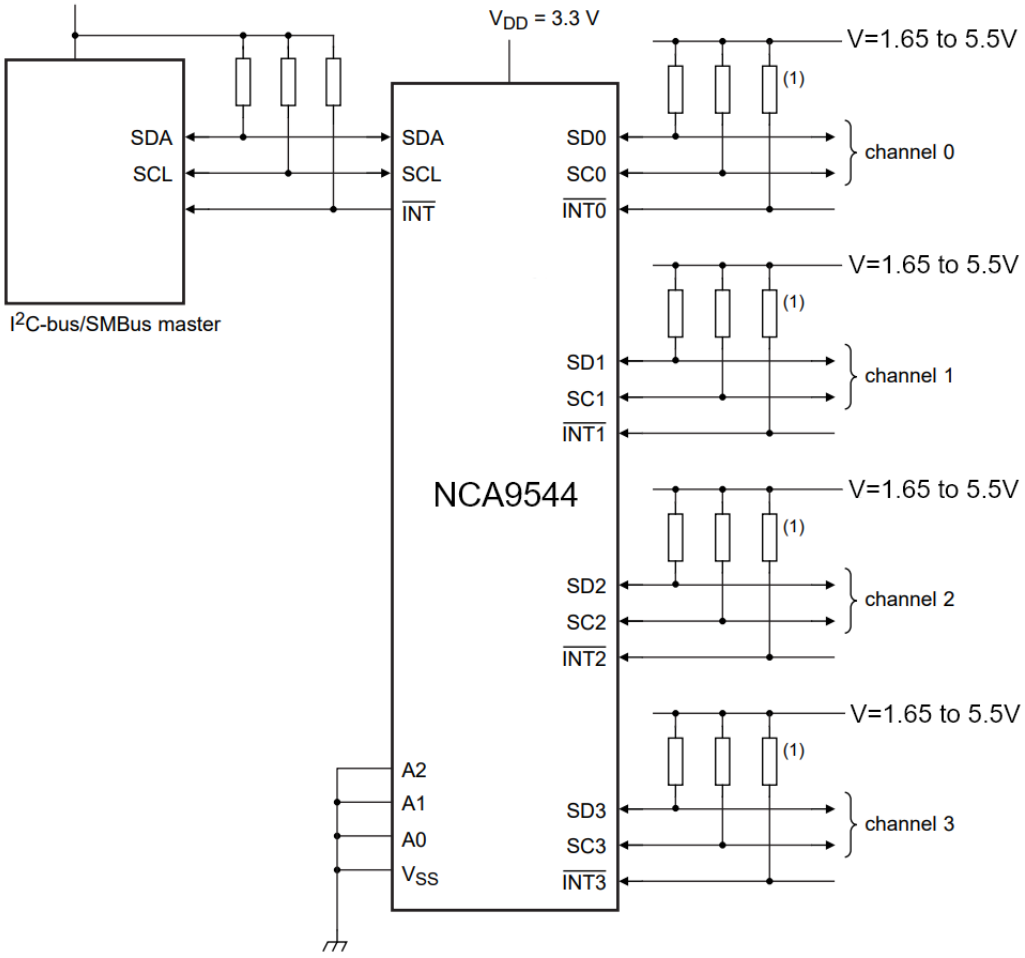


Figure 8.1 Typical Application Schematic

8.2. Design Requirements

The pull-up resistors on the /INT3-/INT0 terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0,A1and A2 terminals are hardware selectable to control the slave address of the NCA9544. These terminals may be tied directly to GND or VCC in the application.

The pass-gate transistors of the NCA9544 are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I²C bus to another.

Figure 8.2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Electrical Characteristics section of this data sheet). In order for the NCA9544 to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 8.2, Vpass(max) is 2.7 V when the NCA9544 supply voltage is 4 V or lower, so the NCA9544 supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 8.1).

8.3. Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUV} - V_{OL(max)}}{I_{OL}} \qquad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, tr (300 ns for fast-mode operation, f_{SCL} =400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \qquad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the NCA9544, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

8.4. NCA9544 Application Curves

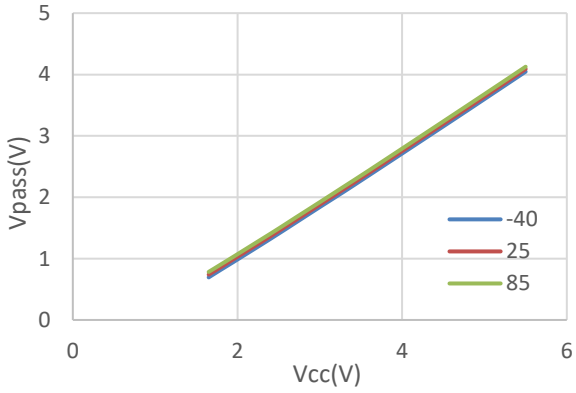
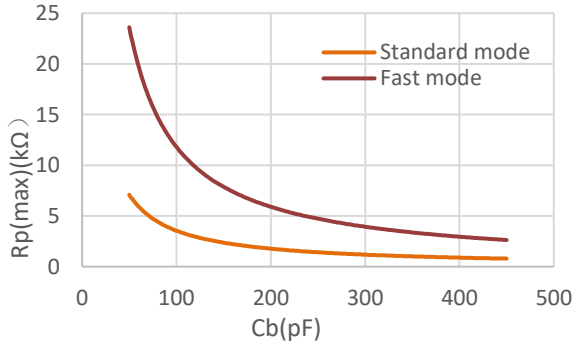
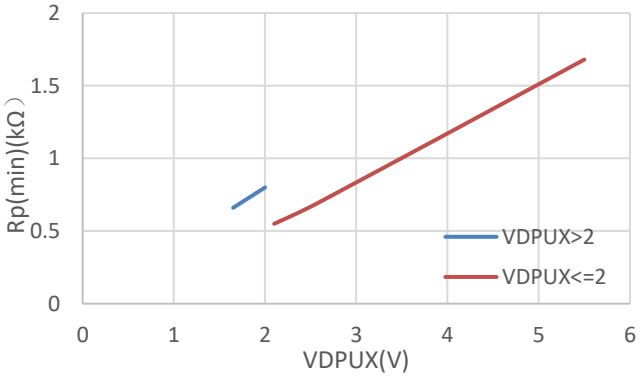


Figure 8.2 Pass-Gate Voltage (V_{pass}) vs Supply Voltage(V_{CC}) at Three Temperature Points



Standard mode(fscl=100kHz,tr=1us);Fast mode: (fscl=400kHz,tr=300ns)

Figure 8.3 Maximum Pull-Up resistance($R_{p(max)}$) vs Bus Capacitance(C_b)



VOL=0.2*VDPUX,IOL=2mA when VDPUX<=2V; VOL=0.4V,IOL=3mA when VDPUX>2V

Figure 8.4 Minimum Pull-Up resistance($R_{p(min)}$) vs Pull-up reference voltage(V_{DPUX})

9. Layout

9.1. Layout Guidelines

For PCB layout of the NCA9544, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedance and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all VDPUX voltages and VCC could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SCn, SDn and INTn) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

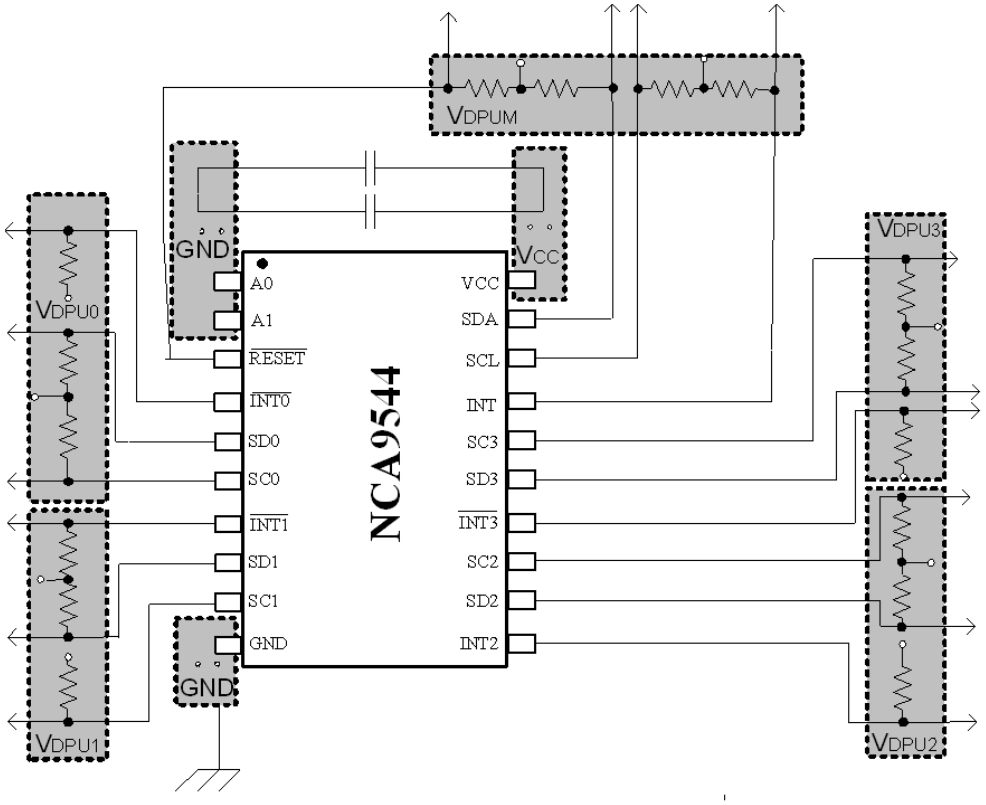
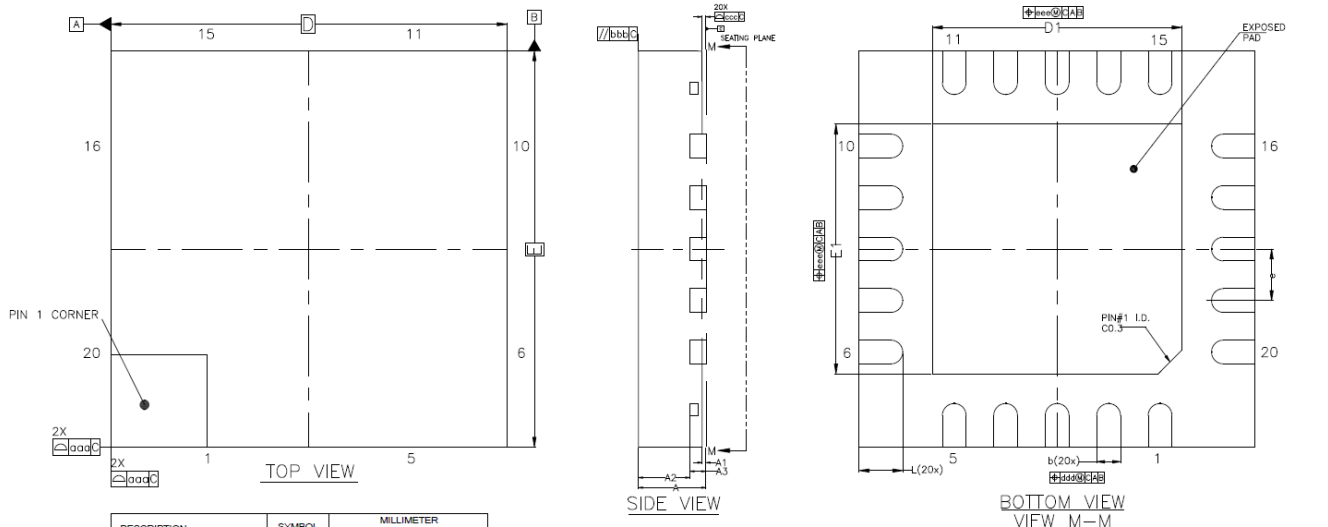


Figure 9.1 Typical Application PCB

10. Package Information



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.25	0.30	0.35
BODY SIZE	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
LEAD PITCH		e	0.65 BSC		
LEAD LENGTH		L	0.50	0.55	0.60
EP SIZE	X	D1	3.10	3.15	3.20
	Y	E1	3.10	3.15	3.20
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

Figure 10.1 Package outline for QFN20

11. Order information

Part Number	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*Package Qty*
NCA9544-DQNTR	-40 to 105℃	3	QFN20	QFN20	3000

12. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*selection guide*
NCA9544	Click here	Click here	Click here	Click here

13. Tape and Reel Information

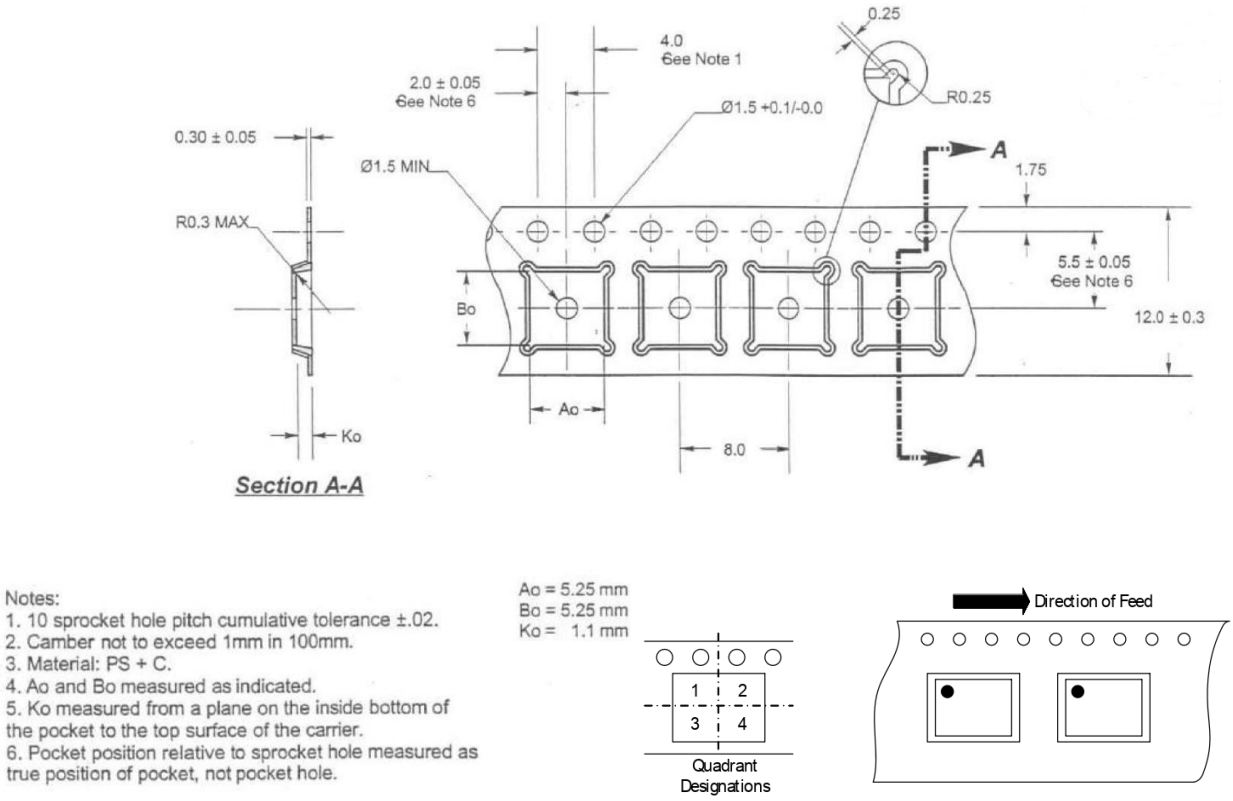


Figure 13.1 Tape and Reel Information of QFN20

14. Revision History

Revision	Description	Date
1.0	Initial version	2024/4/14

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