NCA9548A-Q100

8-channel I²C-bus switch with reset

Rev. 1 — 20 August 2025 Product data sheet

1. General description

The NCA9548A-Q100 is an octal bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active LOW reset input allows the NCA9548A-Q100 to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I²C-bus state machine and causes all the channels to be deselected as does the internal Power-on reset function.

The pass gates of the switches are constructed such that the V_{CC} pin can be used to limit the maximum high voltage which will be passed by the NCA9548A-Q100. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 6 V tolerant.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 1-of-8 bidirectional translating switches
- I²C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- Three address pins allowing up to eight devices on the I²C-bus
- Channel selection via I²C-bus, in any combination
- Power-up with all switch channels deselected
- Low R_{on} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 1.65 V to 5.5 V
- 6 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Two packages offered: TSSOP24, and HWQFN24
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2 kV
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1 kV

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NCA9548APW-Q100	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
NCA9548ABY-Q100	-40 °C to +125 °C	HWQFN24	plastic thermal enhanced very very thin Quad Flat packages; no leads; 24 terminals; 0.5 mm pitch; 4 × 4 × 0.75 mm body	SOT8041-1

4. Marking

Table 2. Marking

Type number	Marking code
NCA9548APW-Q100	NCA9548
NCA9548ABY-Q100	CA9548

5. Block diagram

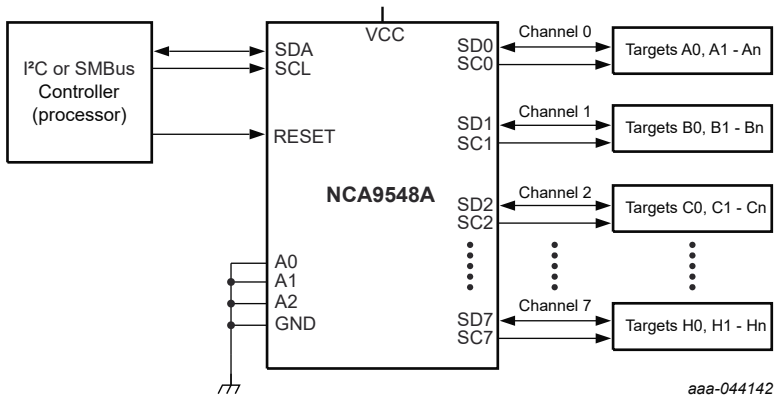


Fig. 1. Simplified application diagram of NCA9548A-Q100

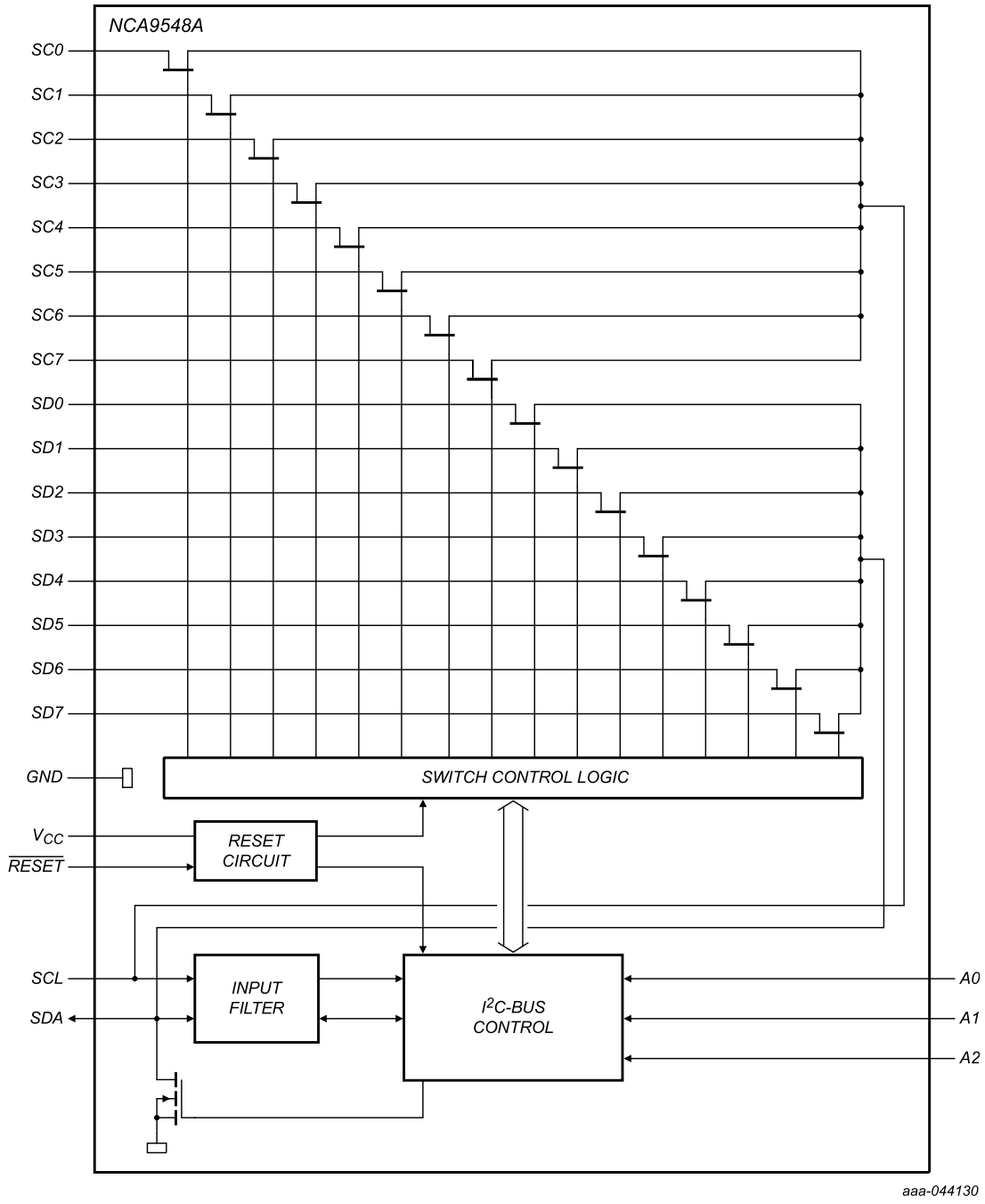


Fig. 2. Block diagram of NCA9548A-Q100

6. Pinning information

6.1. Pinning

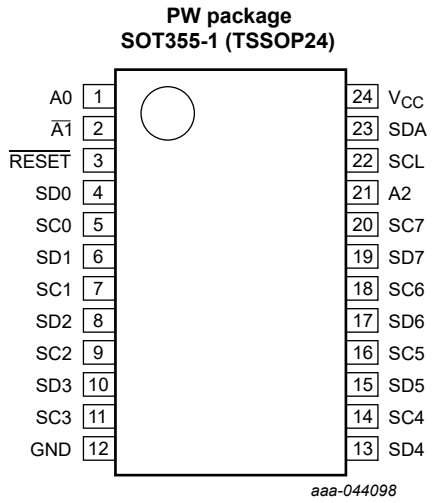
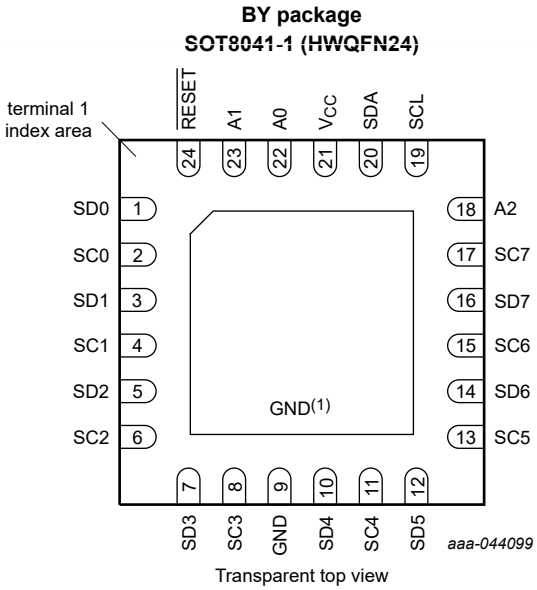


Fig. 3. Pin configuration for SOT355-1 (TSSOP24)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 4. Pin configuration for SOT8041-1 (HWQFN24)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP24	HVQFN24	
A0	1	22	address input 0
A1	2	23	address input 1
$\overline{\text{RESET}}$	3	24	active LOW reset input
SD0	4	1	serial data 0
SC0	5	2	serial clock 0
SD1	6	3	serial data 1
SC1	7	4	serial clock 1
SD2	8	5	serial data 2
SC2	9	6	serial clock 2
SD3	10	7	serial data 3
SC3	11	8	serial clock 3
GND	12	9 [1]	supply ground
SD4	13	10	serial data 4
SC4	14	11	serial clock 4
SD5	15	12	serial data 5

Symbol	Pin		Description
	TSSOP24	HVQFN24	
SC5	16	13	serial clock 5
SD6	17	14	serial data 6
SC6	18	15	serial clock 6
SD7	19	16	serial data 7
SC7	20	17	serial clock 7
A2	21	18	address input 2
SCL	22	19	serial clock line
SDA	23	20	serial data line
V_{CC}	24	21	supply voltage

[1] HWQFN24 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Fig. 2.

7.1. Device address

Following a START condition, the bus controller must output the address of the target it is accessing. The address of the NCA9548A-Q100 is shown in Fig. 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

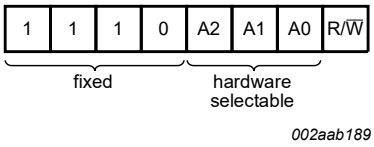


Fig. 5. Target address

The last bit of the target address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.2. Control register

Following the successful acknowledgement of the target address, the bus controller will send a byte to the NCA9548A-Q100, which will be stored in the control register. If multiple bytes are received by the NCA9548A-Q100, it will save the last byte received. This register can be written and read via the I²C-bus.

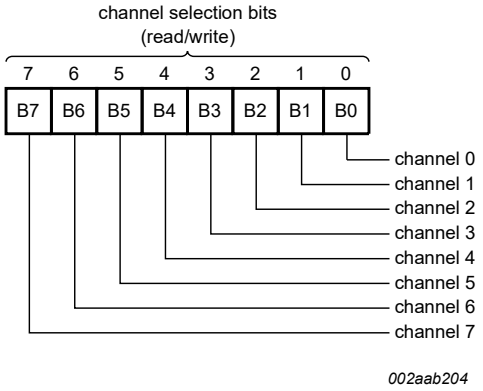


Fig. 6. Control register

7.2.1. Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the NCA9548A-Q100 has been addressed. The contents of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 4. Control register: Write-channel selection; Read-channel status

B7	B6	B5	B4	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1 enabled
X	X	X	X	X	0	X	X	channel 2 disabled
					1			channel 2 enabled
X	X	X	X	0	X	X	X	channel 3 disabled
				1				channel 3 enabled
X	X	X	0	X	X	X	X	channel 4 disabled
			1					channel 4 enabled
X	X	0	X	X	X	X	X	channel 5 disabled
		1						channel 5 enabled
X	0	X	X	X	X	X	X	channel 6 disabled
	1							channel 6 enabled
0	X	X	X	X	X	X	X	channel 7 disabled
1								channel 7 enabled

Remark: Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that channels 7, 5, 4, 1 and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. Default condition is all zeroes.

7.3. $\overline{\text{RESET}}$ input

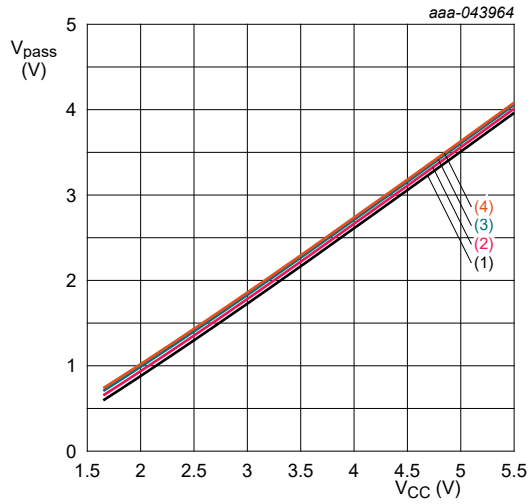
The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the NCA9548A-Q100 will reset its register and I²C-bus state machine and will deselect all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

7.4. Power-on reset

When power is applied to V_{CC}, an internal Power-On Reset (POR) holds the NCA9548A-Q100 in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the NCA9548A-Q100 register and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. V_{CC} must be lowered below 0.2 V for at least 5 µs in order to reset the device.

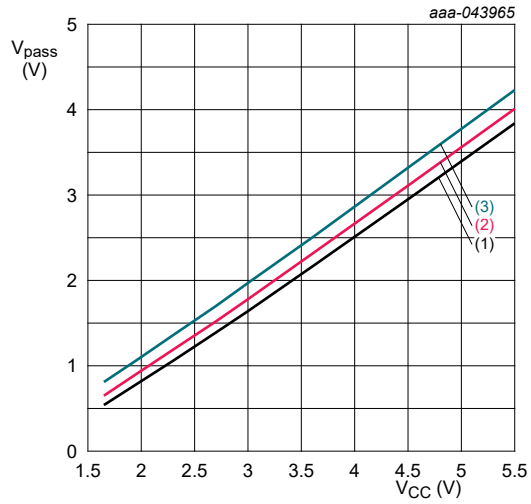
7.5. Voltage translation

The pass gate transistors of the NCA9548A-Q100 are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.



(1) -40 °C
(2) 25 °C
(3) 85 °C
(4) 125 °C

Fig. 7. Pass gate voltage versus supply voltage



(1) Min
(2) Typ
(3) Max

Fig. 8. Pass gate voltage versus supply voltage

Fig. 7 shows the voltage characteristics of the pass gate transistors (note that the NCA9548A-Q100 is only tested at the points specified in Section 13 of this data sheet). In order for the NCA9548A-Q100 to act as a voltage translator, the V_{pass} voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then V_{pass} should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Fig. 7, we see that $V_{pass(max)}$ will be at 2.7 V when the NCA9548A-Q100 supply voltage is 3.5 V or lower, so the NCA9548A-Q100 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Fig. 15).

More Information can be found in Application Note AN**<TBD>**: NCA954x family of I²C/SMBus multiplexers and switches.

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1. Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (START and STOP conditions) (see Fig. 9).

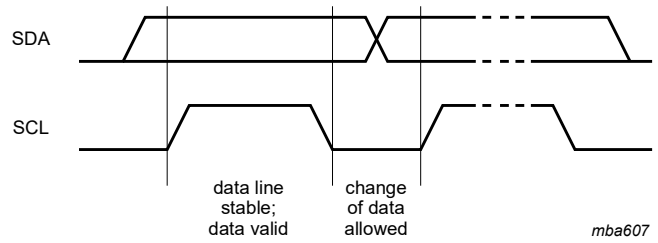


Fig. 9. Bit transfer

8.2. START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Fig. 10).

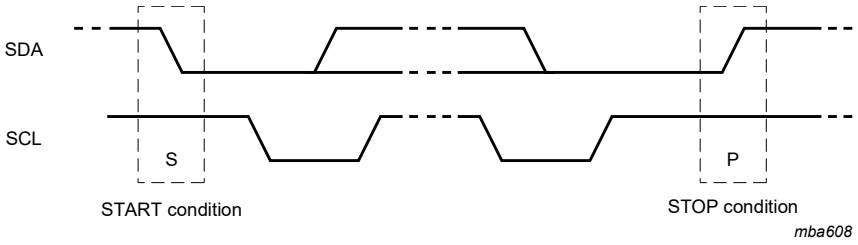


Fig. 10. Definition of START and STOP conditions

8.3. System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘controller’ and the devices which are controlled by the controller are the ‘targets’ (see Fig. 11).

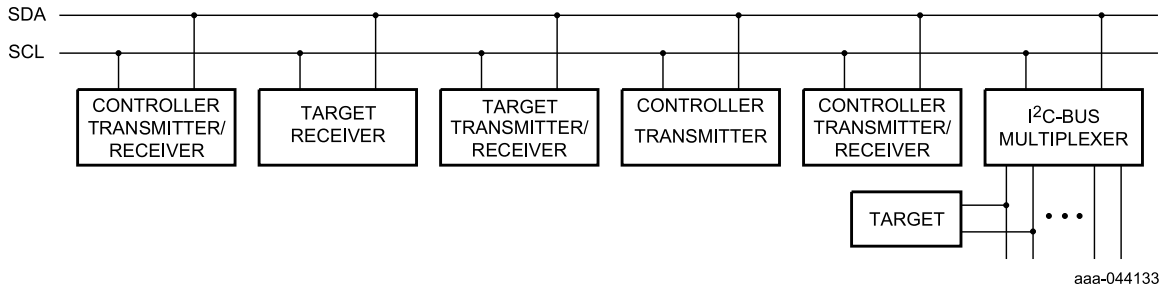


Fig. 11. System configuration

8.4. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the controller generates an extra acknowledge related clock pulse.

A target receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a controller must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull-down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

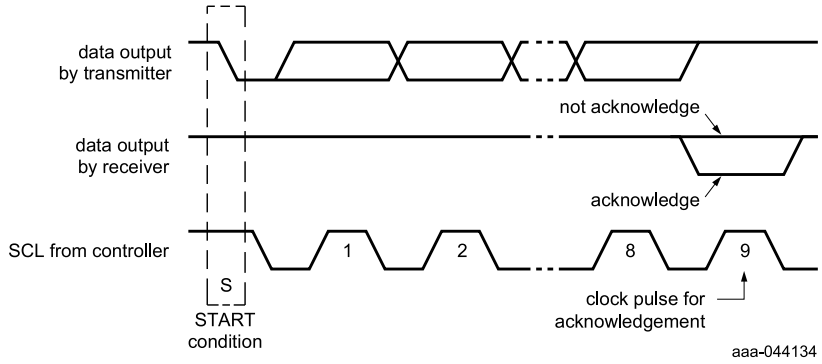


Fig. 12. Acknowledgement on the I²C-bus

8.5. Bus transactions

Data is transmitted to the NCA9548A-Q100 control register using the Write mode as shown in Fig. 13.

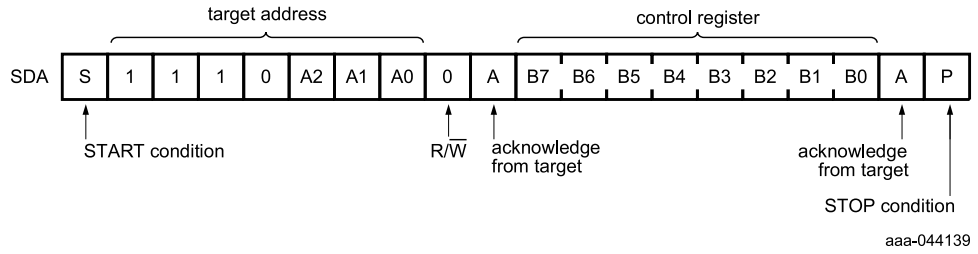


Fig. 13. Write control register

Data is read from NCA9548A-Q100 using the Read mode as shown in Fig. 14.

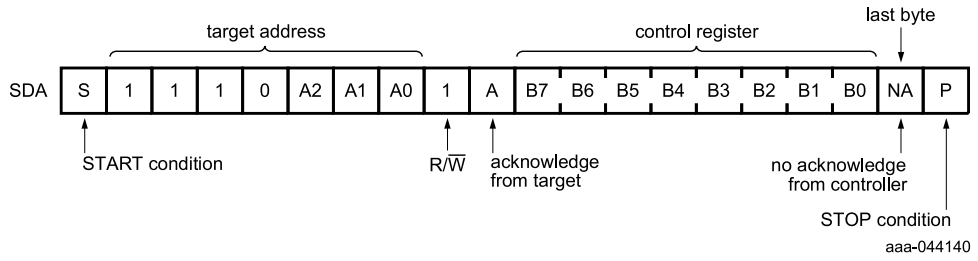


Fig. 14. Read control register

9. Application design-in information

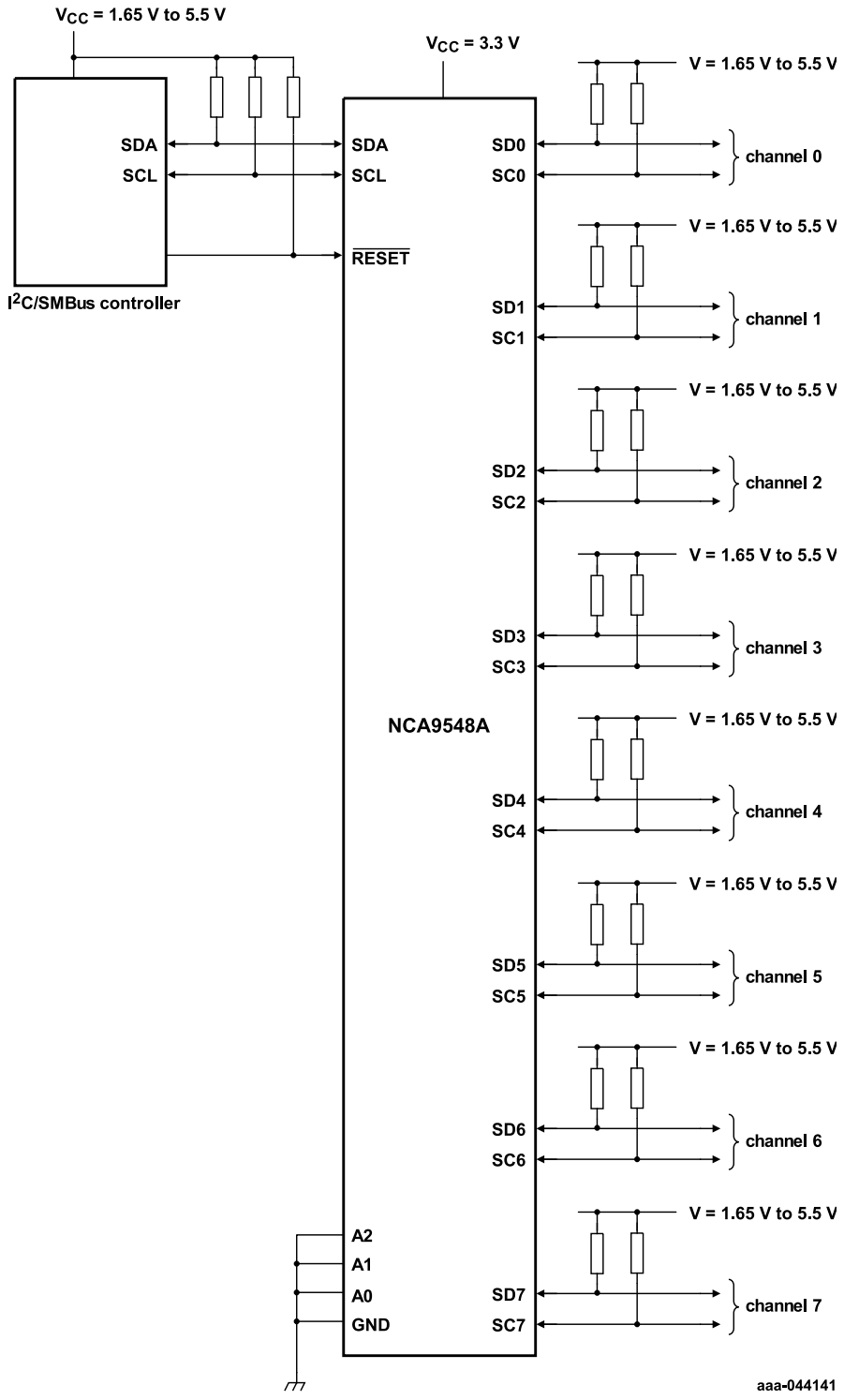


Fig. 15. Typical application

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
I_{CC}	supply current		-	±100	mA
I_{GND}	ground supply current		-	±100	mA
P_{tot}	total power dissipation		-	400	mW
$T_{j(max)}$	maximum junction temperature		-	125	°C
T_{stg}	storage temperature		-65	+150	°C

11. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	+5.5	V
V_I	input voltage	A0, A1, A2, $\overline{\text{RESET}}$	-0.5	+6.0	V
$V_{I/O}$	input/output voltage	SCL, SDA, SCn, SDn	-0.5	+6.0	V
T_{amb}	ambient temperature	operating in free air	-40	+125	°C

12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP24 package	[1]	100	K/W
		HWQFN24 package	[1]	32.6	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

13. Static characteristics

Table 8. Static characteristics

At recommended operating conditions. Voltages are referenced to ground (GND = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
Supply								
I_{CC}	supply current	operating mode; $V_I = V_{CC}$ or GND; no load						
		f_{SCL} = 400 kHz; V_{CC} = 5.5 V	-	39	40	-	40	µA
		f_{SCL} = 400 kHz; V_{CC} = 3.6 V	-	15	16	-	16	µA
		f_{SCL} = 400 kHz; V_{CC} = 2.7 V	-	8	9	-	9	µA
		f_{SCL} = 400 kHz; V_{CC} = 1.65 V	-	3.5	4	-	4	µA
		f_{SCL} = 100 kHz; V_{CC} = 5.5 V	-	14.8	15	-	15	µA
		f_{SCL} = 100 kHz; V_{CC} = 3.6 V	-	4.7	5	-	5	µA
		f_{SCL} = 100 kHz; V_{CC} = 2.7 V	-	2.2	3	-	3	µA
		f_{SCL} = 100 kHz; V_{CC} = 1.65 V	-	1	2	-	2	µA
		standby mode; $V_I = V_{CC}$ or GND				-		
		V_{CC} = 5.5 V	-	0.1	1	-	1	µA
		V_{CC} = 3.6 V	-	0.1	1	-	1	µA
		V_{CC} = 2.7 V	-	0.1	1	-	1	µA
		V_{CC} = 1.65 V	-	0.1	1	-	1	µA
ΔI_{CC}	additional supply current	SCL, SDA, $\overline{RESET}$, A0, A1, A2; one input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND; V_{CC} = 1.65 to 5.5 V	-	3	16	3	18	µA
V_{PORR}	power-on reset voltage	no load; $V_I = V_{CC}$ or GND	-	1.2	1.5	1.2	1.5	V
Input SCL; input/output SDA								
V_{IL}	LOW-level input voltage		-0.5	-	$+0.3V_{CC}$	-	$+0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	-	6	$0.7V_{CC}$	6	V
I_{OL}	LOW-level output current	SDA pin						
		V_{OL} = 0.4 V	3	6	-	3	-	mA
		V_{OL} = 0.6 V	6	9	-	6	-	mA
I_{IO}	input/output leakage current	$V_I = V_{CC}$ or GND	-1	-	+1	-1	+1	µA
$C_{io(off)}$	off-state input/output capacitance	V_I = GND or V_{CC}	-	12	17	-	19	pF
Select inputs A0, A1 A2, $\overline{RESET}$								
V_{IL}	LOW-level input voltage		-0.5	-	$+0.3V_{CC}$	-0.5	$+0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	-	6	$0.7V_{CC}$	6	V
I_I	input leakage current	V_I = GND or V_{CC}	-1	-	+1	-1	+1	µA
C_i	input capacitance	V_I = GND or V_{CC}	-	2	3.5	-	3.5	pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
Pass gate								
R_{on}	ON-state resistance	V_{CC} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	4	10	14	4	14	Ω
		V_{CC} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA	5	12	16	5	16	Ω
		V_{CC} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	7	15	21	7	21	Ω
		V_{CC} = 1.65 V to 1.95 V; V_O = 0.4 V; I_O = 10 mA	10	25	34	10	34	Ω
V_{pass}	pass voltage	$V_{i(sw)}$ = V_{CC} = 4.5 V to 5.5 V; $I_{o(sw)}$ = -100 µA	2.6	3.6	4.5	2.6	4.5	V
		$V_{i(sw)}$ = V_{CC} = 3.0 V to 3.6 V; $I_{o(sw)}$ = -100 µA	1.5	1.9	2.8	1.5	2.8	V
		$V_{i(sw)}$ = V_{CC} = 2.3 V to 2.7 V; $I_{o(sw)}$ = -100 µA	1.0	1.4	1.8	0.95	1.8	V
		$V_{i(sw)}$ = V_{CC} = 1.65 V to 1.95 V; $I_{o(sw)}$ = -100 µA	0.55	0.9	1.25	0.45	1.2	V
I_{IO}	input/output leakage current	V_I = V_{CC} or GND	-1	-	+1	-1	+1	µA

[1] All typical values are measured at T_{amb} = 25 °C.

14. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions. Voltages are referenced to ground (GND = 0 V).

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
t_{PD}	propagation delay	from SDA to SDx, or SCL to SCx [1]	-	0.3	-	0.3	ns
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	[2]	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0 [3]	[4]	0 [3]	[4]	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [5]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$ [5]	300	ns
C_b	capacitive load for each bus line		-	400	-	400	pF
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
$t_{VD;DAT}$	data valid time	HIGH-to-LOW [6]	-	1	-	1	µs
		LOW-to-HIGH [6]	-	0.6	-	0.6	µs
$t_{VD;ACK}$	data valid acknowledge time		-	1	-	1	µs
$\overline{\text{RESET}}$							
$t_{w(rst)L}$	LOW-level reset time		4	-	4	-	ns
t_{rst}	reset time	SDA clear	-	500	-	500	ns
$t_{REC;STA}$	recovery time to START condition		0	-	0	-	ns

[1] Pass gate propagation delay is calculated from the 20 Ω typical R_{on} and the 15 pF load capacitance.
[2] After this period, the first clock pulse is generated.
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
[4] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
[5] C_b = total capacitance of one bus line in pF.
[6] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

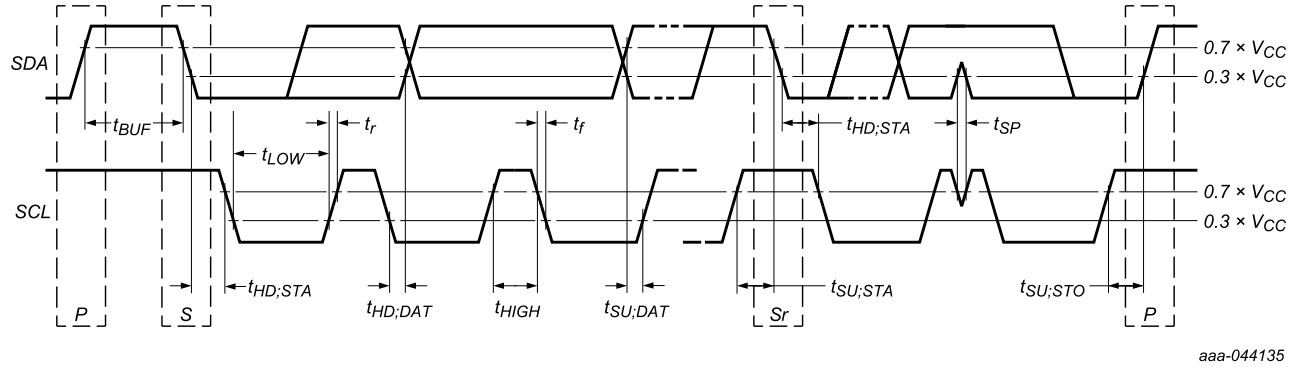


Fig. 16. Definition of timing on the I²C-bus

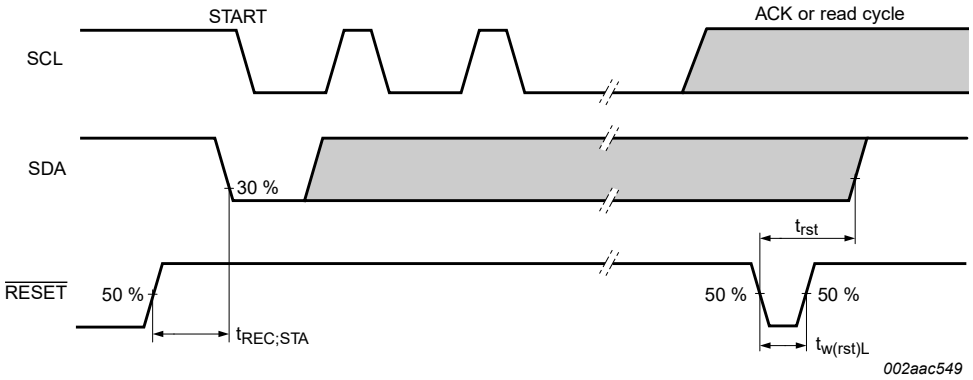


Fig. 17. Definition of $\overline{\text{RESET}}$ timing

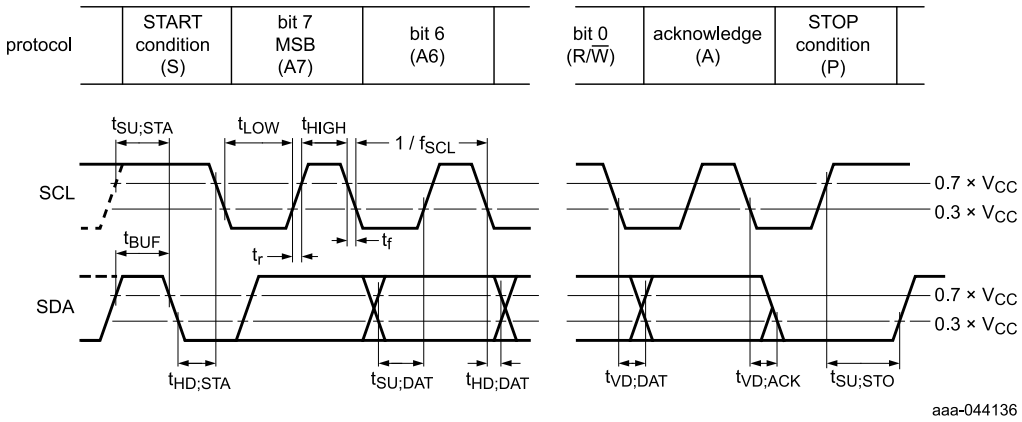


Fig. 18. I²C-bus timing diagram

15. Power-on reset requirements

In the event of a glitch or data corruption, NCA9548A-Q100 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application. The power-on reset feature is shown in Fig. 19.

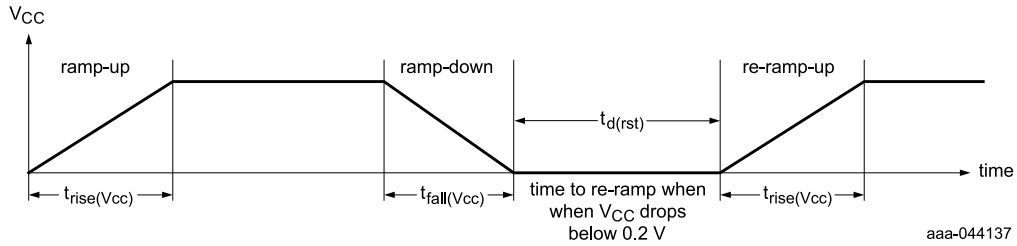


Fig. 19. V_{CC} is lowered below 0.2 V and then ramped up to V_{CC}

Table 10 specifies the performance of the power-on reset feature for NCA9548A-Q100.

Table 10. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
$t_{rise(V_{CC})}$	supply rise time	see Fig. 19	0.1	-	100	ms
$t_{fall(V_{CC})}$	supply fall time	see Fig. 19	1	-	100	ms
$t_{d(rst)}$	reset delay time	see Fig. 19	5	-	-	µs
$V_{CC(gl)}$	minimum glitch supply voltage	level that V_{CC} can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)V_{CC}}$ < 1 µs; see Fig. 20	-	-	1.2	V
$t_{w(gl)V_{CC}}$	supply voltage glitch pulse width	glitch width that will not cause a functional disruption when $V_{CC(gl)}$ = 0.5 x V_{CC}; see Fig. 20	-	-	10	µs

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)V_{CC}}$) and glitch level ($V_{CC(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Fig. 20 and Table 10 provide more information on how to measure these specifications.

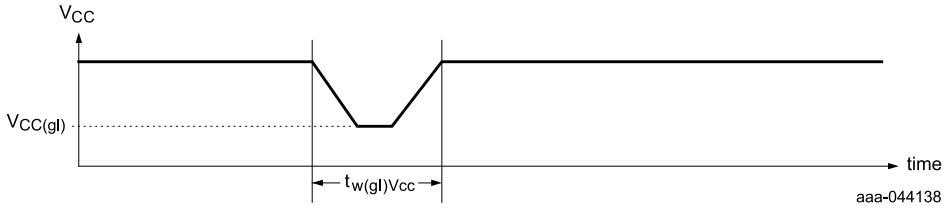
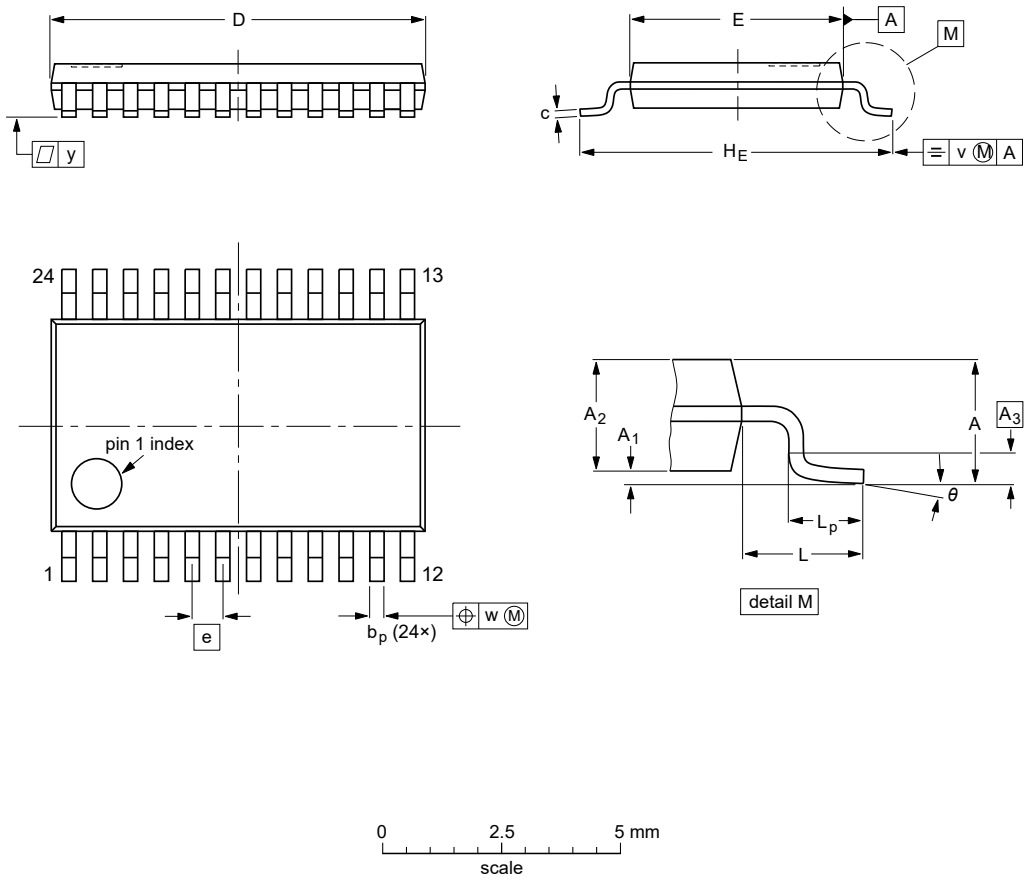


Fig. 20. Glitch width and glitch height

16. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05	0.25 BSC	0.30	0.20	7.90	4.50	0.65 BSC	6.60	1.00 REF	0.75	0.2	0.1	0.1	8°
	nom																
	min		0.05	0.80		0.19	0.09	7.70	4.30		6.20		0.45				0°

Notes

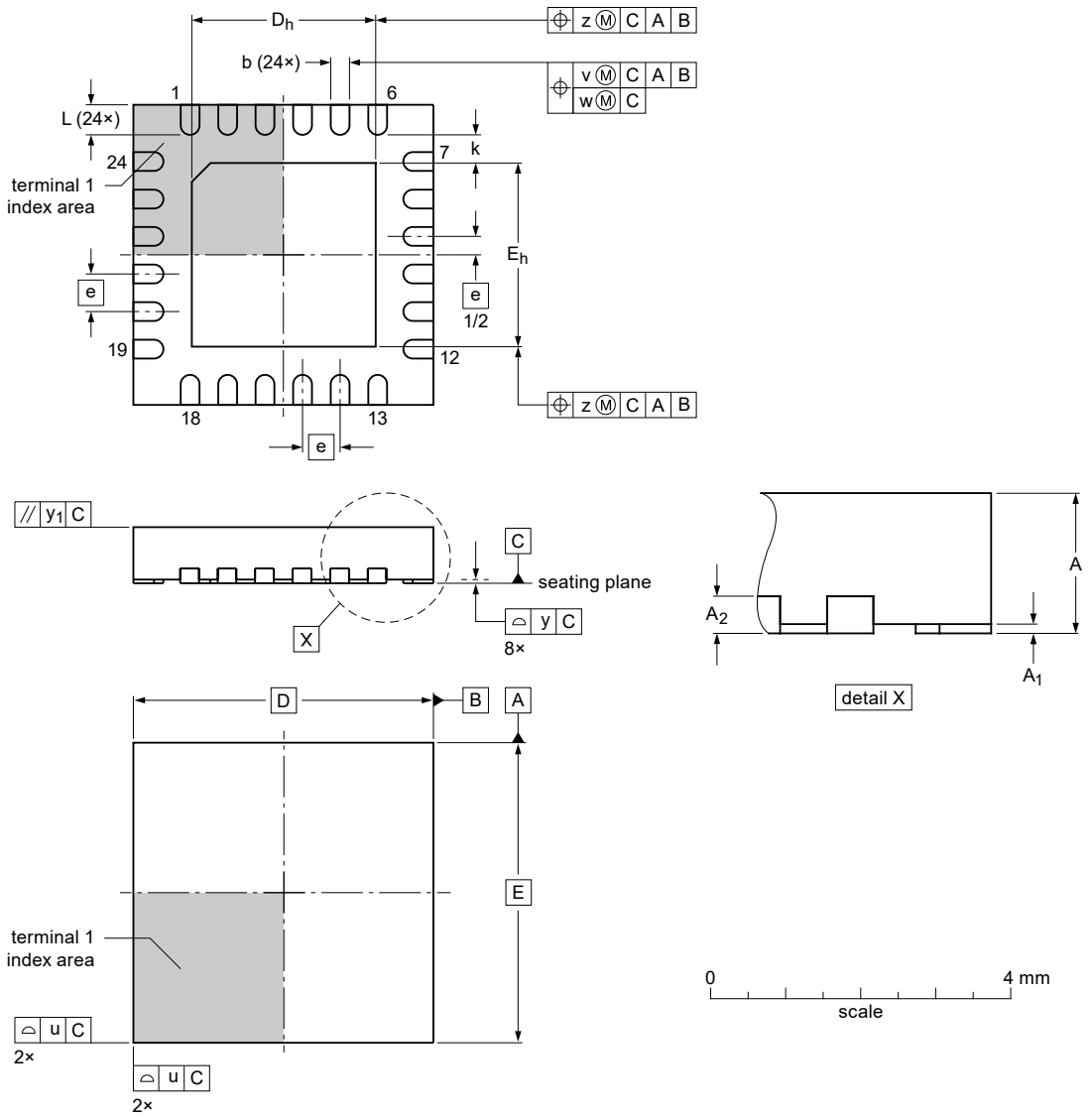
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot355-1_po

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~03-02-19~~ 24-11-07

Fig. 21. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin Quad Flat packages, no leads; 24 terminals; 0.5 mm pitch; 4 x 4 x 0.75 mm body **SOT8041-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_h	E	E_h	e	k	L	u	v	w	y	y_1	z
mm	max	0.80	0.05	0.2 Ref.	0.30	4 BSC	2.55	4 BSC	2.55	0.5 BSC	0.375 Ref.	0.50	0.10	0.10	0.05	0.08	0.10	0.10
	nom	0.75			0.25		2.45		2.45			0.40						
	min	0.70	0.00		0.20		2.35		2.35			0.30						

sot8041-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8041-1		MO-220 (WGGD-8)				~~22-04-01~~ 22-04-25

Fig. 22. Package outline SOT8041-1 (HWQFN24)

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA9548A_Q100 v.1	20250820	Product data sheet	-	-

19. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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