

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE01H21TC uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of other applications.

General Features

- $V_{DSS} = 100V, I_D = 210A$
 $R_{DS(ON)} < 4.2m\Omega @ V_{GS}=10V$ (Typ: 3.3 m Ω)

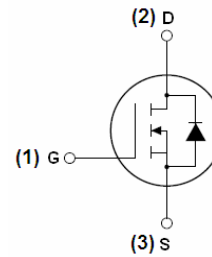
- Good stability and uniformity with high E_{AS}
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- DC motor drive
- High efficiency synchronous rectification in SMPS
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits

100% UIS TESTED!

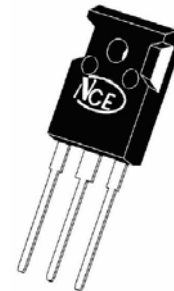
100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-247 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE01H21TC	NCE01H21TC	TO-247	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	140	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	385	W
Derating factor		2.57	W/ $^\circ C$

Single pulse avalanche energy ^(Note 3)	E_{AS}	2300	mJ
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	13	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 1)	$R_{\theta JC}$	0.39	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

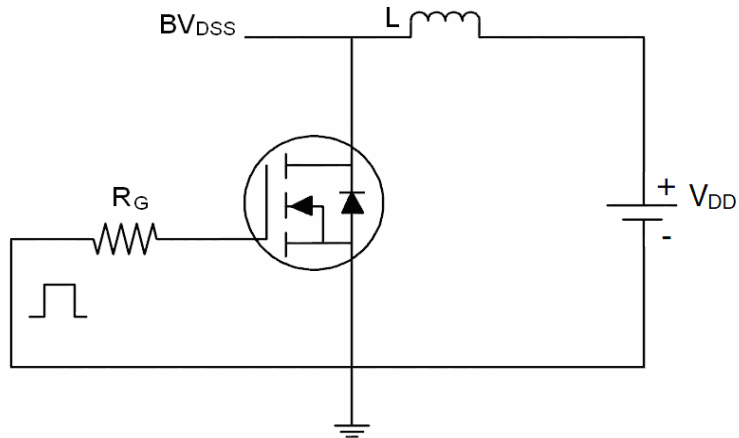
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	-	3.3	4.2	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=40A$	300	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	13500	-	PF
Output Capacitance	C_{oss}		-	862	-	PF
Reverse Transfer Capacitance	C_{rss}		-	659	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$ (Note2)	-	68	-	nS
Turn-on Rise Time	t_r		-	45	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	215	-	nS
Turn-Off Fall Time	t_f		-	56	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$ (Note2)	-	304	-	nC
Gate-Source Charge	Q_{gs}		-	64	-	nC
Gate-Drain Charge	Q_{gd}		-	95	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 75A$ $di/dt = 100A/\mu s$ (Note2)	-	65	-	nS
Reverse Recovery Charge	Q_{rr}		-	98	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

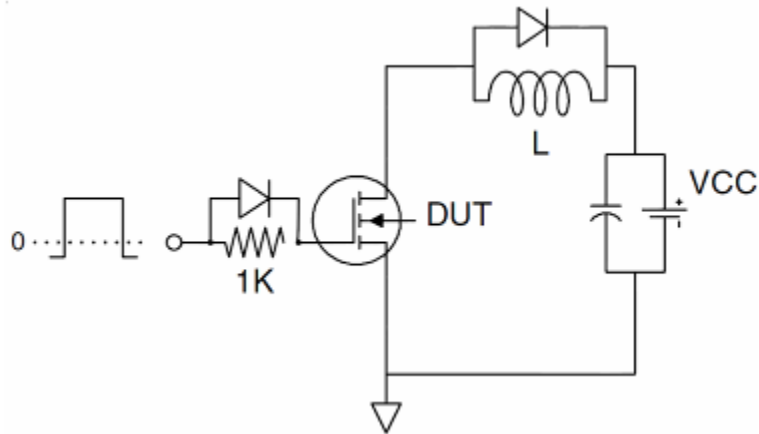
- Surface Mounted on FR4 Board, $t \leq 10$ sec.
- Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
- EAS condition: $T_J=25^\circ\text{C}, V_{DD}=37.5V, V_G=10V, L=2mH, R_g=25\Omega, I_{AS}=37A$
- $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$

Test Circuit

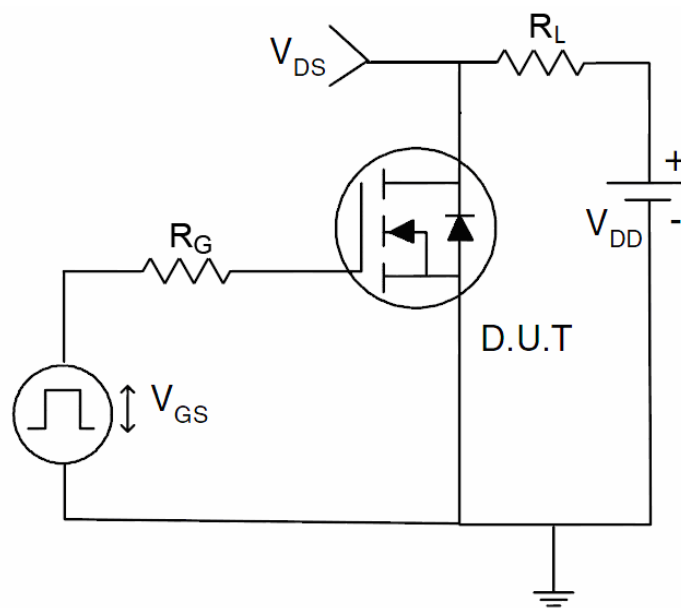
1) E_{AS} Test Circuits



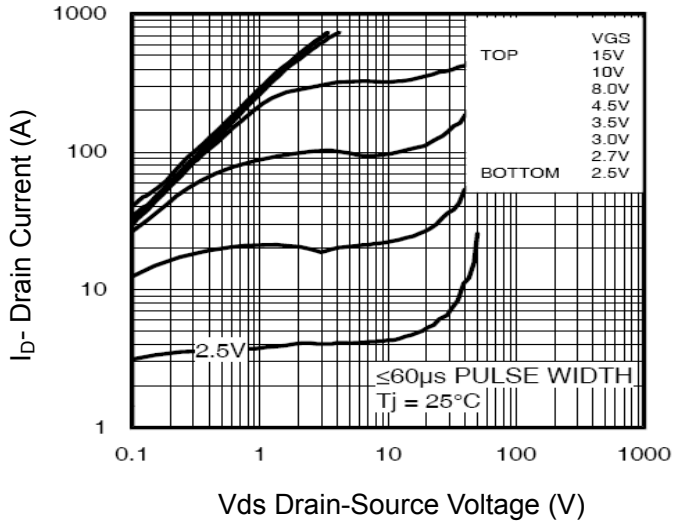
2) Gate Charge Test Circuit:



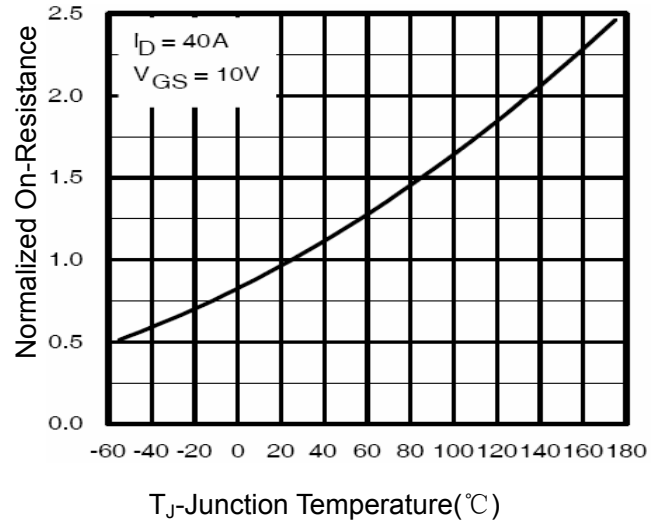
3) Switch Time Test Circuit:



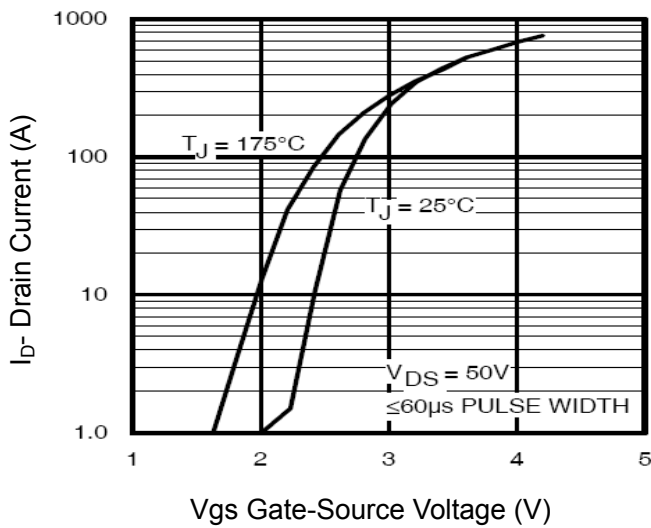
Typical Electrical and Thermal Characteristics



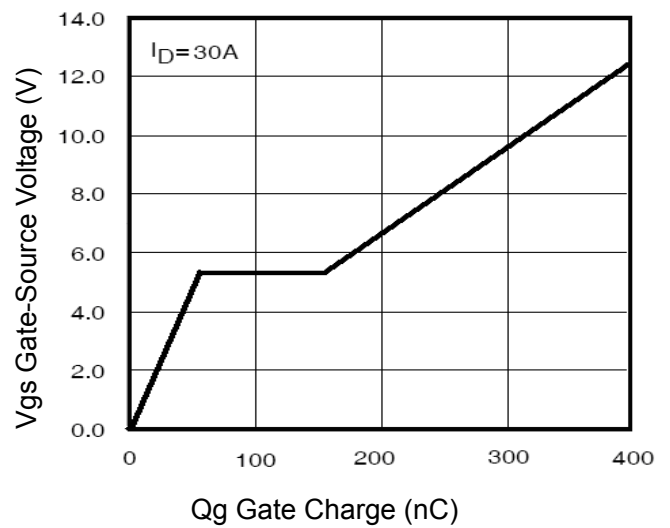
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



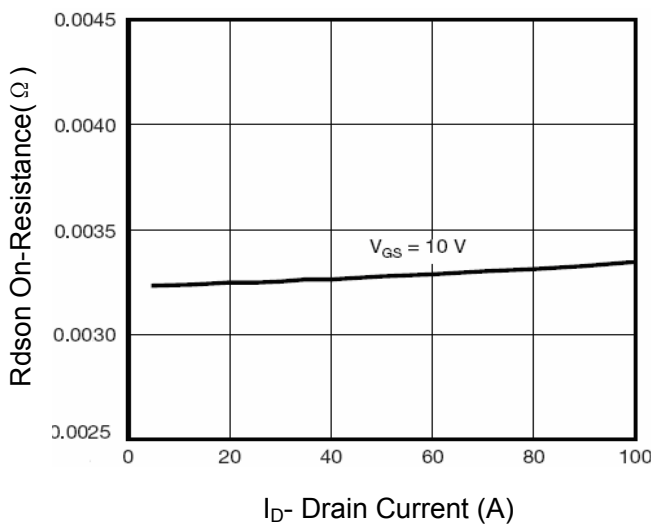
T_J -Junction Temperature($^\circ C$)
Figure 4 R_{dson} -Junction Temperature



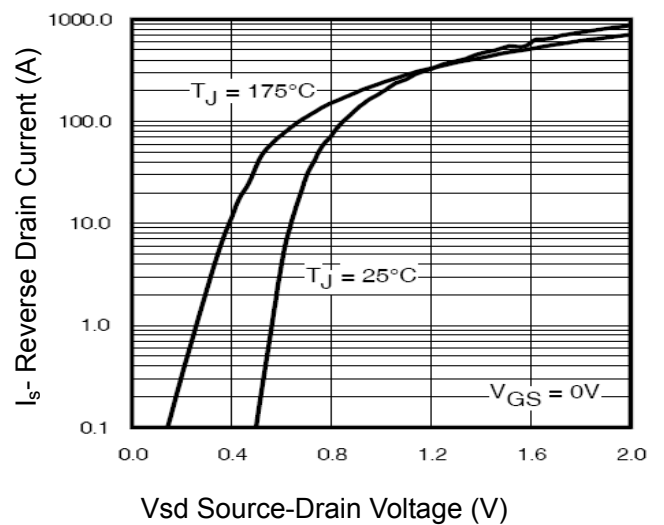
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



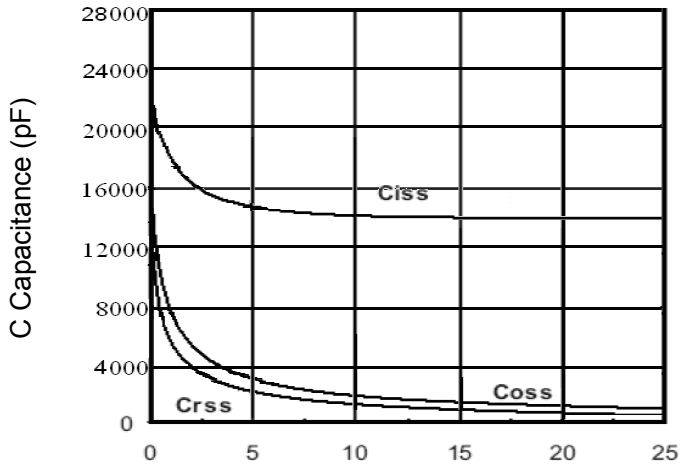
Qg Gate Charge (nC)
Figure 5 Gate Charge



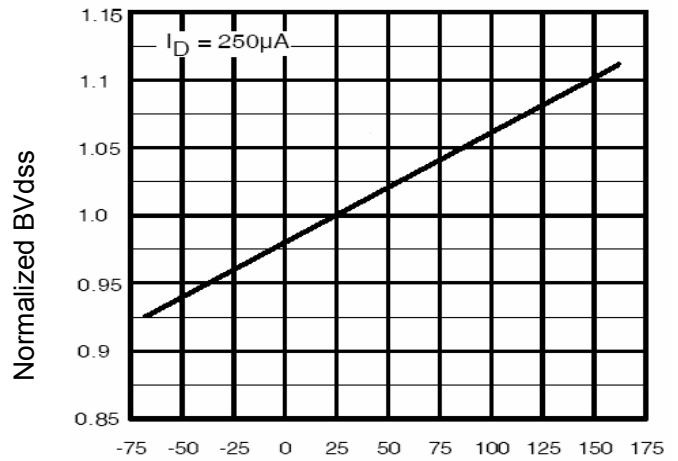
I_D - Drain Current (A)
Figure 3 R_{dson} - Drain Current



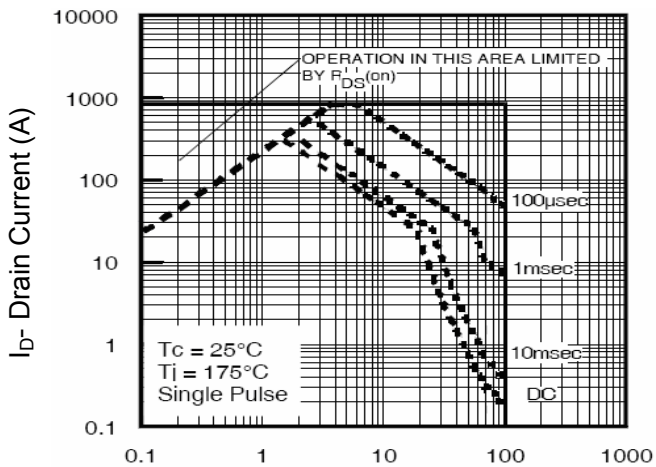
Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



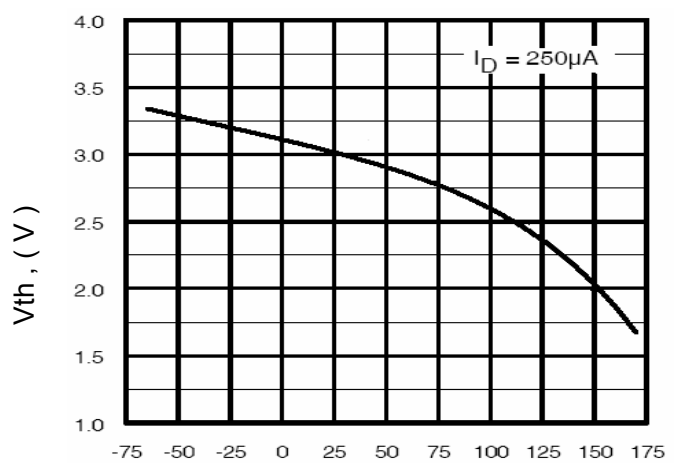
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature

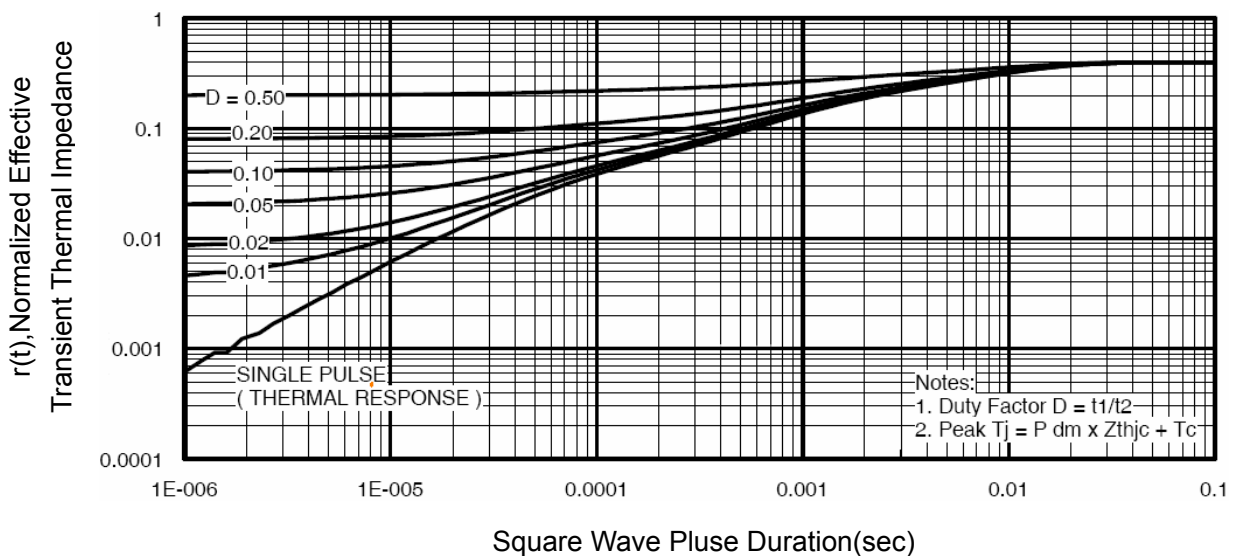
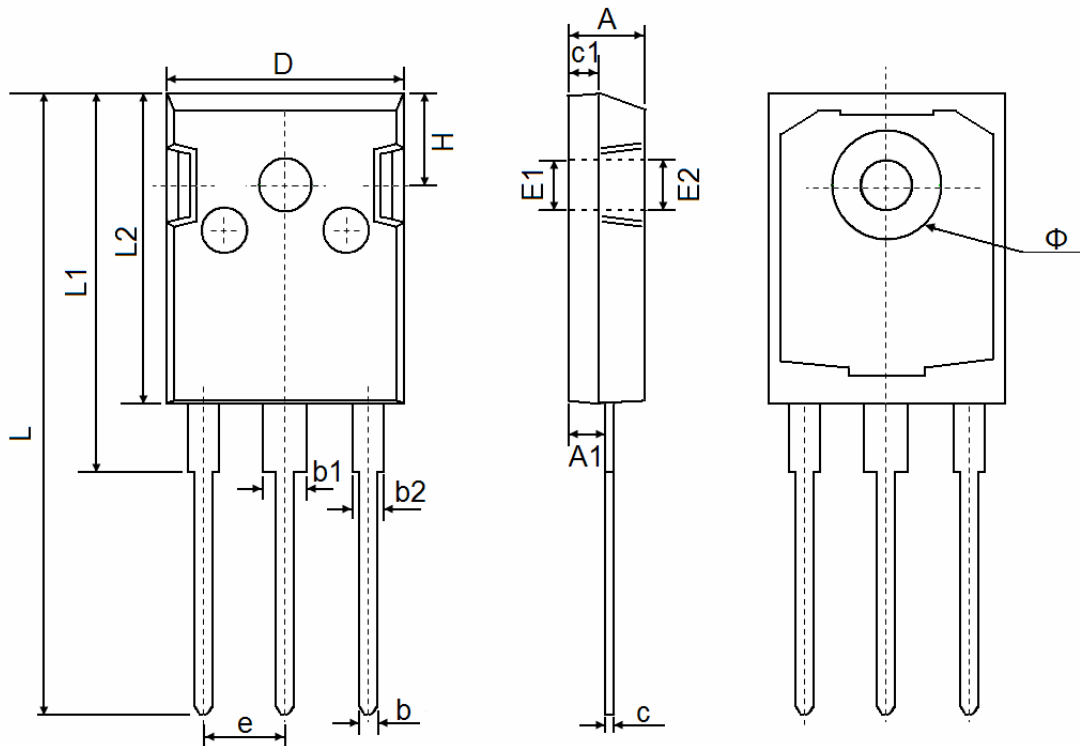


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-247 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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