

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

The NCE0213 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

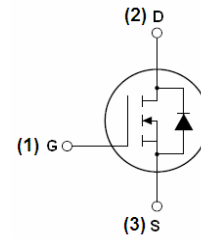
- $V_{DS} = 200V, I_D = 13A$   
 $R_{DS(ON)} < 140m\Omega @ V_{GS} = 10V$  (Typ: 123m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- Boost converters
- LED backlighting
- Uninterruptible power supply

**100% UIS TESTED!**

**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-220-3L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0213	NCE0213	TO-220-3L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	200	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	13	A
$I_D(100^\circ C)$	Drain Current-Continuous( $T_C = 100^\circ C$ )	9	A
$I_{DM}$	Pulsed Drain Current	45	A
$P_D$	Maximum Power Dissipation	95	W
	Derating factor	0.6	W/ $^\circ C$
$E_{AS}$	Single pulse avalanche energy <sup>(Note 5)</sup>	200	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

**Thermal Characteristic**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	1.6	°C/W
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**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	200	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=200V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics <sup>(Note 3)</sup></b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=8A$	-	123	140	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=10V, I_D=8A$	-	6	-	S
<b>Dynamic Characteristics <sup>(Note 4)</sup></b>						
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	2000	-	PF
$C_{oss}$	Output Capacitance		-	260	-	PF
$C_{riss}$	Reverse Transfer Capacitance		-	150	-	PF
<b>Switching Characteristics <sup>(Note 4)</sup></b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=100V, R_G=8\Omega$ $V_{GS}=10V, I_D=8A$	-	11.5	-	nS
$t_r$	Turn-on Rise Time		-	22	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	18	-	nS
$t_f$	Turn-Off Fall Time		-	10	-	nS
$Q_g$	Total Gate Charge	$V_{DS}=160V, I_D=8A,$ $V_{GS}=10V$	-	27	-	nC
$Q_{gs}$	Gate-Source Charge		-	4.4	-	nC
$Q_{gd}$	Gate-Drain Charge		-	11.6	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sup>(Note 3)</sup>	$V_{GS}=0V, I_S=8A$	-	-	1.2	V
$I_S$	Diode Forward Current <sup>(Note 2)</sup>	-	-	-	13	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 8A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	32	-	nS
$Q_{rr}$	Reverse Recovery Charge		-	53	-	nC
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25\Omega$

**Test Circuit**

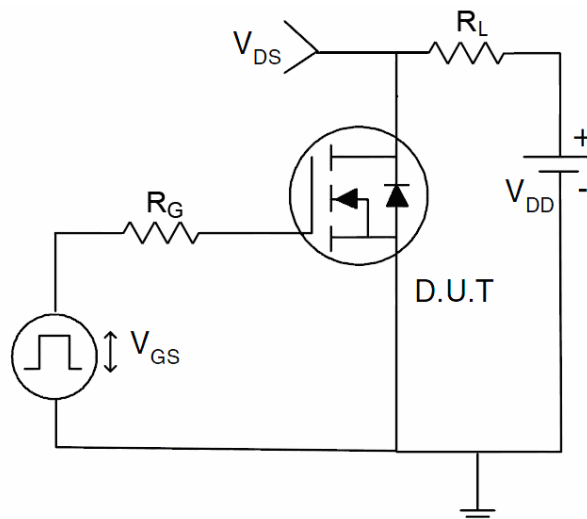
**1) E<sub>AS</sub> Test Circuit**



**2) Gate Charge Test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics (Curves)

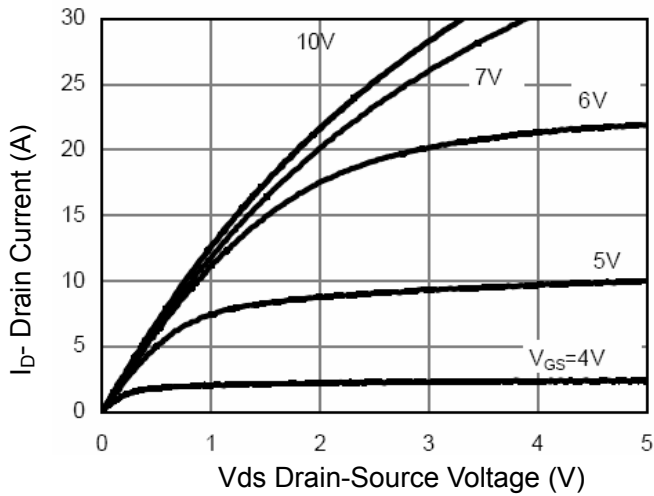


Figure 1 Output Characteristics

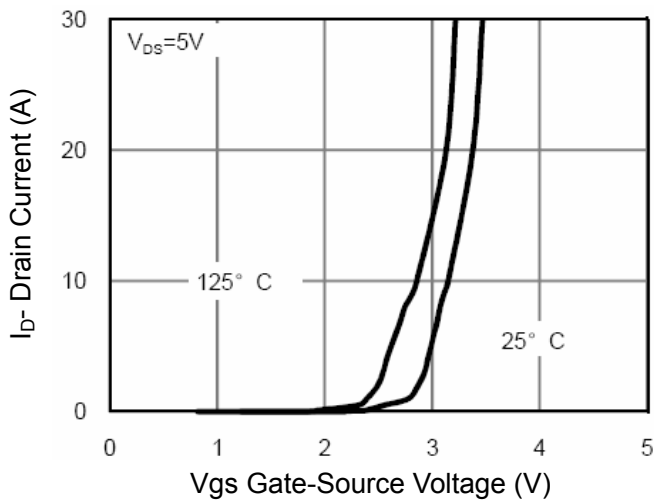


Figure 2 Transfer Characteristics

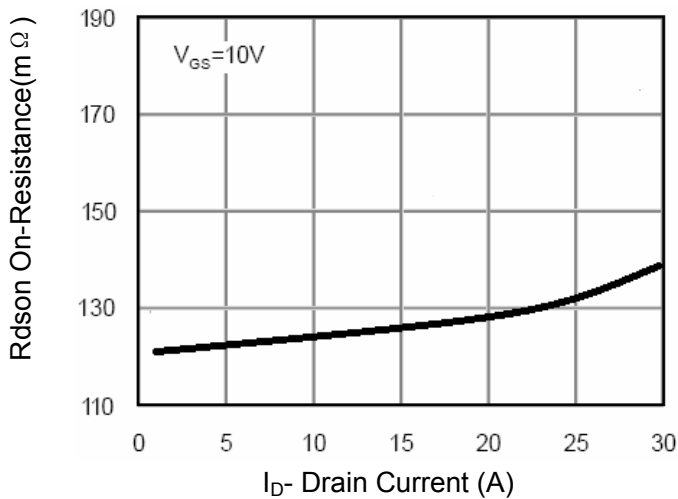


Figure 3 Rdson- Drain Current

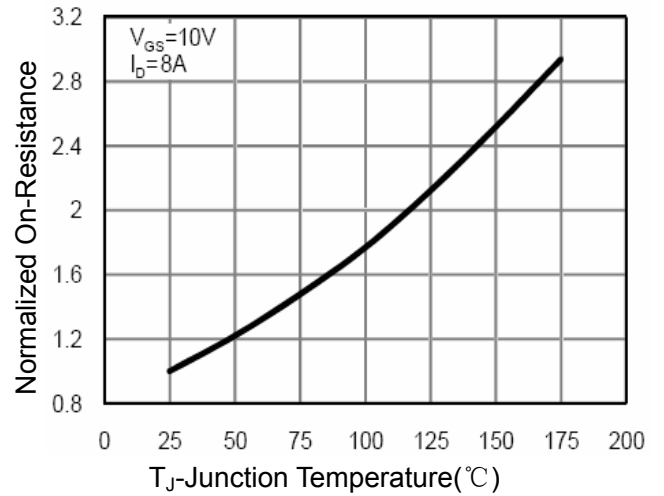


Figure 4 Rdson-Junction Temperature

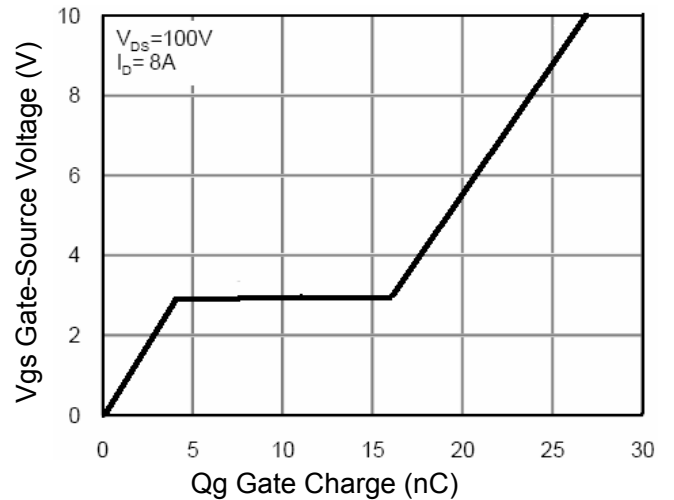


Figure 5 Gate Charge

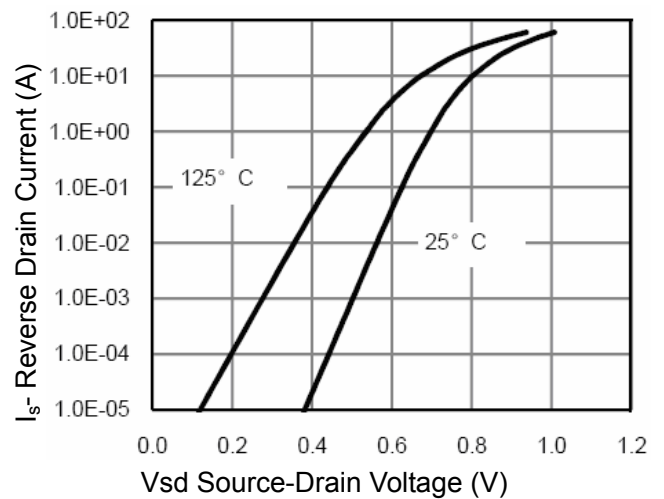


Figure 6 Source- Drain Diode Forward

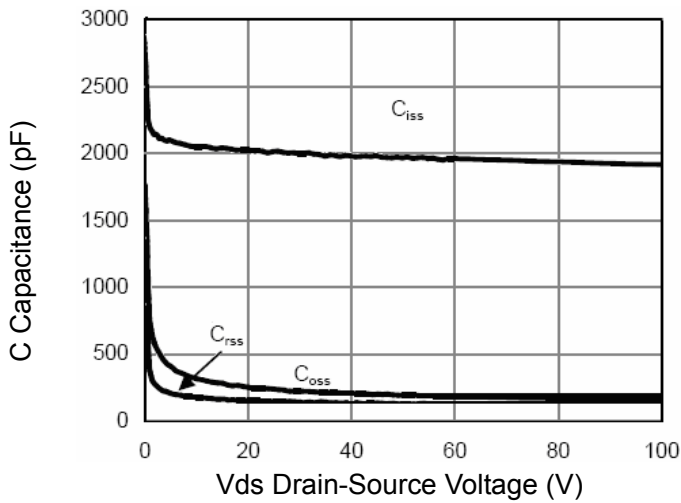


Figure 7 Capacitance vs Vds

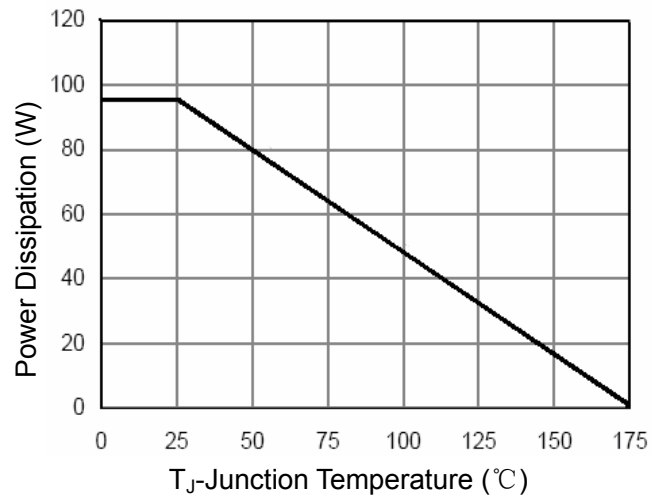


Figure 9 Power De-rating

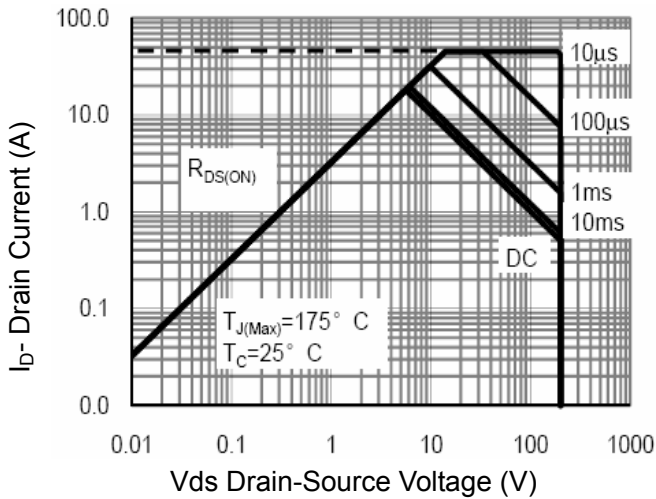


Figure 8 Safe Operation Area

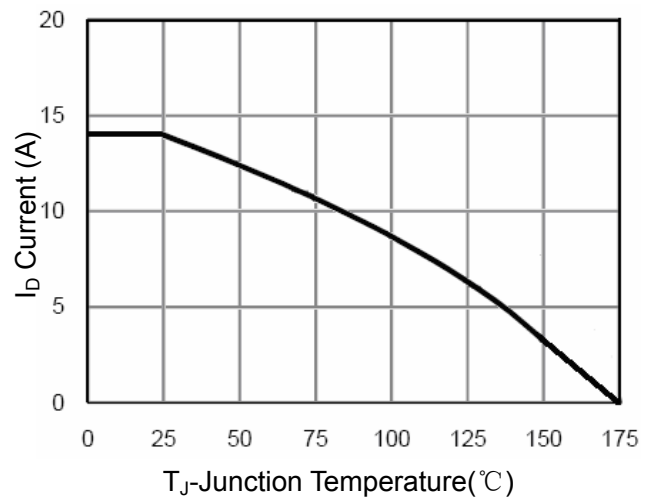


Figure 10 ID Current- Junction Temperature

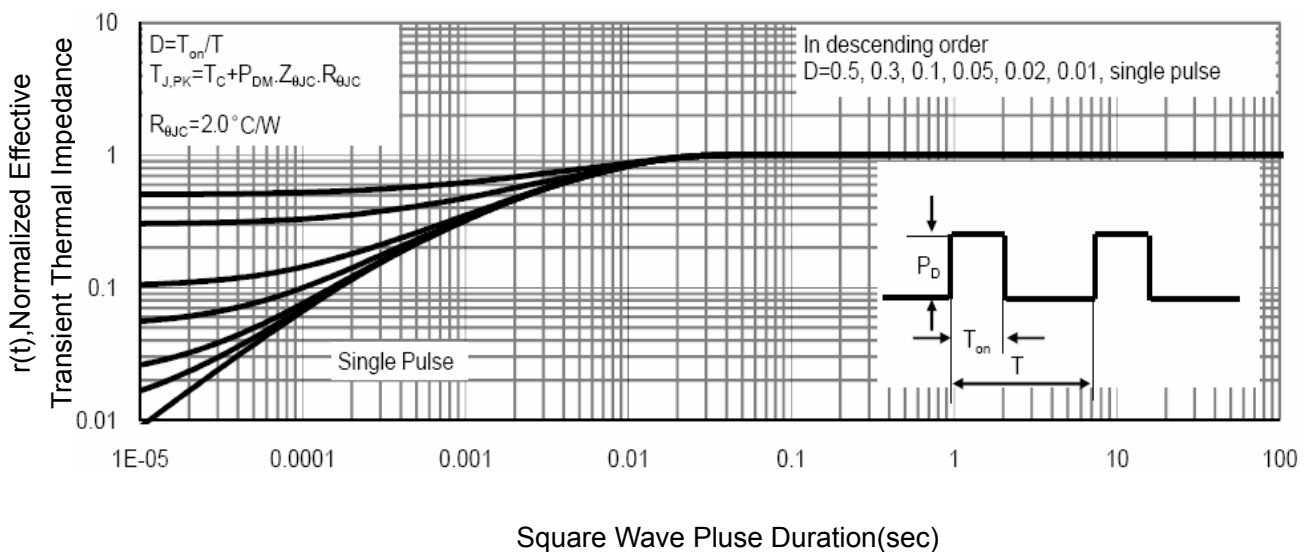
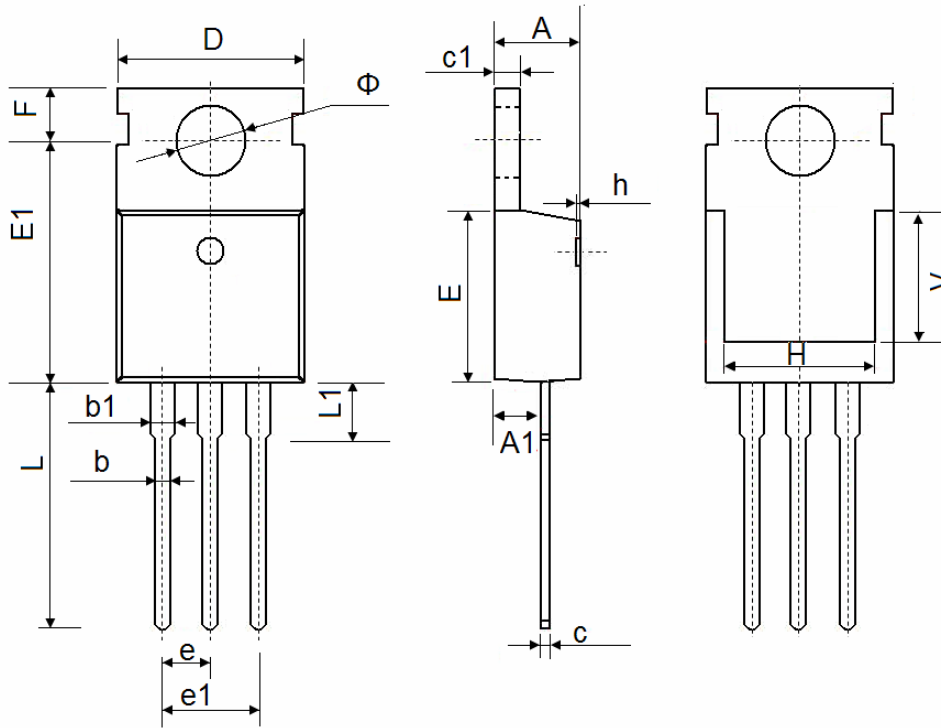


Figure 11 Normalized Maximum Transient Thermal Impedance

**TO-220-3L Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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