

## NCE N-Channel Enhancement Mode Power MOSFET

### DESCRIPTION

The NCE1540D uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### GENERAL FEATURES

- $V_{DS} = 150V, I_D = 40A$   
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = 10V$  (Typ: 35m $\Omega$ )
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

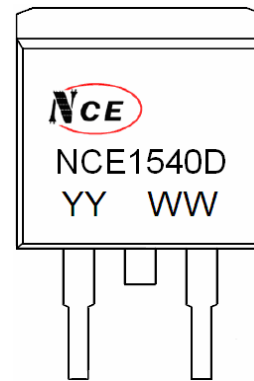
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

**100% UIS TESTED!**

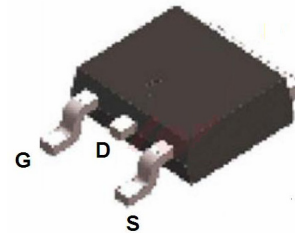
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin Assignment



TO-263-2L top view

### Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE1540D	NCE1540D	TO-263-2L	-	-	-

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	40	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	29	A
Pulsed Drain Current	$I_{DM}$	164	A
Maximum Power Dissipation	$P_D$	140	W
Derating factor		0.93	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	$E_{AS}$	310	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.07	$^{\circ}\text{C/W}$
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### Electrical Characteristics (TA=25 $^{\circ}\text{C}$ unless otherwise noted)

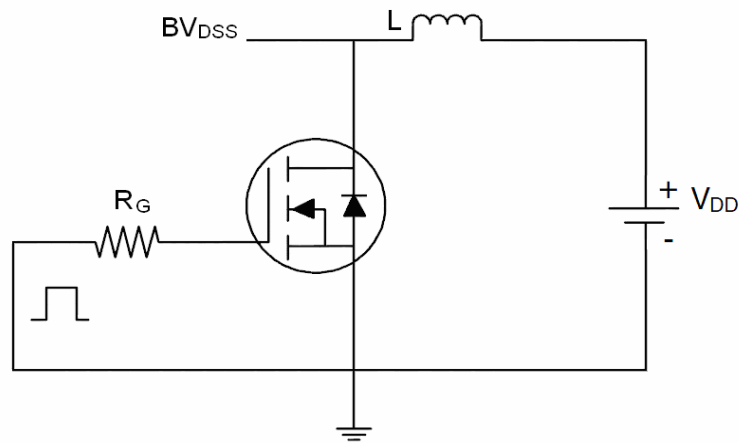
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	150	170	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=150V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.2	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=18A$	-	35	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=15V, I_D=18A$	38	-	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4200	-	PF
Output Capacitance	$C_{oss}$		-	203	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	96	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	17.8	-	nS
Turn-on Rise Time	$t_r$		-	11.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	56	-	nS
Turn-Off Fall Time	$t_f$		-	14.6	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$	-	105	-	nC
Gate-Source Charge	$Q_{gs}$		-	21	-	nC
Gate-Drain Charge	$Q_{gd}$		-	31.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=18A$	-	0.82	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	40	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 18A$ $di/dt = 100A/\mu s$ (Note 3)	-	70	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	230	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=75V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

## Test circuit

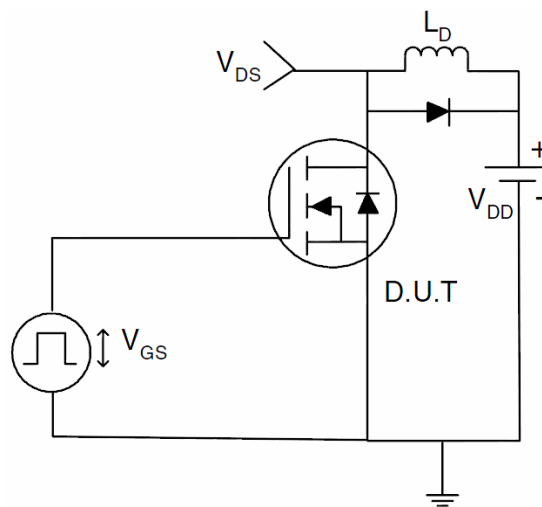
### 1) E<sub>AS</sub> test Circuits



### 2) Gate charge test Circuit:



### 3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

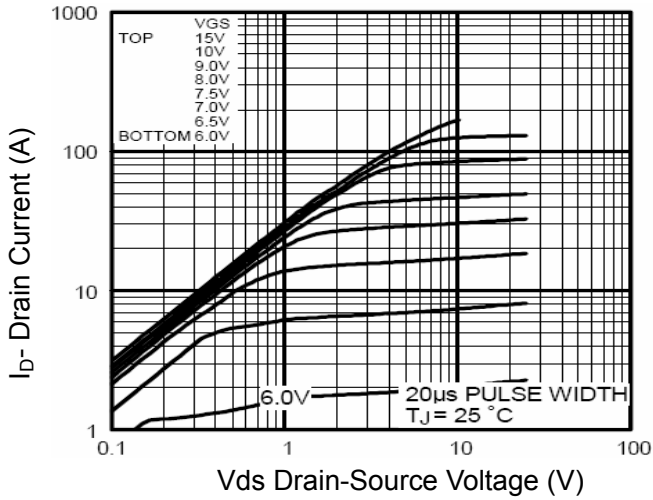


Figure 1 Output Characteristics

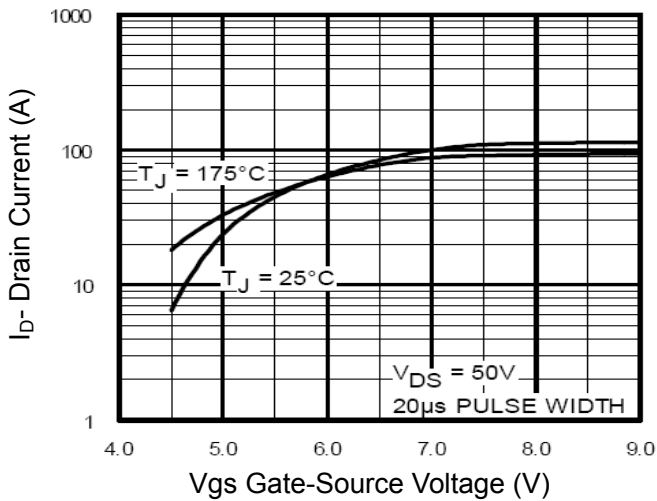


Figure 2 Transfer Characteristics

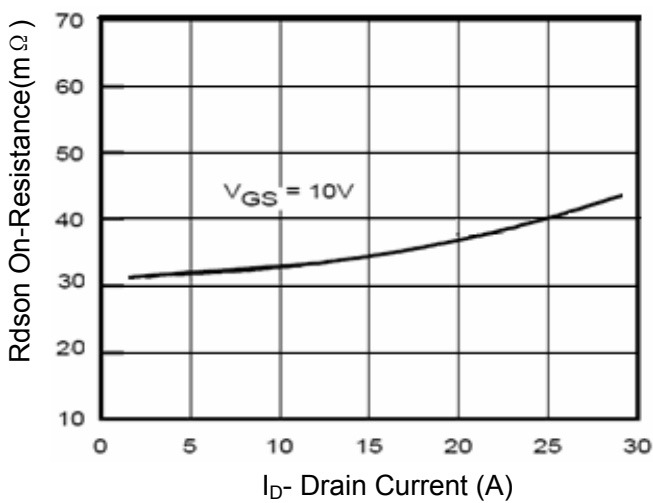


Figure 3  $R_{DS(on)}$ - Drain Current

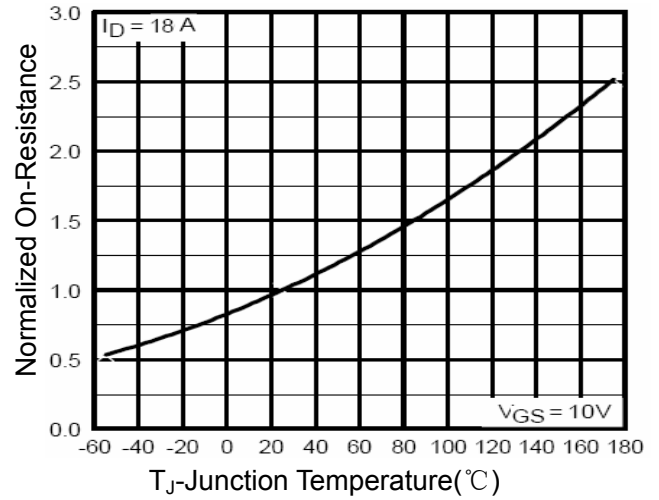


Figure 4  $R_{DS(on)}$ -Junction Temperature

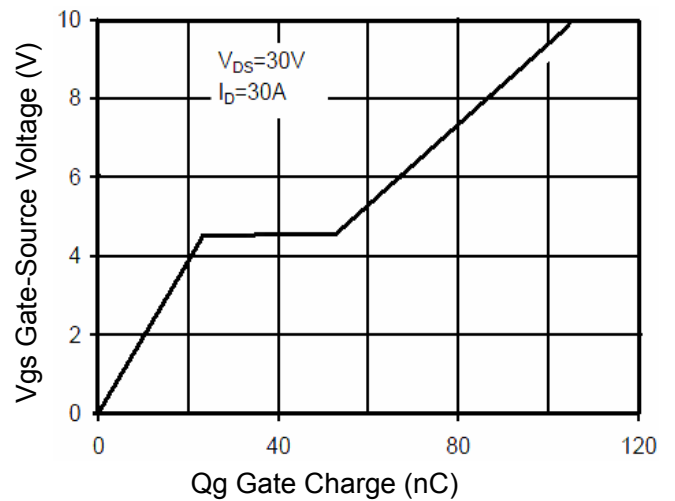


Figure 5 Gate Charge

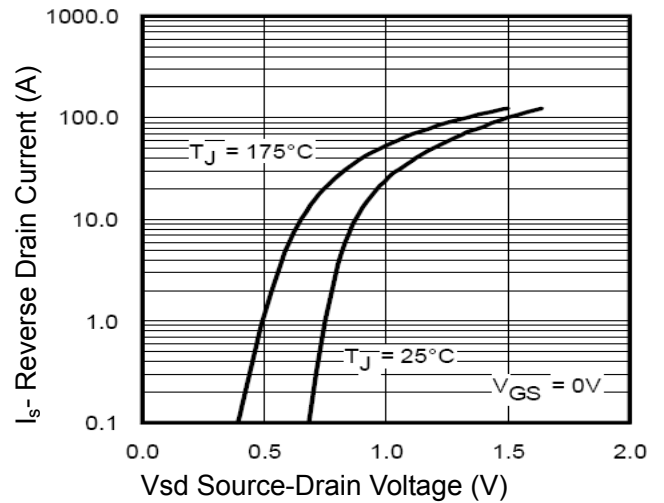


Figure 6 Source- Drain Diode Forward

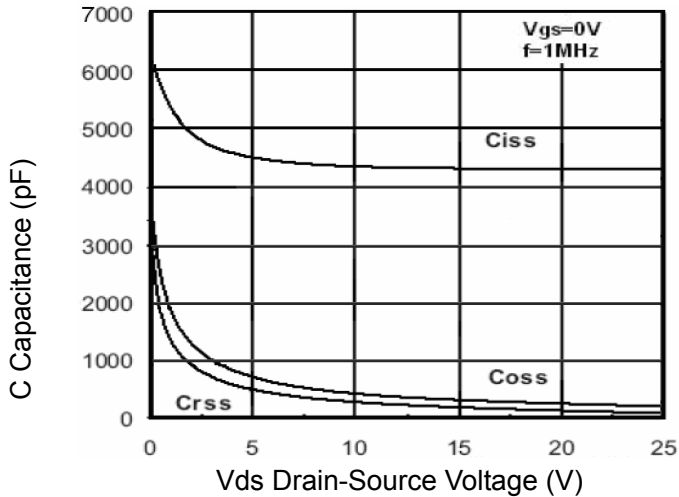


Figure 7 Capacitance vs Vds

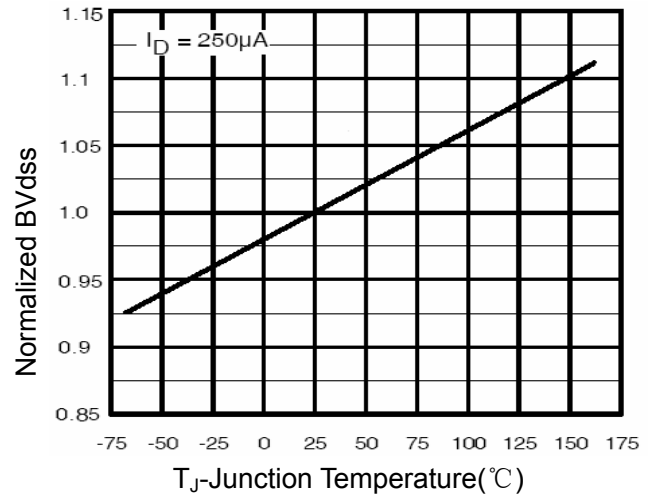


Figure 9  $BV_{DSS}$  vs Junction Temperature

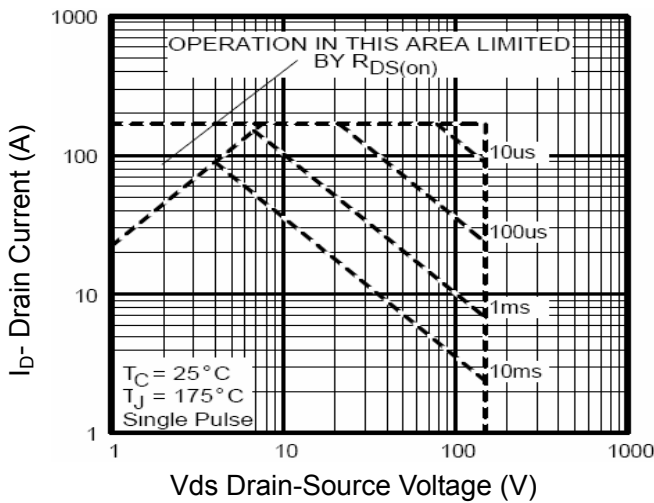


Figure 8 Safe Operation Area

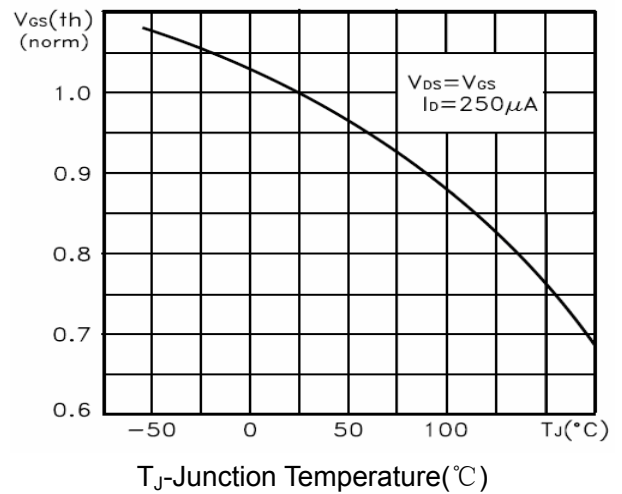


Figure 10  $V_{GS(th)}$  vs Junction Temperature

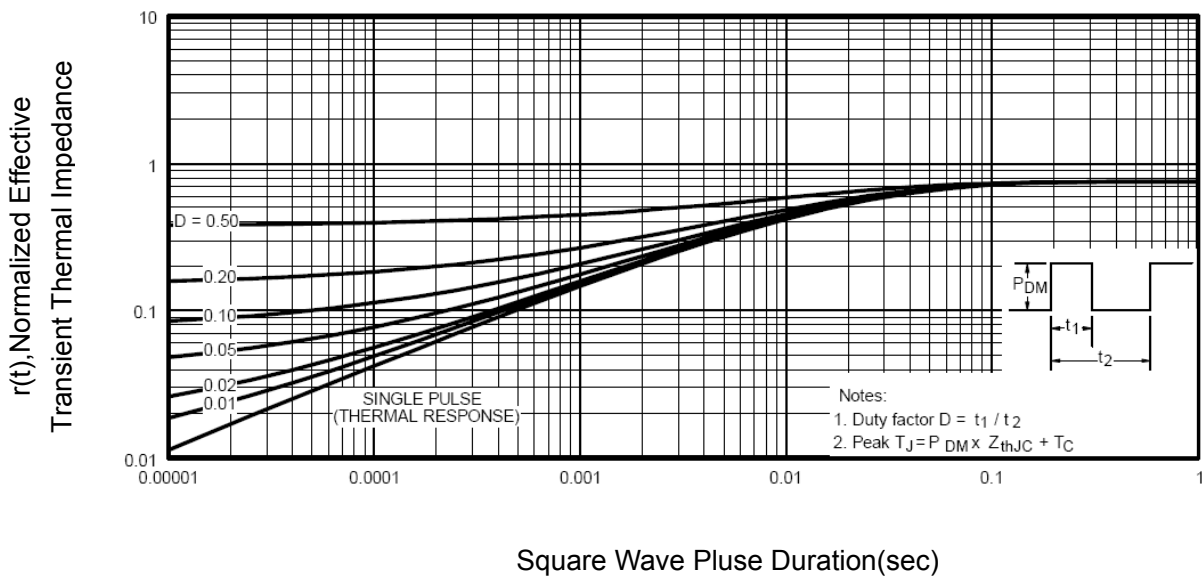
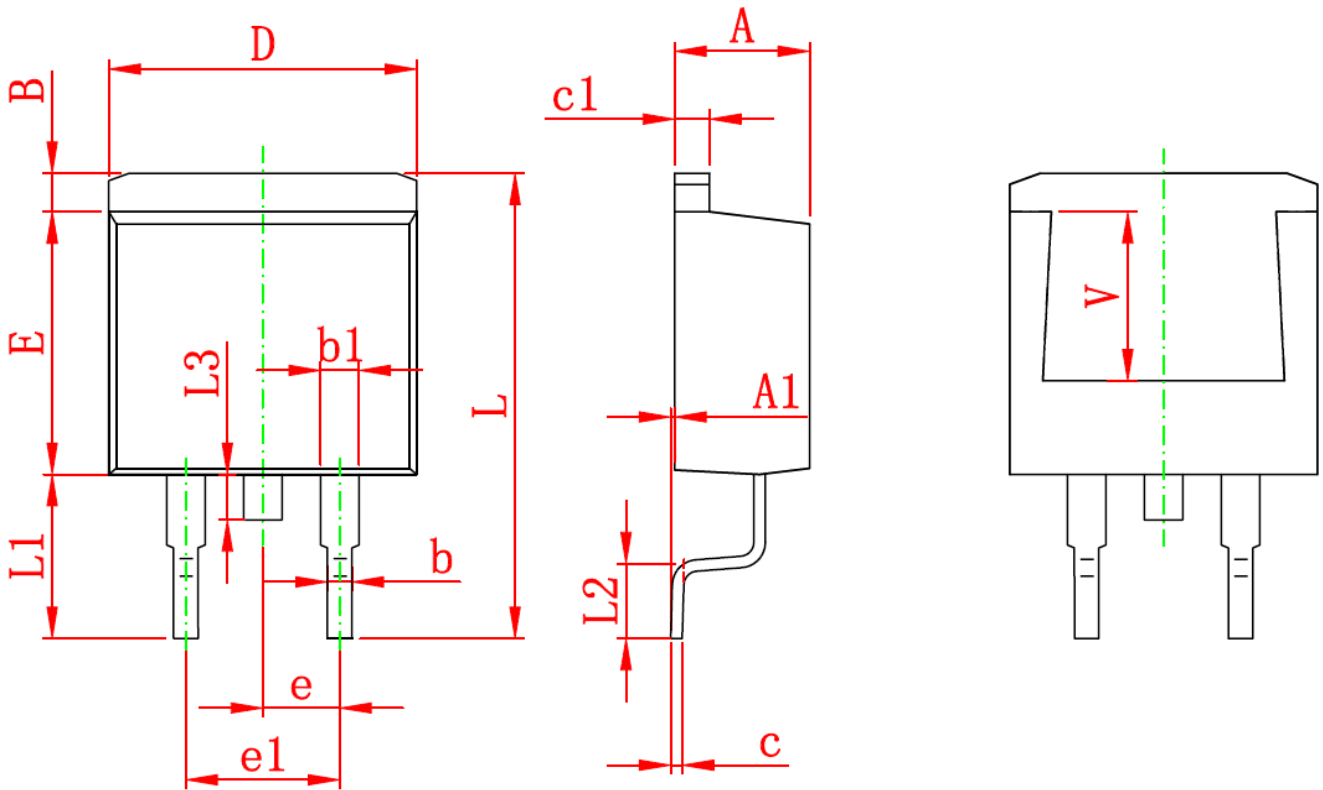


Figure 11 Normalized Maximum Transient Thermal Impedance

**TO-263-2L PACKAGE INFORMATION**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 (TYP.)		0.100 (TYP.)	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF.		0.220 REF.	

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