

### NCE N-Channel Enhancement Mode Power MOSFET

#### **Description**

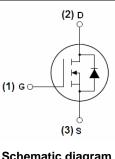
The NCE5520Q uses advanced trench technology and design to provide excellent R<sub>DS(ON)</sub> with low gate charge. It can be used in a wide variety of applications.

#### **General Features**

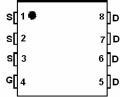
- V<sub>DS</sub> =55V,I<sub>D</sub> =20A  $R_{DS(ON)} < 22m\Omega$  @  $V_{GS}=10V$  (Typ:19m $\Omega$ )
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current

### **Application**

- Industrial power supplies
- LED backlighting



#### Schematic diagram



Pin assignment



**DFN3X3 EP top view** 

### **Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity	
NCE5520Q	NCE5520Q	DFN3X3EP	-	-	-	

## Absolute Maximum Ratings (T<sub>C</sub>=25 ℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	55	V
Gate-Source Voltage	V <sub>G</sub> S	±20	V
Drain Current-Continuous	I <sub>D</sub>	20	А
Drain Current-Continuous(T <sub>C</sub> =100 °C)	I <sub>D</sub> (100℃)	14	Α
Pulsed Drain Current	I <sub>DM</sub>	60	Α
Maximum Power Dissipation	P <sub>D</sub>	35	W
Derating factor		0.23	W/°C
Operating Junction and Storage Temperature Range	$T_{J}, T_{STG}$	-55 To 150	$^{\circ}$

#### **Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{ heta JC}$	3.6	°C/W



# **NCE5520Q**

Electrical Characteristics (T<sub>C</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						•
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	55		-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =55V,V <sub>GS</sub> =0V	-	-	1	μΑ
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						•
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	19	22	mΩ
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>lss</sub>	), 05), ()	-	1340	-	PF
Output Capacitance	Coss		-	123	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.UIVIDZ	-	10	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>		-	6	-	nS
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =25 $V$ , $I_{D}$ =2 $A$ ,	-	2.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$	$R_L=3\Omega,R_G=3\Omega$	-	22	-	nS
Turn-Off Fall Time	t <sub>f</sub>	V <sub>DS</sub> =25V,V <sub>GS</sub> =0V, F=1.0MHz V <sub>DD</sub> =25V,I <sub>D</sub> =2A,	-	2.5	-	nS
Total Gate Charge	Qg	)/ OF)/  40A	-	21	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	5	-	nC
Gate-Drain Charge	$Q_{gd}$	V <sub>GS</sub> =10V	-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	20	Α
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =10A	-	16		nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs <sup>(Note3)</sup>	-	38		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD				

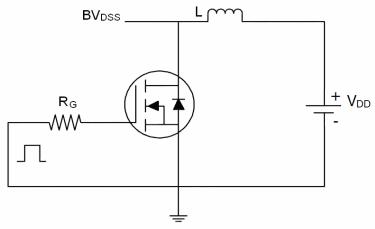
#### Notes:

- $\textbf{1.} \ \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature.}$
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- **5.** E<sub>AS</sub> condition: Tj=25  $^{\circ}$ C,V<sub>DD</sub>=25V,V<sub>G</sub>=10V,L=0.5mH,Rg=25 $\Omega$

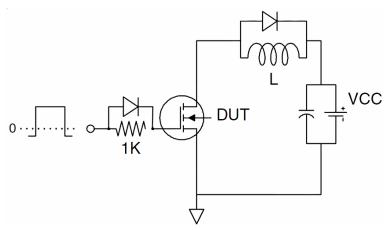


### **Test circuit**

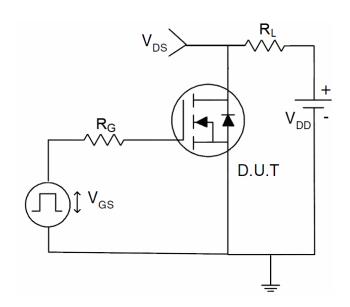
# 1) E<sub>AS</sub> test Circuits



# 2) Gate charge test Circuit



# 3) Switch Time Test Circuit



125

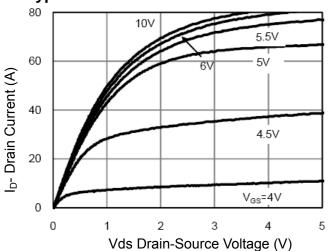
150

175

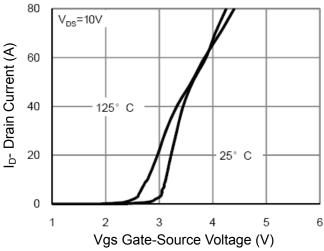
**Pb Free Product** 



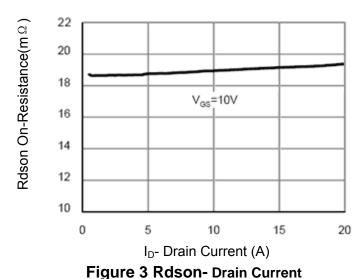
## Typical Electrical and Thermal Characteristics (Curves)



**Figure 1 Output Characteristics** 



**Figure 2 Transfer Characteristics** 



1.8 V<sub>GS</sub>=10V Normalized On-Resistance  $I_D = 10A$ 1.6 1.4 1.2

Figure 4 Rdson-JunctionTemperature

75

T<sub>J</sub>-Junction Temperature(°C)

100

0.8

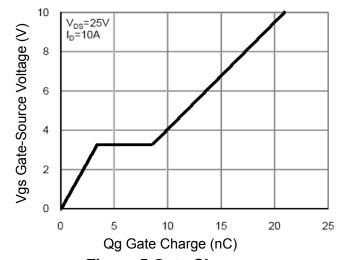


Figure 5 Gate Charge

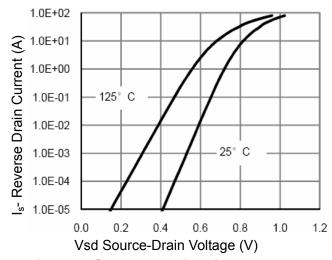
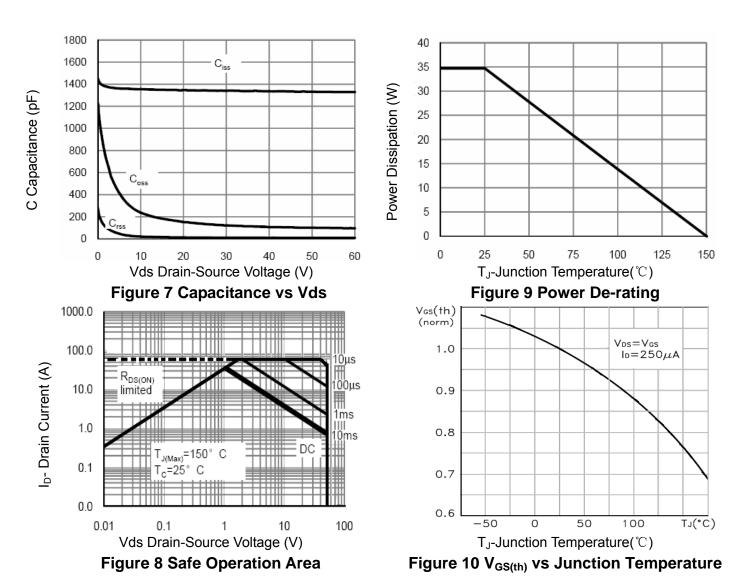
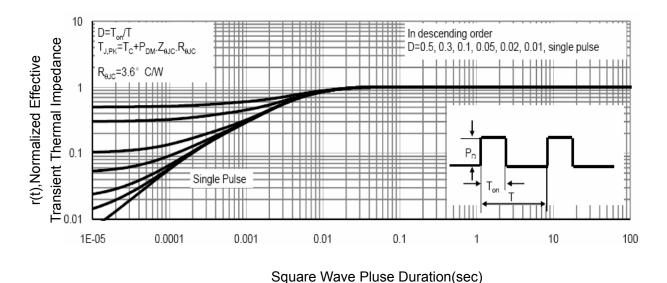


Figure 6 Source- Drain Diode Forward



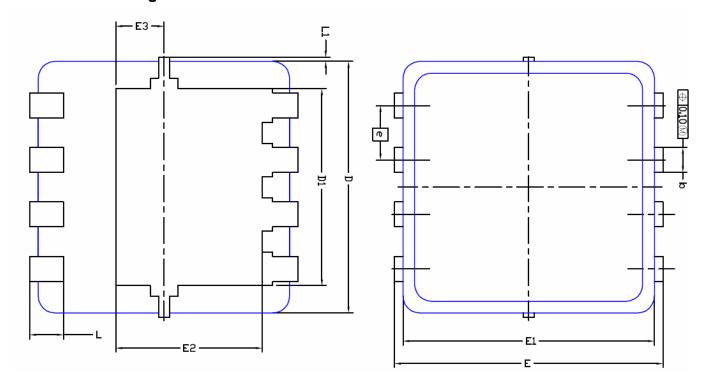


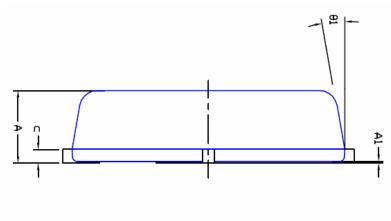


**Figure 11 Normalized Maximum Transient Thermal Impedance** 



# **DFN3X3 EP Package Information**





DIM.	MILLIMETERS			INCHES			
יויודת	MIN	NDM	MAX	MIN	NDM	MAX	
Α	0.700	0.80	0.900	0.0276	0.0315	0.0354	
A1	0.00	-	0.05	0.000		0.002	
b	0,24	0,30	0,35	0,009	0.012	0.014	
C	0,10	0,152	0,25	0,004	0,006	0.010	
D	3	3.00 BSC 0.118 BS0			C		
D1	2.35 BSC			0.093 BSC			
E	3	3.20 BS	С	0.126 BSC			
E1	3	3.00 BS	С	0.118 BSC			
E2	1	.75 BS	С	0,069 BSC			
E3	0.	575 BS	BSC 0.023 BSC			C	
е	0	.65 BS	С	0'056 B2C			
L	0.30	0.40	0,50	0.0118	0.0157	0.0197	
L1	0		0.100	0		0.004	
91	0°	10°	12°	0°	10°	12*	



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