

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP035N85GU uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

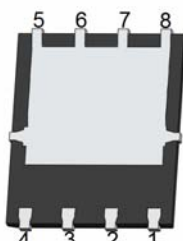
- $V_{DS} = 85V, I_D = 135A$
 $R_{DS(on)} = 2.9m\Omega$ (typical) @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔV_{ds} TESTED!

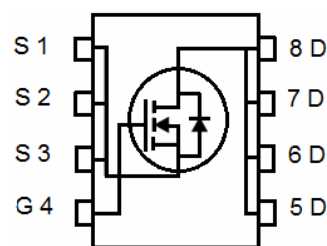
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P035N85GU	NCEP035N85GU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	85	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	135	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	97.2	A
Pulsed Drain Current	I_{DM}	540	A
Maximum Power Dissipation	P_D	160	W
Derating factor		1.28	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	920	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.78	$^\circ C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	85		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=85V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=65A$	-	2.9	3.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=65A$		60	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V,$ $F=1.0MHz$	-	4950	-	PF
Output Capacitance	C_{oss}		-	850	-	PF
Reverse Transfer Capacitance	C_{rss}		-	40	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=65A$ $V_{GS}=10V, R_G=3\Omega$	-	18	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	t_f		-	9	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=65A,$ $V_{GS}=10V$	-	88	-	nC
Gate-Source Charge	Q_{gs}		-	22		nC
Gate-Drain Charge	Q_{gd}		-	25		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=65A$	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	130	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 65A$	-	72	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s^{(Note3)}$	-	102	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=40V, V_G=10V, L=0.5mH, R_G=25\Omega$

Typical Electrical and Thermal Characteristics

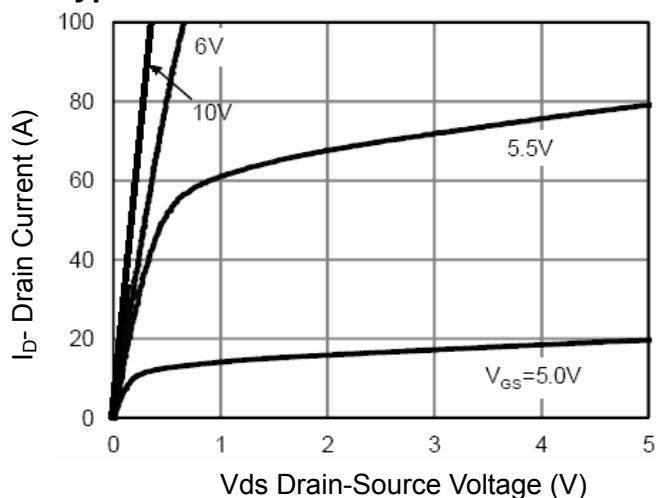


Figure 1 Output Characteristics

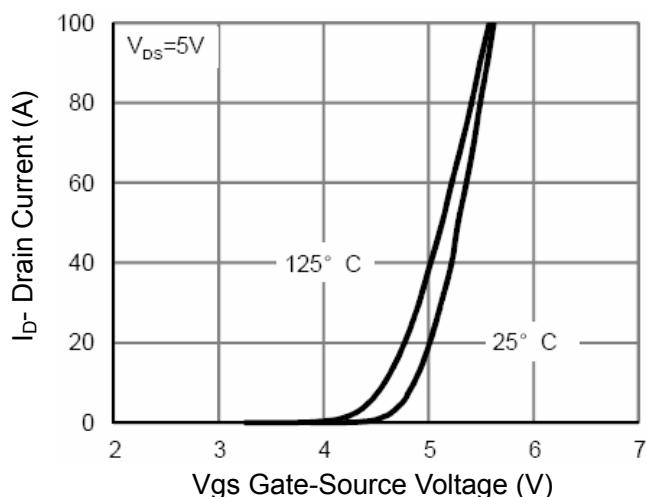


Figure 2 Transfer Characteristics

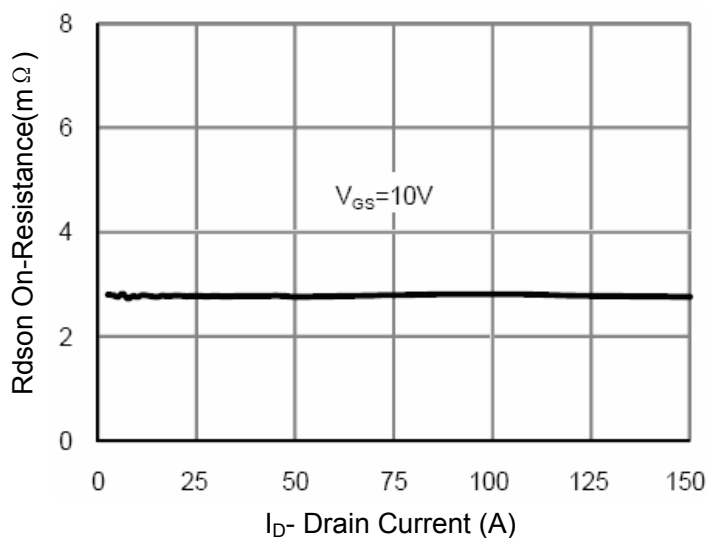


Figure 3 $R_{DS(on)}$ - Drain Current

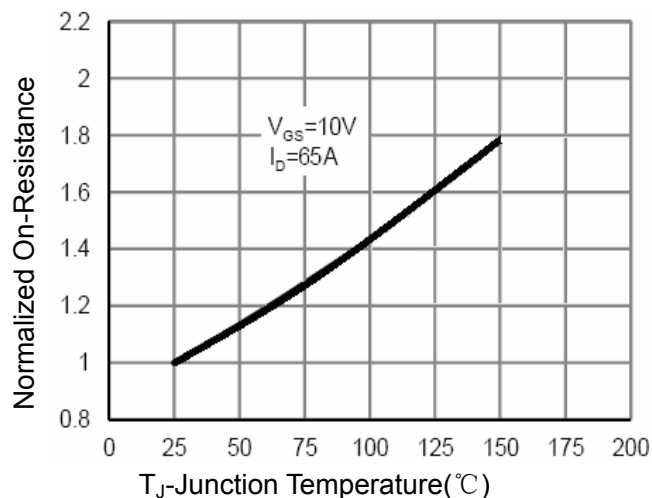


Figure 4 $R_{DS(on)}$ -Junction Temperature

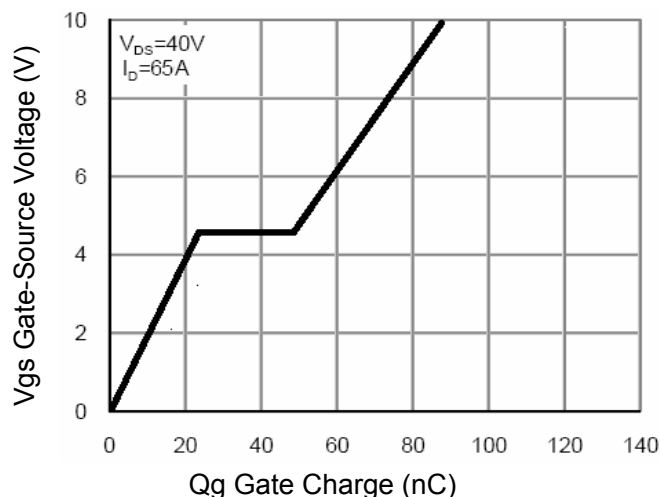


Figure 5 Gate Charge

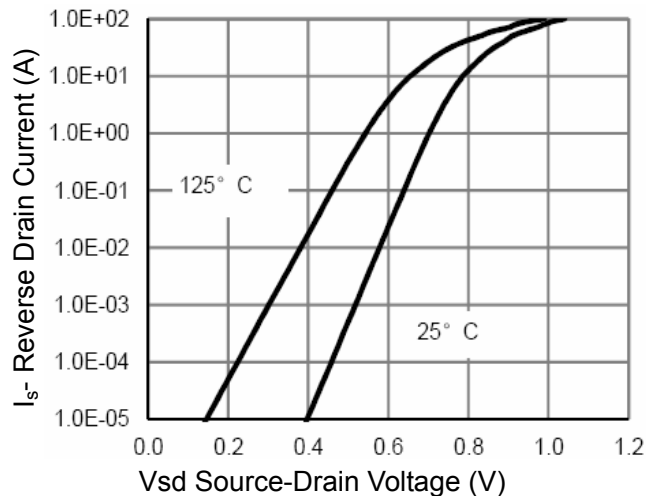


Figure 6 Source- Drain Diode Forward

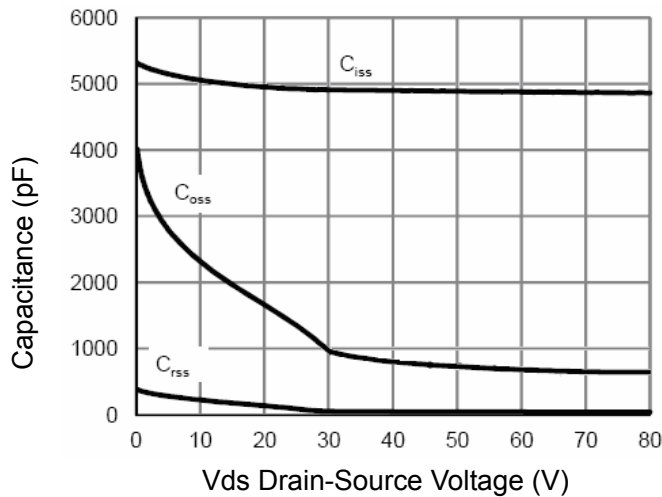


Figure 7 Capacitance vs Vds

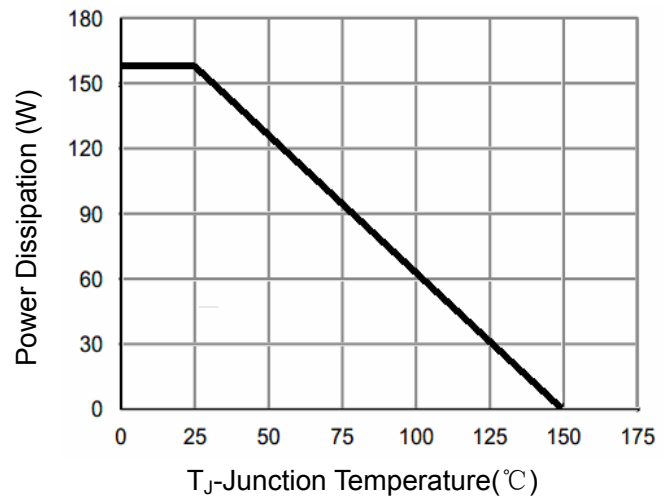


Figure 9 Power De-rating

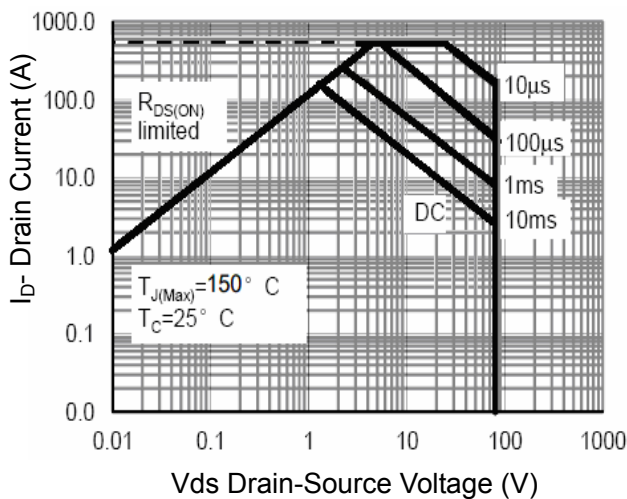


Figure 8 Safe Operation Area

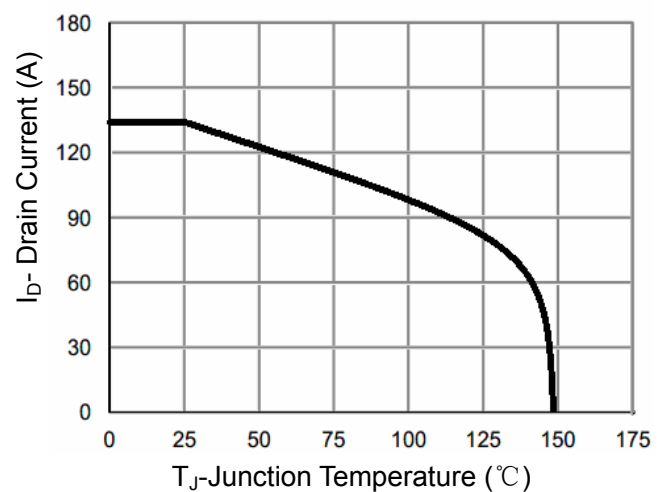


Figure 10 Current De-rating

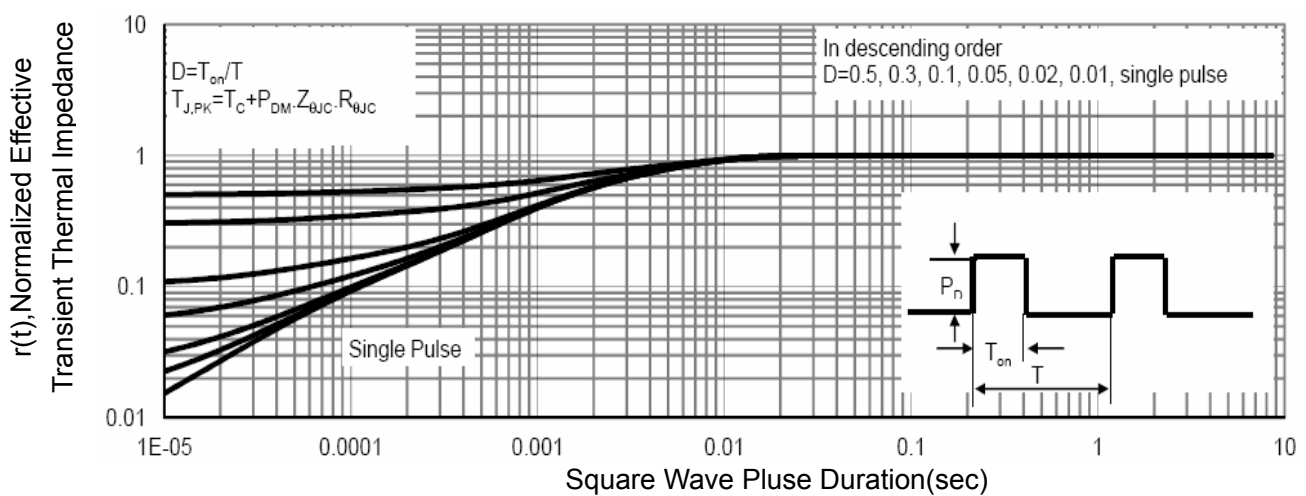
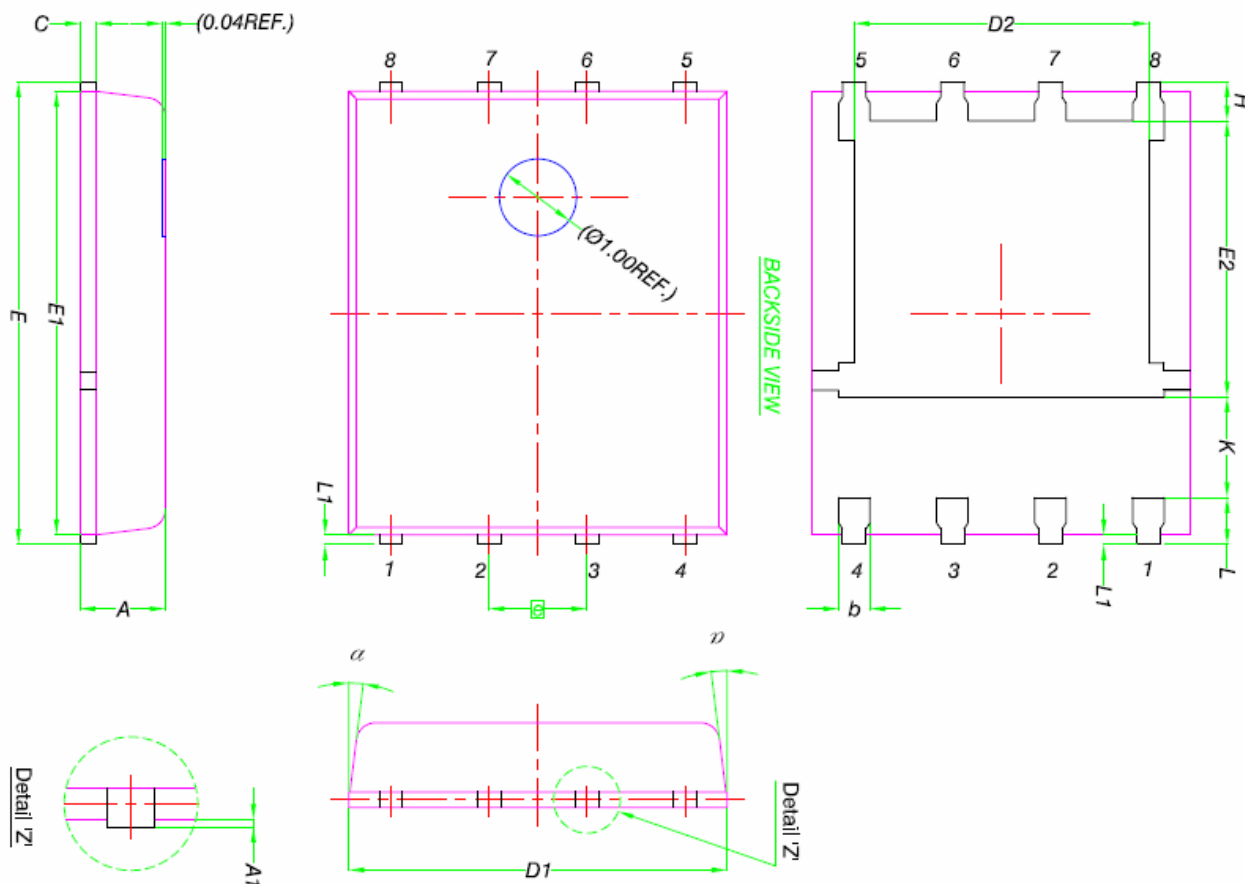
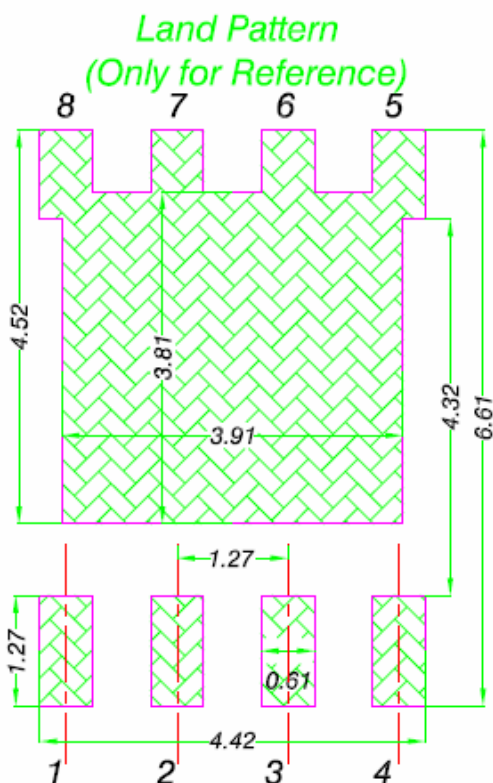


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°



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