Integrated Driver and MOSFET

NCP302155R

The NCP302155R integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP302155R integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 55 A
- Capable of Peak Currents up to 80 A
- Capable of Switching at Frequencies up to 2 MHz
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3−level PWM Inputs
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel® Power State 4
- Thermal Warning output

Applications

- Desktop and All−in−One Computers, V−Core and Non−V−Core DC−DC Converters
- High−Current DC−DC Point−of−Load Converters
- Small Form−Factor Voltage Regulator Modules

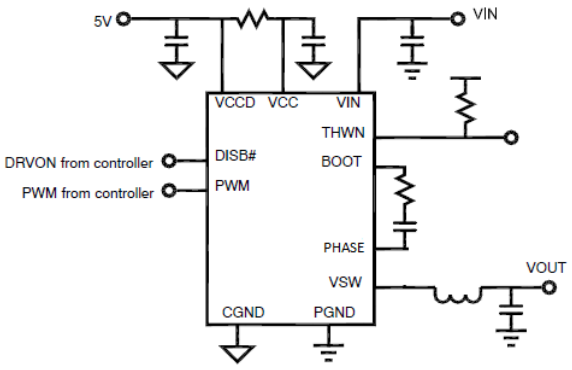
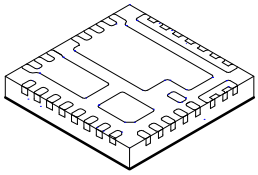
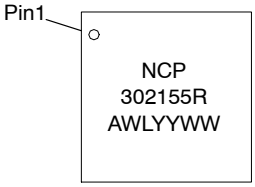


Figure 1. Application Schematic



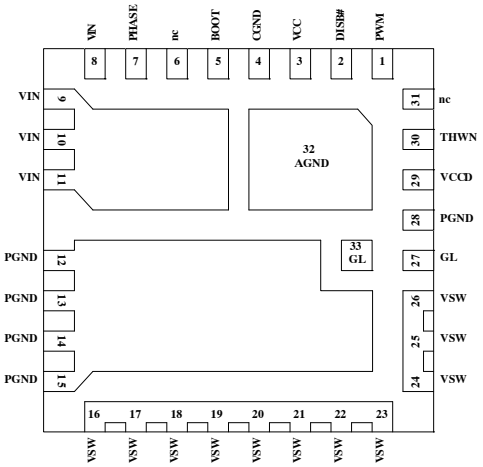
PQFN31 5X5, 0.5P
CASE 483BR

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCP302155RMNTWG	PQFN31 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

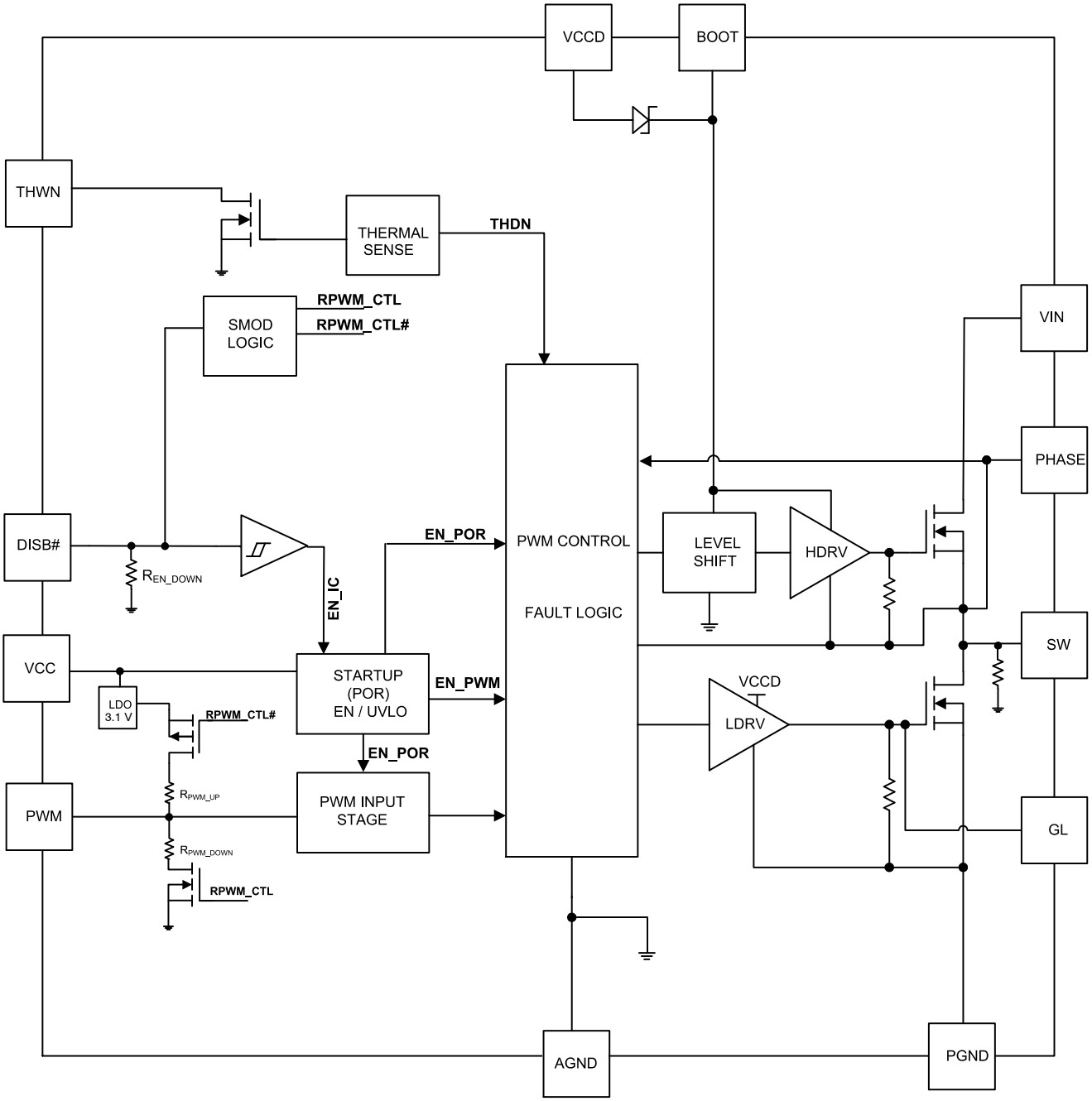


Figure 2. Block Diagram

Table 1. PIN LIST AND DESCRIPTION

Pin No.	Symbol	Description
1	PWM	PWM Control Input
2	DISB#	Output disable pin. High = Enabled with normal PWM operation without ZCD. Connects PWM to internal resistor divider placing a bias voltage on PWM pin. Low = Driver is disabled and in a low power state. There is an internal pull−down resistor to GND on this pin.
3	VCC	Control Power Supply Input
4, 32	CGND, AGND	Signal Ground (pin 4 and pad 32 are internally connected)
5	BOOT	Bootstrap Voltage
6	NC	Open pin (not used)
7	PHASE	Bootstrap Capacitor Return
8−11	VIN	Conversion Supply Power Input
12−15, 28	PGND	Power Ground
16−26	VSW	Switch Node Output
27, 33	GL	Low Side FET Gate Access (pin 27 and pad 33 are internally connected)
29	VCCD	Driver Power Supply Input
30	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver die reaches T_{THWN}, this pin is pulled low.
31	NC	Open pin (not used)

Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information − all signals referenced to PGND unless noted otherwise)

Pin Name / Parameter	Min	Max	Unit
VCC, VCCD	−0.3	6.5	V
VIN	−0.3	30	V
BOOT (DC)	−0.3	30	V
BOOT (< 20 ns)	−0.3	35	V
BOOT to PHASE (DC)	−0.3	6.5	V
BOOT to PHASE (< 20 ns)	−0.3	9.0	V
VSW, PHASE (DC)	−0.3	30	V
VSW, PHASE (< 20 ns)	−5	36	V
All Other Pins	−0.3	V_{VCC} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance (under On Semi SPS Thermal Board)	θ_{JA}	12.4	°C/W
	θ_{J-PCB}	1.8	°C/W
Operating Junction Temperature Range (Note 1)	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	

1. The maximum package power dissipation must be observed.
2. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
3. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCC, VCCD		4.5	5.0	5.5	V
Conversion Voltage	VIN		4.5	−	20	V
Junction Temperature			−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCC SUPPLY CURRENT						
Operating		DISB# = 5 V, PWM = 400 kHz	–	1	2	mA
No switching		DISB# = 5 V, PWM = 0 V	–	–	2	mA
Disabled		DISB# = 0 V	–	0.4	1	μA
UVLO Start Threshold	V_{UVLO}	VCC rising	3.65	–	4.1	V
UVLO Hysteresis			400	500	–	mV
VCCD SUPPLY CURRENT						
Enabled, No switching		DISB# = 5 V, PWM = 0 V, V_{PHASED} = 0 V	–	175	300	μA
Disabled		DISB# = 0 V	–	0.4	1	μA
Operating		DISB# = 5 V, PWM = 400 kHz	–	–	30	mA
DISB# INPUT						
Input Resistance		To Ground	–	467	–	kΩ
Upper Threshold	V_{UPPER}		–	–	2.0	V
Lower Threshold	V_{LOWER}		0.8	–	–	V
Hysteresis		V_{UPPER} − V_{LOWER}	200	–	–	mV
Enable Delay Time		Time from DISB# transitioning HI to when VSW responds to PWM.	–	28	52	μs
Disable Delay Time		Time from DISB# transitioning LOW to when both output FETs are off.	–	21	50	ns
PWM INPUT						
Input Voltage High	V_{PWM_HI}		2.95	–	–	V
Input Mid−state Voltage	V_{PWM_MID}		1.25	–	2.3	V
Input Low Voltage	V_{PWM_LO}		–	–	0.7	V
Input Resistance	R_{PWM_BIAS}	DISB# = 5 V	9.2	14.6	20	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	DISB# = 5 V	1.2	1.7	2.3	V
Non−overlap Delay, Leading Edge	T_{NOL_L}	GL Falling = 1 V to GH−VSW Rising = 1 V	–	13	–	ns
Non−overlap Delay, Trailing Edge	T_{NOL_T}	GH−VSW Falling = 1 V to GL Rising = 1 V	–	12	–	ns
PWM Propagation Delay, Rising	T_{PWM,PD_R}	PWM = High to GL = 90%	–	13	35	ns
PWM Propagation Delay, Falling	T_{PWM,PD_F}	PWM = Low to SW = 90%	–	50	65	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−Low	$T_{PWM\_EXIT\_L}$	PWM = Mid−to−Low to GL = 10%	–	14	25	ns
THERMAL WARNING						
Thermal Warning Temperature	T_{THWN}	Temperature at Driver Die	–	150	–	°C
Thermal Warning Hysteresis	T_{THWN_HYS}		–	15	–	°C
THWM Open Drain Current	I_{THWN}		–	–	5	mA
BOOT STRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA	–	380	–	mV
LOW−SIDE DRIVER						
Output Impedance, Sourcing	R_{SOURCE_GL}	Source Current = 100 mA	–	0.9	–	Ω

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOW−SIDE DRIVER						
Output Impedance, Sinking	R_{SINK_GL}	Sink Current = 100 mA	–	0.4	–	Ω
GL Rise Time	T_{R_GL}	GL = 10% to 90%	–	12	–	ns
GL Fall Time	T_{F_GL}	GL = 90% to 10%	–	6	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. LOGIC TABLE

DISB#	PWM	GH (not a pin)	GL
L	X	L	L
H	H	H	L
H	L	L	H
H	MID	L	L

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN}=12 V, V_{CC}=PV_{CC}=5 V, V_{OUT}=1 V, L_{OUT}=250 nH, T_A=25°C and natural convection cooling, unless otherwise noted)

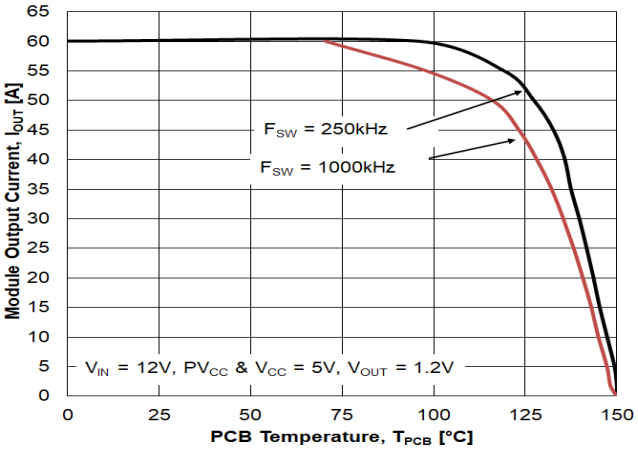


Figure 3. Safe Operating Area with 12 V_{IN}

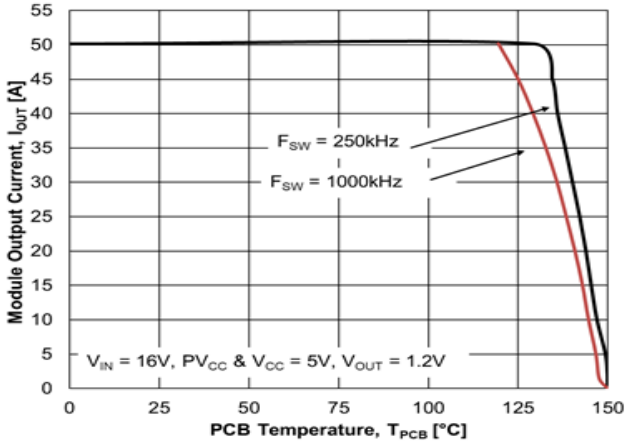


Figure 4. Safe Operating Area with 16 V_{IN}

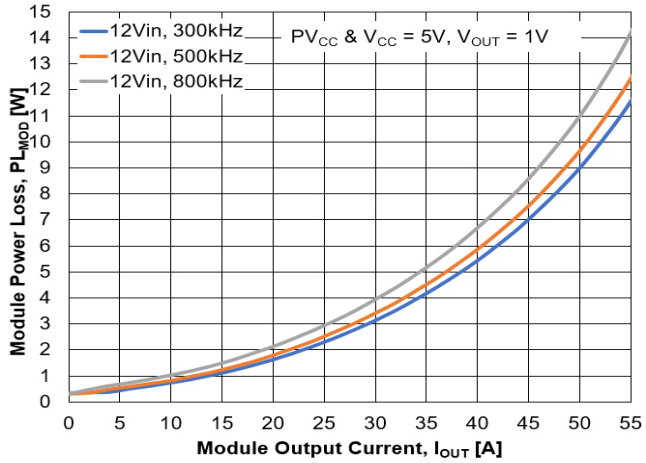


Figure 5. Power Loss vs. Output Current with 12 V_{IN}

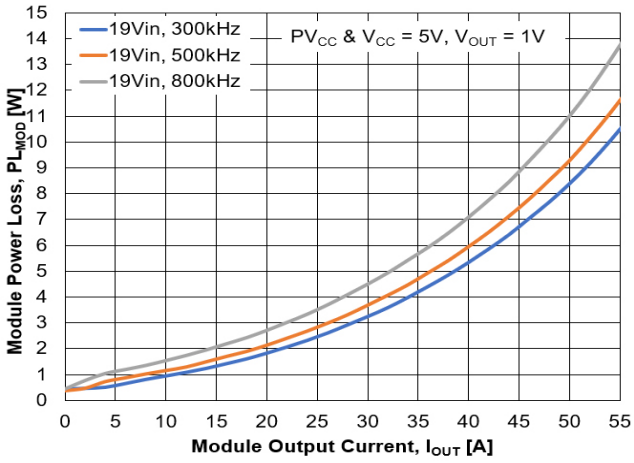


Figure 6. Power Loss vs. Output Current with 19 V_{IN}

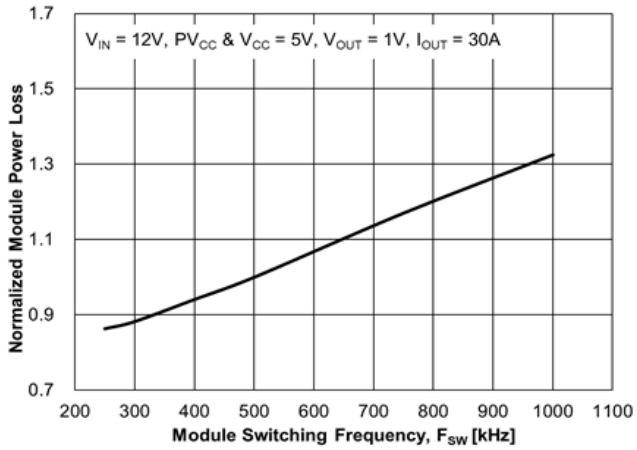


Figure 7. Power Loss vs. Switching Frequency

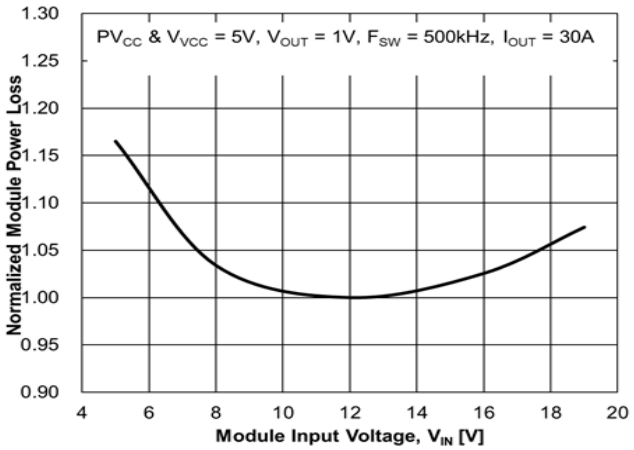


Figure 8. Power Loss vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN}=12 V, V_{CC}=PV_{CC}=5 V, V_{OUT}=1 V, L_{OUT}=250 nH, T_A=25°C and natural convection cooling, unless otherwise noted)

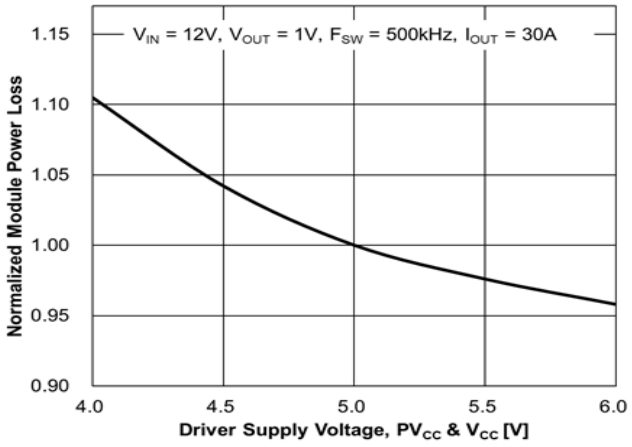


Figure 9. Power Loss vs. Driver Supply Voltage

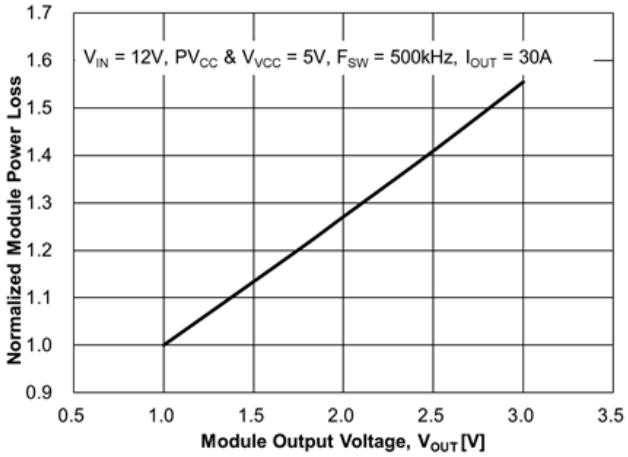


Figure 10. Power Loss vs. Output Voltage

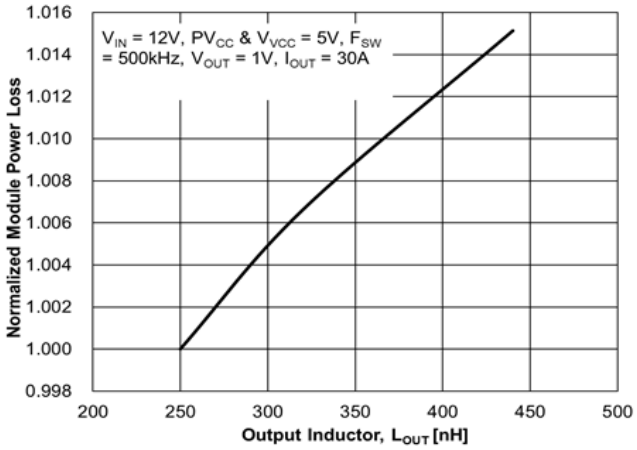


Figure 11. Power Loss vs. Output Inductor

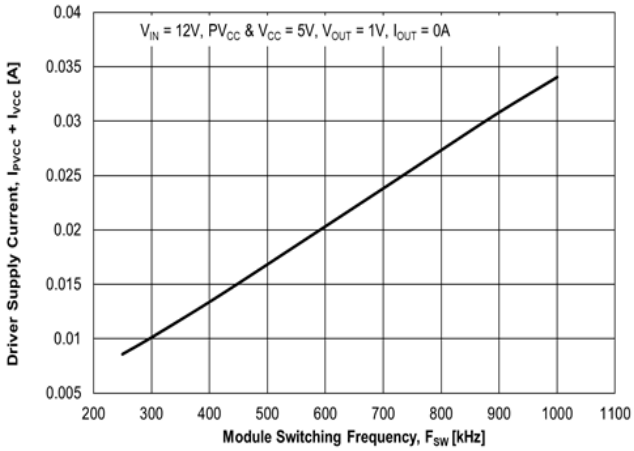


Figure 12. Driver Supply Current vs. Switching Frequency

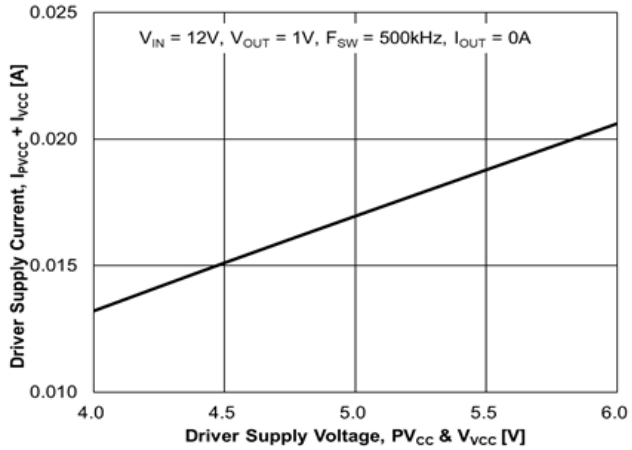


Figure 13. Driver Supply Current vs. Driver Supply Voltage

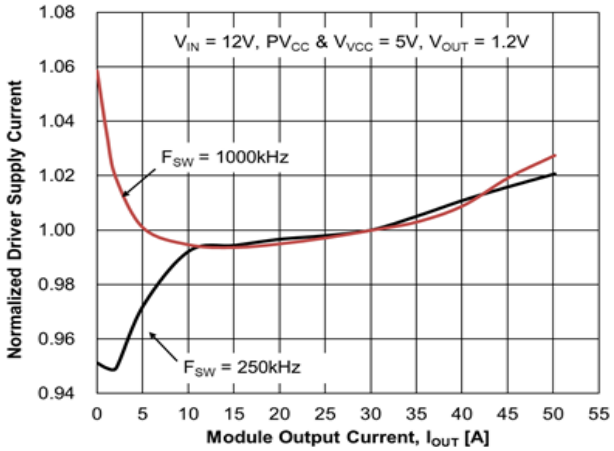


Figure 14. Driver Supply Current vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN}=12 V, V_{CC}=PV_{CC}=5 V, V_{OUT}=1 V, L_{OUT}=250 nH, T_A=25°C and natural convection cooling, unless otherwise noted)

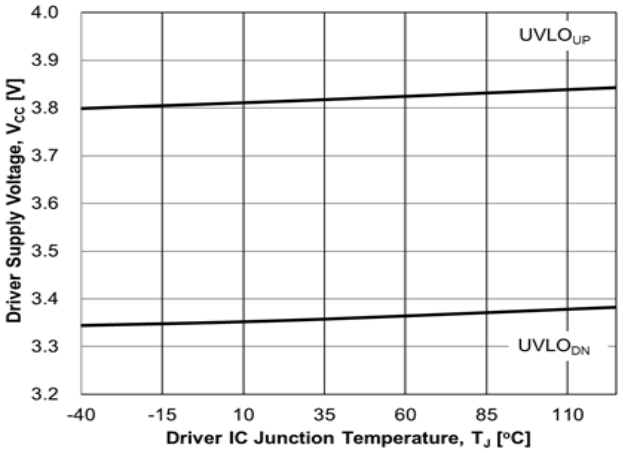


Figure 15. UVLO Threshold vs. Temperature

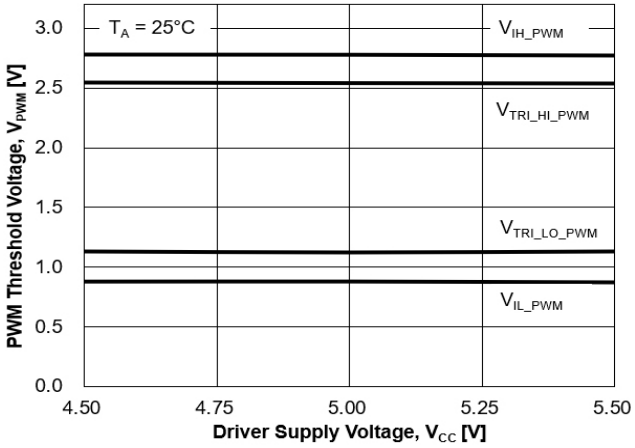


Figure 16. PWM Threshold vs. Driver Supply Voltage

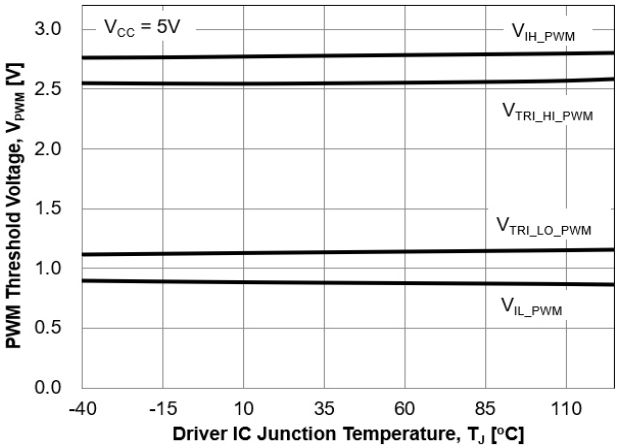


Figure 17. PWM Threshold vs. Temperature

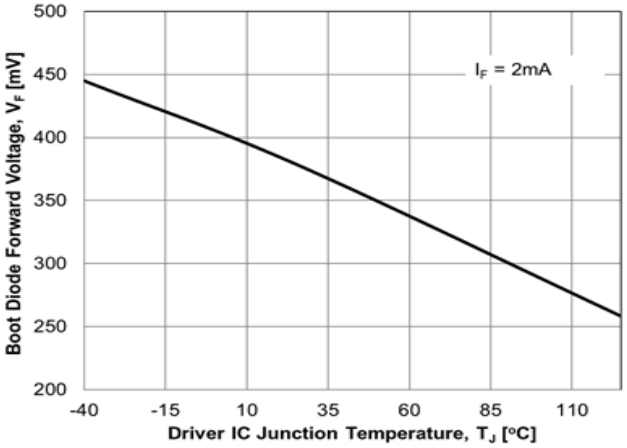


Figure 18. Body Diode Forward Voltage vs. Temperature

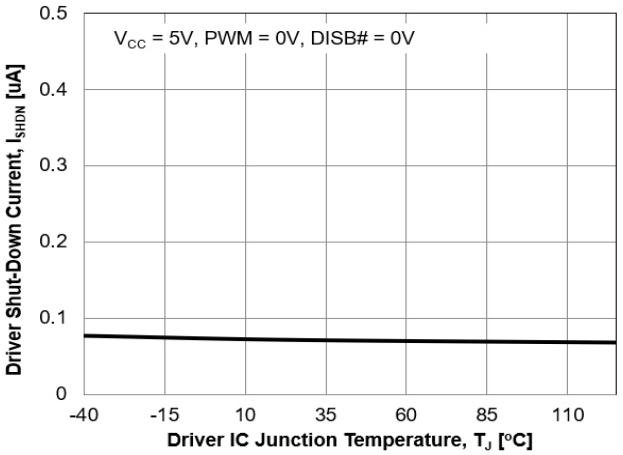


Figure 19. Driver Shutdown vs. Temperature

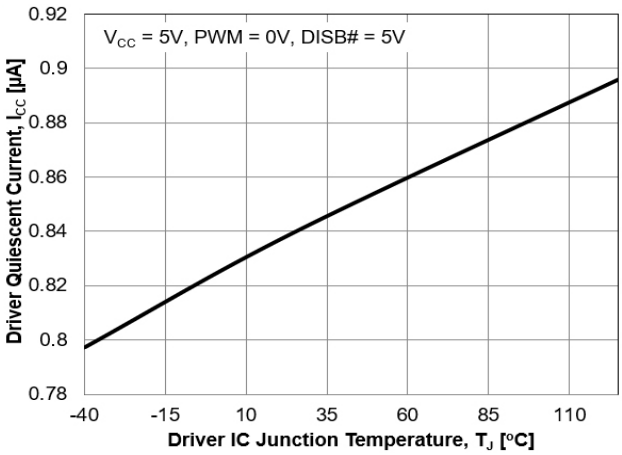


Figure 20. Driver Quiescent Current vs. Temperature

Theory of Operation

The NCP302155R is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP302155R supports PWM Tristate control. A PWM input signal is required to control the drive signals to the high−side and low−side integrated MOSFETs.

Low−Side Driver

The low−side driver drives an internal, ground−referenced low−R_{DS}(on) N−Channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCCD and PGND pins.

High−Side Driver

The high−side driver drives an internal, floating low−R_{DS}(on) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSW and PHASE) pins.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the NCP302155R is starting up, the VSW pin is at ground, allowing the bootstrap capacitor to charge up to VCCD through the bootstrap diode (See Figure 1). When the PWM input is driven high, the high−side driver turns on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the VSW and PHASE pins rises. When the high−side MOSFET is fully turned on, the switch node settles to VIN and the BST pin settles to VIN + VCCD (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the HS Driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used as the bootstrap capacitor. An optional 1 to 4 Ω resistor in series with the bootstrap capacitor decreases the VSW overshoot. The boot resistor is strongly recommended when VIN is higher than 15 V.

Power Supply Decoupling

The NCP302155R sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCD) a low−ESR capacitor should be placed near the power and ground pins. A multi−layer ceramic capacitor (MLCC) between 1 μF and 4.7 μF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1 μF ceramic capacitor should be placed on this pin in close proximity to the NCP302155R. It is good practice to separate the VCC and VCCD decoupling capacitors with a resistor (10 Ω typical) to avoid coupling driver noise to the analog and digital circuits that control the driver function (See Figure 1).

Safety Timer and Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NCP302155R prevents cross−conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non−overlap (NOL) time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). When the PWM input pin is driven high, the gate of the low−side MOSFET (LSGATE) goes low after a propagation delay (tpdlGL). The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate.

The NCP302155R monitors the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer delays (tpdhGH) the turn−on of the high−side MOSFET. When the PWM input pin goes low, the gate of the high−side MOSFET (HSGATE) goes low after the propagation delay (tpdlGH). The time to turn off the high−side MOSFET (tfGH) is dependent on the total gate charge of the high−side MOSFET. A timer is triggered once the high−side MOSFET stops conducting, to delay (tpdhGL) the turn−on of the low−side MOSFET.

PWM Input

The PWM Input pin is a tri−state input used to control the HS MOSFET ON/OFF state. It also determines the state of the LS MOSFET. See Table 6 for logic operation.

When DISB# is high the PWM pin undriven default voltage is set to Mid−State with internal divider resistances.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High−Side FET to prevent power transfer when set to low. The pin has a pull−down resistance to force a disabled state when it is left unconnected. When DISB# is set to high it enables normal PWM operation without ZCD. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP302155R.

Table 7. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table 1)
H	Open	Disabled (GH = GL = 0)

Thermal Warning

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin is pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin goes high.

FOR USE WITH CONTROLLERS WITH 3−STATE PWM CONTROLLERS DETECTION CAPABILITY:

Table 8. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH ZCD

PWM	DISB#	GH (not a pin)	GL
H	H	ON	OFF
M	H	OFF	OFF
L	H	OFF	ON

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NCP302155R to turn off the LS FET. When the controller detects zero current, it needs to set PWM to mid−state, which causes the NCP302155R to pull both GH and GL to their off states without delay.

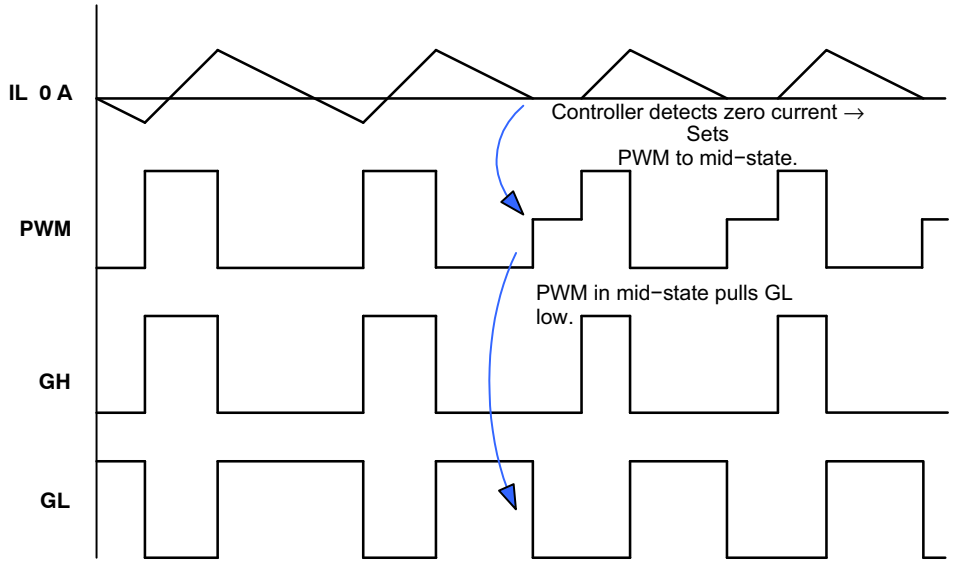


Figure 21. Timing Diagram − 3−state PWM Controller, with ZCD

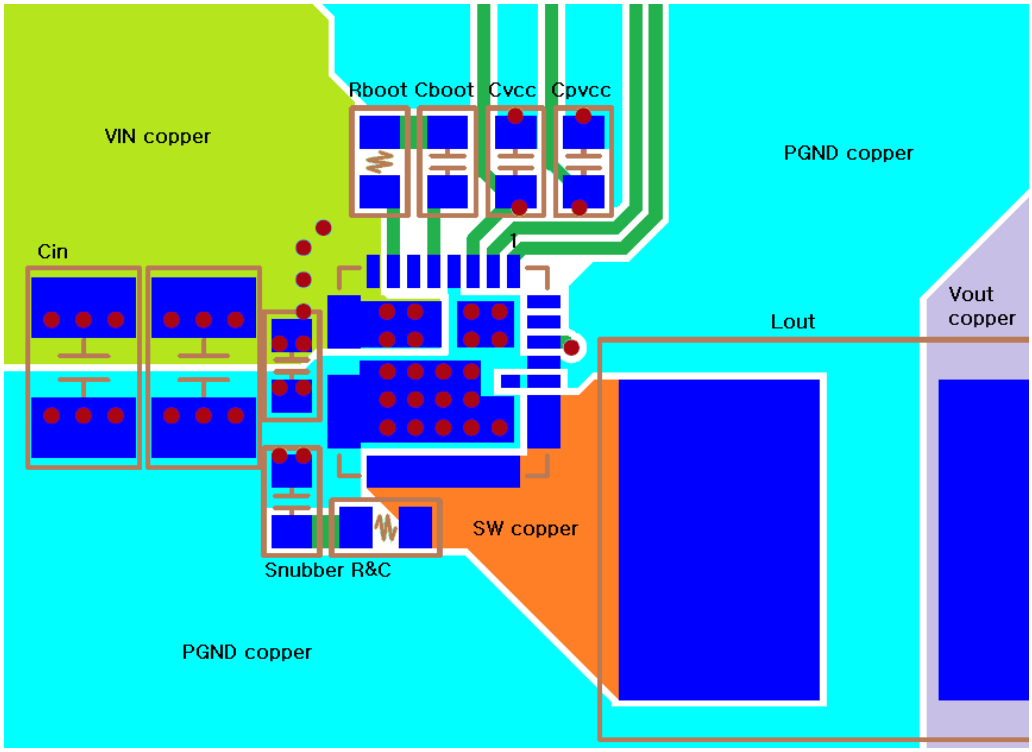


Figure 22. Top Copper Layer

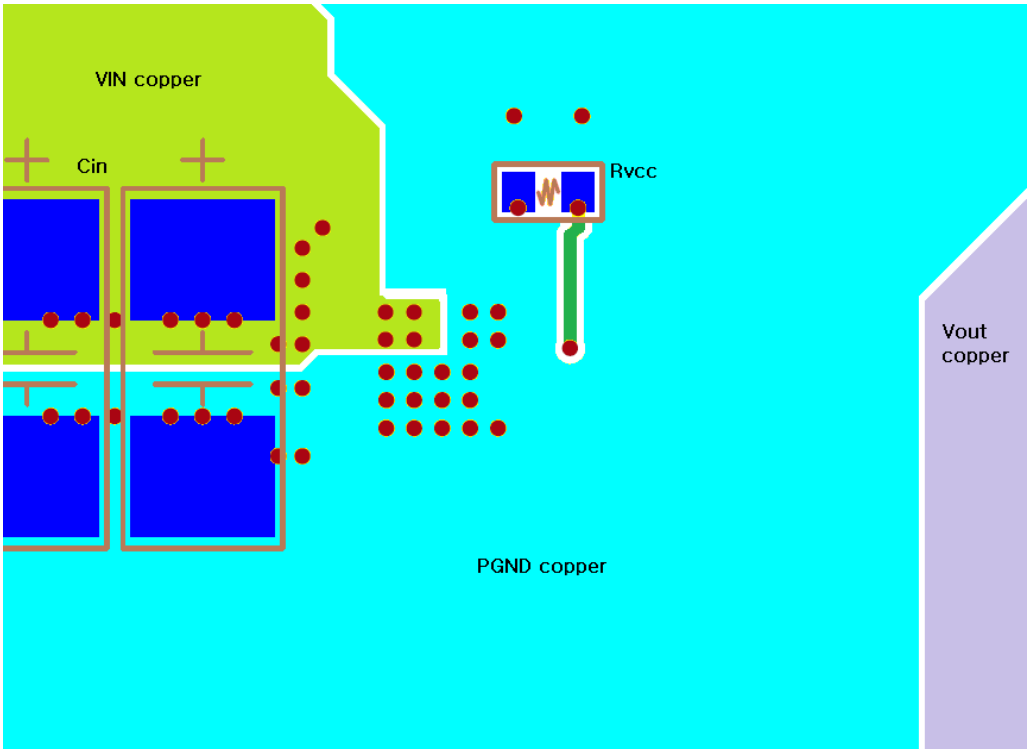
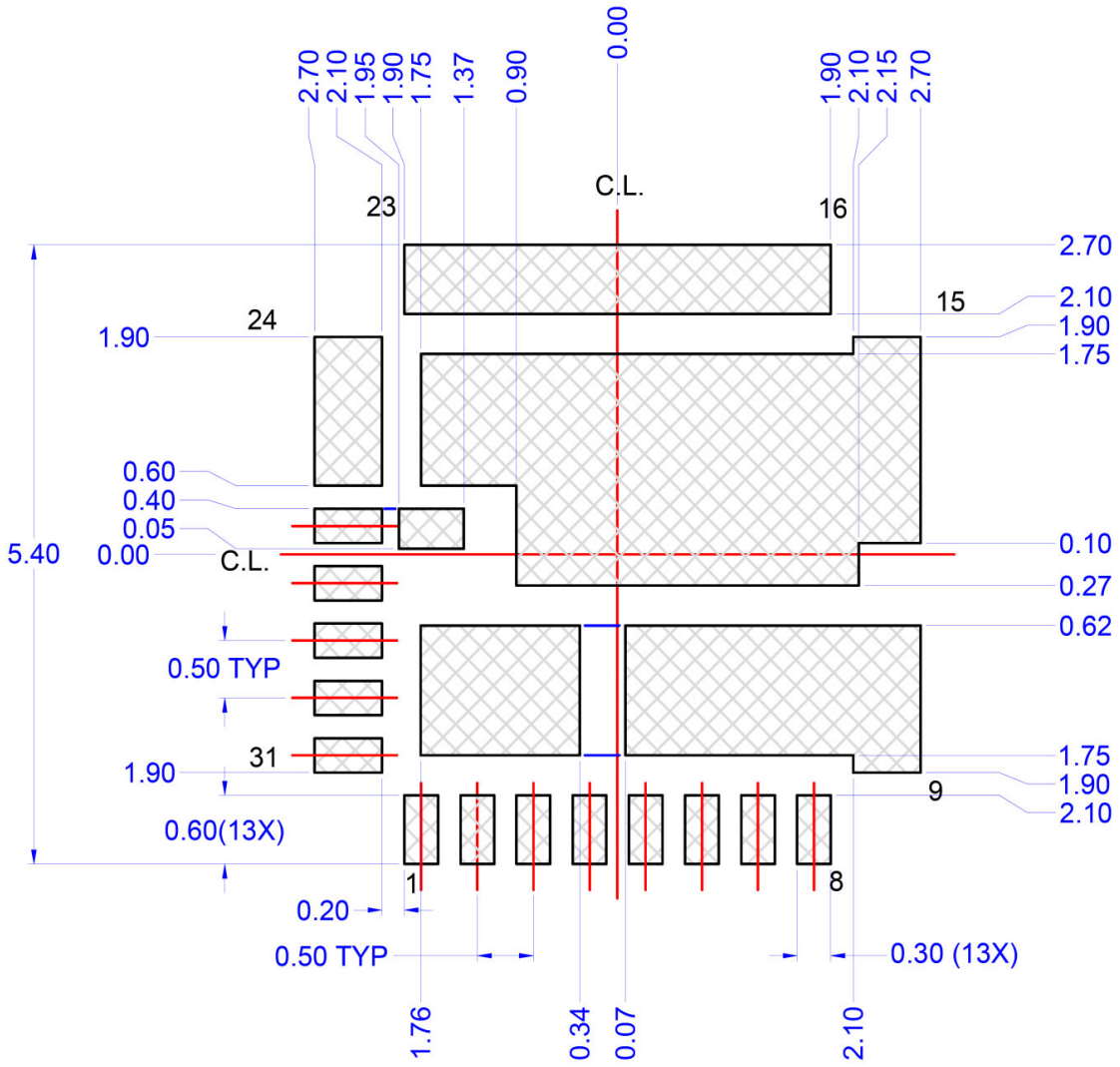


Figure 23. Bottom Copper Layer

RECOMMENDED PCB FOOTPRINT
(Option 1)



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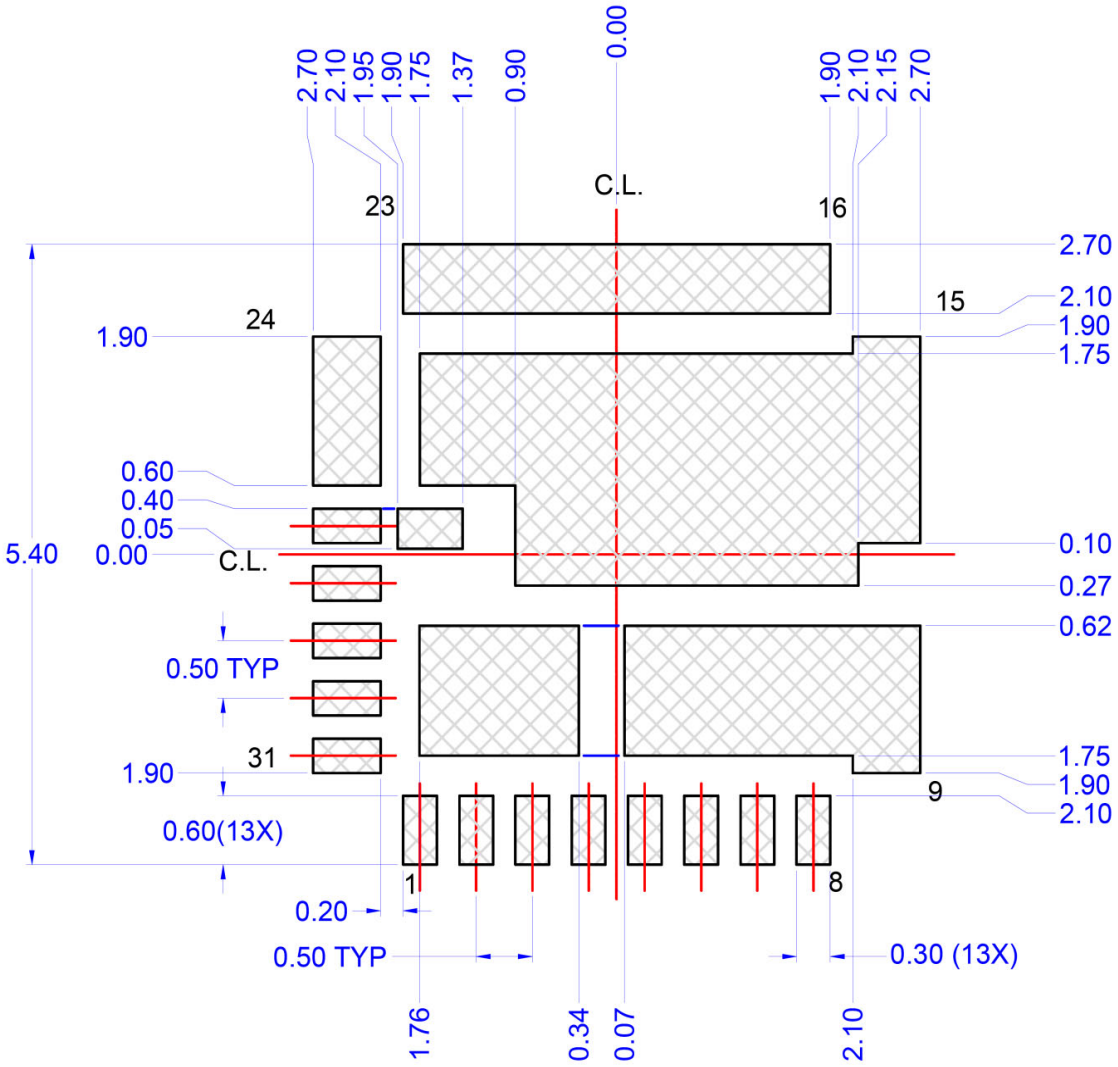
RECOMMENDED PCB FOOTPRINT
(Option 2)



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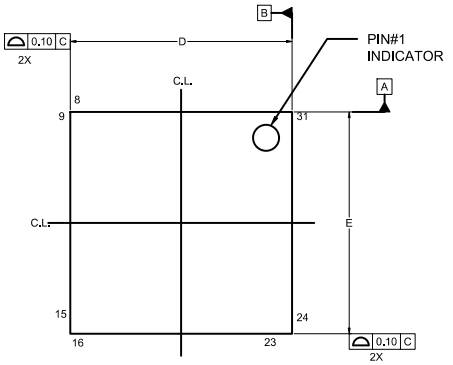
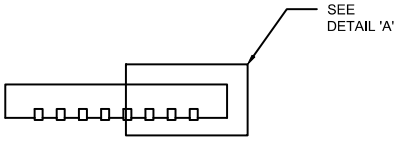
PACKAGE DIMENSIONS

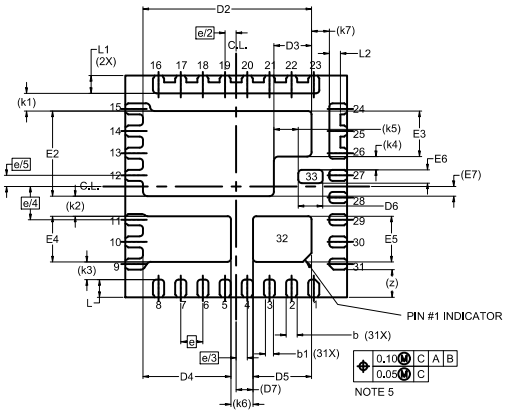
PQFN31 5X5, 0.5P
CASE 483BR
ISSUE C



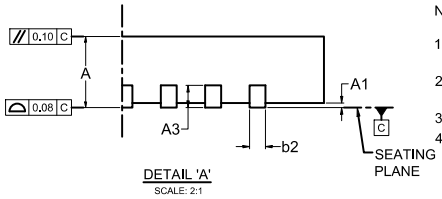
TOP VIEW



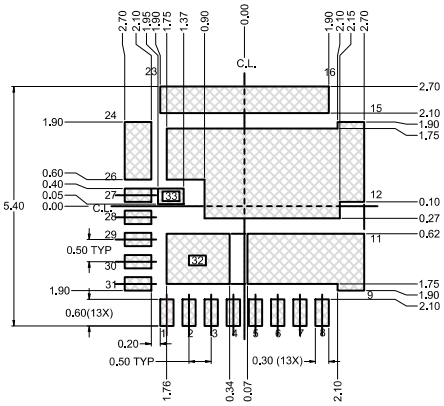
FRONT VIEW



BOTTOM VIEW



DETAIL 'A'
SCALE: 2:1



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*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

1. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATED MAY/2005.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSIONS DO NOT INCLUDE BURRS AND SMEAR OR MOLD FLASH.
   MOLD FLASH OR BURRS AND SMEAR DOES NOT EXCEED 0.10MM.
5. DIMENSION b AND b1 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.13	0.18	0.30
b2	0.13	0.18	0.30
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
D3	0.75	0.85	0.95
D4	1.88	1.98	2.08
D5	1.22	1.32	1.42
D6	0.45	0.55	0.65
D7	0.38 REF		
E	4.90	5.00	5.10
E2	1.82	1.92	2.02
E3	0.93	1.03	1.13
E4	0.93	1.03	1.13
E5	0.93	1.03	1.13
E6	0.20	0.30	0.40
E7	0.22 REF		
e	0.50 BSC		
e/2	0.25 BSC		
e/3	0.25 BSC		
e/4	0.75 BSC		
e/5	0.25 BSC		
k1	0.40 REF		
k2	0.45 REF		
k3	0.40 REF		
k4	0.30 REF		
k5	0.55 REF		
k6	0.50 REF		
k7	0.40 REF		
L	0.30	0.40	0.50
L1	0.30	0.40	0.50
L2	0.15	0.25	0.35
z	0.625 REF		

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