25 A Stackable Synchronous Buck Regulator

NCP3294

The NCP3294 is a highly efficient stackable synchronous buck regulator, capable of operating with an input range from 3 V to 18 V and supporting up to 25 A continuous load currents. Higher output currents can be achieved by 2 parallel NCP3294 devices operating as an interleaved two−phase buck regulator.

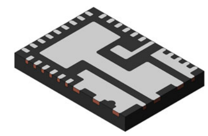
The NCP3294 utilizes fixed−frequency current−mode control to provide accurate voltage regulation and fast transient response. Flexible programming of function and parameters supports multiple applications.

Features

- V_{IN}: 3−18 V with Input Feed−Forward
- V_{OUT}: 0.5−5.5 V with Remote Output Voltage Sense
- 25 A Continuous Output Current – Stackable to 50 A
- Fixed Frequency Current Mode Control
- Integrated 5 V LDO or External Supply
- Enable with Programmable VIN UVLO
- Programmable Boot−Up Voltage
- Programmable Soft−Start
- Pre−Bias Start−Up
- Programmable Current Limit
- Power Good Indicator
- Selectable Protection Mode (Latch−off or Hiccup)
- Under−Voltage and Over−Voltage Protection
- Output Discharge in Shutdown
- 150°C Operating Junction Temperature

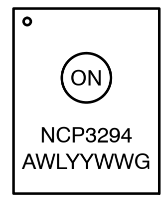
Typical Applications

- Networking – Routers and Switches
- Telecom Digital Baseband
- Telecom Radio Unit
- Server and Desktop Computers, Notebooks, Gaming
- High Density Power Solutions
- DC−DC Modules
- General Purpose POL Regulator



WQFN34 5x7, 0.5P
CASE 510CL

MARKING DIAGRAM



NCP3294	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Designator

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

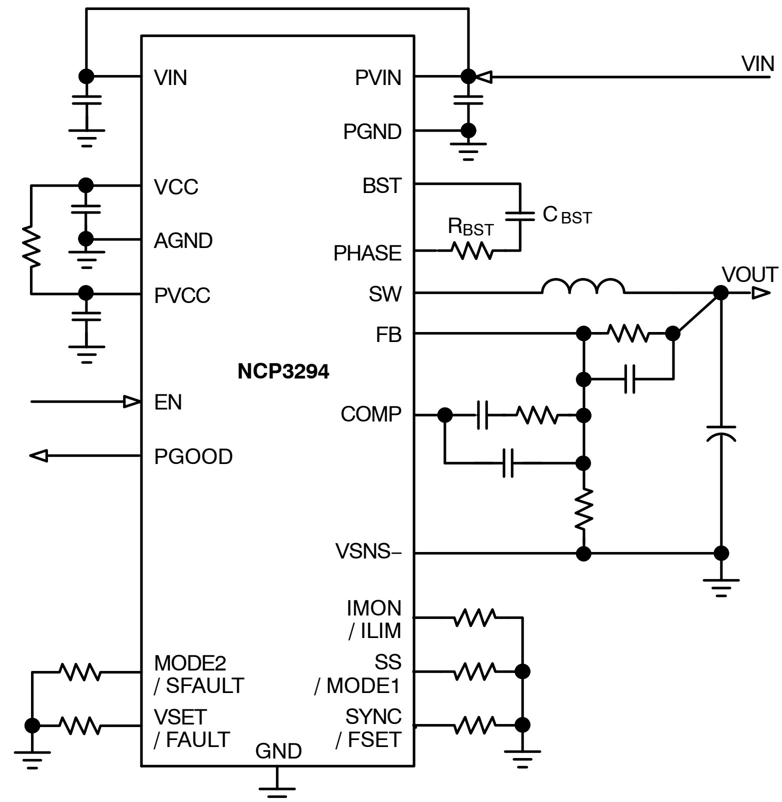


Figure 1. Typical 12 V_{IN}, 25 A Application Circuit for Single Input Supply (LDO Enabled)

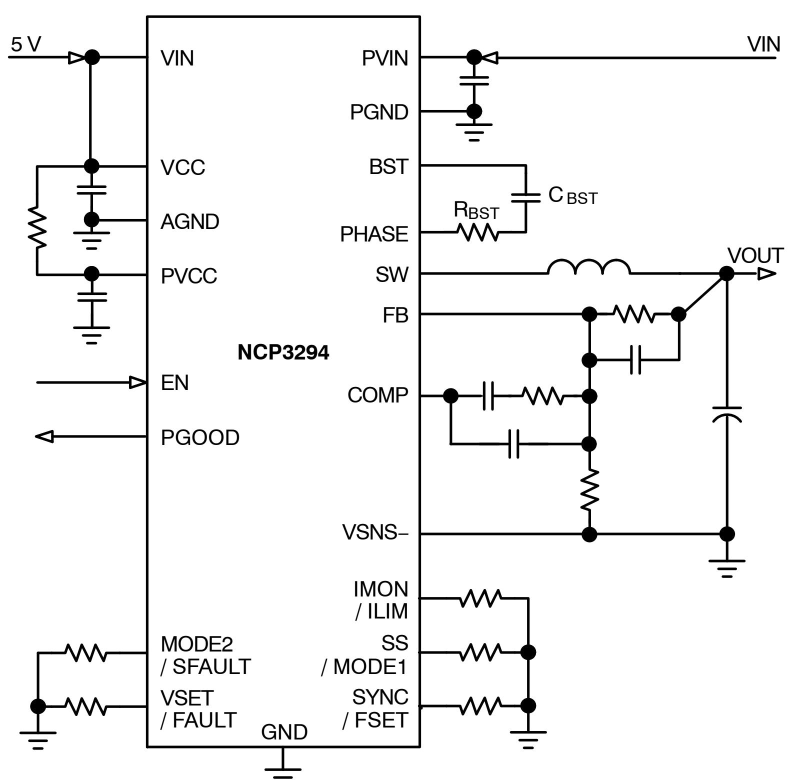


Figure 2. Typical 12 V_{IN}, 25 A Application Circuit with External 5 V VCC Supply (LDO Disabled)

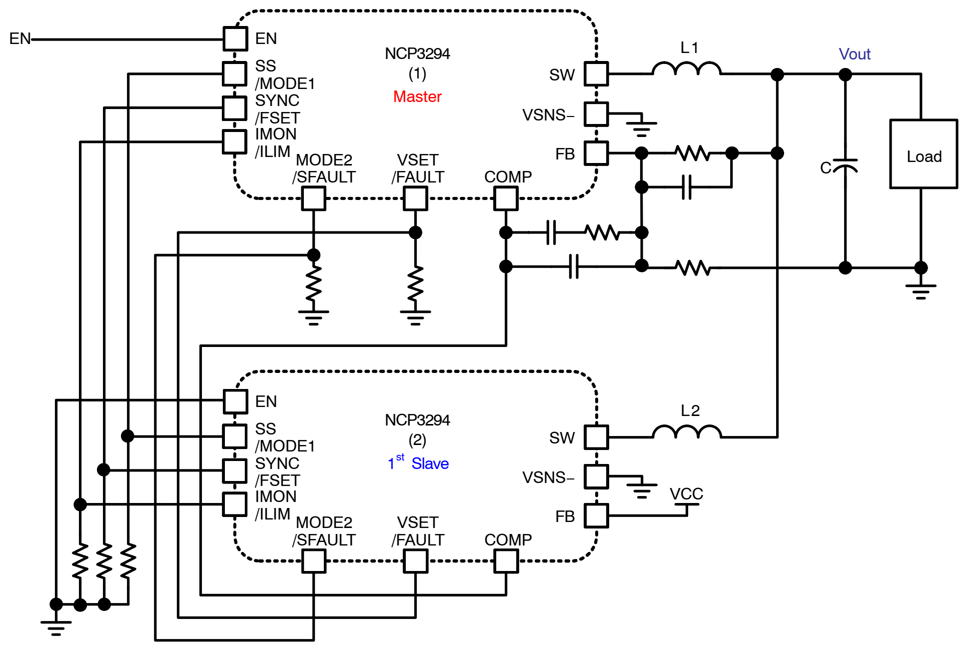


Figure 3. Typical 50 A Application Circuit with 2 Parallel NCP3294

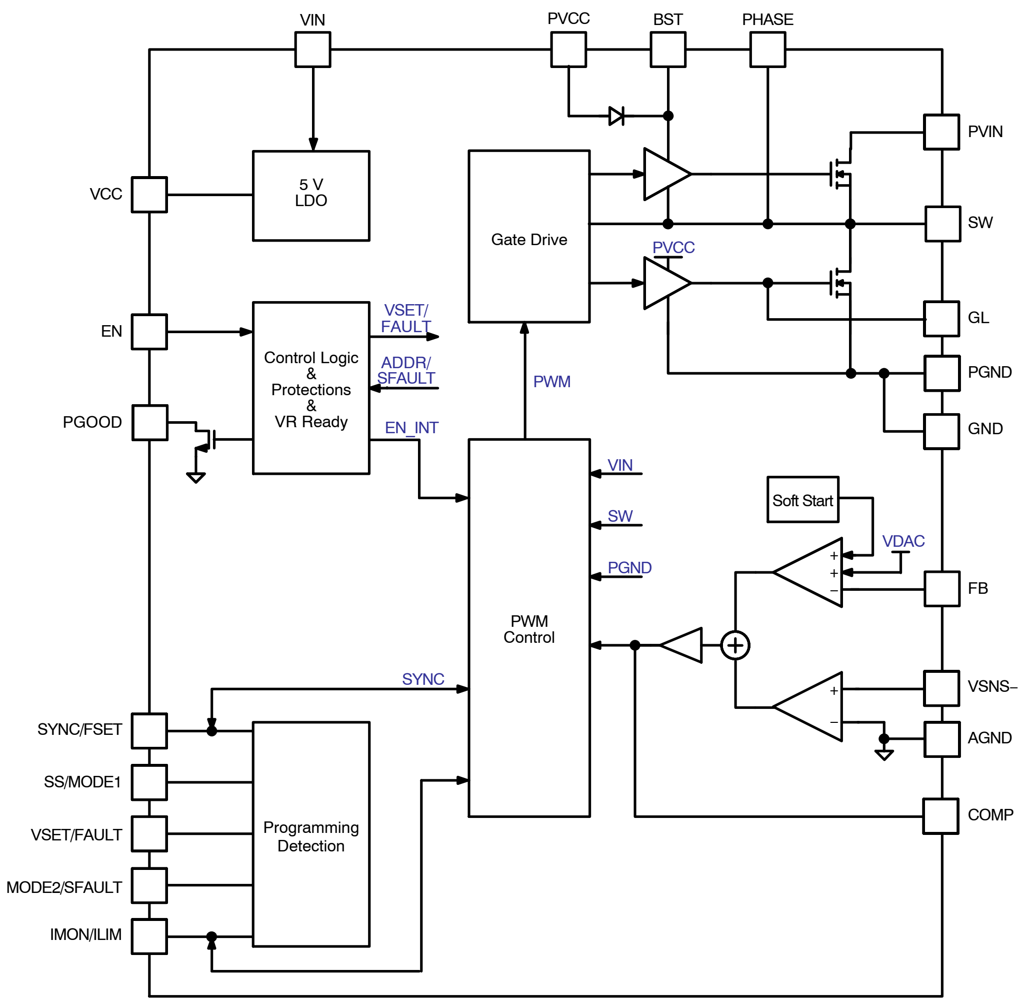


Figure 4. Functional Block Diagram

PIN CONNECTIONS

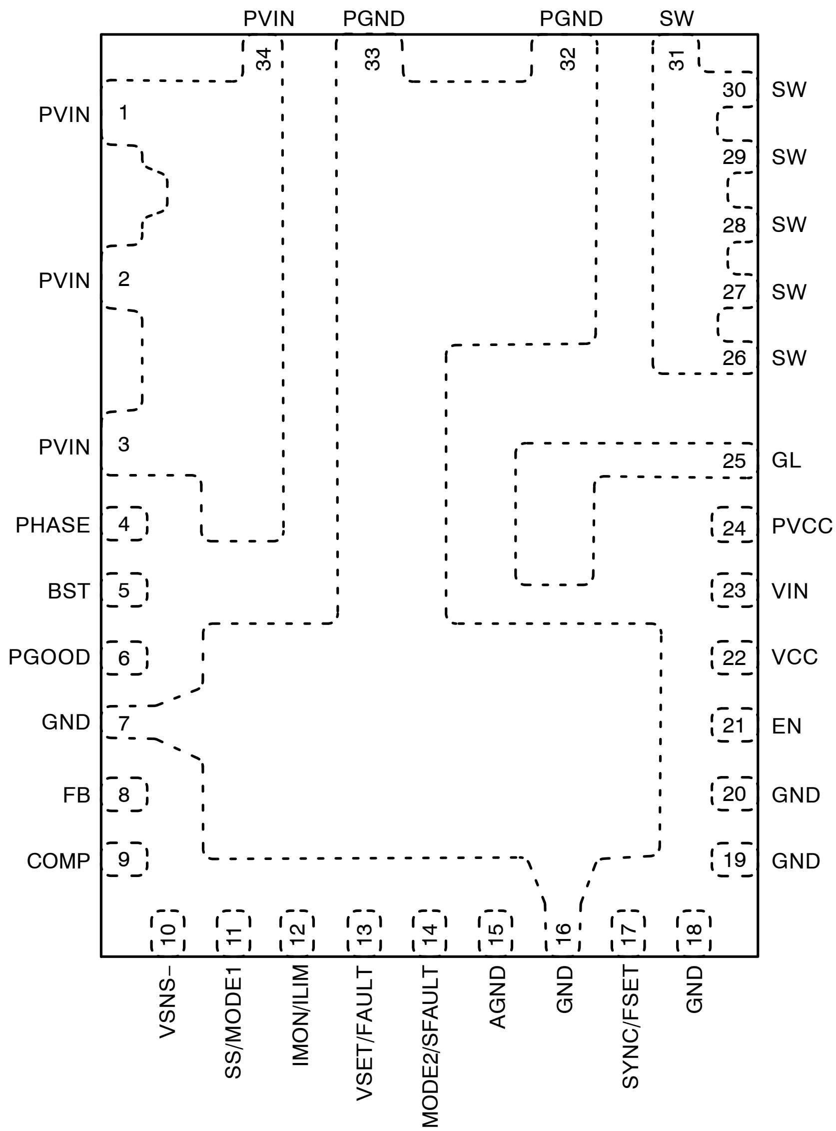


Figure 5. Pin Assignment, Top Transparent View (5 x 7 mm, 0.5 mm Pitch)

PIN DESCRIPTION

Pin	Name	Type	Description
1~3, 34	PVIN	Power	**Power Supply Input**. Power supply input pins of the device, which are connected to the drain of internal high−side power MOSFET. Bypass directly to PGND with ≥22 μF ceramic capacitors using the lowest impedance possible connections to the IC pins.
4	PHASE	Power	**Phase Node**. Provides a return path for integrated high−side gate driver, which is internally connected to the source of the high−side MOSFET.
5	BST	Power	**Bootstrap**. Provides bootstrap voltage for high−side gate driver. A 0.22 μF, 25 V ceramic capacitor is required from this pin to PHASE. A resistor (R_{BST}) in series with capacitor (C_{BST}) is also recommended.
6	PGOOD	Logic Output	**Power GOOD**. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in the regulation window.
7, 16, 18~20, 32~33	GND PGND	Power Ground	**Power Ground**. Power supply ground pins of the device, which are connected to the source of the internal low−side power MOSFET. Must be connected to the system ground using lowest possible impedance path.
8	FB	Analog Input	**Feedback**. Inverting input to error amplifier. Also used to program the slave phase number.
9	COMP	Analog Output	**Compensation**. Output of error amplifier.
10	VSNS−	Analog Input	**Voltage Sense Negative Input**. Connect this pin to remote voltage negative sense point. Also used to program the slave phase number.
11	SS / MODE1	Analog Input	**Soft Start and Mode 1**. A 1% resistor between this pin and ground sets default soft start time, operation mode, and VOUT_SCALE_LOOP.
12	IMON / ILIM	Analog I/O	**IMON and Current Limit**. IMON voltage output/input pin. A 1% resistor between this pin and ground programs the per−phase valley current limit and protection mode.
13	VSET / FAULT	Analog I/O	**Boot−Up Voltage and FAULT**. A resistor from this pin to ground programs the boot−up voltage. Output pin of fault signal from master.
14	MODE2 / SFAULT	Analog I/O	**Mode 2 and SFAULT**. A resistor from this pin to ground programs the device operation mode and phase count. Output pin of fault signal from slave.
15	AGND	Analog Ground	**Analog Ground**. Ground of controller. Must be connected to the system ground using a low impedance single−point connection to GND/PGND.
17	SYNC / FSET	Analog I/O	**Synchronization Clock and Frequency Set**. Synchronization clock output from master. A resistor between this pin and ground programs frequency.
21	EN	Logic Input	**Enable**. High enables the controller. Input supply UVLO can be programmed at this pin with external resistor divider.
22	VCC	Power	**Output of LDO and Supply Voltage Input of Controller**. Output of LDO and bias supply input of controller. A 2.2 μF or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to the pin.
23	VIN	Power	**Power Supply Input of LDO**. Power supply input of LDO. Use 1.0 μF or more ceramic bypass capacitor to power ground. The capacitors should be placed as close as possible to this pin. For applications using an external VCC source, connect this pin to VCC and the 5 V source.
24	PVCC	Power	**Supply Voltage Input of Gate Drivers**. A 4.7 μF, 25 V or larger ceramic capacitor bypasses this input to PGND. This capacitor should be placed as close as possible to this pin.
25	GL	Analog Output	**Gate of Low−Side MOSFET**. Directly connected with the gate of the low−side power MOSFET. No external connection is necessary.
26~31	SW	Power	**Switch Node**. Connect to the external inductor. These pins are interconnection between internal high−side MOSFET and low−side MOSFET.

MAXIMUM RATINGS (All voltages with respect to GND/PGND, unless otherwise specified.)

Rating (Note 1)		Symbol	Min	Max	Unit
Input Voltage		V_{VIN}, V_{PVIN}	−0.3	22	V
Driver Supply Voltage		V_{PVCC}	−0.3	6.5	V
Analog Supply Voltage to AGND		V_{VCC}	−0.3	6.5	V
SW, PHASE Voltage		V_{SW}, V_{PHASE}	−0.5, −5 (<10 ns)	25, 28 (<10 ns)	V
BST Voltage		V_{BST}	−0.3	30	V
BST to SW/PHASE Voltage		V_{BST-SW}	−0.3	6.5	V
GL Voltage		V_{GL}	−0.3, −2 (<50 ns)	V_{PVCC} + 0.3	V
VSNS− to AGND	Normal Dynamic Operation Range	V_{SNS-}	−0.2	0.2	V
	During Slave Configuration at Start−up		−0.2	V_{VCC} + 0.3	
SCL, SDA, PGOOD, ALERT# Pins			−0.3	6.5	V
Other Pins			−0.3	V_{VCC} + 0.3	V
GND/PGND to AGND (Note 2)		V_{AGND}	−0.3	0.3	V
Operating Junction Temperature		T_J	−40	150	°C
Storage Temperature		TSTG	−55	150	°C
Lead Temperature Soldering Reflow (Note 3)		T_{SLD}	260		°C
ESD, Human Body Model Tested per AEC−Q100−002 (EIA/JESD22−A114)		ESD_{HBM}	2	−	kV
ESD, Machine Model, Tested per AEC−Q100−003 (EIA/JESD22−A115)		ESD_{CDM}	200	−	V
Maximum Latch−up Current Rating, Tested per JEDEC Standard: JESD78		I_{LU}	−	150	mA
Moisture Sensitivity Level per IPC/JEDEC Standard: J−STD−020A		MSL	1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. GND and PGND are internally connected. AGND requires PCB connection to GND.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	14.6	°C/W
Thermal Resistance, MOSFET Junction−to−PCB	$R_{\theta JB}$	1.5	°C/W

4. Values are based upon **onsemi** Evaluation Board of 2 oz. copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 5)	V_{VIN}, V_{PVIN}	3	18	V
Output Voltage	V_{OUT}	0.5	5.5	V
Output Current, Continuous	I_{OUT}	0	25	A
SW Voltage, Peak (Note 6)	$V_{SW\ pk}$	−	22	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
5. Operation at <4.5V_{IN} requires external 5 V supply be applied to the VIN and VCC pins per Figure 2.
6. Operation above $V_{SW\ pk}$ may result in reduced IMON accuracy ($V_{IMON\ ACY}$).

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J = 25°C$, min/max: $-40°C \le T_J \le 150°C$, unless otherwise specified.)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT						
Input Shutdown Current	EN = 0, VIN = PVIN, LDO Enabled	I_{PVIN_SD}	–	7	9	mA
	EN = 0, LDO Disabled, VCC = 5.2 V			375	480	μA
Input Quiescent Current	12 V_{IN}, VIN = PVIN, no switching	I_{PVIN_Q}	–	10	17	mA
	18 V_{IN}, VIN = PVIN, no switching		–	10	17	
INTERNAL LINEAR REGULATOR						
LDO Output Voltage	6 V ≤ V_{VIN} ≤ 18 V, EN = 0, I_{VCC} = 0 – 50 mA external	V_{CC}	4.8	5.0	5.3	V
LDO Drop–Out Voltage	V_{VIN} = 5 V, EN = 0, I_{VCC} = 50 mA external	V_{DO}	–	–	250	mV
LDO Current Limit	V_{VIN} = 5.4 V, EN = 0	I_{CC_MAX}	95	–	–	mA
VCC UVLO Threshold	V_{VCC} rising	V_{CC_OK}	–	4.4	4.5	V
	V_{VCC} falling	V_{CC_UV}	4.0	4.2	–	
	Hysteresis	V_{CC_HYS}	–	200	–	mV
ENABLE						
EN On Threshold	EN rising	V_{EN_TH}	1.08	1.20	1.32	V
Hysteresis Resistance		R_{HYS}	–	40	–	kΩ
Hysteresis Current		I_{EN_HYS}	–	5.2	–	μA
EN Input Leakage Current	EN = 1 V	I_{EN_LKG}	–	–	0.5	μA
DEFAULT PROGRAMMING /DETECTION						
Source Current from Pin	SS/MODE1 pin	I_{SS}	9.7	10	10.3	μA
	IMON/ILIM pin	I_{ILIM}	9.7	10	10.3	
	VSET/FAULT pin	I_{VSET}	9.7	10	10.3	
	MODE2/SFAULT pin	I_{ADDR}	9.7	10	10.3	
	SYNC/FSET pin	I_{FSW}	9.7	10	10.3	
PWM MODULATOR						
Minimum On–Time (Note 7)		T_{ON_MIN}	–	35	55	ns
Minimum Off–Time (Note 7)		T_{OFF_MIN}	–	275	300	ns
VOLTAGE ERROR AMPLIFIER						
Open Loop DC Gain (Note 7)		AV_{EA}	–	80	–	dB
Unity Gain Bandwidth (Note 7)		GBW_{EA}	–	12	–	MHz
Slew Rate (Note 7)		SR_{COMP}	–	15	–	V/μs
Output Source/Sink Current	V_{COMP} = 1.2 V	I_{COMP}	10	20	–	mA
COMP Voltage Swing	$I_{COMP(SOURCE)}$ = 2 mA	V_{COMP_H}	3.1	3.4	–	V
	$I_{COMP(SINK)}$ = 2 mA	V_{COMP_L}	–	0.55	0.78	V
FB Bias Current	V_{FB} = 1.00 V	I_{FB}	–150	–	150	nA
CURRENT SENSE AMPLIFIER						
Closed Loop DC Gain		AV_{CA}	–	–10	–	mV/A
–3dB Gain Bandwidth (Note 7)		BW_{CA}	–	7	–	MHz
REFERENCE VOLTAGE						
Reference Voltage (Note 7)	Programmable Range, $R_{SS/MODE1}$ = 10.0 kΩ	V_{FB}	0.50	–	1.25	V
	Resolution, $R_{SS/MODE1}$ = 10.0 kΩ		–	50	–	mV
	Setting/Value		Determined by $R_{VSET/FAULT}$			V

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J$ = 25°C, min/max: −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (continued)

Parameter	Conditions		Symbol	Min	Typ	Max	Unit
REFERENCE VOLTAGE							
Reference Voltage Accuracy	0°C ≤ T_J ≤ 125°C	R_{VSET} = 10.0 kΩ	V_{FB_ACCY}	494	500	506	mV
		R_{VSET} = 82.5 kΩ		994	1000	1006	
		R_{VSET} = open		1243	1250	1257	
	−40°C ≤ T_J ≤ 150°C	R_{VSET} = 10.0 kΩ		492	500	508	
		R_{VSET} = 82.5 kΩ		992	1000	1008	
		R_{VSET} = open		1241	1250	1259	
CYCLE−BY−CYCLE CURRENT LIMIT							
Valley Current Limit (Note 7)	Threshold Range		I_{VLY}	10	−	32	A
	Resolution	10 ≤ A I_{VLY} < 20 A		−	2	−	
		20 ≤ A I_{VLY} < 32 A		−	4	−	
	Setting			Determined by $R_{IMON/ILIM}$			
	Accuracy, I_{VLY} ≥ 12 A, 0°C < T_J < 125°C			−5	−	10	%
	Accuracy, I_{VLY} ≥ 12 A, −40°C < T_J < 150°C			−10	−	15	
Over−Current Protection De−Bounce Time (Note 7)	Consecutive cycles before fault state entry		T_{D_VLY}	−	32 / F_{SW}	−	s
Negative Current Limit Threshold (Note 7)	Low−Side FET		I_{LIM_NEG}	−	25	−	A
SWITCHING FREQUENCY							
Switching Frequency, 1 Phase	Programmable Range		F_{SW}	200	−	2000	kHz
	Resolution	200 ≤ F_{SW} < 400 kHz		−	50	−	
		400 ≤ F_{SW} < 1,000 kHz		−	100	−	
		1,000 ≤ F_{SW} ≤ 2,000 kHz		−	200	−	
	Setting			Determined by $R_{SYNC/FSET}$			
	Accuracy			−10		10	%
SYNCHRONIZATION (SYNC/FSET PIN)							
Logic High Output Voltage, Master	ISYNC = 4 mA (sourcing)		VOH_SYNC	VCC − 0.3	−	−	V
Logic Low Output Voltage, Master	ISYNC = −4 mA (sinking)		VOL_SYNC		−	0.3	V
Logic High Input Voltage, Slave			VIH_SYNC	VCC − 1.0	−	−	V
Logic Low Input Voltage, Slave			VIL_SYNC	−	−	1.0	V
Hysteresis (Slave)				−	1.3	−	V
Input Current Bias, Slave			IIN_SYNC	−0.5	−	0.5	μA
Input Capacitance, Slave (Note 7)				−	5.0	−	pF
MASTER/SLAVE FAULTS (FAULT, SFAULT PINS)							
Tri−State Voltage	$I_{FAULT} = I_{SFAULT}$ = 0		V_{FLT_3ST}	1.7	2.0	2.3	V
Tri−State Source Current	$V_{FAULT} = V_{SFAULT}$ = 1.6 V		I_{3ST_UP}	230	300	370	μA
Tri−State Sink Current	$V_{FAULT} = V_{SFAULT}$ = 2.4 V		I_{3ST_DN}	80	100	120	μA
Output Pull−Up Impedance	$I_{FAULT} = I_{SFAULT}$ = 2 mA (sourcing)		R_{FLT_HI}	25	36	60	Ω
Output Pull−Down Impedance	$I_{FAULT} = I_{SFAULT}$ = −2 mA (sinking)		R_{FLT_LO}	240	260	300	Ω
Input Logic Low Threshold			V_{FLT_IL}	−	−	0.4	V
Input Logic High Threshold			V_{FLT_IH}	VCC − 1.5	−	−	V

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1. Typical values: $T_A = T_J$ = 25°C, min/max: −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
SOFT START						
Soft Start Delay Time	Setting	T_{ON_DLY}	–	1	–	ms
Soft Start Delay Time	Accuracy	T_{ON_DLY}	−0.8	–	1.4	ms
Soft Start Time (0–V_{FB})	Programmable Range	T_{SS}	1	–	20	ms
Soft Start Time (0–V_{FB})	Resolution	T_{SS}		1, 3, 5, 10, 15, or 20		ms
Soft Start Time (0–V_{FB})	Setting	T_{SS}		Determined by $R_{SS/MODE1}$		ms
Soft Start Time (0–V_{FB})	Accuracy: Valid R_{VSET} values ≥ 1.00 V_{OUT}	T_{SS}	−20	–	20	%
Soft Start Time (0–V_{FB})	Accuracy: Valid R_{VSET} values < 1.00 V_{OUT}	T_{SS}	−25	–	25	%
DISABLE / SHUTDOWN						
Output Fall Time OVP, (V_{FB}–0)	Setting	T_{OFF}	–	5	–	ms
Output Fall Time OVP, (V_{FB}–0)	Accuracy (for valid $R_{VSET/FAULT}$ values)	T_{OFF}	−20	–	20	%
Output Discharge Load	SW to GND	R_{SW_D}	–	5	–	kΩ
INPUT VOLTAGE PROTECTION						
Input Over–Voltage Protection	Threshold Range, V_{PVIN} rising	V_{PVIN_OVP}	–	18	–	V
Input Over–Voltage Protection	Accuracy	V_{PVIN_OVP}	−5	–	5	%
Input Over–Voltage Protection	Hysteresis	V_{PVIN_HYS}	–	200	–	mV
Input Over–Voltage Protection	De–Bounce Time	T_{D_VINOV}	–	1	–	μs
Input UVLO Threshold, Rising	Threshold (V_{PVIN})	V_{PVIN_ON}	–	3.0	–	V
Input UVLO Threshold, Rising	Accuracy	V_{PVIN_ON}	−6	–	5	%
Input UVLO Threshold, Falling	Threshold (V_{PVIN})	V_{PVIN_OFF}	–	2.5	–	V
Input UVLO Threshold, Falling	Accuracy	V_{PVIN_OFF}	−6	–	5	%
OUTPUT VOLTAGE PROTECTION						
Output Over–Voltage Fault Threshold (FB to VSNS–, Rising FB)	Threshold	V_{OVP_TH}	–	121	–	% V_{FB}
Output Over–Voltage Fault Threshold (FB to VSNS–, Rising FB)	Accuracy	V_{OVP_TH}	−2	–	2	% V_{FB}
Output Over–Voltage Fault Threshold (FB to VSNS–, Rising FB)	Hysteresis	V_{OVP_TH}	–	25	–	mV
Output Over–Voltage Fault Threshold (FB to VSNS–, Rising FB)	De–Bounce Time	T_{D_OVP}	–	1	–	μs
Output Under–Voltage Fault Threshold (FB to VSNS–, Falling FB)	Threshold	V_{UVP_TH}	–	20	–	% V_{FB}
Output Under–Voltage Fault Threshold (FB to VSNS–, Falling FB)	Accuracy	V_{UVP_TH}	−3.5	–	2	% V_{FB}
Output Under–Voltage Fault Threshold (FB to VSNS–, Falling FB)	Hysteresis	V_{UVP_TH}	–	1	–	% V_{FB}
Output Under–Voltage Fault Threshold (FB to VSNS–, Falling FB)	De–Bounce Time	T_{D_UVP}	–	1	–	μs
Absolute Over–Voltage Threshold during Soft Start (FB to VSNS–)	Threshold, rising	V_{OV_A}	2.02	2.20	2.38	V
Absolute Over–Voltage Threshold during Soft Start (FB to VSNS–)	Hysteresis	V_{OV_HYS}	–	25	–	mV
THERMAL PROTECTION						
Thermal Shutdown Threshold (Note 7)	T_J rising	T_{SD}	160	170	–	°C
Restart Temperature Threshold (Note 7)	T_J falling	T_{RST}	–	155	–	°C
IMON						
Output Offset Voltage	I_{OUT} = 0 A	V_{IMON_0}	–	1.00	–	V
Output Voltage Gain	V_{IMON} = [1.00 + (0.015625 * I_{OUT})] V	V_{IMON_I}	–	15.625	–	mV/A
Output Accuracy (Note 7)	I_{OUT} = 25 A	V_{IMON_ACY}	–	±8	–	%
Output Accuracy (Note 7)	I_{OUT} = 15 A	V_{IMON_ACY}	–	±10	–	%
Output Accuracy (Note 7)	I_{OUT} = 5 A	V_{IMON_ACY}	–	±20	–	%

ELECTRICAL CHARACTERISTICS (VIN = PVIN = 12 V, VOUT = 1.0 V, F_{SW} = 500 kHz, circuit of Figure 1.
Typical values: $T_A = T_J$ = 25°C, min/max: −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
POWER GOOD (AS A PERCENTAGE OF V_{OUT})						
PGOOD Assertion (V_{OUT} Rising)	Threshold	V_{PG_ON}	–	90	–	$\%V_{FB}$
	Accuracy		−2	–	2	
PGOOD Leakage Current	V_{PGOOD} = 5 V	I_{IOH_PG}	–	–	1.0	μA
PGOOD Startup Delay	From end of soft−start (V_{OUT} ramping) until PGOOD asserts	T_{DH_PD}	–	560	720	μs
PGOOD De−Assert (V_{OUT} Falling)	Threshold	V_{PG_OFF}	–	84	–	$\%V_{FB}$
	Accuracy		−2	–	2	
PGOOD Low Voltage	I_{PGOOD} = −4 mA (sinking)	V_{OL_PG}	–	–	0.3	V
PGOOD Shutdown Delay	Falling EN or V_{FB} < POWER_GOOD_OFF until PGOOD de−asserts	T_{DL_PD}	–	2	5	μs
AUTO RESTART						
Automatic−Restart (Hiccup) Delay Time	Setting	T_{HCP}	–	32	–	ms
	Accuracy		−15	–	20	%
POWER STAGE						
High−Side MOSFET On Resistance	$V_{BST} - V_{PHASE}$ = 5 V	R_{DS_HI}	–	2.9	–	mΩ
Low−Side MOSFET On Resistance	V_{PVCC} = 5 V	R_{DS_LO}	–	2.0	–	mΩ
High−Gate Pull−Up Resistance (Note 7)	$V_{BST} - V_{PHASE}$ = 5 V, I_{HG} = 2 mA (source)	R_{HG_UP}	–	1.5	–	Ω
High−Gate Pull−Down Resistance (Note 7)	$V_{BST} - V_{PHASE}$ = 5 V, I_{HG} = 2 mA (sink)	R_{HG_DN}	–	0.6	–	Ω
Leading Edge Dead Time (Note 7)	SW/PHASE rising, $V_{BST} - V_{PHASE}$ = 5 V	T_{SWD_UP}	–	14	–	ns
Low−Gate Pull−Up Resistance (Note 7)	V_{PVCC} = 5 V, I_{LG} = 2 mA (source)	R_{LG_UP}	–	0.8	–	Ω
Low−Gate Pull−Down Resistance (Note 7)	V_{PVCC} = 5 V, I_{LG} = 2mA (sink)	R_{LG_DN}	–	0.4	–	Ω
Trailing Edge Dead Time (Note 7)	SW/PHASE falling, V_{PVCC} = 5 V	T_{SWD_DN}	–	9	–	ns
BST Rectifier On Resistance	V_{PVCC} = 5 V, I_F = 2 mA	R_{BST_ON}	–	50	–	Ω
BST Rectifier Reverse Leakage Current	V_{PVCC} = 5 V, V_{PHASE} = 25 V	R_{BST_LKG}	–	–	3	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance over the indicated operating temperature range by design and/or characterization and may not be production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

(Results use Figure 1 circuit, V_{IN} = 12 V, V_{OUT} = 1.0 V, F_{SW} = 500 kHz, R_{BST} = 4.3 Ω, T_A = 25°C, unless otherwise specified. L and C_{OUT} values (Note 8).)

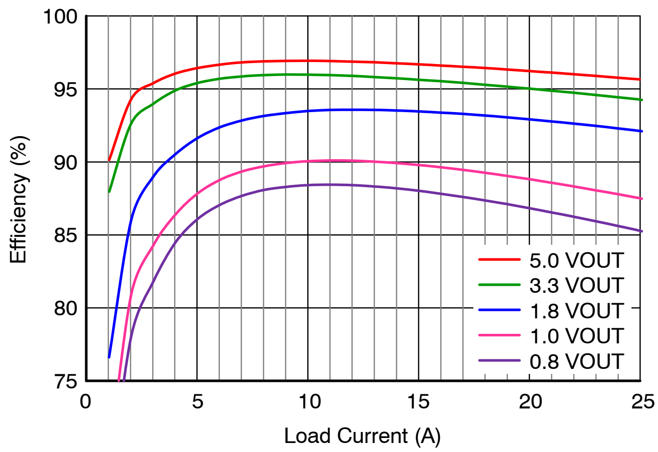


Figure 6. Efficiency vs. Load

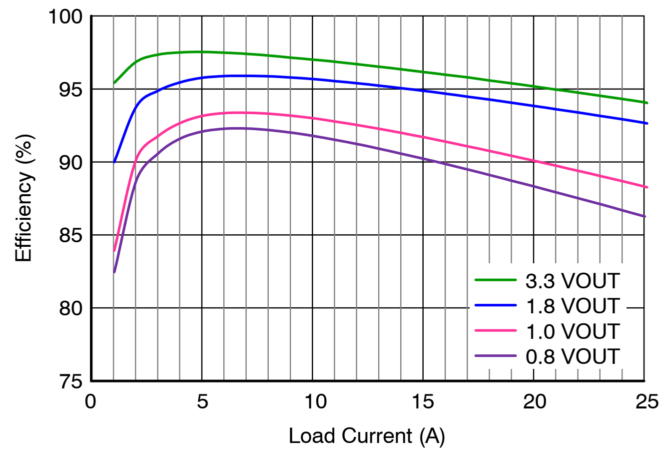


Figure 7. Efficiency vs. Load, 5 V_{IN}, R_{BST} = 0 Ω

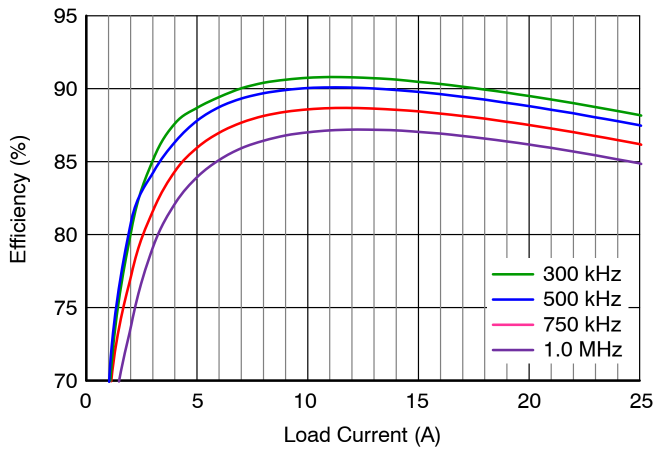


Figure 8. Efficiency vs. Frequency

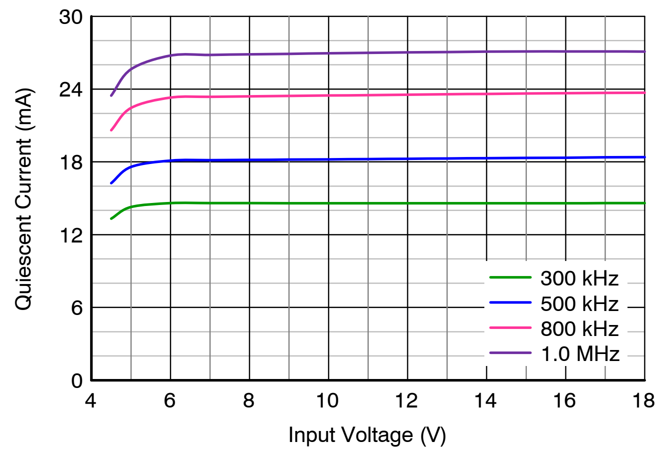


Figure 9. Device Quiescent Current vs. V_{IN} and Frequency

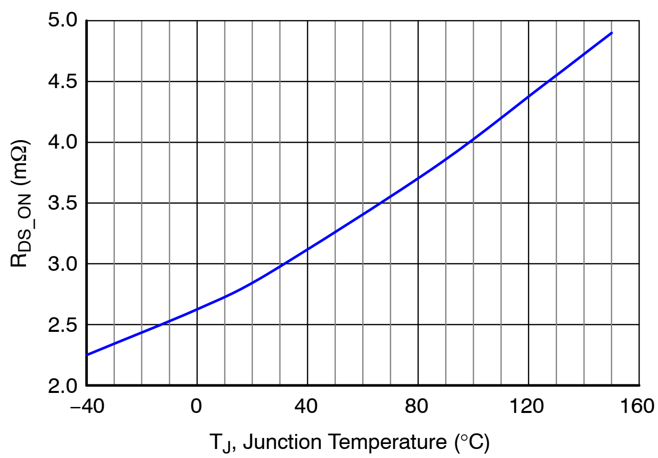


Figure 10. High−Side R_{DS_ON} vs. Temperature, 5 V_{GS}

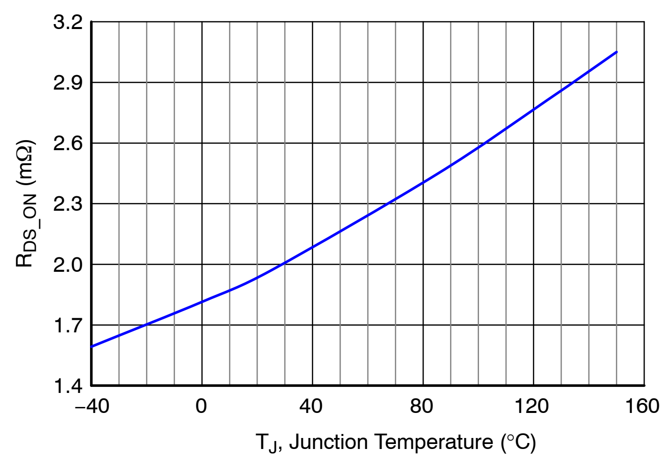


Figure 11. Low−Side R_{DS_ON} vs. Temperature, 5 V_{GS}

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

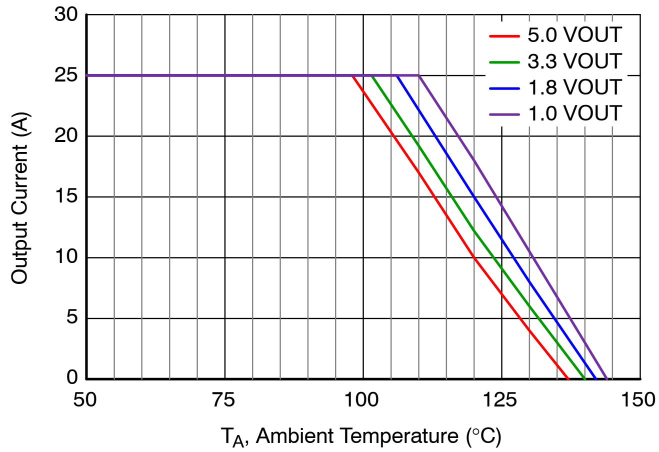


Figure 12. Thermal Safe Operating Area, No Airflow

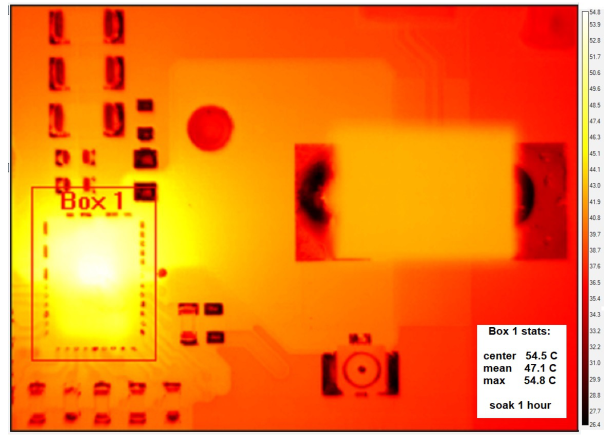


Figure 13. Thermal Image, No Airflow, I_{OUT} = 25 A

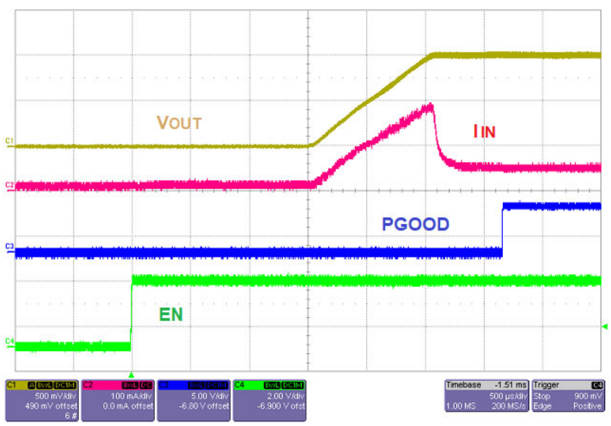


Figure 14. Start−Up, No Load, $R_{SS/MODE1}$ = 10 kΩ

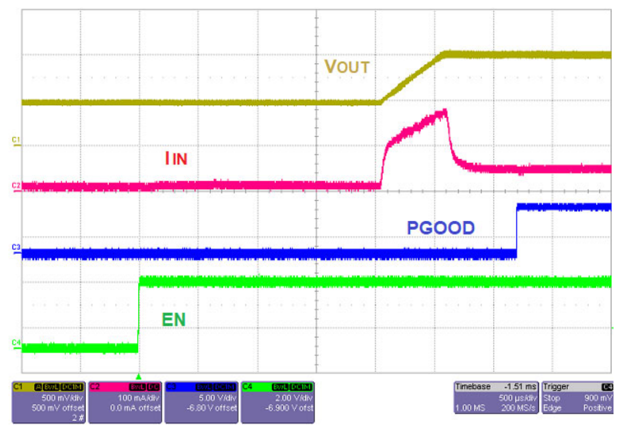


Figure 15. Pre−Bias Start−Up, No Load, $R_{SS/MODE1}$ = 10 kΩ

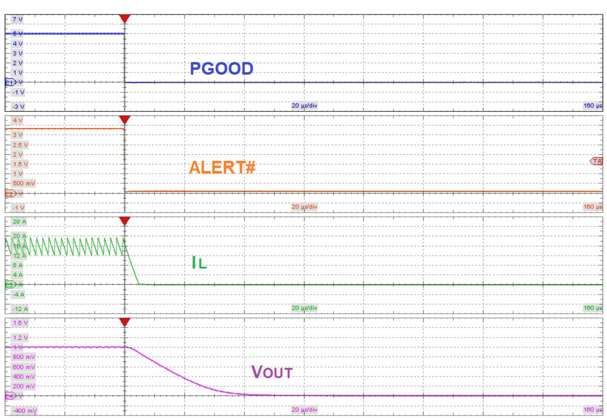


Figure 16. Over−Current Protection Response, Latch−Off, I_{VLY} = 12 A

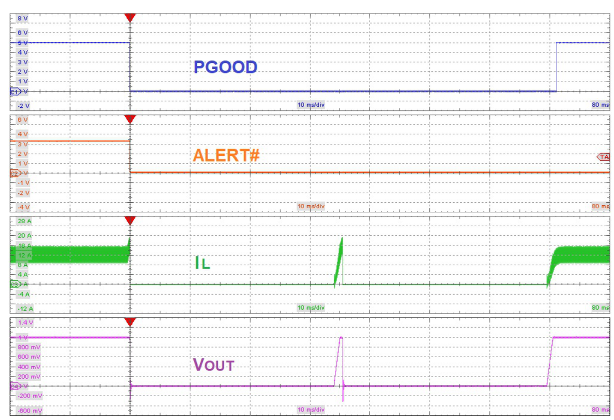


Figure 17. Over−Current Protection Response and Auto−Restart, Hiccup, I_{VLY} = 12 A

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

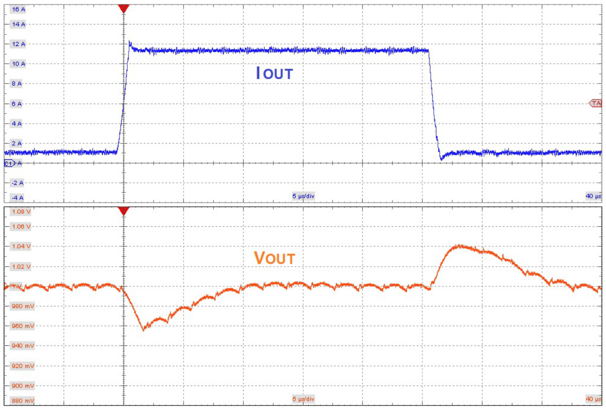


Figure 18. Load Transient Response, 1−11 A, 10 A/μs

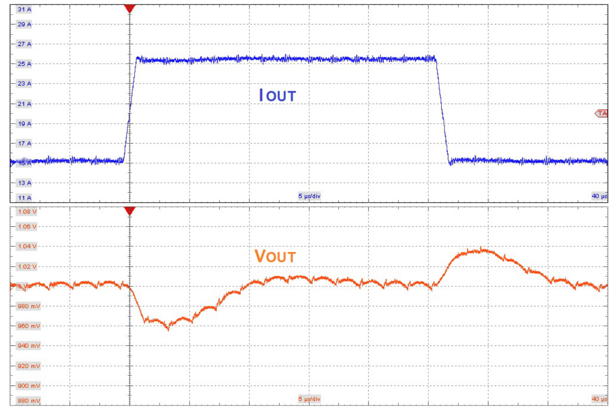


Figure 19. Load Transient Response, 15−25 A, 10 A/μs

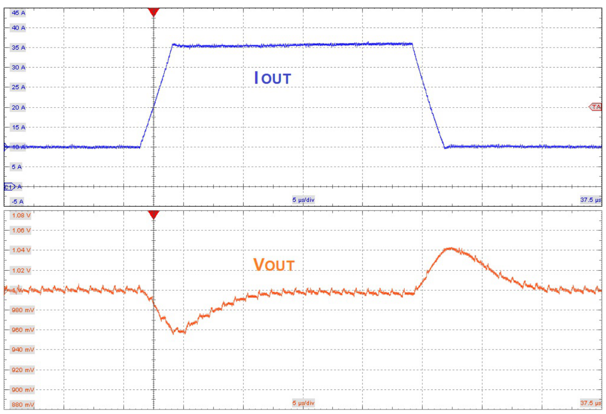


Figure 20. 2−Phase Load Transient Response, 10−40 A, 10 A/μs

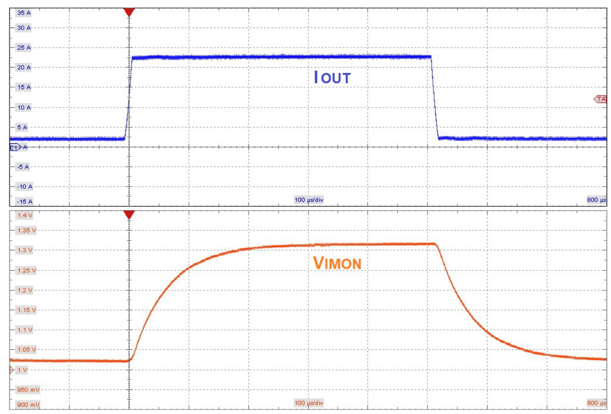


Figure 21. Dynamic IMON Tracking, 2−22 A, 2 A/μs

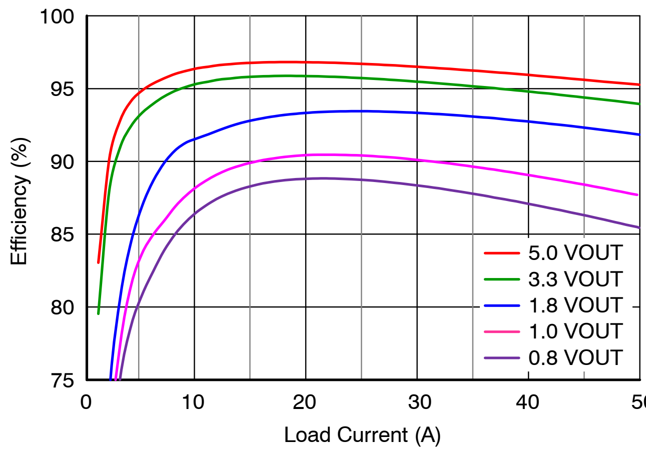


Figure 22. Efficiency vs. Load, 2−Phase

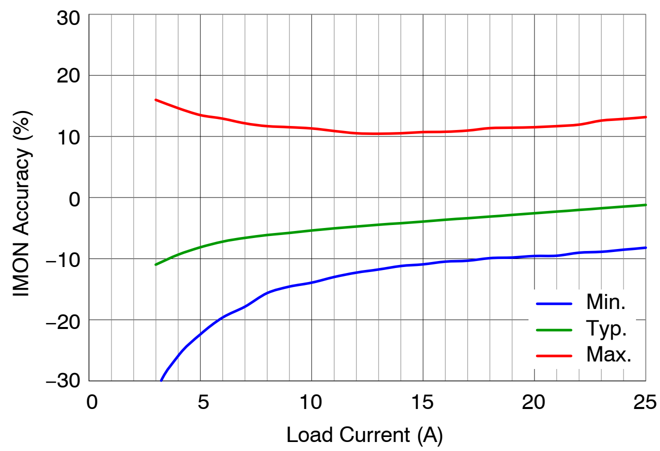


Figure 23. IMON Accuracy vs. Load

NOTE:

8.

V_{OUT}	C_{OUT}	Supplier	L (nH)	Supplier
$V_{OUT} \leq 1.2$ V	470 μF, 2.5 V, 6 mΩ, 1 per phase	Panasonic 2R5PF470M6L	330 nH, 370 μΩ	Wurth 744308033
1.8 V_{OUT}	470 μF, 6.3 V, 10 mΩ, 1 per phase	Panasonic 6TPF470MAH	470 nH, 320 μΩ	Wurth 744301047
$V_{OUT} \geq 3.3$ V	470 μF, 6.3 V, 10 mΩ, 1 per phase	Panasonic 6TPF470MAH	1.0 μH, 1.5 mΩ	Pulse PA4343.102NLT
All	10 || 47 μF, 6.3 V, X5R, 0805	Generic		

APPLICATION INFORMATION

General

The NCP3294, a highly efficient stackable synchronous buck regulator, is capable of operating over an input voltage range of 3.0V to 18V, supporting load currents up to 25 A. Higher output currents can be achieved by paralleling two NCP3294 devices.

The NCP3294 employs a fixed frequency current mode control scheme to provide accurate voltage regulation and fast transient response. Flexible programmability of function and parameters support multiple applications.

V_{OUT} Scale Loop Setting

For V_{OUT} Scale other than 1, a resistor divider of equivalent ratio is required from V_{OUT} to FB to VSNS−.

Using Table 2, select the value (R_{PIN}) for $R_{SS/MODE1}$ corresponding to the desired V_{OUT} Scale level and soft−start time (T_{SS}).

V_{OUT} Setting

Use Table 2 to select the value (R_{PIN}) for $R_{VSET/FAULT}$ corresponding to the desired V_{OUT} level for the previously established V_{OUT} Scale setting.

Setting Frequency

Use Table 2 to select the value (R_{PIN}) for $R_{SYNC/FSET}$ associated with the desired switching frequency per phase and the total number of phases to be implemented.

Current Limit Setting

The per phase current limit setting (I_{VLY}) and protection mode (hiccup/latch−off) are established by $R_{IMON/ILIM}$, according to the R_{PIN} value (R_{PIN}) shown in Table 2.

Master/Slave Configuration

The NCP3294 can be configured as either a master or slave in an interleaved, multi−phase POL system, by its FB and VSNS− pin configuration, as shown in Table 1.

Table 1. MASTER/SLAVE CONFIGURATION

	FB	VSNS−	Application
Master	V_{OUT}	GND	1 or 2 phase
Slave	VCC	GND	2 phase

Operation Modes

Device operating mode is determined by 1% resistor selection (R_{PIN}) at the appropriate device pin, as shown in Table 2.

Table 2. OPERATING MODE SELECTION

	$R_{VSET/FAULT}$ Pin			$R_{SS/MODE1}$ Pin		$R_{IMON/ILIM}$ Pin	$R_{MODE2/SFAULT}$ Pin		$R_{SYNC/FSET}$ Pin	
	Set V_{OUT}			Set V_{OUT} Scale and Soft−Start Time (T_{SS})		Set Current Limit (I_{VLY}), per Phase	Set Phase Count and Protection Mode		Set Frequency (F_{SW}), per Phase	
R_{PIN} (kΩ)	1 Scale (V)	1/2 Scale (V)	1/4 Scale (V)	T_{SS} (ms)	V_{OUT}− Scale (N)	I_{LIM} (A)	Phases (N)	Mode	1φ (kHz)	2φ (kHz)
10.0	0.50	1.30	2.40	1	1	10	1 phase (1φ)	Hiccup	200	200
15.0	0.55	1.35	2.50	3		12			250	250
18.2	0.60	1.40	2.60	5		14		Latch−Off	300	300
22.1	0.65	1.45	2.70	10		16			350	350
27.4	0.70	1.50	2.80	15		18	2 phase (2φ)	Hiccup	400	400
33.2	0.75	1.55	2.90	1	1/2	20			500	450
39.2	0.80	1.60	3.00	3		24		Latch−Off	600	500
47.5	0.85	1.65	3.10	5		28			700	550
56.2	0.90	1.70	3.20	10		32			800	600
68.1	0.95	1.75	3.30	15					900	650
82.5	1.00	1.80	3.40	1	1/4				1,000	700
100	1.05	1.90	3.50	3					1,200	750
121	1.10	2.00	4.00	5					1,400	800
150	1.15	2.10	4.50	10					1,600	850
182	1.20	2.20	5.00	15					1,800	900
221	1.25	2.30	5.50	20					2,000	1,000

The use of substitute resistor values is not recommended.

Soft Start

The NCP3294 soft−start function allows starting into a pre−biased output. When the device is enabled, the soft−start ramp time (T_{SS}) begins after a fixed delay (T_{ON_DLY}).

During the soft−start ramp, switching is prevented when pre−biased V_{FB} exceeds the target reference voltage. At the end of soft−start, if V_{FB} continues to be greater than the programmed reference level, switching will commence to bring the output into compliance.

When the device is disabled, or at falling UVLO, the device shuts down immediately and the power MOSFETs are forced off.

Enable

The NCP3294 is enabled when the rising EN voltage (V_{EN_H}) exceeds V_{EN_TH}, as illustrated below:

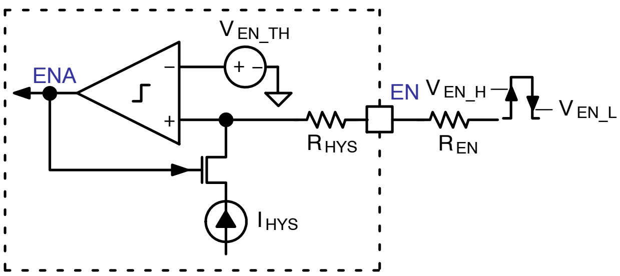


Figure 24. Enable Thresholds and Hysteresis

Optional R_{EN} can be added externally to increase the amount of hysteresis to reach the falling threshold. The falling threshold can be calculated by:

$$V_{EN\_L} = V_{EN\_TH} - I_{HYS} \cdot (R_{HYS} + R_{EN}) \qquad \text{(eq. 1)}$$

The EN pin can also be used to implement an input supply UVLO function using the circuit below:

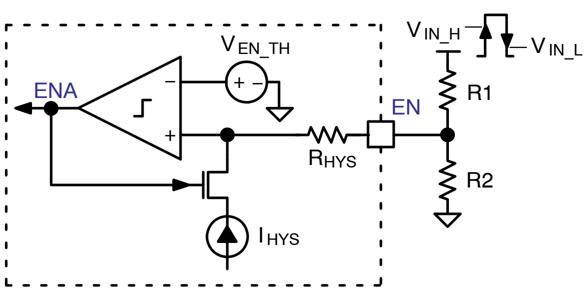


Figure 25. EN Pin Input UVLO Circuit

The associated rising and falling V_{IN} thresholds are:

$$V_{IN\_H} = V_{EN\_TH} \cdot \left(\frac{R1}{R2} + 1\right) \qquad \text{(eq. 2)}$$

$$V_{IN\_L} = K + R1 \cdot \left(\frac{K}{R2} - I_{HYS}\right) \qquad \text{(eq. 3)}$$

where:

$$K = V_{EN\_TH} - I_{HYS} \cdot R_{HYS} \qquad \text{(eq. 4)}$$

To avoid unintended or undefined operation, the EN pin should not be left floating in the application.

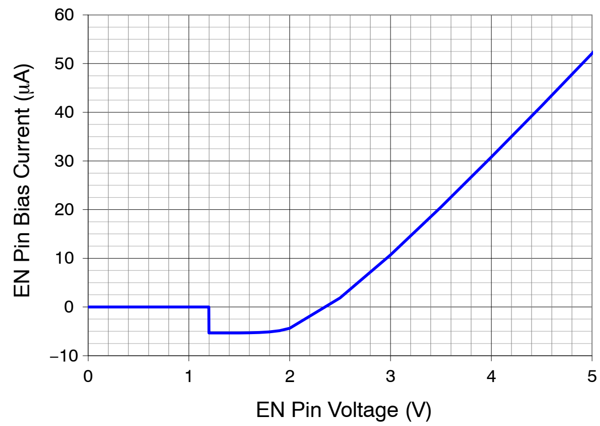


Figure 26. Typical EN Pin Bias Current

Over−Current Protection (OCP)

The NCP3294 employs a cycle−by−cycle valley current limit (I_{VLY}) threshold to protect the regulator. The average current limit (I_{LIM}) value can be calculated from the inductor ripple current and I_{VLY} using:

$$I_{LIM} = I_{VLY} + \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{2 \cdot V_{IN} \cdot L \cdot F_{SW}} \qquad \text{(eq. 5)}$$

OCP detection starts at the beginning of the soft−start ramp (T_{SS}) and extends until shutdown. Inductor current is monitored between SW and PGND. If the OCP event lasts for more than 32 consecutive switching cycles, the device enters fault state (hiccup or latch−off). If V_{OUT} is falling rapidly, the device may trip under−voltage protection before the 32 current limit cycles accumulate.

To restart the device from an OCP latch−off condition, the system needs to toggle VCC or EN off, then back on.

Output Under−Voltage Protection (UVP)

UVP detection is active from when PGOOD asserts at the end of soft−start, until shutdown. The NCP3294 will force PGOOD low and turn off both power MOSFETs once the FB pin voltage falls below V_{UVP_TH} threshold for more than T_{D_UVP}.

To restart the device after a UVP latch−off, the system needs to toggle VCC or EN off, and then back on.

Output Over−Voltage Protection (OVP)

The NCP3294 offers output over−voltage protection to protect the regulator and prevent the possible destruction of the downstream load. OVP is active from the beginning of soft−start until shutdown, latch−off, or during hiccup idle time.

During operation, if the FB pin voltage exceeds the V_{OVP_TH} threshold for longer than T_{D_OVP}, OVP is triggered and PGOOD is forced low.

Once OVP triggers, FCCM operation is maintained while the DAC voltage ramps down at the T_{OFF} rate, preventing large negative voltage spikes from occurring at the output. Once the DAC reaches 0, the high−side FET is turned off, while the low−side FET remains on.

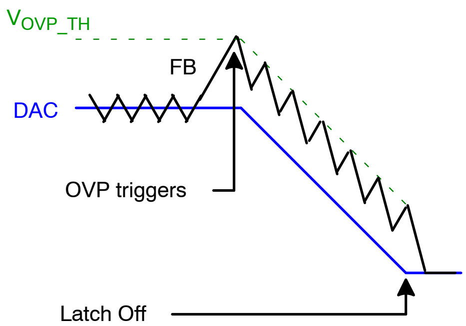


Figure 27. OVP Behavior during Normal Operation

During soft−start, the OVP threshold is set to a fixed absolute value of V_{OV_A}.

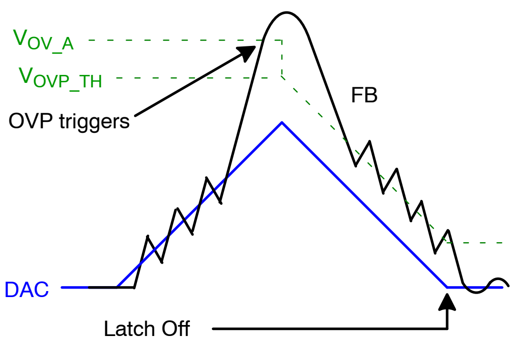


Figure 28. OVP Behavior during Start−Up

To restart the device after an OVP latch−off, the system needs to toggle VCC or EN off, and then back on.

Thermal Shutdown (T_{SD})

Severe overheating is prevented by forcing the entire device into shutdown when die temperature (T_J) reaches the thermal shutdown threshold (T_{SD}). T_{SD} detection activates when VCC and EN are valid. Once the thermal protection is triggered, the entire chip remains off until T_J cools to T_{RST}, where an automatic recovery and soft−start sequence commence.

Input Over−Voltage Protection (V_{IN} OVP)

When the input voltage, measured at the PVIN pin, exceeds the V_{PVIN_OVP} threshold for the de−bounce time of T_{D_VINOV}, the device enters fault state and switching ceases.

Once the input voltage falls below $V_{PVIN\_OVP} - V_{PVIN\_HYS}$, an automatic restart occurs after a fixed 32 ms delay.

Hiccup / Latch−Off Mode

The selected resistor value at the MODE2/SFAULT pin ($R_{MODE2/SFAULT}$) determines whether hiccup or latch−off protection mode is applied under V_{OUT} OVP, V_{OUT} UVP, or OCP conditions.

To restart a device in latch−off mode, EN or VCC need to be toggled. In hiccup mode, the idle time counter (T_{HCP}) begins counting when the device shuts down for OCP, UVP, or the end of OVP DAC ramp down. A normal start−up sequence automatically occurs once T_{HCP} expires.

PGOOD Pin

The PGOOD signal is held low during soft−start and in shutdown state.

PGOOD is high while V_{FB} remains within the adjustable regulation envelope determined by the V_{OVP_TH} and V_{UVP_TH} thresholds.

During thermal shutdown (T_{SD}), PGOOD is low until the device sufficiently cools. PGOOD will be low during all fault conditions.

2−Phase Frequency and Synchronization

Per phase switching frequency (F_{SW}) and phase count (N) are programmed by $R_{SYNC/FSET}$ and $R_{MODE2/SFAULT}$ resistor value selections per Table 2. The master and slave phases are determined by FB and VSNS− pin connections shown in Table 1.

In a 2−phase system, the master outputs a SYNC signal to the the slaves' SYNC pins to establish a common switching frequency and evenly space the phases, as shown in the subsequent figure:

The falling edge of the SYNC pulse resets the ramp, beginning the interleaved PWM on−cycles after a narrow propagation delay. The vertical dotted lines signify the modulated PWM edge (duty cycle).

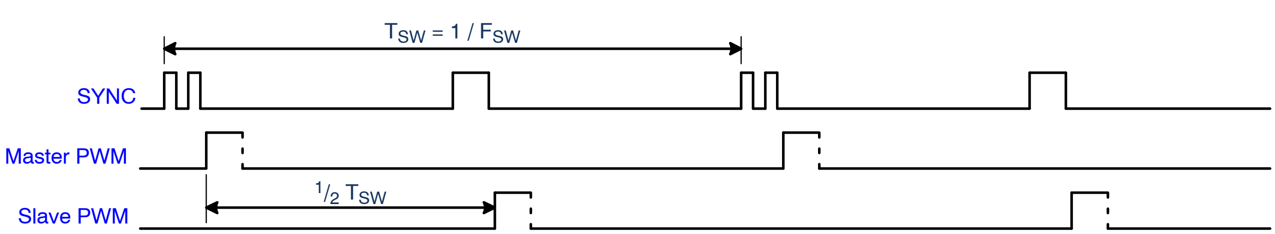


Figure 29. 2−Phase Synchronization Timing

FAULT and SFAULT Operation

In a 2−phase application, communication between the master and slaves is accomplished via signaling over the VSET/FAULT and MODE2/SFAULT pins.

The following table is a summary of NCP3294 actions in response to the main fault conditions:

Table 3. MASTER / SLAVE ACTIONS BY PROTECTION TYPE

Master / Standalone		Protection Type	Slave	
Detection	**Action**		**Detection**	**Action**
V_{CC}	Auto recoverable Both power MOSFETS off FAULT pulled high SFAULT pulled low	UVLO	V_{CC}	Auto recoverable Both power MOSFETS off FAULT pulled high SFAULT pulled low
T_J	Auto recoverable Both power MOSFETS off FAULT pulled low	TSD	T_J	Auto recoverable Both power MOSFETS off SFAULT pulled low
I_{DRAIN}	Cycle−by−cycle current limit Both power MOSFETS off FAULT pulled low	OCP	I_{DRAIN}	Cycle−by−cycle current limit Both power MOSFETS off SFAULT pulled low
V_{FB}	Both power MOSFETS off FAULT pulled low	UVP	Master V_{FB}	Both power MOSFETS off after Master pulls FAULT low
V_{FB}	Ramp down DAC with FCCM High−side FET turns off Low−side FET remains on SFAULT pulled high	OVP	Master V_{FB}	Once Master pulls SFAULT high: High−side FET turns off Low−side FET remains on

FAULT and SFAULT Signaling

The VSET/FAULT and MODE2/SFAULT pins utilize bi−directional signaling for master/slave communication and fault management. The figures below illustrate how the circuit works:

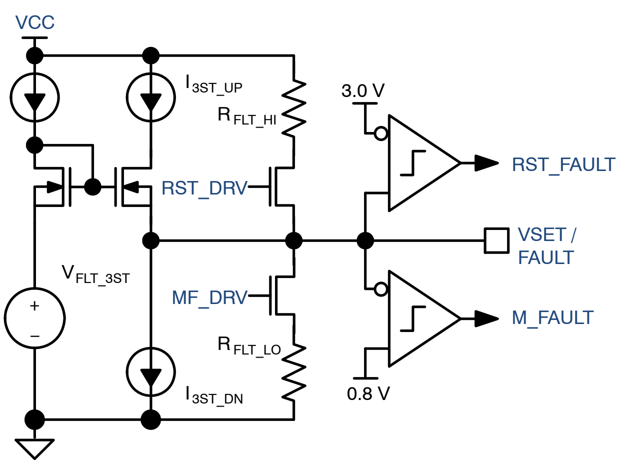


Figure 30. VSET/FAULT Pin Circuit

The internal signal MF_DRV asserts high when a master fault occurs. RST_DRV gets asserted to reset the system. M_FAULT and RST_FAULT are the associated fault signals (active high).

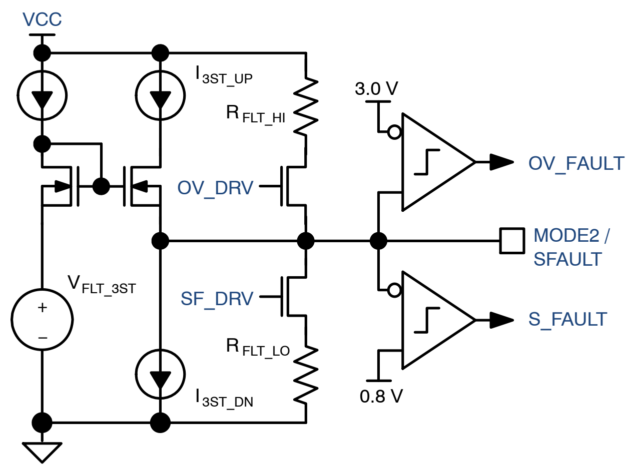


Figure 31. MODE2/SFAULT Pin Circuit

The internal signal OV_DRV asserts when the master detects an output OVP event, which forces the MODE2/SFAULT pin high. SF_DRV asserts when a slave needs to signal a fault condition. OV_FAULT and S_FAULT are the associated fault signals (active high).

When EN = 0, the master forces both VSET/FAULT and MODE2/SFAULT low. Switching is prohibited.

The VSET/FAULT and MODE2/SFAULT signals remain tri−stated (2 V) during normal operation.

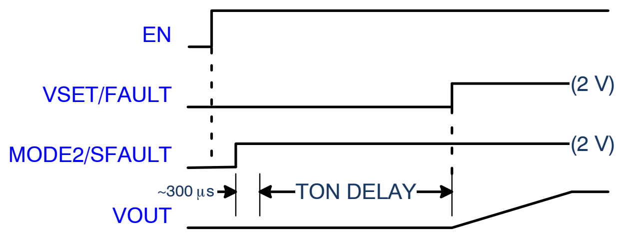


Figure 32. Master/Slave Start−Up Signals

At start−up, once EN is asserted, the master imposes a small housekeeping delay before tri−stating the MODE2/SFAULT pin, which awakens the slave. While VSET/FAULT is low, all the master and slave FETs remain off.

After the TON_DELAY period expires, the master tri−states the VSET/FAULT pin and the soft−start cycle begins.

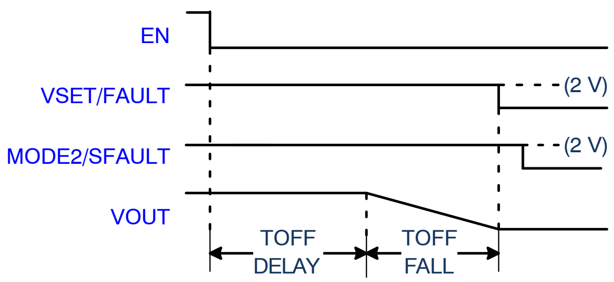


Figure 33. Master/Slave Power−Off Signals

When EN goes low, the VSET/FAULT and MODE2/SFAULT pins remain tri−stated until the TOFF_DELAY and TOFF_FALL intervals expire. Then, the master lowers the VSET/FAULT pin which halts switching and all FETs are turned off. Later, the master lowers the MODE2/SFAULT pin, returning the slaves to their stand−by (inactive) state.

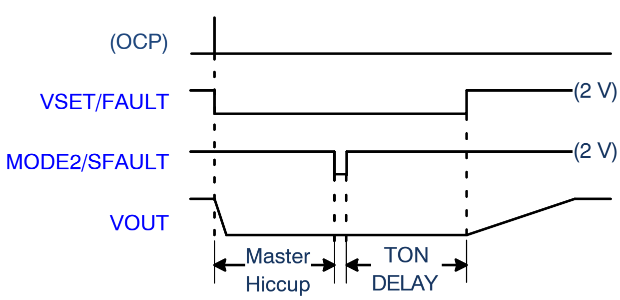


Figure 34. Master/Slave Signals, Master OCP or UVP

When the master encounters an over−current fault situation, indicated here by internal logic signal (OCP) high, it lowers the VSET/FAULT pin to instruct the slave to stop switching.

Once the master completes its hiccup cycle, it momentarily cycles MODE2/SFAULT low to reset and re−activate the slave.

Upon expiration of the TON_DELAY interval, the master tri−states the VSET/FAULT pin and a soft−start cycle commences.

The same signaling/sequence is used in response to output under−voltage (UVP) faults.

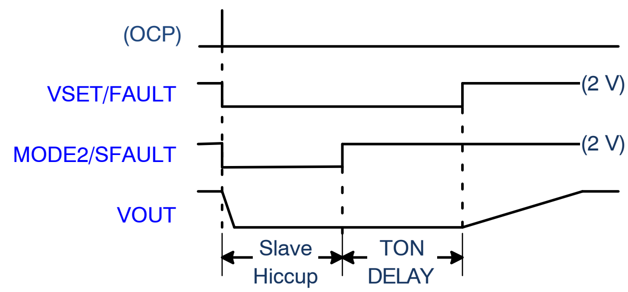


Figure 35. Master/Slave Signals, Slave OCP or OT Fault

When any slave encounters an over−current event, it signals the master by lowering the MODE2/SFAULT pin. As a result, the master forces VSET/FAULT low to halt all switching.

Once the slave hiccup period expires, it releases the MODE2/SFAULT signal. The master holds VSET/FAULT low to prevent all switching until TON_DELAY elapses. When the master releases the VSET/FAULT signal to the tri−state level, the soft−start cycle commences.

The same signaling/sequence is used in response to an over−temperature (OT) fault.

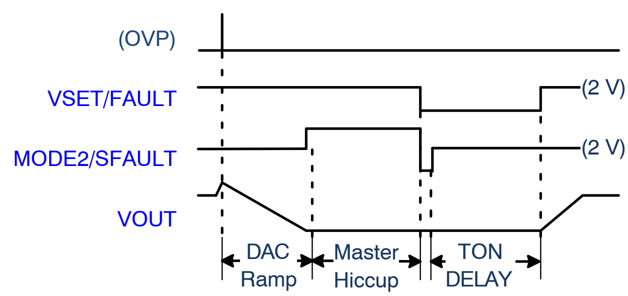


Figure 36. Master/Slave Signals, OVP Fault

In the event of an output over−voltage fault (OVP), the VSET/FAULT and MODE2/SFAULT pins both remain at 2 V until the DAC ramps down the output in a controlled fashion.

During the hiccup interval, the master pulls MODE2/SFAULT high, instructing the slaves to turn off high−side FETs and enhance low−side FETs.

After the hiccup cycle, the master forces both signals low, momentarily, which resets the slaves. Slaves re−activate when the master releases the MODE2/SFAULT signal during the TON_DELAY interval. When the master releases the VSET/FAULT signal, the re−start ramp begins.

Operating / Fault States

The table below provides a summary of device and pin states during operating and/or fault conditions:

Table 4. STATE TRUTH TABLE

State/Condition	Action/Function				
	PGOOD Pin	COMP Pin	OCP	OVP	UVP
POR V_{CC} < UVLO	N/A	N/A	N/A	N/A	N/A
Disabled, EN low, V_{CC} > UVLO	Low	Low	Disabled	Disabled	Disabled
Start−Up Delay EN low, V_{CC} > UVLO, before SS ramp begins	Low	Low	Disabled	Disabled	Disabled
Soft Start EN high, V_{CC} > UVLO	Low	Active	Active	Active, (threshold = V_{OV_A})	Disabled
Normal Operation	High	Active	Active	Active, (threshold = V_{OVP_TH})	Active
Over−Current (OCP)	Low		Cycle−by−Cycle	Active until shutdown	Active until shutdown
Over−Voltage (OVP)	Low		Disabled		Disabled
Under Voltage (UVP)	Low		Disabled	Disabled	
Thermal Shutdown (T_{SD})	Low	Low	Disabled	Disabled	Disabled
Hiccup Idle Time	Low	Low	Disabled	Disabled	Disabled

PCB LAYOUT GUIDELINE

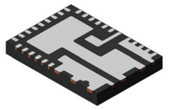
Good electrical layout is key to ensure proper operation, high efficiency, and noise reduction.

- *Bias Decoupling*: Place the decoupling caps as close as possible to the controller's VCC and VDRV pins. The VCC pin filter resistor should be ≤ 2.2 Ω to prevent a large voltage drop.
- *Input Supply Decoupling*: Place and route the input capacitors to maintain the shortest possible current loop length to reduce parasitic inductance, input voltage spikes, and noise emission. Commonly, a low ESL MLCC capacitor is placed adjacent to the PVIN and PGND pins for high frequency noise reduction.
- *Power Paths*: Use the widest and shortest possible traces for high current paths such as PVIN, VOUT, SW, and PGND to minimize series ESL and ESR. ESR contributes to power losses and temperature rise.
- *Switching Node*: The SW, PHASE, and BST pins contain high−voltage discontinuous switching waveforms with sharp edges. Care should be taken to avoid capacitive coupling to sensitive signals like FB, VSNS−, and COMP. Avoid routing these sensitive signals adjacent to or over/under on adjacent layers without GND shields, to the discontinuous switching signals.
  It is recommended to add RC snubber component locations to the PCB design should these be required to provide additional damping for peak SW voltages. The snubber devices should be placed adjacent to the IC, between SW and GND.
- *Bootstrap*: The bootstrap capacitor (C_{BST}) and series resistor (R_{BST}) should be connected directly between the BST and PHASE pins using a low impedance path. It is not necessary to establish a connection between PHASE and SW, as this is already accomplished within the IC. The series resistor is used for limiting peak SW voltages to safe levels, particularly at elevated V_{IN} levels. R_{BST} works similar to a RC snubber by slowing the switching edges, which may also be used, although either can negatively impact efficiency.
- *Voltage Sense*: Use a Kelvin sense pair to route from the FB and VSNS− pins to the remote sense point. The pair is best routed over solid GND plane, if possible. Avoid routing adjacent to switching nodes or other noise sources.
- *Compensation Network*: All components of the RC network connected to FB and COMP should be placed as close as possible to the IC pins with care to avoid routing traces adjacent to noise sources.
- *Ground*: Directly connect the exposed PGND pad to the GND plane using multiple vias. The use of multiple system GND planes is recommended.
  Connect AGND pin to the system GND plane at a single location, near the IC's AGND pin, using a robust, low impedance path.
- *Master/Slave Signals*: In a multi−phase/stacked system, master and slave interconnections should be routed using low impedance traces avoiding switching noise sources. This is particularly important for the COMP signal.
- *Thermal Layout Considerations*:
  Ensure the large exposed pad (DAP) under the IC, is securely soldered.
  Improved heat spreading can be achieved by using multiple GND layers with liberally applied thermal vias around the IC connected to those GND planes.
  Use large copper pours (areas), where possible, to improve thermal conduction and radiation.
  Keep the inductor away from the IC to distribute heat sources and reduce vicinity heating.

ORDERING INFORMATION

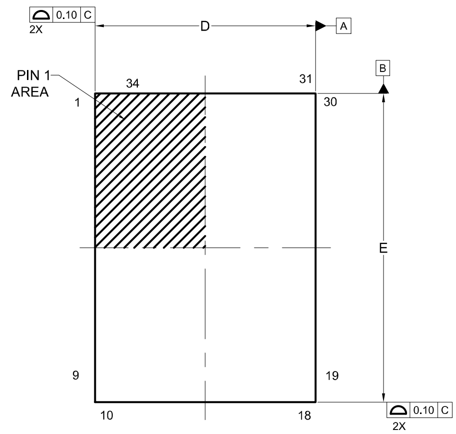
Device	Current	Package	Shipping†
NCP3294MNTXG	25 A	WQFN34, 5 x 7 mm (Pb−Free)	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

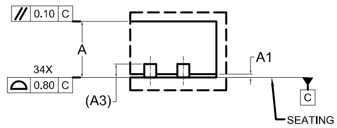


WQFN34 5x7, 0.5P
CASE 510CL
ISSUE B

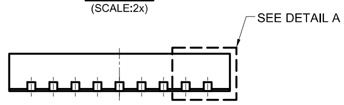
DATE 08 DEC 2022



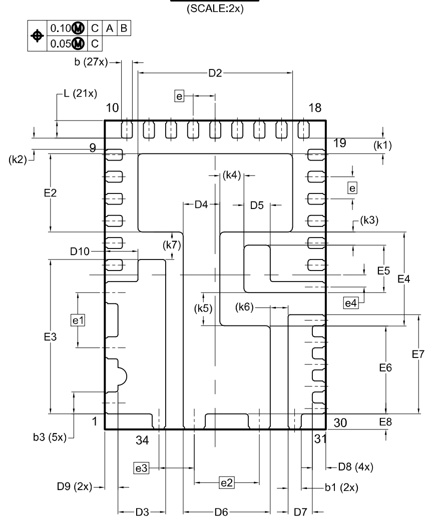
TOP VIEW
(SCALE:2x)



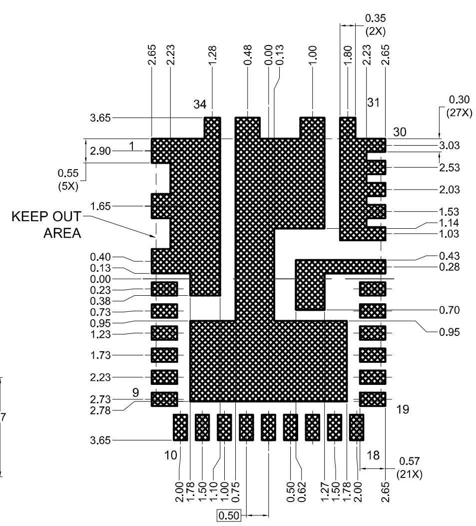
DETAIL A
(SCALE:3x)



FRONT VIEW
(SCALE:2x)



BOTTOM VIEW
(SCALE:2x)



LAND PATTERN
RECOMMENDATION

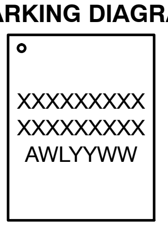
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATED MAY/2005.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	--	0.50
A3	0.20 REF		
b	0.20	0.25	0.30
b1	0.25	0.30	0.35
b2	0.40	0.50	0.60
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
D3	0.98	1.08	1.18
D4	0.73	0.83	0.93
D5	0.50	0.60	0.70
D6	1.87	1.97	2.07
D7	0.45	0.55	0.65
D8	0.20	0.30	0.40
D9	0.20	0.30	0.40
D10	0.65	0.75	0.85
E	6.90	7.00	7.10
E2	1.68	1.78	1.88
E3	3.40	3.50	3.60
E4	2.03	2.13	2.23
E5	0.98	1.08	1.18
E6	1.89	1.99	2.09
E7	2.15	2.25	2.35
E8	0.25	0.35	0.45
e	0.50 BSC		
e1	1.25 BSC		
e2	1.50 BSC		
e3	0.80 BSC		
e4	0.275BSC		
k1	0.35 REF		
k2	0.25 REF		
k3	0.30 REF		
k4	0.54 REF		
k5	0.75 REF		
k6	0.40 REF		
k7	0.63 REF		
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WQFN34 5x7, 0.5P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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For additional information, please contact your local Sales Representative at
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