NCP4350

Supervisory IC for Desktop Power Supply Monitoring

The NCP4350 provides all the necessary functions to monitor and control a multi−output power supply providing fault protection shutdown signals, and On/Off control. The NCP4350 provides the ability to monitor the status of the +5 Vdc, +12 Vdc (A and B outputs), and +3.3 Vdc output (voltage and current). The controller has built in delay to prevent tripping during transient conditions to eliminate false shutdowns.

OVP/UVP (OverVoltage/UnderVoltage Protection) monitors 3.3 V, 5 V, and dual 12 V to protect the power supply, FPOB output goes high when one of these supply voltages exceed their limits.

OCP (OverCurrent Protection) monitors 3.3 V, 5 V, and dual 12 V output current. Overcurrent limit is adjustable by I_{REF} and current protection resistor.

The PGI (Power Good Input) and OTP (OverTemperature Protection) input pin provides the flexibility for design protection circuit.

The PGO (Power Good Output) signal gives personal computer notice when the output supplies are ready or power supply is going to shutdown or fail, therefore it can provide a reliable power supply environment.

Features

- Individual Overvoltage and Undervoltage Monitoring for +3.3 V, +5 V, +12 VA, +12 VB Outputs and Lockout
- Individual Overcurrent Monitoring for +3.3 V, +5 V, +12 VA, +12 VB Outputs and Lockout
- Fault Output with 5 mA of Sink Capability
- Remote On/Off
- Power Good Output Signal with 5 mA of Sink Capability
- Built−in Delays for OVP, UVP, and Overload to avoid False Tripping
- Low Power Consumption 10 mW at V_{CC} = 5 V Typical
- Overtemperature Input
- Wide Power Supply Range (4 V − 16 V)

Typical Applications

- ATX Computers

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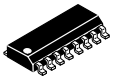


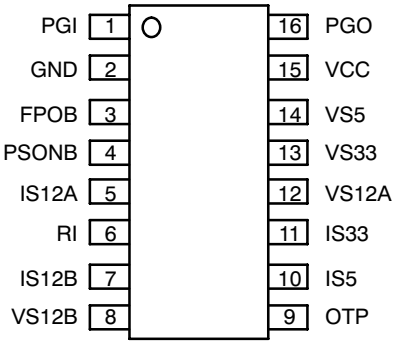
SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM

1

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Device

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4350DR2G	SOIC−16 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

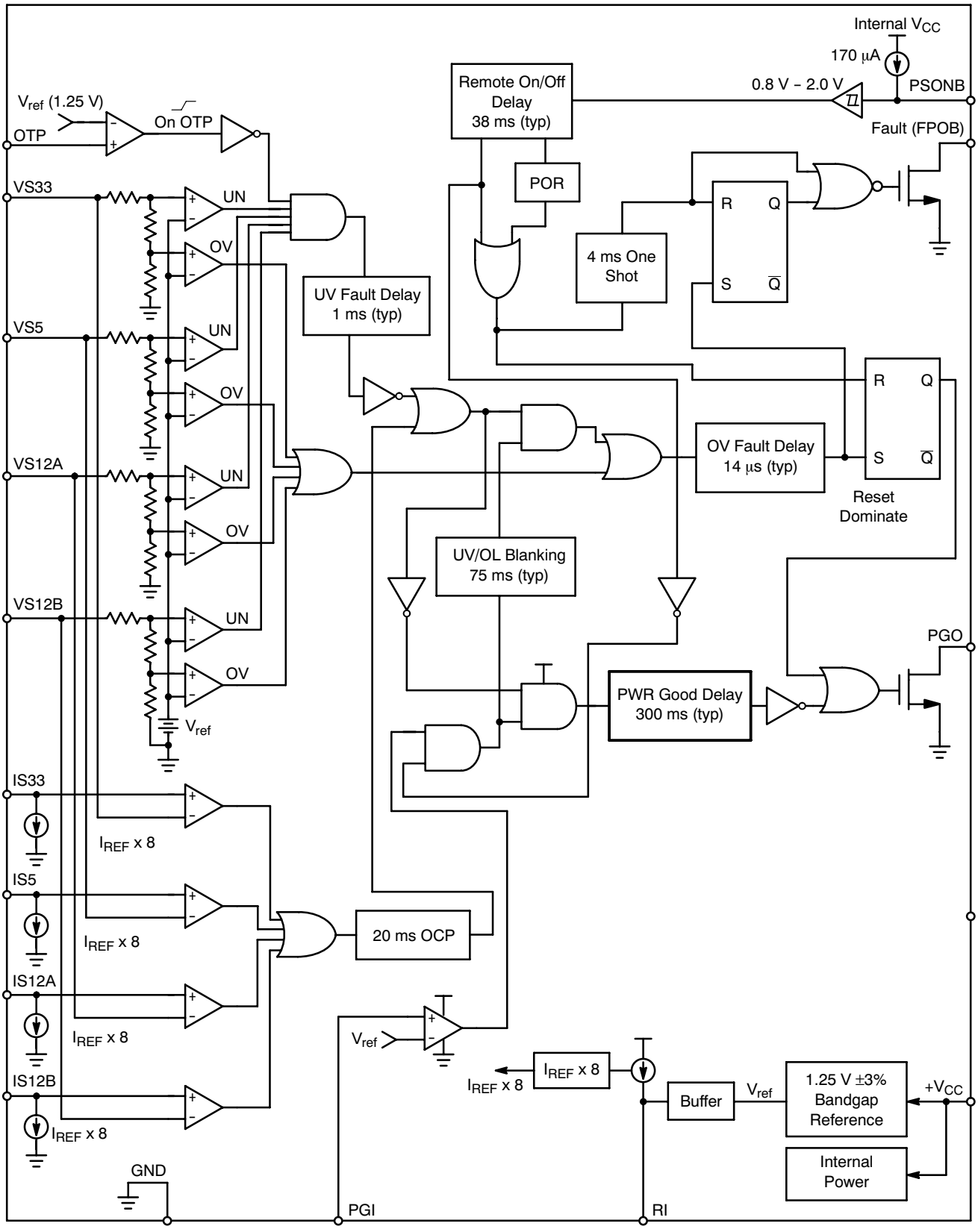


Figure 1. Detailed Block Diagram

PIN DESCRIPTION

Pin	Pin#	Description
PGI	1	The pin is used for a power good input signal.
GND	2	Ground
FPOB	3	This is an open drain output for Fault protection shutdown.
PSONB	4	This pin is used for a REMOTE on/off switch input and acts as a reset signal after a fault condition.
IS12A	5	This pin is an input to the +12 VA output current monitoring comparator.
RI	6	A resistor to ground sets the I_{REF} current for overcurrent monitoring.
IS12B	7	This pin is an input to the +12 VB output current monitoring comparator.
VS12B	8	This pin is an input to the +12 VB output voltage monitoring comparator.
OTP	9	Overtemperature or external protection input.
IS5	10	This pin is an input to the +5 V output current monitoring comparator.
IS33	11	This pin is an input to the +3.3 V output current monitoring comparator.
VS12A	12	This pin is an input to the +12 VA output voltage monitoring comparator.
VS33	13	This pin is an input to the +3.3 V output voltage monitoring comparator.
VS5	14	This pin is an input to the +5 V output voltage monitoring comparator.
$+V_{CC}$	15	This is the input pin for V_{CC}.
PGO	16	This pin provides an open drain power good output signal.

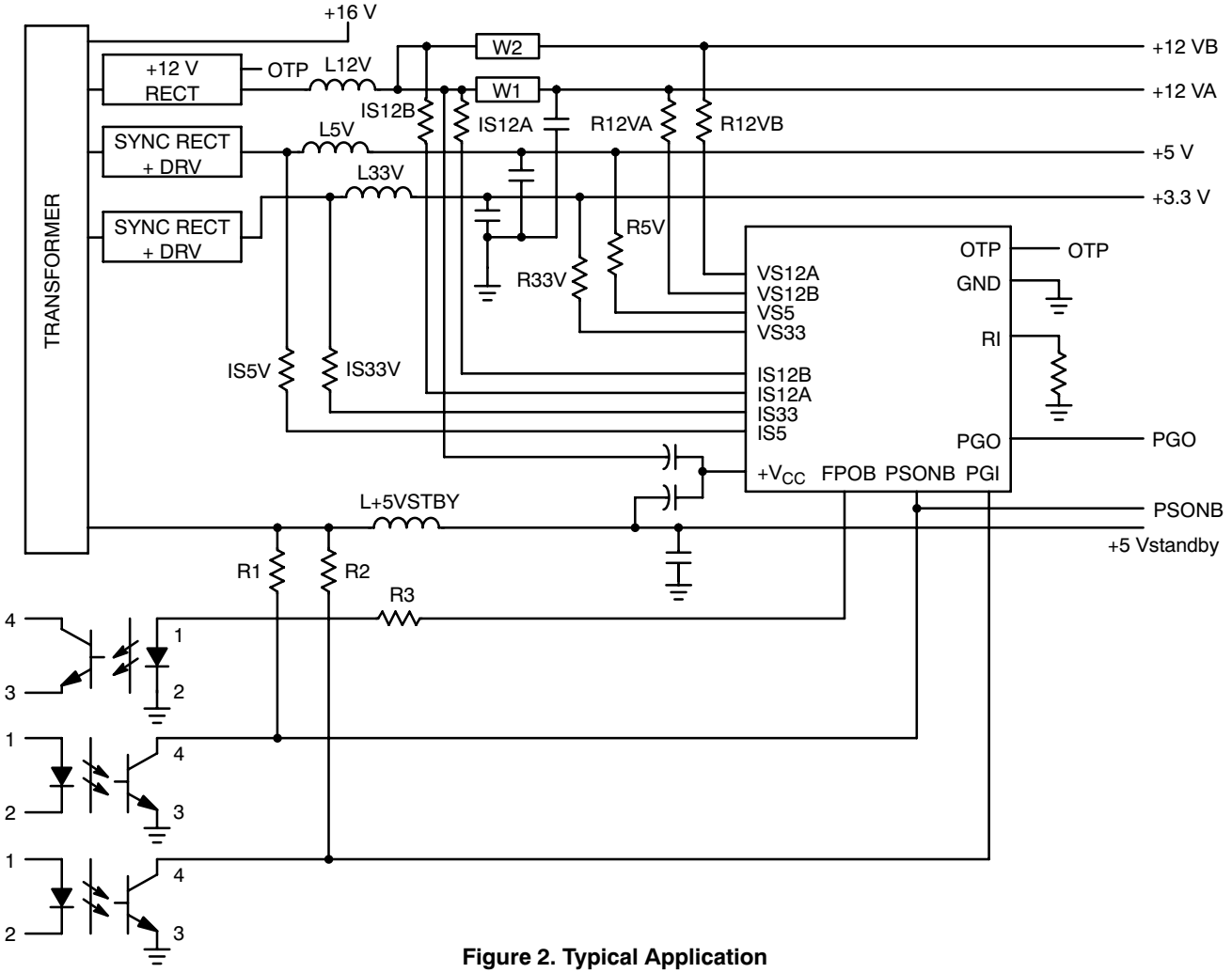


Figure 2. Typical Application

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Current	V_{CC}	−0.3 to 16 100	V mA
Maximum Voltage Current	VS12A VS12B IS12A IS12B	−0.3 to 16 100	V mA
Maximum Voltage Current	PGI PSONB OTP VS33 IS33	−0.3 to 5.5 100	V mA
Maximum Voltage	V_{RI}	2.0	V
Power Good Output and FPOB Sink Current	IPGO IFPOB	5.0	mA
Maximum Voltage	V_{OH}PGO, V_{OH}FPOB VS5 IS5	7.5	V
Output Current from RI	I_{REF}	100	μA
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature Range	T_{SMAX}	−65 to 150	°C
Lead Temperature (Soldering, 10s)	T_{LMAX}	300	°C
Total Power Dissipation	P_D	TBD	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1−16: Human Body Model 2000V per Mil−Std−883, Method 3015.
   Machine Model Method 200V
2. This device contains Latch−up protection and exceeds ±100ma per JEDEC Standard JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Min	Typ	Max	Unit
V_{CC}	Operating Supply Voltage	4.0		16	V
I_{REF}	Output Current from RI	12.5		62.5	μA
T_J	Operating Junction Temperature Range	0		105	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, for typical values T_J = 25°C, for min/max values, T_J = 0°C to +105°C, Max T_J = 150°C, R_I =33 kΩ, unless otherwise noted.)

Symbol	Rating	Min	Typ	Max	Unit
I_{CC}	Operating Supply Current (VCC = 16V, FPOB↓ and PGO↑)	–	1.5	2.0	mA
Overvoltage/Undervoltage Protection					
V33OVP	+3.3V Output Overvoltage Threshold (includes V_{IO}) T_J =0°C to +105°C	3.8	3.9	4.0	V
$V33OVP_{HYS}$	Hysteresis (Note 3)	–	40	–	mV
V5OVP	+5 V Output Overvoltage Threshold (includes V_{IO}) T_J =0°C to +105°C	5.6	5.8	6.0	V
$V5OVP_{HYS}$	Hysteresis (Note 3)	–	60	–	mV
V12OVP (A and B)	+12V Output Overvoltage Threshold (includes V_{IO}) T_J =0°C to +105°C	13.5	13.85	14.2	V
$V12OVP_{HYS}$ (A and B)	Hysteresis (Note 3)	–	130	–	mV
V33UVP	+3.3V Output Undervoltage Threshold (includes V_{IO}) T_J =0°C to +105°C	2.8	2.9	3.0	V
$V33UVP_{HYS}$	Hysteresis (Note 3)	–	30	–	mV
V5UVP	+5 V Output Undervoltage Threshold (includes V_{IO}) T_J =0°C to +105°C	4.2	4.4	4.6	V
$V5UVP_{HYS}$	Hysteresis (Note 3)	–	45	–	mV
V12UVP (A and B)	+12V Output Undervoltage Threshold (includes V_{IO}) T_J =0°C to +105°C	10.3	10.65	11.0	V
$V12UVP_{HYS}$ (A and B)	Hysteresis (Note 3)	–	100	–	mV
Interface I/O					
V_{OLFPOB}	Low Level Output Voltage Fault (I_{Sink} = 5 mA)			0.4	V
I_{LFAULT}	Leakage Current (V_{DS}= 5V)			10	μA
V_{THPGI}	Input Voltage Threshold	1.18	1.25	1.32	V
V_{OLPGO}	Low Level Output Voltage (I_{Sink} = 5 mA)			0.4	V
I_{LPGO}	Leakage Current (V_{DS} = 5V)			10	μA
$V_{OLPSONB}$	Low Level Input Voltage			0.8	V
$V_{OHPSONB}$	High Level Input Voltage	2.0			V
$V_{PSONBHYS}$	PSONB Input Hysteresis	300	–	–	mV
$PSONBV_{IH}$	Open Circuit Voltage (I_{IN} = 0 mA)	2.5		5.25	V
I_{LPSONB}	Input Pull−up Current (V_{PSONB} = 0V)	120	170	220	μA
Current Monitoring Comparators					
$IS12AV_{IO}$	Input Offset Voltage 12VA Comparator, T_J = +25°C	−4.0		4.0	mV
$IS12BV_{IO}$	Input Offset Voltage 12VB Comparator, T_J = +25°C	−4.0		4.0	mV
$IS33V_{IO}$	Input Offset Voltage 33V Comparator, T_J = +25°C	−4.0		4.0	mV
$IS5V_{IO}$	Input Offset Voltage 5V Comparator, T_J = +25°C	−4.0		4.0	mV
A_{VOL}	Voltage Gain (Note 3)	50	200		V/mV
I_{IB}	Input Bias Current (V_{IS12x} = 12V, V_{IS5} = 5V, V_{IS33} = 3.3V)		300	500	nA
$I_{REFGAIN}$	The Gain of the I_{REF} signal, R_I=33 k ±0.1%, I_{REF} = 1.25/R_I, T_J=+25°C	7.68	8.0	8.32	

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, for typical values T_J = 25°C, for min/max values, T_J = 0°C to +105°C, Max T_J = 150°C, R_I =33 kΩ, unless otherwise noted.)

Symbol	Rating	Min	Typ	Max	Unit
Delay Characteristics					
$Tdly_{PSONB}$	Time delay On/Off PSONB (PGO↓) 50% of the pull up voltage (PSONB>$V_{OHPSONB}$, $R_{pull-up}$ FPOB =1k, $V_{pull-up}$ = +5 V)	24	38	62	msec
$Tdly_{FOP}$	Time delay between PGO↓ and FPOB↑	2.0	4.0	8.0	msec
$Tdly_{OV}$	Time delay from an OV to FPOB↑ and PGO↓ 50% of the pull up voltage (PSONB<$V_{OLPSONB}$, $R_{pull-up}$ FPOB =1k, $V_{pull-up}$ = +5 V)	9.0	14	19	μsec
$Tdly_{UV}$	Time delay from an UV to FPOB↑ and PGO↓ 50% of the pull up voltage (PSONB<$V_{OLPSONB}$, $R_{pull-up}$ FPOB =1k, $V_{pull-up}$ = +5 V)	0.5	1.0	2.0	msec
$Tdly_{PGO}$	Time delay PGI↑ to PGO↓ (PSONB<$V_{OLPSONB}$, $R_{pull-up}$ PGO =1k, $V_{pull-up}$ = +5 V)	100	300	438	msec
$Tdlly_{START}$	Time delay on start−up UV, OC, OTP lockout	45	75	130	msec
$Tdelay_{OTP}$	Time delay from an OTP↑ to FPOB↑ and PGO↓ 50% of the pull up voltage (PSONB<$V_{OLPSONB}$, $R_{pull-up}$ FPOB and PGO =1k, $V_{pull-up}$ = +5 V) OTP↓	0.5	1.0	2.0	msec
$Tdly_{OCP}$	Time delay from an OCP to FPOB↑ and PGO↓ 50% of the pull up voltage (PSONB<$V_{OLPSONB}$, $R_{pull-up}$ FPOB and PGO =1k, $V_{pull-up}$ = +5 V)	11	20	32	msec
$Tdly_{PGI}$	Time delay from PSONB↓ to PGO↑ 10−90% of the pull up voltage (PGI>V_{THPGI}, $R_{pull-up}$ PGO=1k, $V_{pull-up}$ = +5V)	124	338	500	msec
Overtemperature Input					
V_{OTP}	Voltage threshold for OTP↓(PGO↓, FPOB↑, PSONB < V_{OL}PSONB, $R_{pull-up}$ FPOB and PGO =1k, $V_{pull-up}$ = +5 V)	1.18	1.25	1.32	V
V_{OTPHYS}	Overtemperature Comparator Hysteresis (Note 3)		50		mV

3. Guaranteed by design.

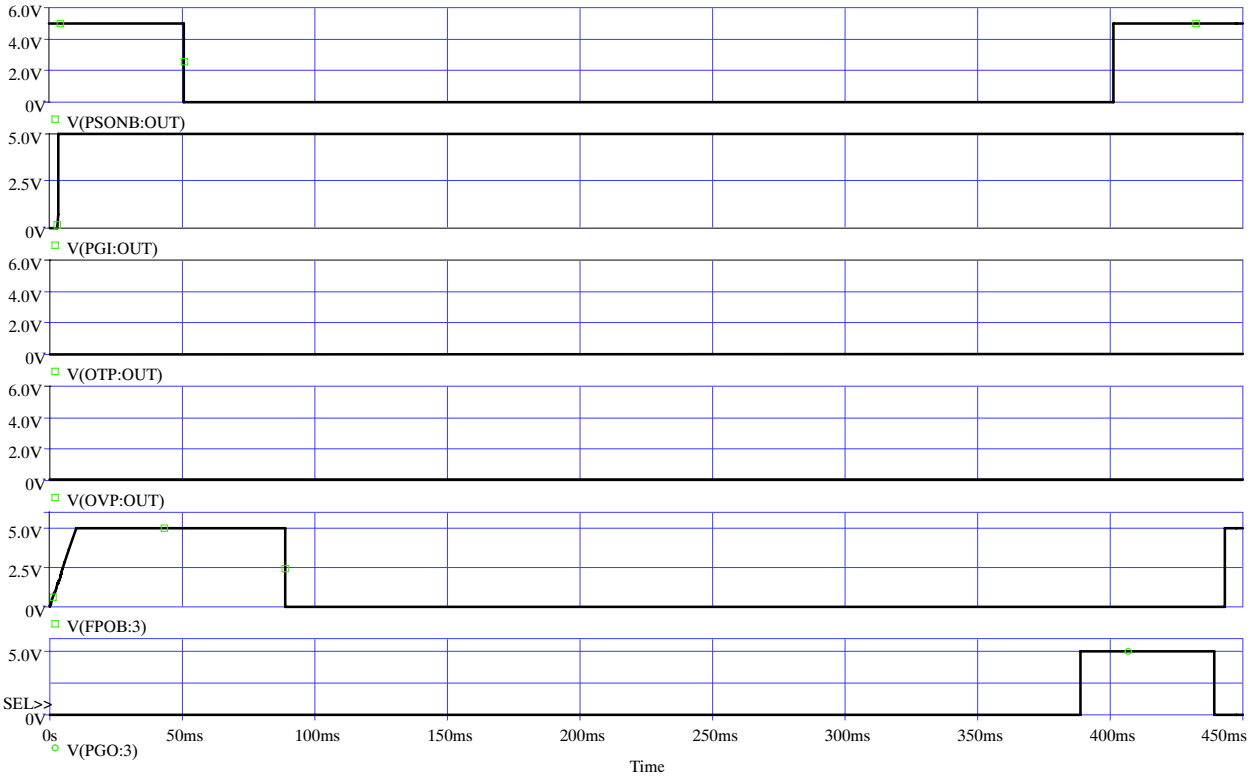


Figure 3. PSONB ON/OFF

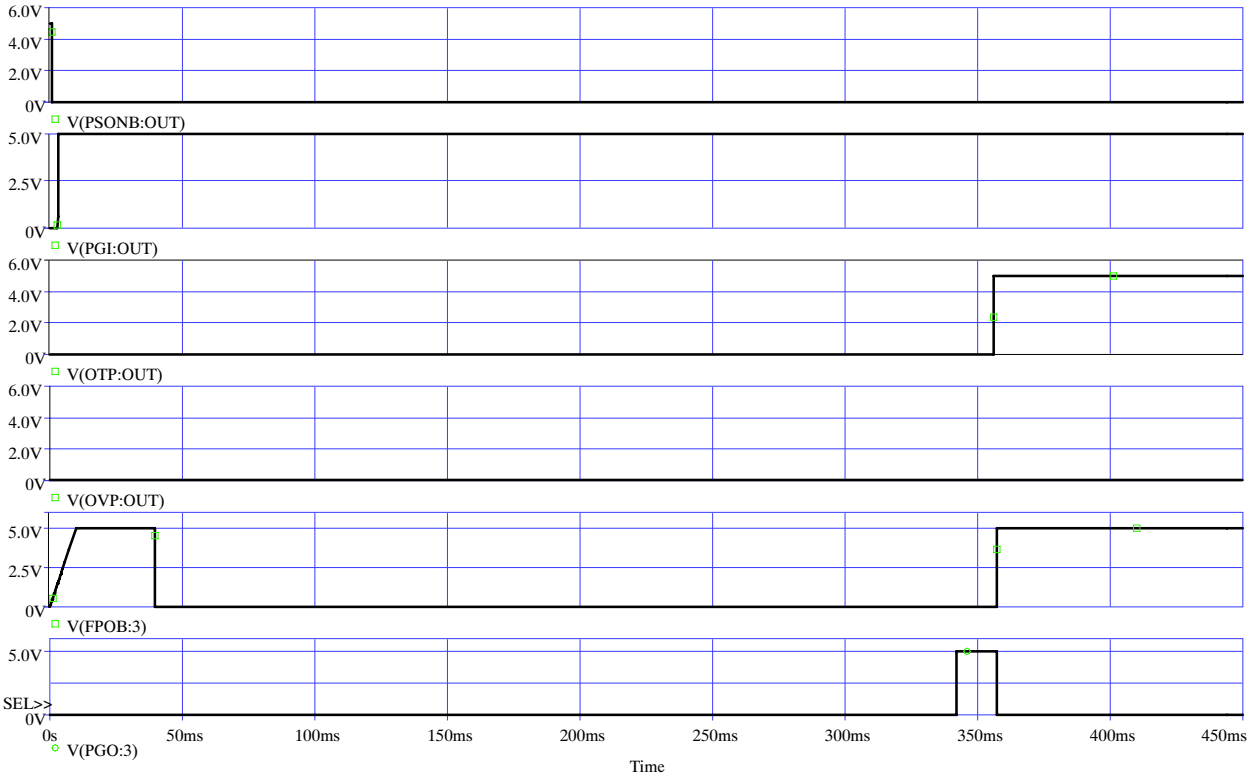


Figure 4. AC Turn−On − UVP, OVP, OCP, OTP Fault

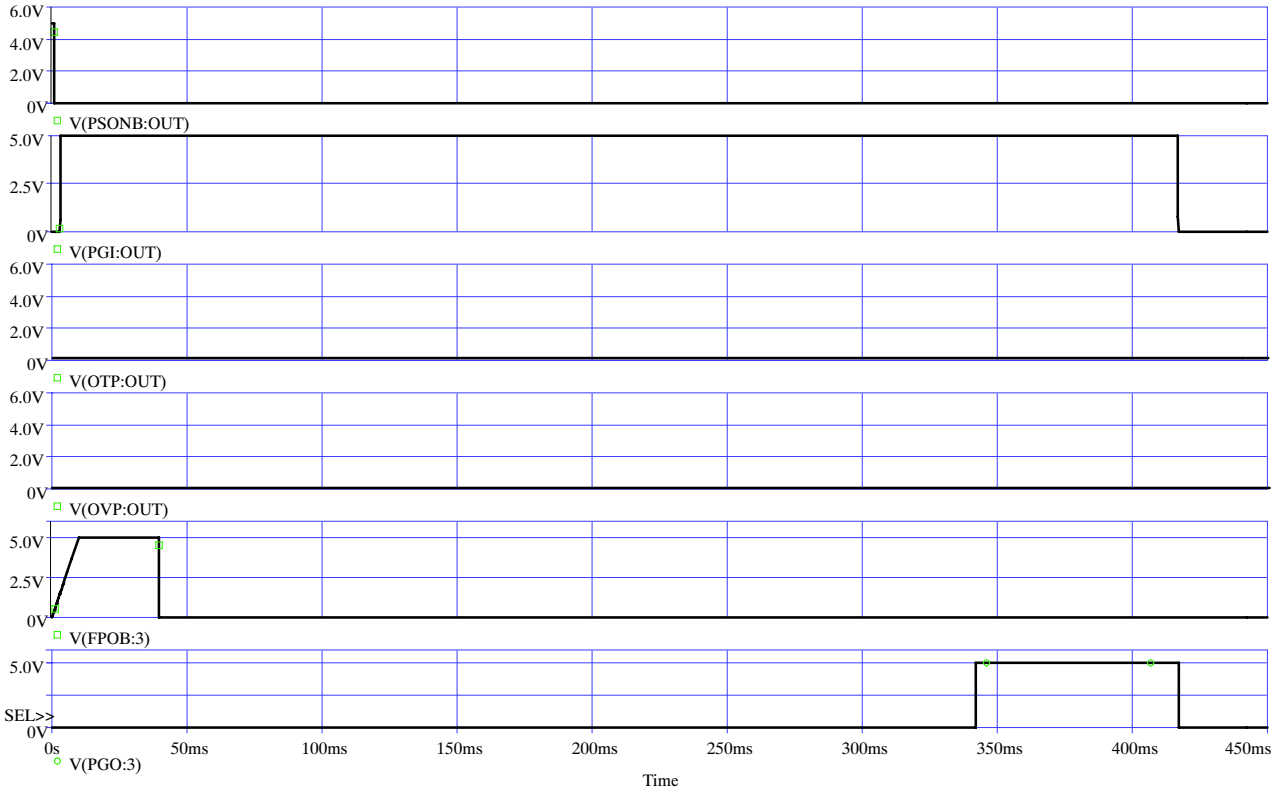


Figure 5. PSONB Turn−On − AC Turn−Off

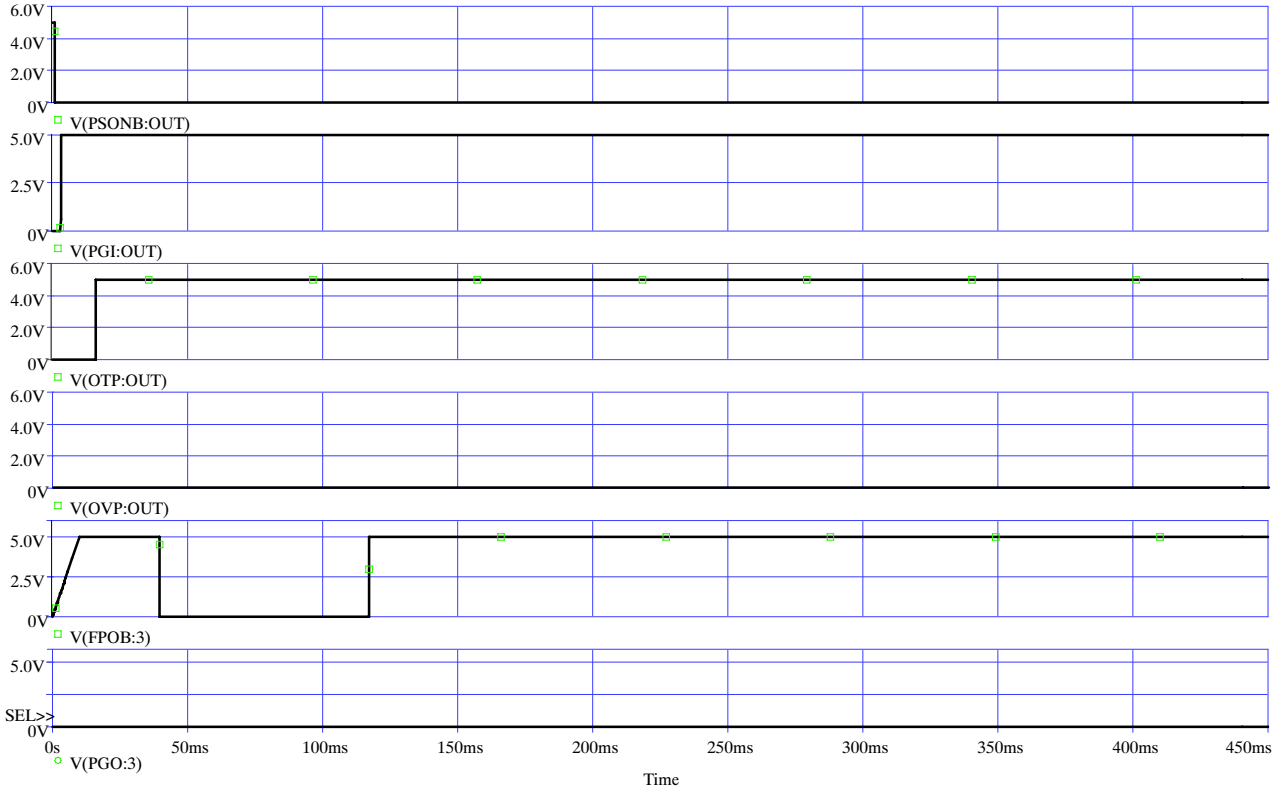


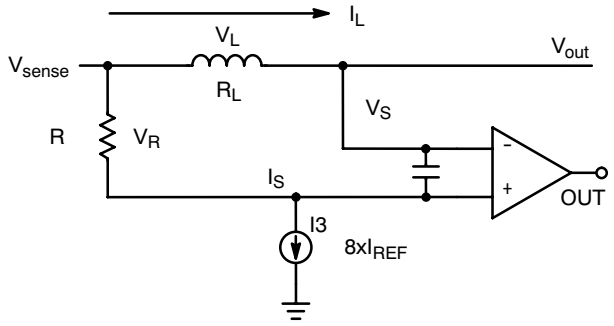
Figure 6. AC Turn−On with OTP, UVP or OCP Fault

TABLE 1: ASIC TRUTH TABLE

PGI	PSONB (REMOTE)	UVP,OVP,OCP	FPOB (FAULT)	PGO
<1.25V(L)	L	No	L	L
<1.25V(L)	L	Yes	L	L
>1.25V(H)	L	No	L	H
>1.25V(H)	L	Yes	H	L

Overload Current Monitoring

In ATX power supplies the output power must be monitored and limited. In the present ATX specification the +3.3 V and +5 V outputs have a very relaxed tolerance for the over current limit set point. As a result customers typically use the dc resistance in the output filter inductor. If very accuracy current sensing is required, as is the case for the +12 V outputs, a precision current shunt is used.



The circuit operates as shown, when the load current increases the voltage drop across the inductor, or current shunt,- in series (the dc resistance) with the output increases reducing the voltage at the negative input of the overcurrent comparator. The voltage at the positive input to the comparator is set by the I_{REF} current source, if the voltage at the negative input to the comparator is less than the voltage at the positive input to the comparator; the comparator output goes high indicating an overload condition. The overload trip level can be determined by the following relationships:

$$V_R = 8 \times I_{REF} \times R$$

$$R = \frac{R_L \cdot I_L}{I_{REF} \cdot 8}$$

Example:
R_I = 33 kΩ
R_L = 0.002 Ω
R = 150 Ω

$$I_{REF} = \frac{V_{REF}}{R_I} = \frac{1.25\ V}{33k}$$

$$I_L = I_{REF} \cdot 8 \cdot \frac{R}{R_L} = 37.87\mu A \cdot 8 \cdot \frac{150}{0.002} = 22.72\ Adc$$

This calculation neglects input voltage offset, biases currents, and other tolerances.

Output Voltage Sensing

Four output voltage sense lines are provided +3.3V, +5.0V, +12VA, +12VB. Each of the sensed input signals is inputted into an undervoltage (UVP) and overvoltage (OVP) comparators. In the event of an output fault (OVP or UVP) the fault trigger signal is delayed and then latch. The delay has been added to prevent the Latch from being set during output transient conditions. During start−up the UVP, OTP and OCP comparators output are ignored.

Power Good Input

The Power Good input (PGI) can be used to monitor an additional logic event, for example the temperature inside an ATX power supply. When the input voltage at the PGI is below the threshold 1.25 V, the Power Good Output (PGO) signal remains in a low state, even if all of the voltage and current sensed inputs are within the voltage and current limits.

PSONB

The PSONB input is active low and is used to turn on/off the primary side controller. The PSONB signal can also be used to reset the PGO output after a fault a condition has occurred. When the PSONB signal is low (the external connection), the Fault signal between the monitoring controller and the power supply is enabled (FAULT will be low, no Fault). In order to reset the Fault latch a minimum width pulse should be applied to the PSONB input, the pulse should be greater than 38 msec (typical).

Power Good Output

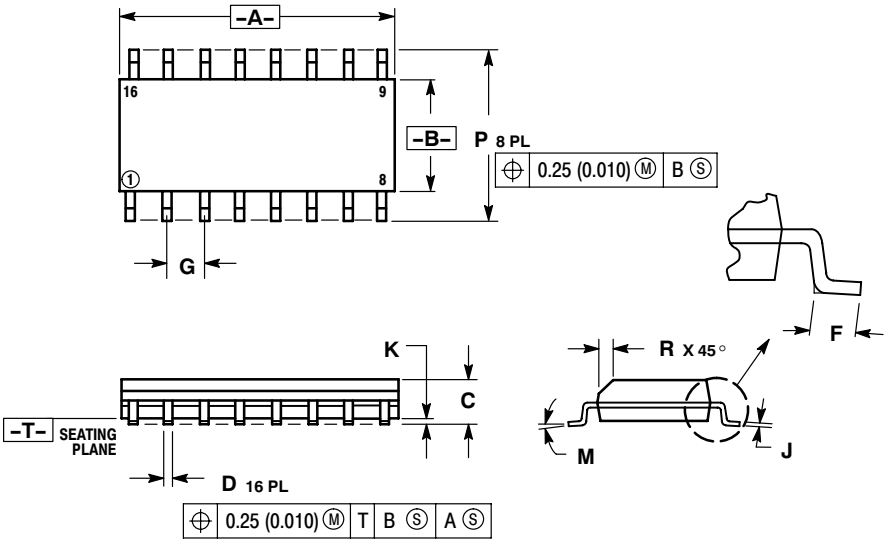
The Power Good (PGO) signal is intended to warn the motherboard that the output voltage or current of at least one of the four outputs is out of tolerance. The PGO signal is delayed by 300 msec (typical) to avoid false tripping due to transient conditions. The PGO output is capable of sinking 5 mA of current.

FPOB Output

In a typical application (refer to Figure 2) the Fault pin is activated (high level) when any one of four outputs is out of range, or there is an output overload condition. The Fault output is the link between the output monitoring circuits and the primary PWM. The Fault output is capable of sinking 5 mA of current.

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

The product described herein (NCP4350), may be covered by U.S. patents including 6,373,734. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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