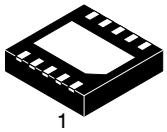
Linear Voltage Regulator 2 A Low Noise Very Low Dropout with Charge Pump

Product Preview

NCP59762



DFN10 – 3 x 3
CASE 506EH

The NCP59762 is a 2 A, low noise, very low dropout linear regulator (VLDO) equipped with the NMOS pass transistor and internal charge pump (without external bias voltage).

The high output current capability with high accuracy, broad bandwidth high PSRR and low noise makes this VLDOs ideal for powering noise sensitive high speed communication devices, high end FPGAs, microprocessors, power demanding ADCs, DACs and RF components.

Features

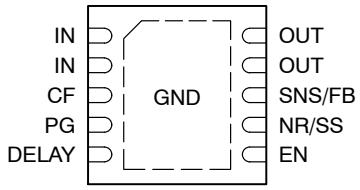
- High Output Current 2 A
- High Accuracy ±1% Including Line/Load Regulation and Temperature Variation
- Input Voltage Range: 1.1 V to 3.6 V
- Fixed and Adjustable Voltage Versions Available
- Output Voltage Range: 0.5 V to 2.0 V (both Fixed and Adjustable)
- Dropout Voltage: 45 mV typ. at 2 A
- Very Low Output Voltage Noise: 4.5 μV_{RMS} typ. (10 Hz – 100 kHz)
- Excellent Transient Response
- Low Quiescent Current Consumption: 1.1 mA typ.
- Programmable Soft Start
- Open Drain Power Good Output with Programmable Delay
- Stable with a 47 µF or Larger Ceramic Output Capacitor
- DFN−10 3.0 x 3.0 mm Package
- These are Pb−Free Devices

Typical Applications

- High Speed Analog VCO, ADC, DAC
- FPGAs, DSPs, SerDes
- Imaging Sensors and ASICs
- Communications, Test, Measurement

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM

59762P	= Specific Device Code
xxx	= Output Voltage Version
y	= Output Discharge Version
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

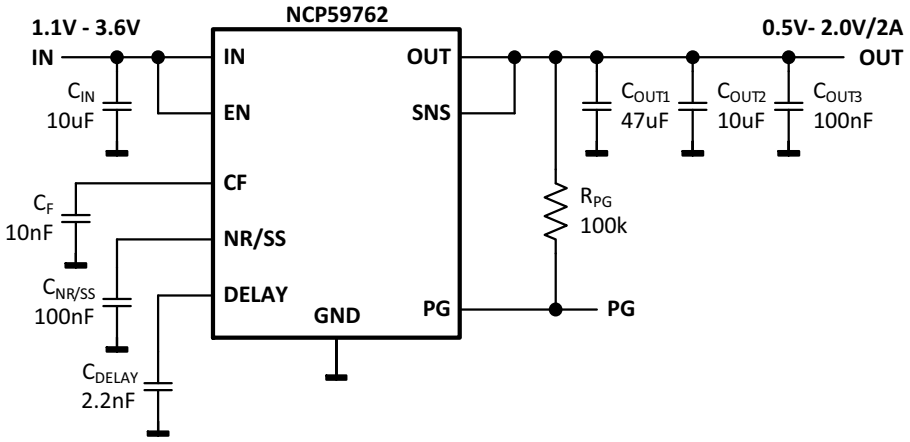


Figure 1. Typical Application Schematic (Fixed Voltage)

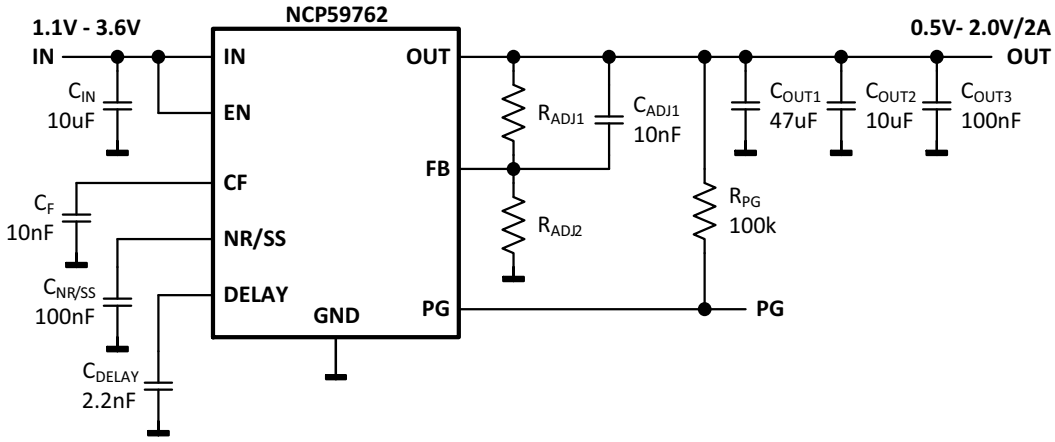


Figure 2. Typical Application Schematic (Adjustable Voltage)

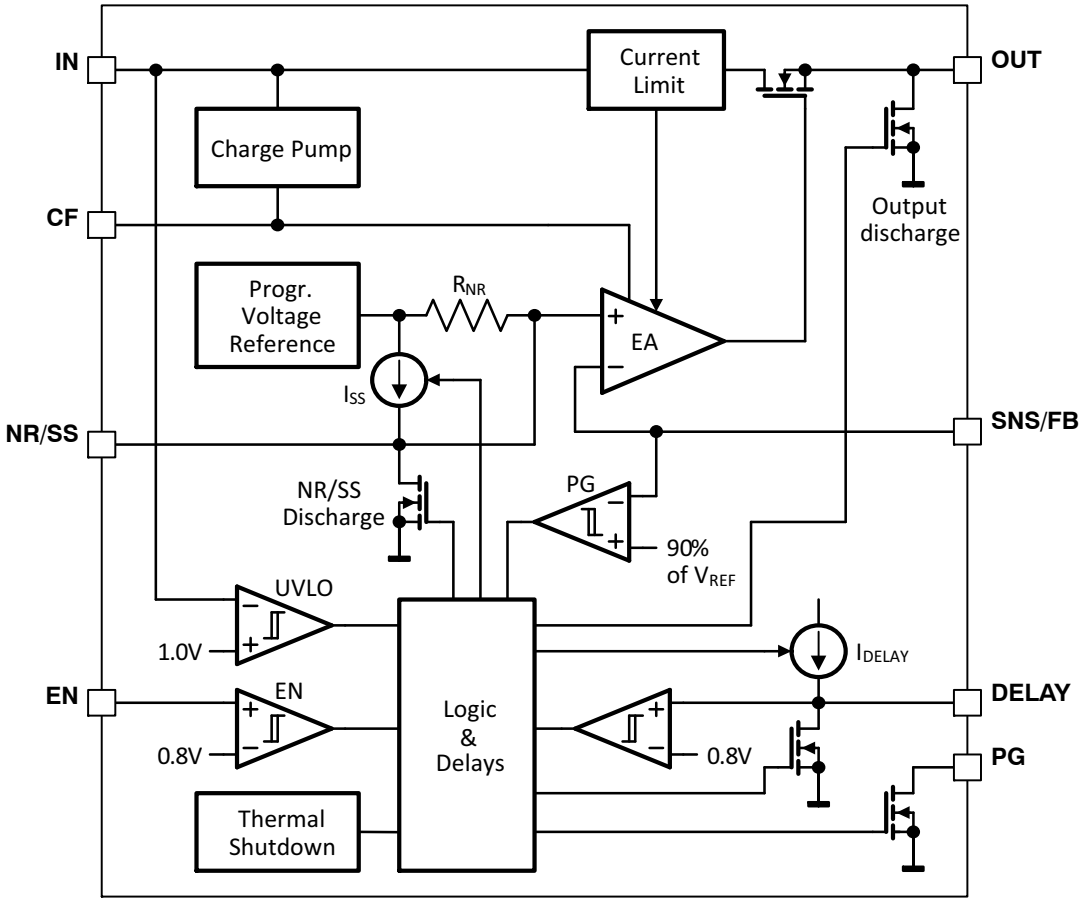


Figure 3. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Name	DFN10	Description
IN	1,2	Input Voltage Supply pins.
CF	3	Internal supply filtering Capacitor.
PG	4	Power−Good (PG) is an open−drain, active−high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high−impedance state. When V_{OUT} is below this threshold the pin is driven to a low−impedance state. A pull−up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply up to 3.6 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
DELAY	5	This pin is intended for adjusting the delay for signaling "V_{OUT} is OK" according to the user application needs. Capacitor connected from this pin to GND with capacitance of 2.2 nF corresponds to 1 ms delay. The maximum delay applicable is 100 ms. If delay not necessary the DELAY pin can be left floating.
EN	6	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
NR/SS	7	Noise−reduction and soft−start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft−start function. Although not required, a 10 nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
SNS (Fixed V_{OUT} Device)	8	Output voltage Sensing Input. Connect to Output voltage node on the PCB.
FB (Adjustable V_{OUT} device)	8	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	9,10	Regulated output voltage. It is recommended that the output capacitor effective capacitance ≥ 47 μF.
GND	TAB	Ground and Thermal Pad.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to +3.6	V
Enable Voltage Range	V_{EN}	−0.3 to +3.6	V
Power−Good Voltage Range	V_{PG}	−0.3 to +3.6	V
PG Sink Current	I_{PG}	0 to +5.0	mA
NR/SS Pin Voltage Range	$V_{NR/SS}$	Connecting to external voltage not allowed	V
CF Pin Voltage Range	V_{CF}	Connecting to external voltage not allowed	V
DELAY Pin Voltage Range	V_{DELAY}	Connecting to external voltage not allowed	V
SNS Pin Voltage Range (Fixed Voltage Devices)	V_{SNS}	−0.3 to +3.6	V
FB Pin Voltage Range (Adjustable Devices)	V_{FB}	−0.3 to +3.6	V
Output Voltage Range	V_{OUT}	-0.3 to $(V_{IN} + 0.3) \leq 3.6$	V
Maximum Output Current	I_{OUT}	Internally Limited	
Output Short Circuit Duration		Indefinite	
Continuous Total Power Dissipation	P_D	See Thermal Characteristics Table and Formula	
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Junction Temperature Range	T_{STG}	−55 to +150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114 (AEC−Q100−002)
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101 (AEC Q100−011D)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient (Note 4)	$R_{\theta JA}$	34	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	19	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 5)	$R_{\theta JC(bot)}$	3.3	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	3.3	°C/W
Characterization Parameter, Junction−to−Top	ψ_{JT}	0.4	°C/W
Characterization Parameter, Junction−to−Board	ψ_{JB}	3.2	°C/W

3. Thermal data based on thermal simulation methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:
   These data were generated with only a single device at the center of a high−K (2s2p) board with 3 in x 3 in copper area which follows the JEDEC51.7 guidelines. Top and bottom layer 2 oz. copper, inner planes 1 oz. copper.
   The GND pad connected to the PCB inner GND plane layer through a 2x3 thermal via array. All the vias are 0.3 mm diameter, plated.
4. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
5. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 6)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	1.1	3.6	V
Output Voltage	V_{OUT}	0.5	2.0	V
Power−Good Voltage	V_{PG}	0	3.6	V
Enable Voltage Range	V_{EN}	0	3.6	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS

At V_{IN} = 1.2 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V whichever is greater, V_{EN} = 1.1 V, FB/SNS connected to OUT, C_F = 10 nF, $C_{NR/SS}$ = 100 nF, C_{IN} = 10 μF, C_{OUT} = 47 μF, I_{OUT} = 50 mA, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. (Note 7)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{UVLO-TH}$	Input voltage UVLO threshold	V_{IN} Rising		0.9	1.00	1.09	V
$V_{UVLO-HYS}$	Input voltage UVLO hysteresis	V_{IN} Falling			0.17		V
V_{OUT}	Output voltage range (Notes 8, 9, 10, 11) (Adjustable devices)	$V_{IN} \geq 1.2$ V, $V_{IN} \geq (V_{OUT(SET)} + 0.4$ V), I_{OUT} = 50 mA to 2 A		V_{OUT} (NOM)		2.0	V
	Accuracy (Note 9, 10)	$V_{IN} \geq 1.2$ V, $V_{IN} \geq (V_{OUT(NOM)} + 0.4$ V), I_{OUT} = 50 mA to 2 A		−1.0		+1.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	$V_{IN} \geq 1.2$ V, $V_{IN} \geq (V_{OUT(NOM)} + 0.4$ V)			0.2		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 2 A			0.01		%/A
V_{DO}	IN−OUT dropout voltage (ADJ)	I_{OUT} = 2 A, V_{FB} = 0 V, V_{IN} = 1.2 to 2.0 V			45	85	mV
	IN−OUT dropout voltage (FIX)	I_{OUT} = 2 A, V_{SNS} = 0 V, V_{IN} = $V_{OUT(NOM)}$, $V_{IN} \geq 1.2$ V					
I_{CL}	Output current limit	$V_{OUT} \geq 90\%$ x $V_{OUT(NOM)}$		2.2	3.0	4.2	A
I_Q	Quiescent current	I_{OUT} = 0 to 2 A			1.1	1.8	mA
I_{SHDN}	Shutdown supply current	$V_{EN} \leq 0.4$ V			1	15	μA
$I_{SNS/FB}$	SNS/FB pin current	$V_{SNS/FB}$ = V_{OUT}		−250	10	250	nA
PSRR	Power supply rejection ratio	I_{OUT} = 1 A	1 kHz		70		dB
			10 kHz		50		
			500 kHz		35		
Noise	Output noise voltage (Fix devices)	10 Hz to 100 kHz, I_{OUT} = 2 A			4.5		μVrms
	Output noise voltage (Adjustable devices) (Note 11)	10 Hz to 100 kHz, I_{OUT} = 2 A			5.0 x $V_{OUT(SET)}$		μVrms
dV_{OUT}/dI_{OUT}	Output voltage load transient response	I_{OUT} = 50 mA to 2 A at 1 A/μs			±17		mV
t_{START}	Minimum startup time	I_{OUT} = 2 A, $C_{NR/SS}$ = open			200		μs
I_{SS}	Soft−start charging current (Fix Volt devices)	$V_{NR/SS}$ = 0 V	$V_{OUT(NOM)} \leq 0.9$ V		6.0		μA
			$V_{OUT(NOM)} > 0.9$ V		12.0		
	Soft−start charging current (Adjustable devices)	$V_{NR/SS}$ = 0 V			6.0		μA
V_{EN-HI}	Enable input high level			0.8		3.6	V
V_{EN-LO}	Enable input low level			0		0.4	V
V_{EN-HYS}	Enable pin hysteresis				100		mV
T_{EN-DGL}	Enable pin deglitch time				20		μs
I_{EN}	Enable pin current	V_{EN} = 3.6 V falling			0.3	1	μA

Table 5. ELECTRICAL CHARACTERISTICS
At V_{IN} = 1.2 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V whichever is greater, V_{EN} = 1.1 V, FB/SNS connected to OUT, C_F = 10 nF, $C_{NR/SS}$ = 100 nF, C_{IN} = 10 μF, C_{OUT} = 47 μF, I_{OUT} = 50 mA, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. (Note 7)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{PG-TH}	PG trip threshold	V_{OUT} falling	86.5	90	93.5	%$V_{OUT(NOM)}$
V_{PG-HYS}	PG trip hysteresis	V_{OUT} rising		3		%$V_{OUT(NOM)}$
V_{PG-LO}	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{PG-TH}			0.3	V
I_{PG-LK}	PG leakage current	V_{PG} = 3.6 V, V_{OUT} > V_{PG-TH}		0.01	1	μA
I_{DELAY}	DELAY pin charging current	V_{DELAY} = 0 V		1.76		μA
$V_{DELAY-TH}$	DELAY trip threshold	V_{DELAY} rising		800		mV
$V_{DELAY-HYS}$	DELAY trip hysteresis	V_{DELAY} falling		30		mV
R_{AD}	Output Active Discharge Resistance (A−option only)	V_{EN} = 0 V, V_{IN} = 3.3 V, V_{OUT} = 2.0 V		100		Ω
TSD	Thermal shutdown temperature threshold high	Temperature rising		165		°C
	Thermal shutdown temperature threshold low	Temperature falling		140		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C.
8. For adjustable devices the $V_{OUT(NOM)}$ is the output voltage specified by OPN. It could be seen at the output pin when FB pin is connected to OUT pin directly (without resistor divider).
9. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
10. The device is not tested under conditions where the power dissipation is higher than the maximum rating of the package.
11. $V_{OUT(SET)}$ is the output voltage set by external resistor divider (adjustable version only). In case FB pin is shorted to OUT pin the $V_{OUT(SET)}$ = $V_{OUT(NOM)}$.

APPLICATIONS INFORMATION

Power−Good (PG) is an open−drain, active−high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high−impedance state with user adjustable delay. This high−impedance state is signaling "V_{OUT} is OK."

When V_{OUT} is below the PG trip threshold the pin is driven to a low−impedance state immediately. A pull−up resistor should be connected from this pin to a supply up to 3.6 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.

DELAY pin is intended for adjusting the delay for signaling "V_{OUT} is OK" according the user application needs. Capacitor connected from this pin to GND with capacitance of 2.2 nF corresponds to 1 ms delay. The maximum delay applicable is 100 ms. If delay not necessary the DELAY pin can be left floating.

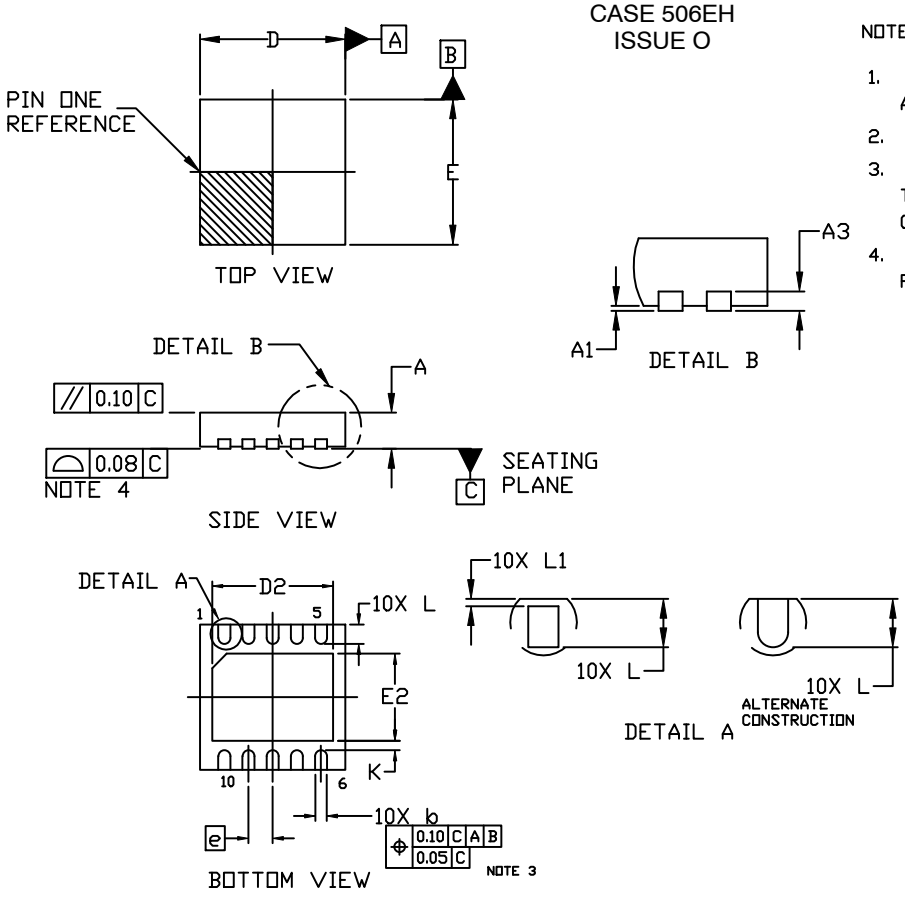
ORDERING INFORMATION

Device	ADJ / FIX version	Output Voltage $V_{OUT(NOM)}$	Output Discharge Version	Marking	Package	Shipping†
NCP59762AMN100TBG	FIX	1.0 V	Output Active Discharge	59762 P100A	DFN10 (Pb−Free)	3000 Tape & Reel
NCP59762AMN05ADJTBG	ADJ	0.5 V	Output Active Discharge	59762 P050A		
NCP59762AMN08ADJTBG	ADJ	0.8 V	Output Active Discharge	59762 P080A		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

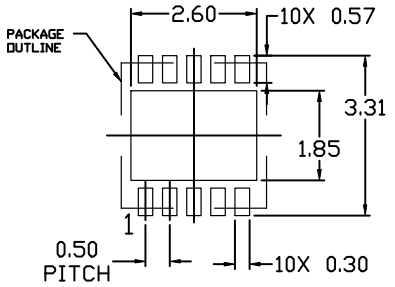
DFN10 3x3, 0.5P
CASE 506EH
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e	0.50 BSC		
K	0.20 REF		
L	0.30	0.40	0.50
L1	---	---	0.10



RECOMMENDED MOUNTING FOOTPRINT

PUBLICATION ORDERING INFORMATION

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