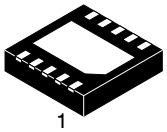
LDO Regulator, 3 A, High Accuracy (1%), Low Noise (4.3 μV_{RMS}), Low Dropout (70 mV)

NCP59763



DFN10, 3x3
CASE 506EH

The NCP59763 is a 3 A capable, low noise (4.3 μV_{RMS}), ultra low dropout (70 mV max. at 3 A), fast load transient response linear regulator (LDO) equipped with an NMOS pass transistor without the need of external bias voltage. The device output voltage is adjustable from 0.5 V to 2.0 V through the use of an external resistor divider and also available in fixed output versions.

The combination of high output current capability, ultra high PSRR across a wide frequency range and low noise makes this LDO ideal for powering noise sensitive high speed communication devices. Power sequencing application flexibility through enable pin, a user programmable soft–start and a user programmable delayed power good circuit. Very low dropout voltage (70 mV) and high output voltage accuracy (1%) enables low input voltage and higher power efficiency.

These set of features makes NCP59763 LDO an ideal solution for powering analog, digital and mixed signal high current demanding circuits like analog–to–digital converters (ADCs), digital–to–analog converters (DACs), high performance serializers and deserializers (SerDes), application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), digital signal processors (DSPs).

Features

- High Output Current 3 A
- High Accuracy ±1% Including Line/Load Regulation and Temperature Variation
- Input Voltage Range: 1.1 V to 3.6 V
- Adjustable and Fixed Output Voltage Options Available
  - Adj Voltage Range: 0.5 V to 2.0 V
  - Fixed: 0.5 V, 0.8 V, 1.0 V, 1.2 V
- Dropout Voltage: 70 mV Typ. at 3 A
- Very Low Output Voltage Noise: 4.3 μV_{RMS} Typ. (10 Hz – 100 kHz)
- Excellent Transient Response (20 mV Undershoot at 0.1–3 A Step)
- High PSRR: 70 dB
- Programmable Soft Start
- Open Drain Power Good Output with Programmable Delay
- DFN10 3.0 x 3.0 mm with Enhanced Thermal Performance
- Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

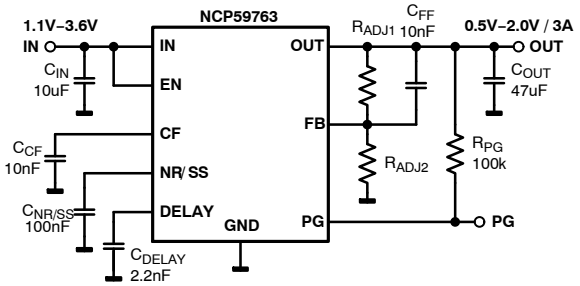


Figure 1. Typical Application Schematic

MARKING DIAGRAM

59763P = Specific Device Code
xxx = Output Voltage Version
y = Output Discharge Version
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 33 of this data sheet.

Typical Applications

- High Speed Analog VCO, ADC, DAC
- FPGAs, DSPs, SerDes
- Imaging Sensors and ASICs
- Communications, Test, Measurement

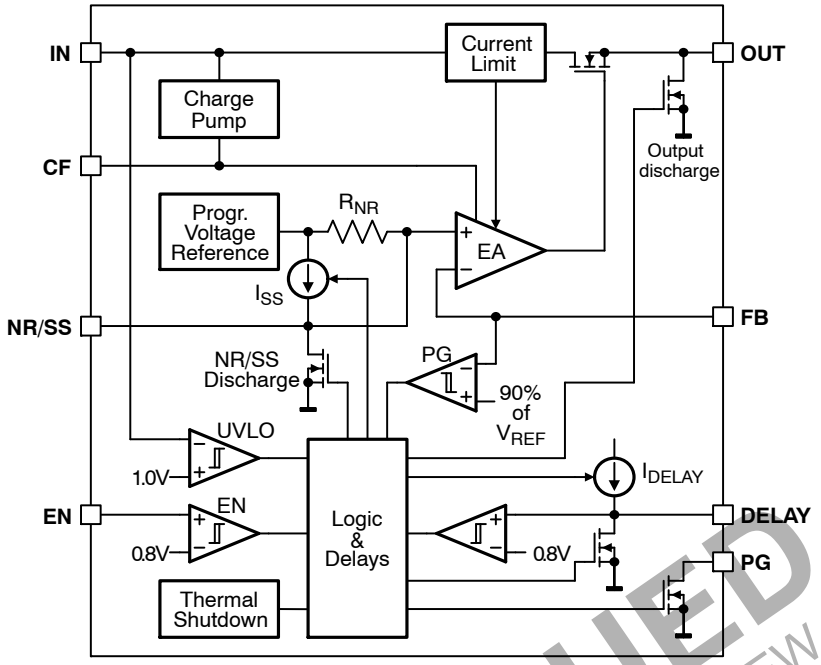


Figure 2. Simplified Schematic Block Diagram

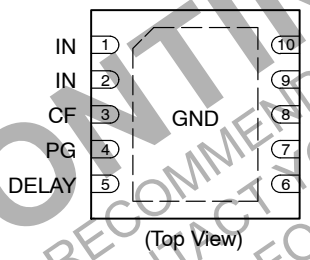


Figure 3. Pin Assignment

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1,2	IN	Input voltage supply pins.
3	CF	Internal supply filtering capacitor.
4	PG	Power−Good (PG) is an open−drain, active−high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high−impedance state. When V_{OUT} is below this threshold the pin is driven to a low−impedance state. A pull−up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply up to 3.6 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
5	DELAY	This pin is intended for adjusting the delay for signaling "V_{OUT} is OK" according to the user application needs. Capacitor connected from this pin to GND with capacitance of 2.2 nF corresponds to 1 ms delay. The maximum delay applicable is 100 ms. If delay not necessary the DELAY pin can be left floating.
6	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
7	NR/SS	Noise−reduction and soft−start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft−start function. Although not required, a 10 nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
8	FB	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. Connect this pin to OUT pin directly when output voltage adjustment is not needed (then the output voltage V_{OUT} will be equal to the nominal voltage V_{NOM}).
9,10	OUT	Regulated output voltage. It is recommended that the output capacitor effective capacitance ≥ 47 μF.
TAB	GND	Ground and thermal pad.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to +3.6	V
Enable Voltage Range	V_{EN}	−0.3 to +3.6	V
Power−Good Voltage Range	V_{PG}	−0.3 to +3.6	V
PG Sink Current	I_{PG}	0 to +5.0	mA
NR/SS Pin Voltage Range	$V_{NR/SS}$	Connecting to external voltage not allowed	V
CF Pin Voltage Range	V_{CF}	Connecting to external voltage not allowed	V
DELAY Pin Voltage Range	V_{DELAY}	Connecting to external voltage not allowed	V
FB Pin Voltage Range (Adjustable Devices)	V_{FB}	−0.3 to +3.6	V
Output Voltage Range	V_{OUT}	-0.3 to $(V_{IN} + 0.3) \leq 3.6$	V
Maximum Output Current	I_{OUT}	Internally Limited	
Output Short Circuit Duration		Indefinite	
Continuous Total Power Dissipation	P_D	See Thermal Characteristics Table and Formula	
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Junction Temperature Range	T_{STG}	−55 to +150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient (Note 4)	$R_{\theta JA}$	24	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	68	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 5)	$R_{\theta JC(bot)}$	3.0	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	3.3	°C/W
Characterization Parameter, Junction−to−Top	ψ_{JT}	1.3	°C/W
Characterization Parameter, Junction−to−Board	ψ_{JB}	3.3	°C/W

3. Thermal data based on thermal simulation methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:
   These data were generated with only a single device at the center of a high−K (2s2p) board with 3 in x 3 in copper area which follows the JEDEC51.7 guidelines. Top and bottom layer 2 oz. copper, inner planes 1 oz. copper.
   The GND pad connected to the PCB inner GND plane layer through a 3x5 thermal via array. All the vias are 0.3 mm diameter, plated.
4. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
5. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 6)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	1.1	3.6	V
Output Voltage	V_{OUT}	0.5	2.0	V
Power−Good Voltage	V_{PG}	0	3.6	V
Enable Voltage Range	V_{EN}	0	3.6	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS
At V_{IN} = 1.2 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V whichever is greater, V_{EN} = 1.1 V, FB connected to OUT, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{IN} = 10 μF, C_{OUT} = 47 μF, I_{OUT} = 50 mA, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. (Note 7, 8, 9, 10)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OUT}	Output voltage range	External resistor divider used		$V_{OUT(NOM)}$		2.0	V
	Output voltage accuracy (Note 11)	$V_{OUT(NOM)} \geq 0.8$ V	T_J = −40°C to 125°C	−1.0		1.0	%
		$V_{OUT(NOM)}$ < 0.8 V	T_J = −40°C to 100°C	−1.0		1.0	
			T_J = 100°C to 125°C	−2.0		1.0	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	$V_{IN} \geq 1.2$ V, $V_{IN} \geq (V_{OUT(NOM)} + 0.4$ V)			0.05		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 3 A			0.01		%/A
V_{DO}	IN−OUT dropout voltage	I_{OUT} = 3 A, V_{FB} = 0 V, V_{IN} = V_{OUT}, $V_{IN} \geq 1.2$ V			70	130	mV
I_{CL}	Output current limit	$V_{OUT} \geq 90\%$ x $V_{OUT(NOM)}$		3.2	4.0	5.2	A
$V_{UVLO-TH}$	Input voltage UVLO threshold	V_{IN} rising		0.85	1.00	1.15	V
$V_{UVLO-HYS}$	Input voltage UVLO hysteresis	V_{IN} falling			0.1		V
I_{GND}	Ground current	I_{OUT} = 0 to 3 A			1.1	1.8	mA
I_{SHDN}	Shutdown supply current	V_{EN} ≤ 0.4 V			1	15	μA
I_{FB}	FB pin current	V_{FB} = V_{OUT}		−250	10	250	nA
PSRR	Power supply rejection ratio	I_{OUT} = 1 A	1 kHz		70		dB
			10 kHz		50		
			500 kHz		35		
Noise	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 3 A			4.3		μV_{RMS}
dV_{OUT}/dI_{OUT}	Output voltage load transient response	I_{OUT} = 50 mA to 3 A at 1 A/μs			±17		mV
t_{START}	Minimum startup time (Note 12)	I_{OUT} = 3 A, NR/SS = open			200		μs
I_{SS}	Soft−start charging current	$V_{NR/SS}$ = 0 V	$V_{OUT(NOM)} \leq 0.9$ V		6.0		μA
			$V_{OUT(NOM)} > 0.9$ V		12.0		
R_{SS-DIS}	Soft−start discharging resistance	V_{IN} = 2.4 V, V_{SS} = 0.5 V			160		Ω
V_{EN-TH}	Enable input threshold	V_{EN} rising		0.4		0.9	V
V_{EN-HYS}	Enable pin hysteresis	V_{EN} falling			50		mV
I_{EN}	Enable pin current	V_{EN} = 3.6 V			0.3	1	μA
V_{PG-TH}	PG trip threshold	V_{OUT} falling		86.5	90	93.5	$\%V_{OUT(NOM)}$
V_{PG-HYS}	PG trip hysteresis	V_{OUT} rising			3		$\%V_{OUT(NOM)}$
V_{PG-LO}	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{PG-TH}				0.3	V
I_{PG-LK}	PG leakage current	V_{PG} = 3.6 V, V_{OUT} > V_{PG-TH}			0.01	1	μA

Table 5. ELECTRICAL CHARACTERISTICS
At V_{IN} = 1.2 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V whichever is greater, V_{EN} = 1.1 V, FB connected to OUT, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{IN} = 10 μF, C_{OUT} = 47 μF, I_{OUT} = 50 mA, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C. (Note 7, 8, 9, 10)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PG-DGL}	PG deglitch time			20		μs
I_{DELAY}	DELAY pin charging current	V_{DELAY} = 0 V		1.8		μA
$V_{DELAY-TH}$	DELAY trip threshold	V_{DELAY} rising		800		mV
$V_{DELAY-HYS}$	DELAY trip hysteresis	V_{DELAY} falling		30		mV
R_{AD}	Output Active Discharge Resistance	V_{EN} = 0 V, V_{IN} = 3.3 V, V_{OUT} = 2.0 V		100		Ω
TSD	Thermal shutdown temperature threshold high	Temperature rising		165		°C
	Thermal shutdown temperature threshold low	Temperature falling		140		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C.
8. $V_{OUT(NOM)}$ is the output voltage specified by OPN. It could be seen at the output pin when FB pin is connected to OUT pin directly (without resistor divider).
9. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
10. The device is not tested under conditions where the power dissipation is higher than the maximum rating of the package.
11. Additional test conditions: $V_{IN} \geq$ 1.2 V and $V_{IN} \geq (V_{OUT(NOM)}$ + 0.4 V), I_{OUT} = 50 mA to 3 A.
12. Minimum startup time is a time measured from EN rising edge to a point where V_{OUT} reaches 95% of V_{NOM}.

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

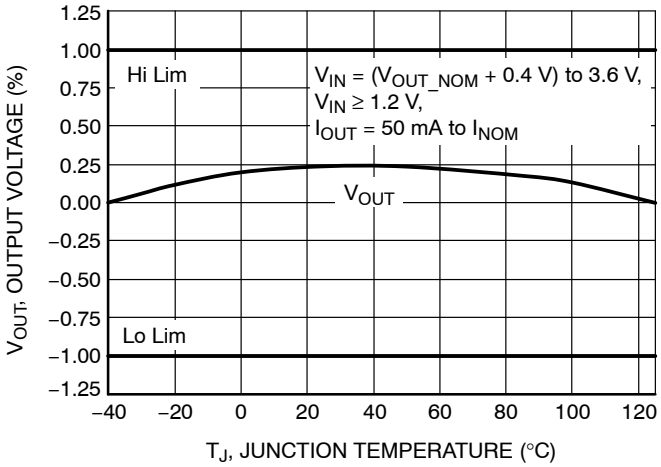


Figure 4. Output Voltage vs. Temperature

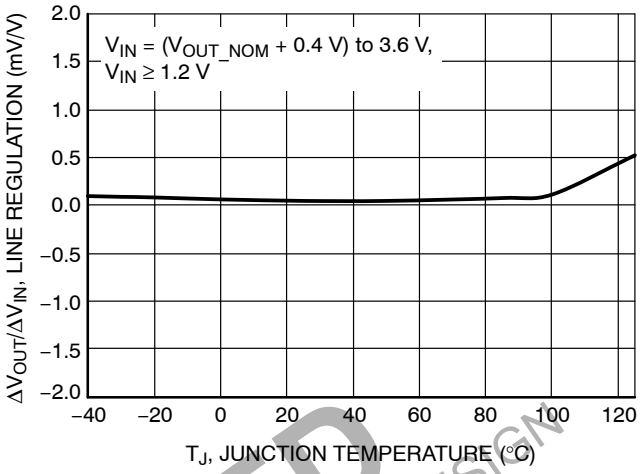


Figure 5. Line Regulation vs. Temperature

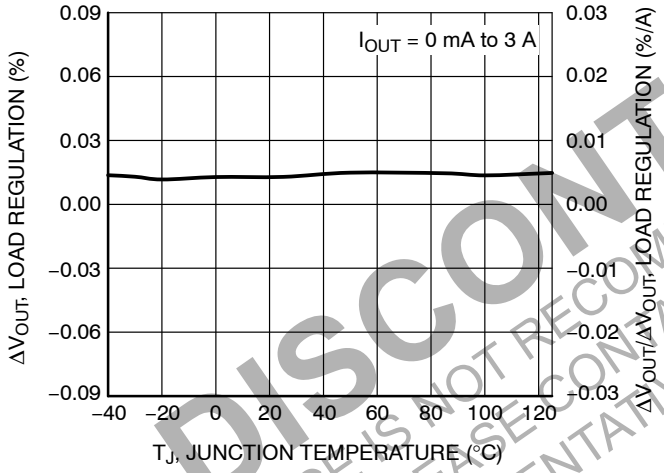


Figure 6. Load Regulation vs. Temperature

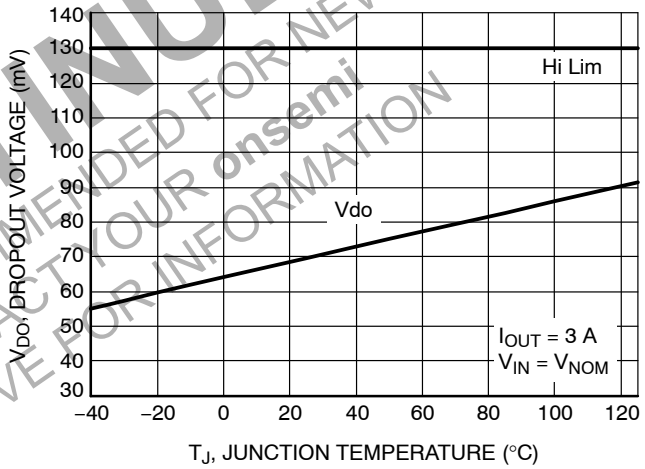


Figure 7. Dropout Voltage vs. Temperature

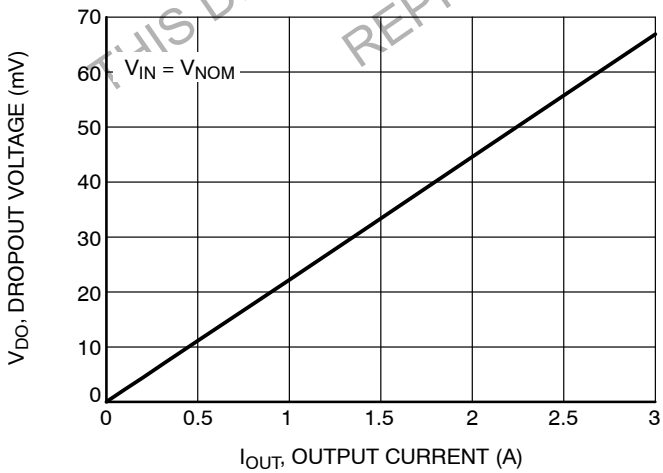


Figure 8. Dropout Voltage vs. Output Current, All Voltage Versions

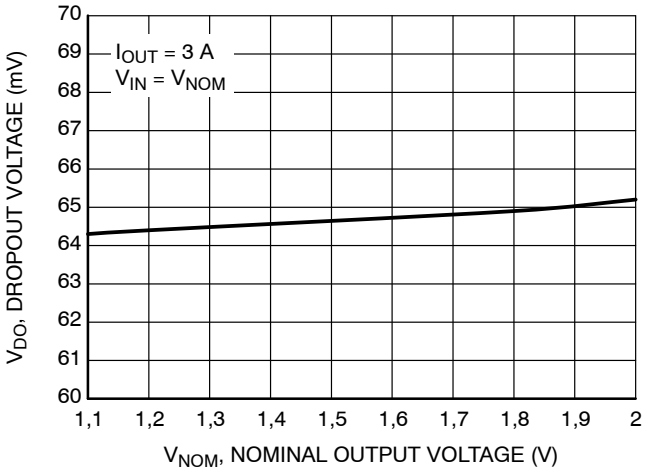


Figure 9. Dropout Voltage vs. V_{NOM}

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

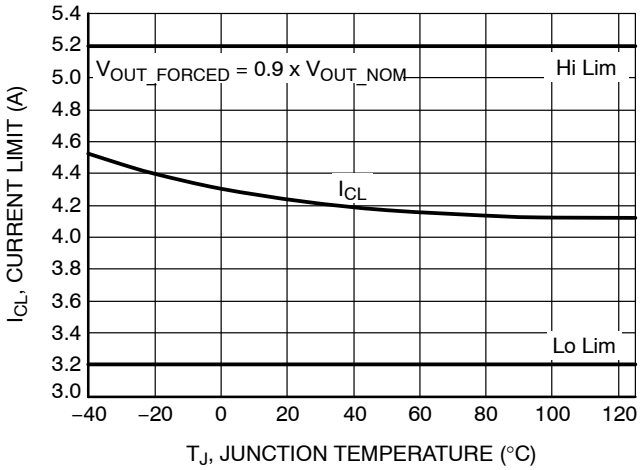


Figure 10. Current Limit vs. Temperature

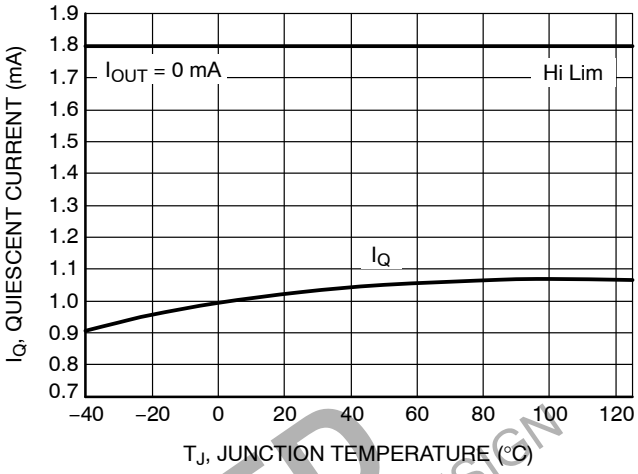


Figure 11. Quiescent Current vs. Temperature

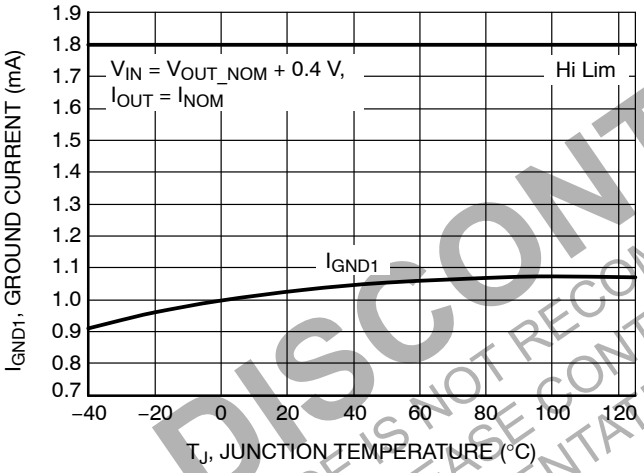


Figure 12. Ground Current vs. Temperature

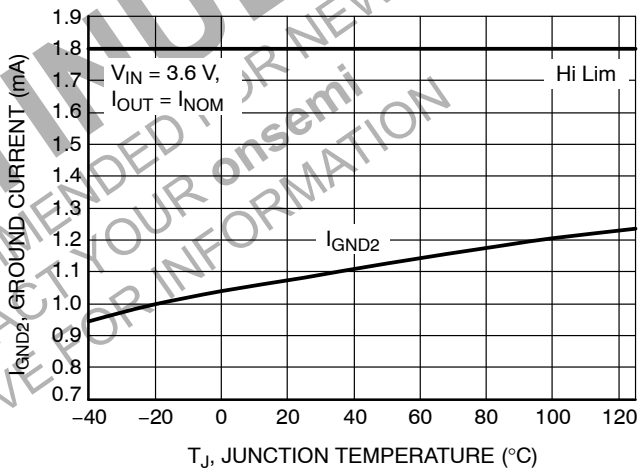


Figure 13. Ground Current vs. Temperature

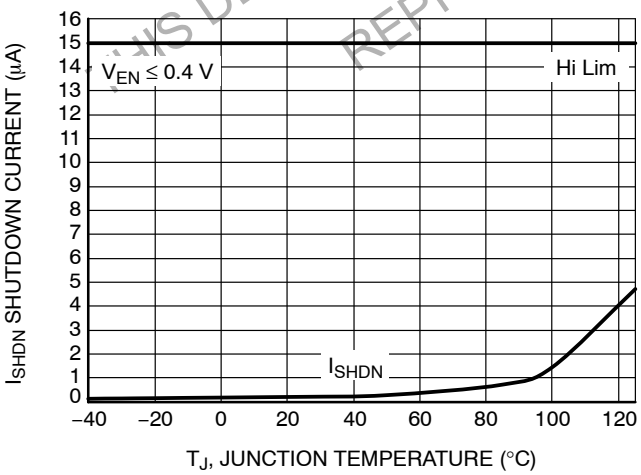


Figure 14. Shutdown Current vs. Temperature

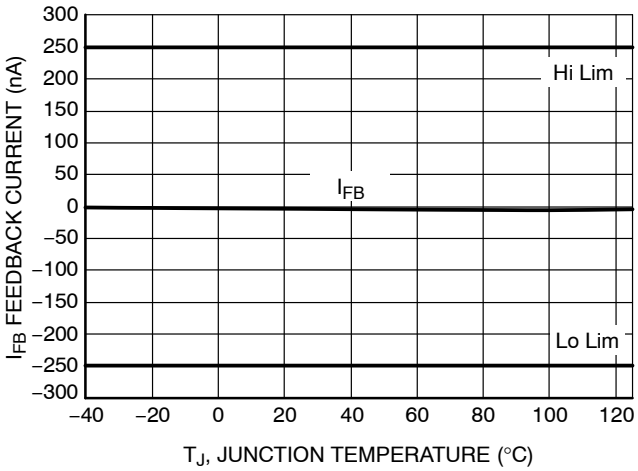


Figure 15. Feedback Current vs. Temperature

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

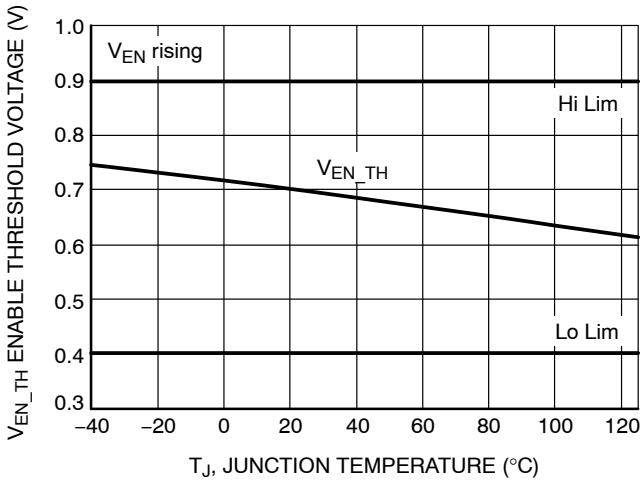


Figure 16. Enable Threshold Voltage vs. Temperature

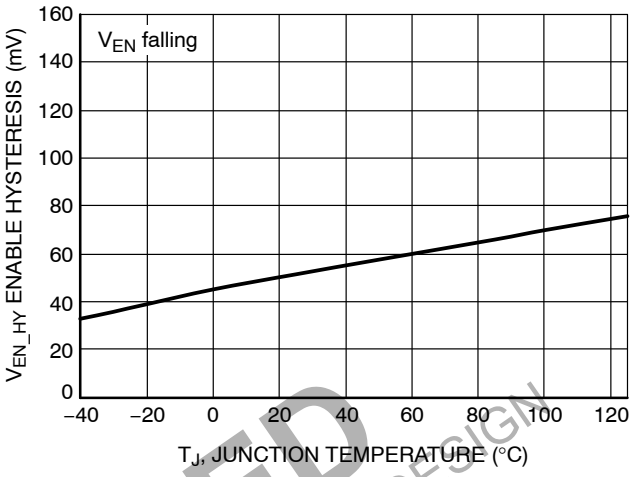


Figure 17. Enable Hysteresis vs. Temperature

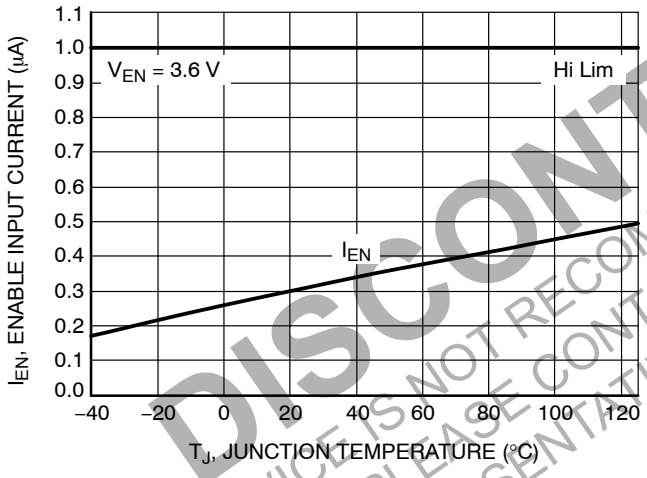


Figure 18. Enable Input Current vs. Temperature

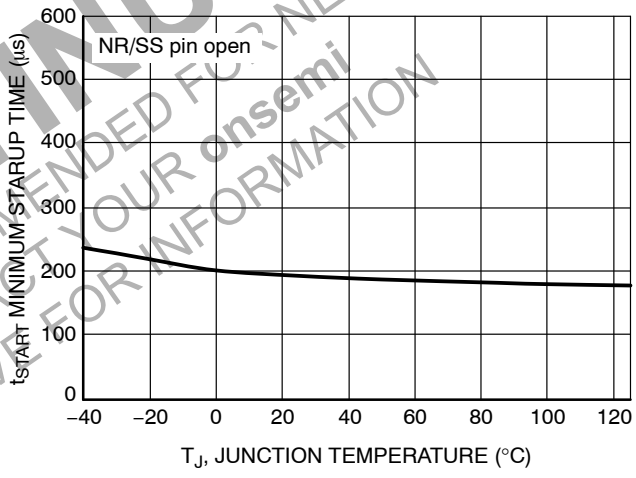


Figure 19. Minimum Startup Time vs. Temperature

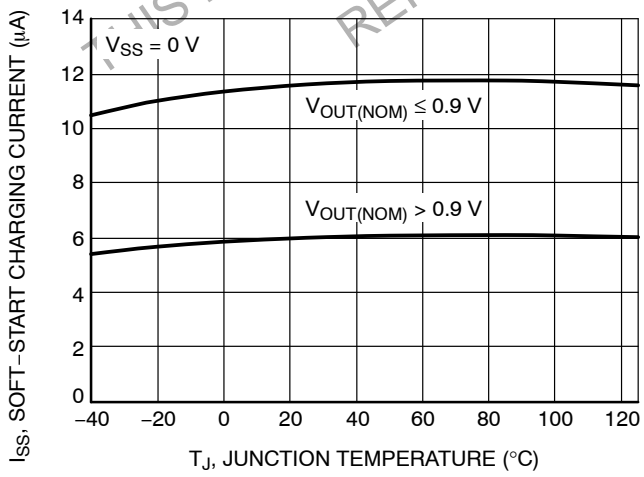


Figure 20. Soft−Start Charging Current vs. Temperature

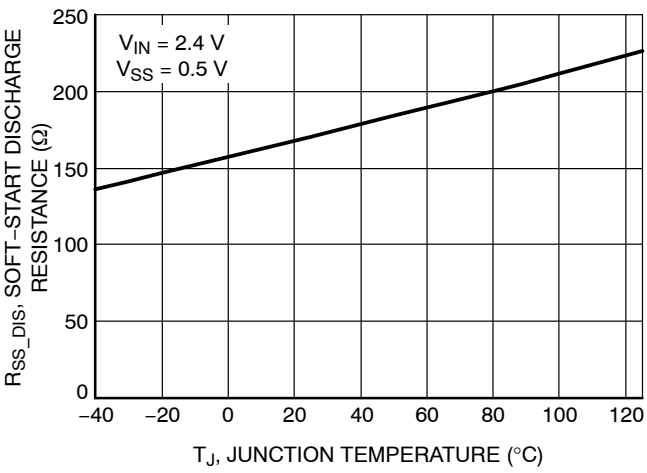


Figure 21. Soft−Start Discharging Resistance vs. Temperature

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

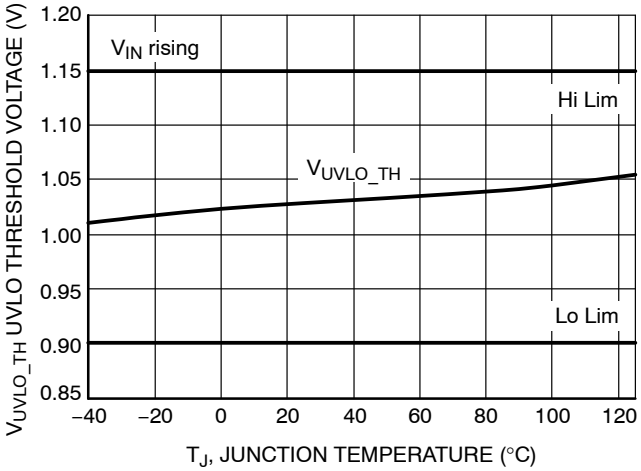


Figure 22. UVLO Threshold Voltage vs. Temperature

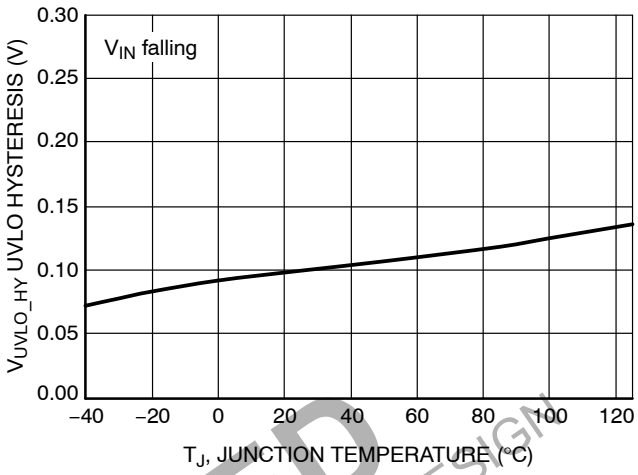


Figure 23. UVLO Hysteresis vs. Temperature

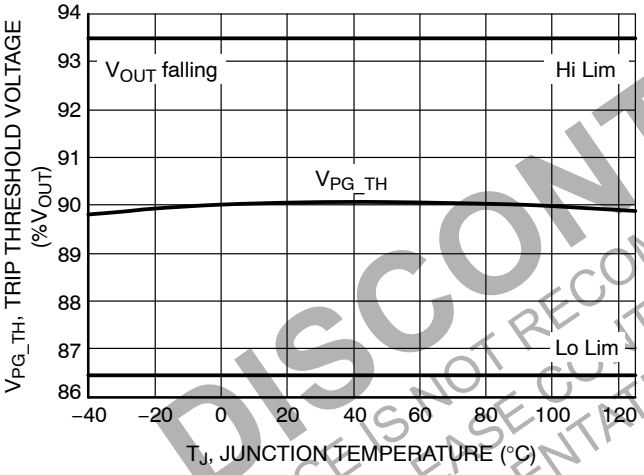


Figure 24. PG Trip Threshold Voltage vs. Temperature

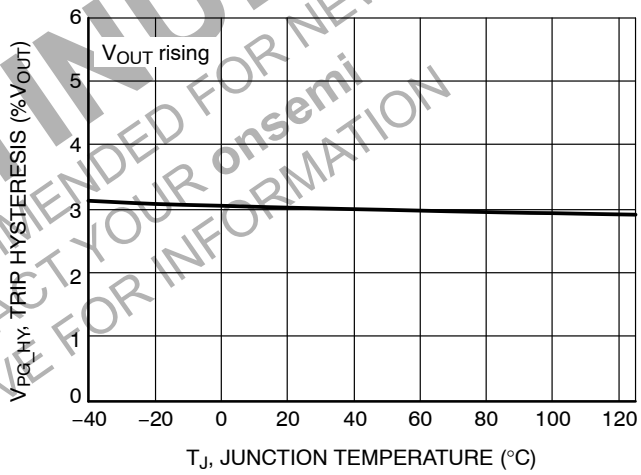


Figure 25. PG Trip Hysteresis vs. Temperature

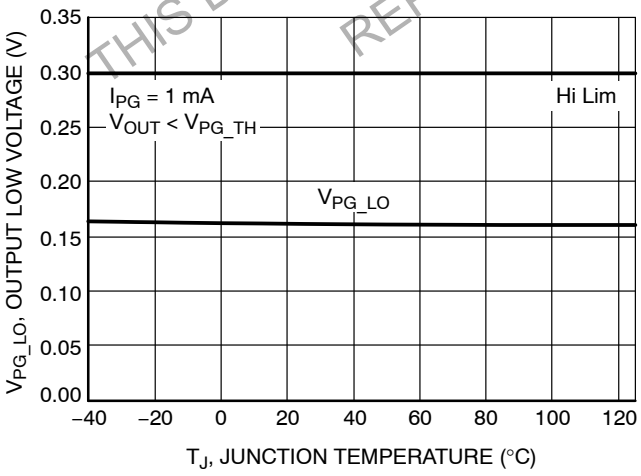


Figure 26. PG Output Low Voltage vs. Temperature

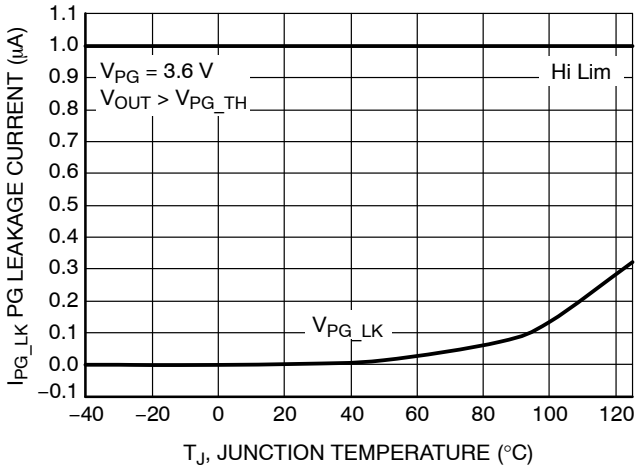


Figure 27. PG Leakage Current vs. Temperature

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 0.4 V and $V_{IN} \geq$ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

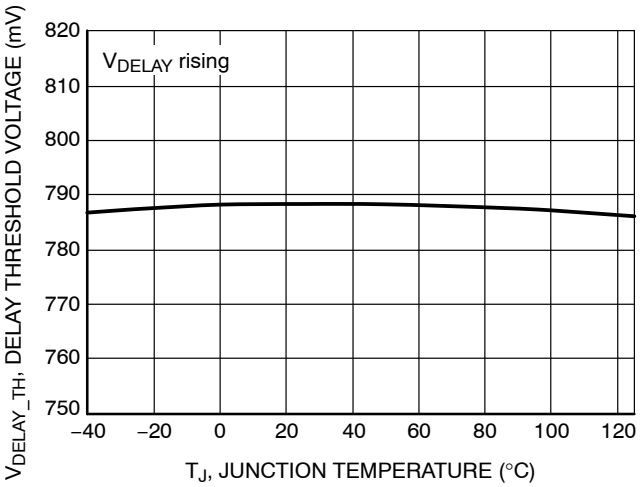


Figure 28. DELAY Threshold Voltage vs. Temperature

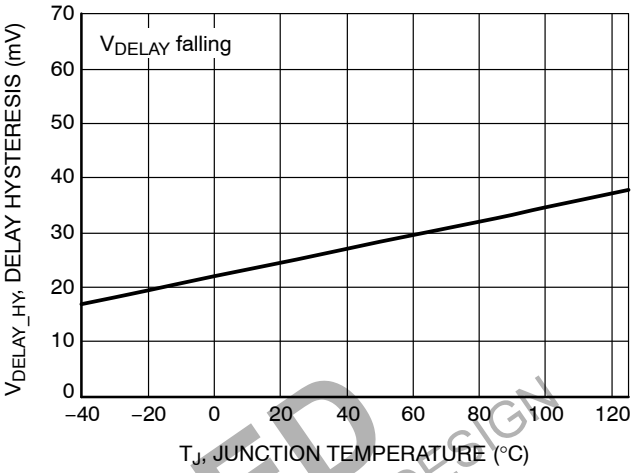


Figure 29. DELAY Hysteresis vs. Temperature

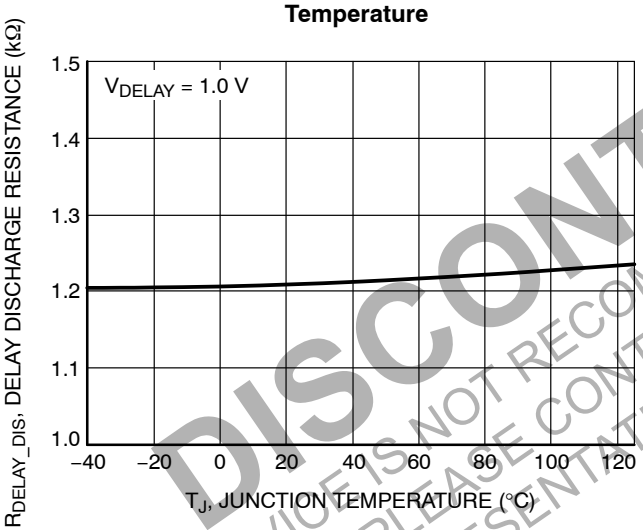


Figure 30. DELAY Discharging Resistance vs. Temperature

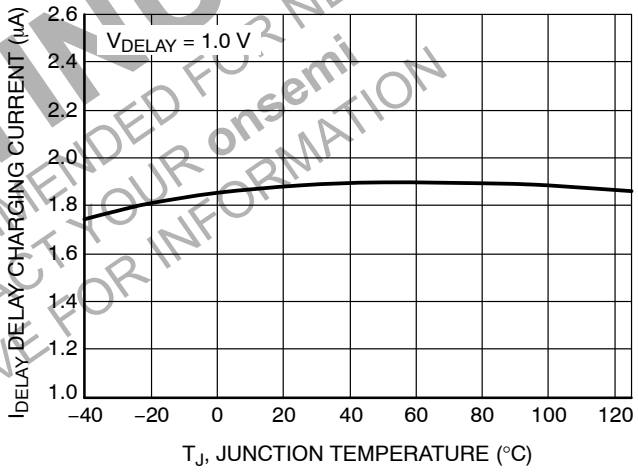


Figure 31. DELAY Charging Current vs. Temperature

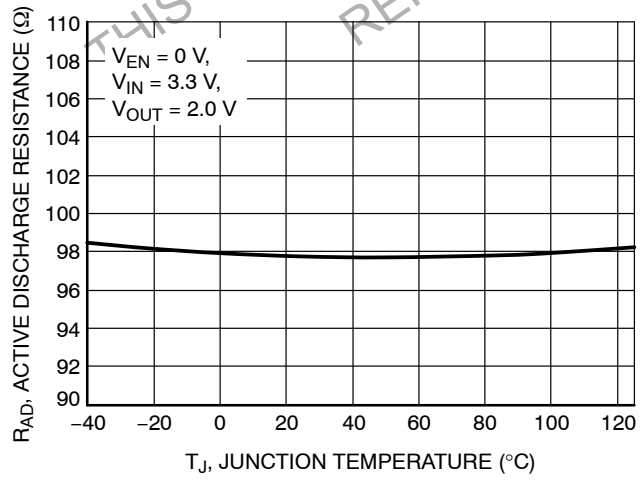


Figure 32. Active Dischare Resistance vs. Temperature

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

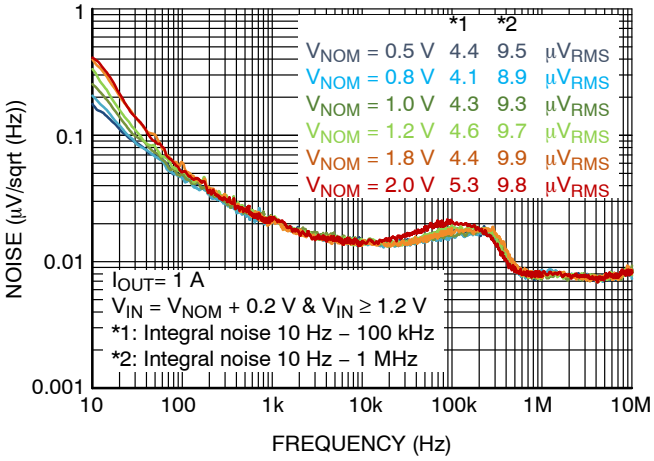


Figure 33. Output Noise Spectral Density vs. Device Voltage Version (V_{NOM}), FIX Application

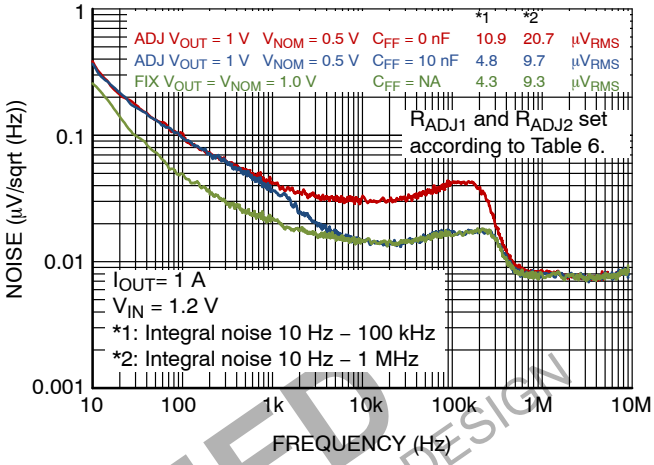


Figure 34. Output Noise Spectral Density of ADJ (w/ and w/o C_{FF}) and FIX Applications

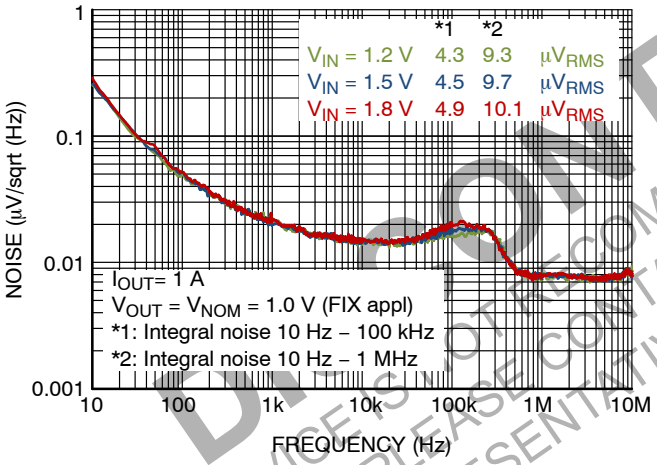


Figure 35. Output Noise Spectral Density vs. Input Voltage (V_{IN}), FIX Application

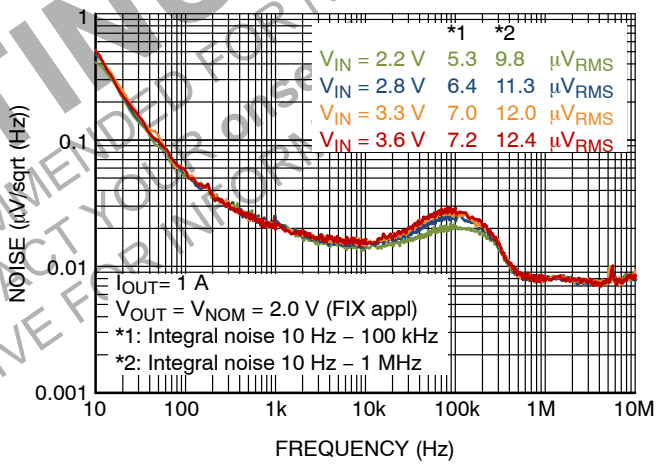


Figure 36. Output Noise Spectral Density vs. Input Voltage (V_{IN}), FIX Application

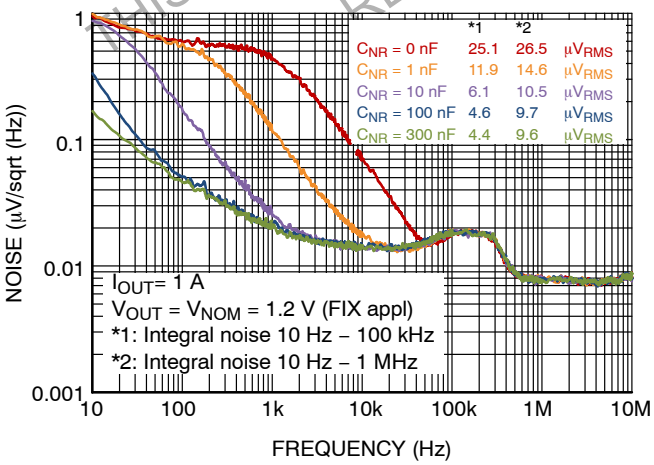


Figure 37. Output Noise Spectral Density vs. Noise Reduction Capacitor (C_{NR}), FIX Application

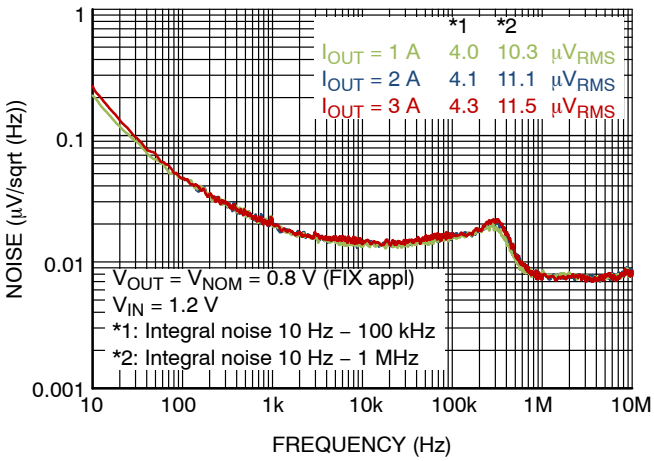


Figure 38. Output Noise Spectral Density vs. Load Current, V_{NOM} = 0.8 V, FIX Application

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

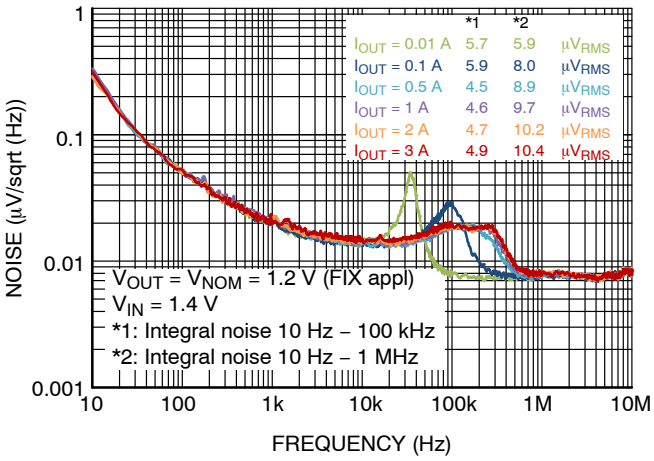


Figure 39. Output Noise Spectral Density vs. Load Current, V_{NOM} = 1.2 V, FIX Application

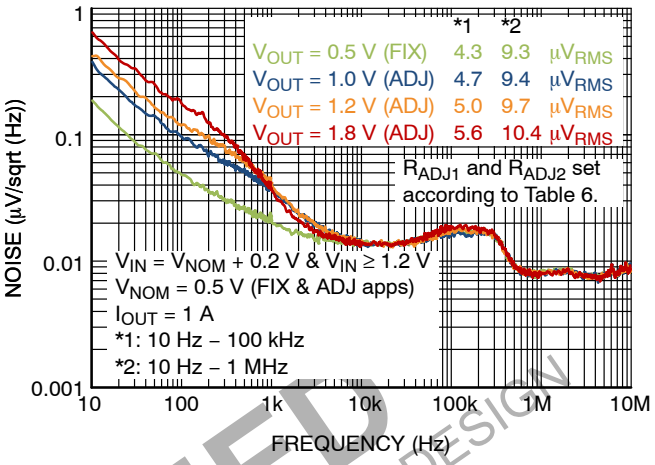


Figure 40. Output Noise Spectral Density vs. V_{OUT}, V_{NOM} = 0.5 V, FIX & ADJ Applications

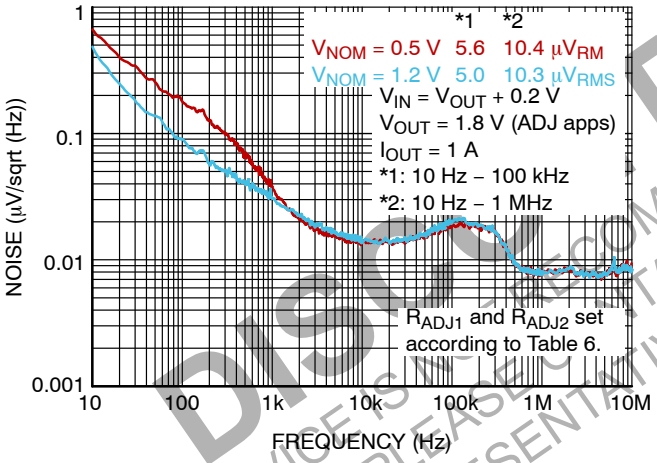


Figure 41. Output Noise Spectral Density vs. V_{NOM}, V_{OUT} = 1.8 V, ADJ Application

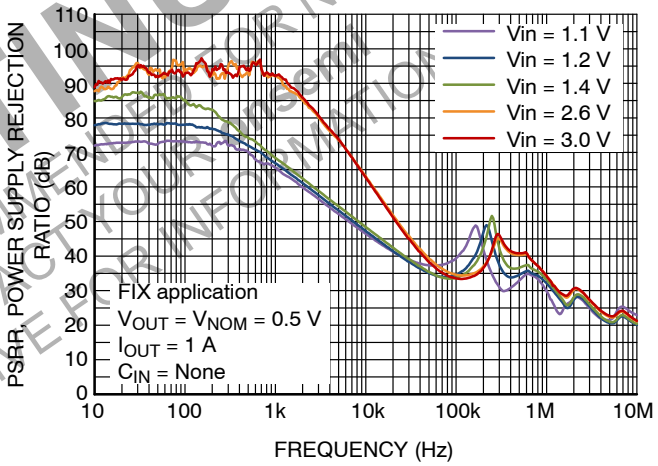


Figure 42. PSRR vs. Frequency and V_{IN}, V_{NOM} = 0.5V, FIX Application

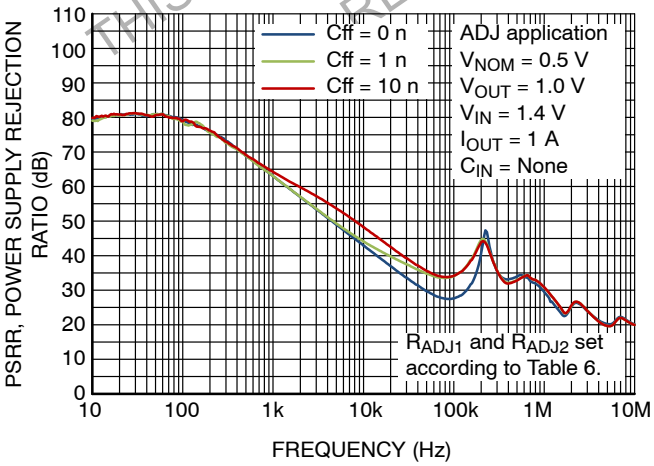


Figure 43. PSRR vs. Frequency and C_{FF}, V_{NOM} = 0.5 V, ADJ Application

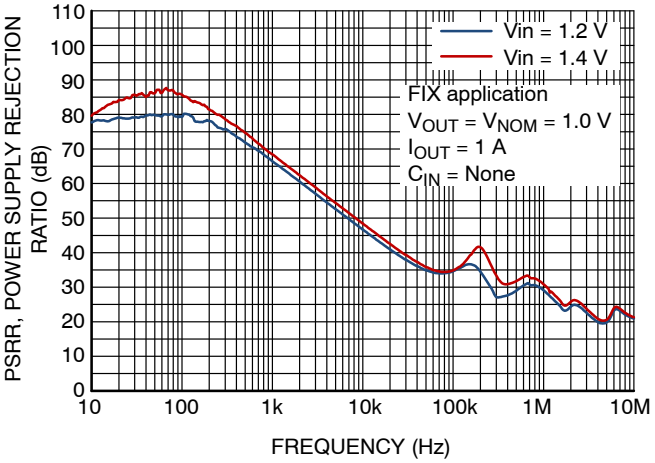


Figure 44. PSRR vs. Frequency and V_{IN}, V_{NOM} = 1.0 V, FIX Application

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

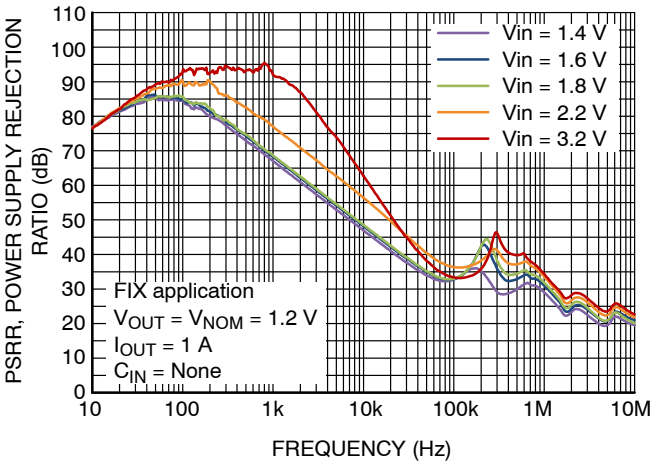


Figure 45. PSRR vs. Frequency and V_{IN}, V_{NOM} = 1.2 V, FIX Application

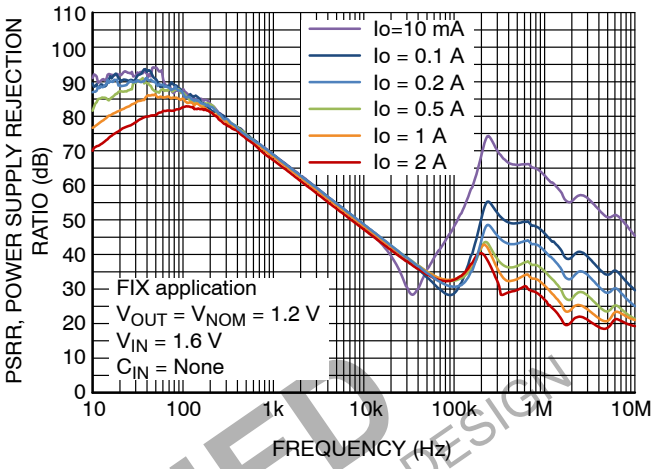


Figure 46. PSRR vs. Frequency and I_{OUT}, V_{NOM} = 1.2 V, FIX Application

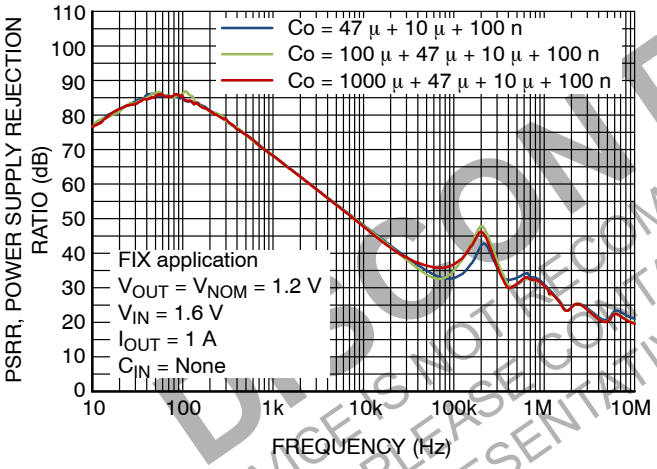


Figure 47. PSRR vs. Frequency and C_{OUT}, V_{NOM} = 1.2 V, FIX Application

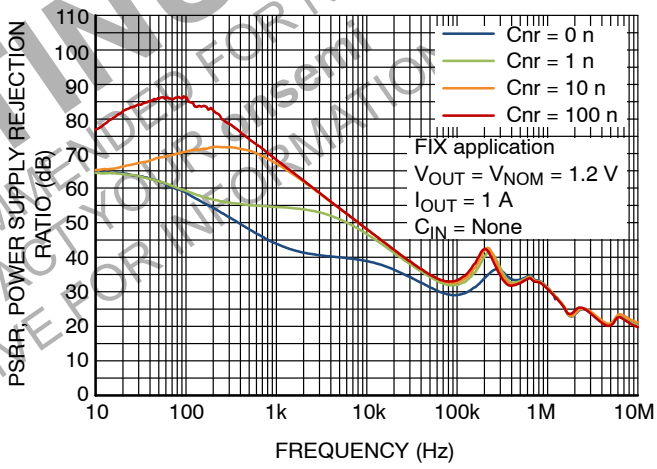


Figure 48. PSRR vs. Frequency and $C_{NR/SS}$, V_{NOM} = 1.2 V, FIX Application

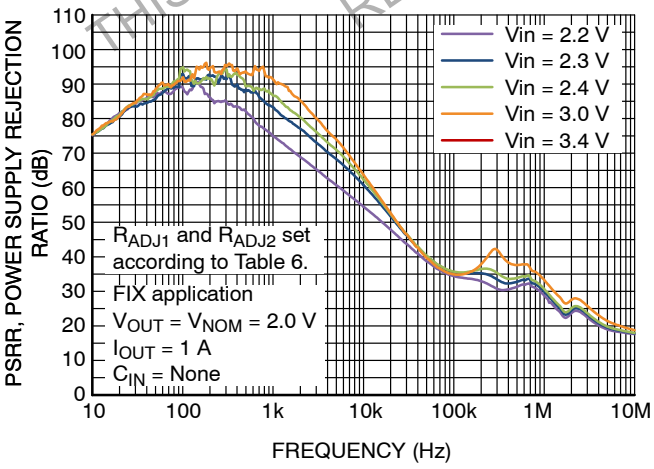


Figure 49. PSRR vs. Frequency and V_{IN}, V_{NOM} = 2.0 V, FIX Application

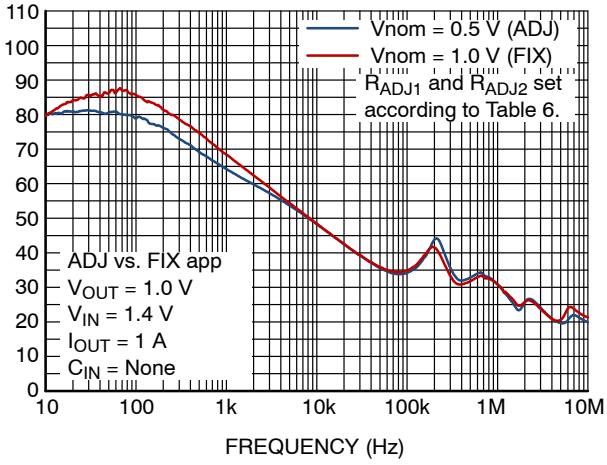


Figure 50. PSRR vs. Frequency of FIX (1.0 V) and ADJ (0.5 V set to 1.0 V) Applications

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

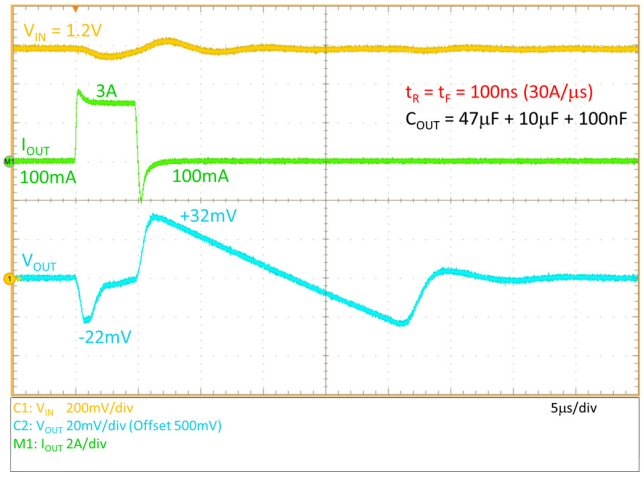


Figure 51. Load Transient Response, FIX−0.5V

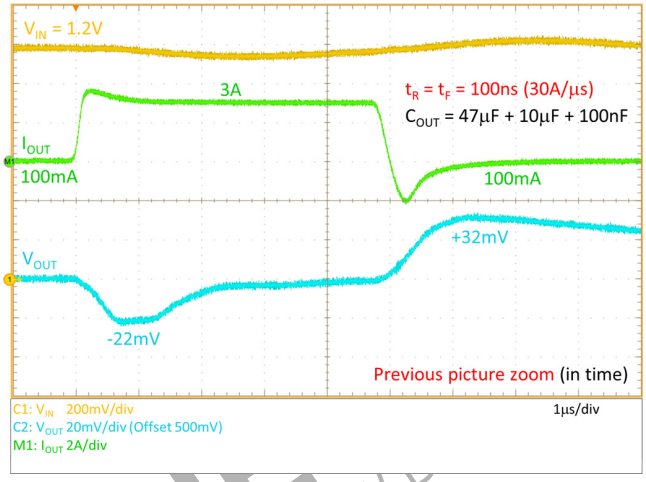


Figure 52. Load Transient Response, FIX−0.5V

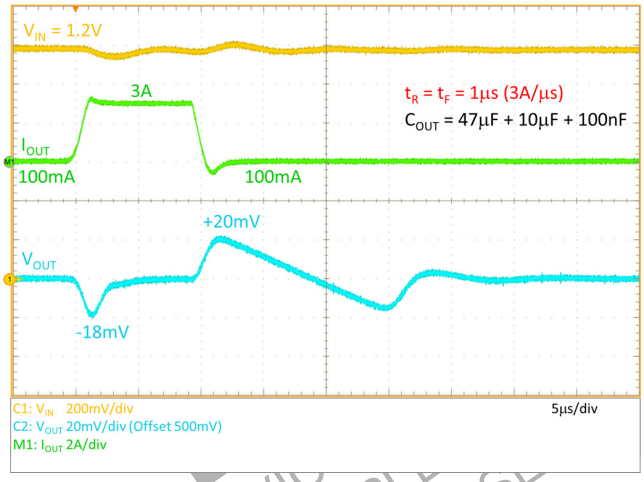


Figure 53. Load Transient Response, FIX−0.5V

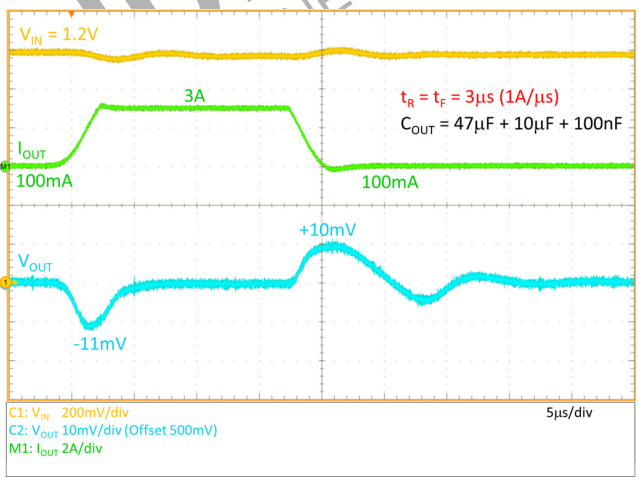


Figure 54. Load Transient Response, FIX−0.5V

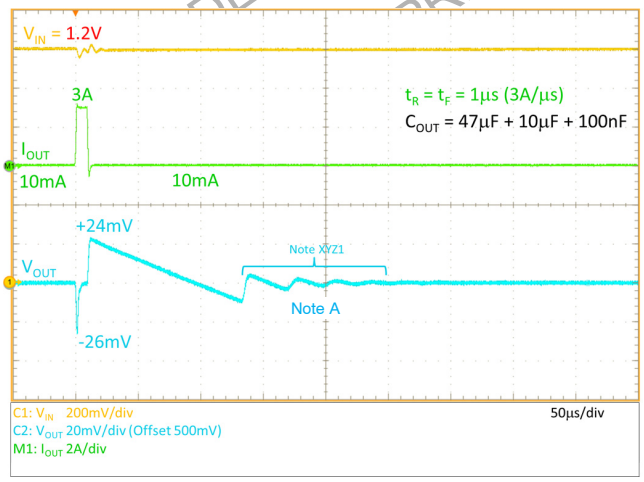


Figure 55. Load Transient Response, FIX−0.5V

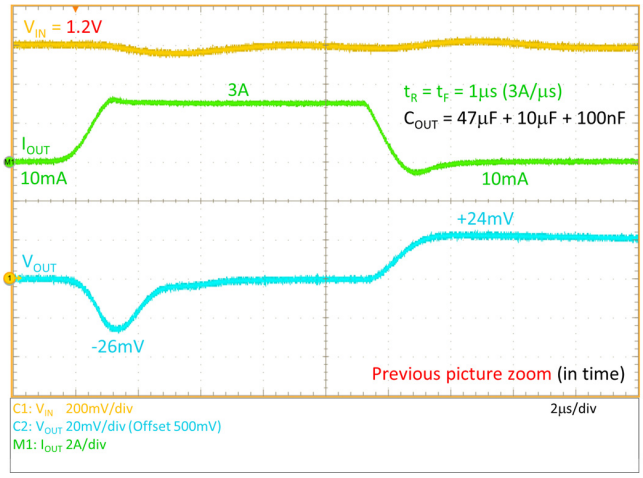


Figure 56. Load Transient Response, FIX−0.5V

Note A: The V_{OUT} cycling after transient going from high to idle (low) load current is not a feedback loop oscillation, it is just a combination of two different actions: small overshoot above $V_{OUT-NOM}$ (caused by limited error amp speed and light load condition at once) what is LDO related and slow C_{OUT} discharging by the light load current, what is related to C_{OUT} and idle I_{OUT} only. Bigger C_{OUT} capacitor value and lower idle state load current makes the cycling amplitude and count higher.

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

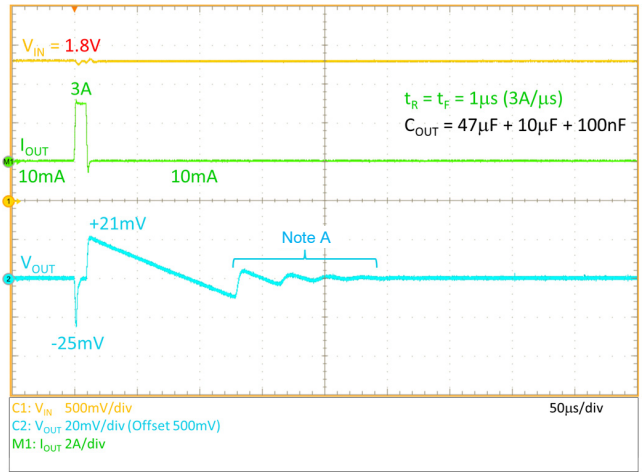


Figure 57. Load Transient Response, FIX−0.5V

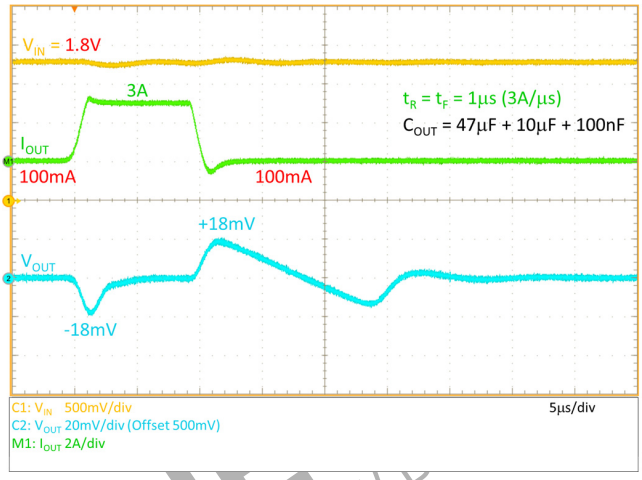


Figure 58. Load Transient Response, FIX−0.5V

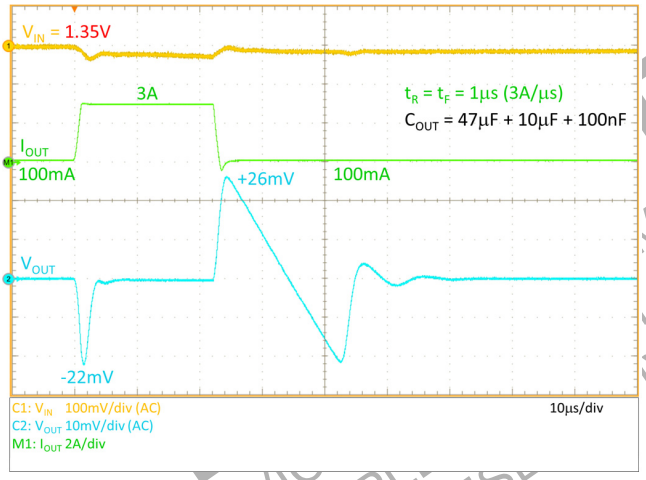


Figure 59. Load Transient Response, FIX−1.2V

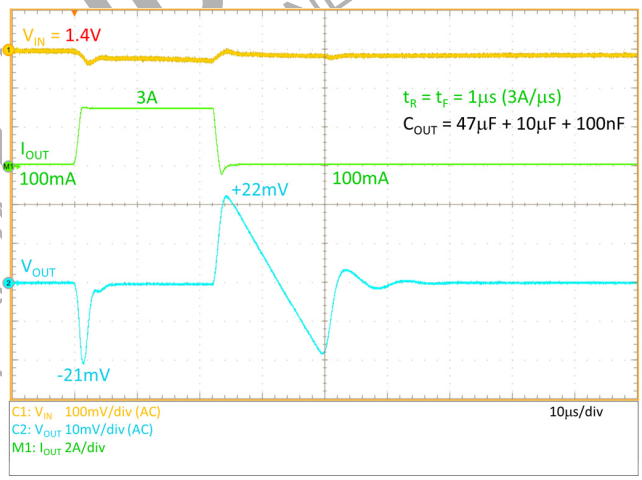


Figure 60. Load Transient Response, FIX−1.2V

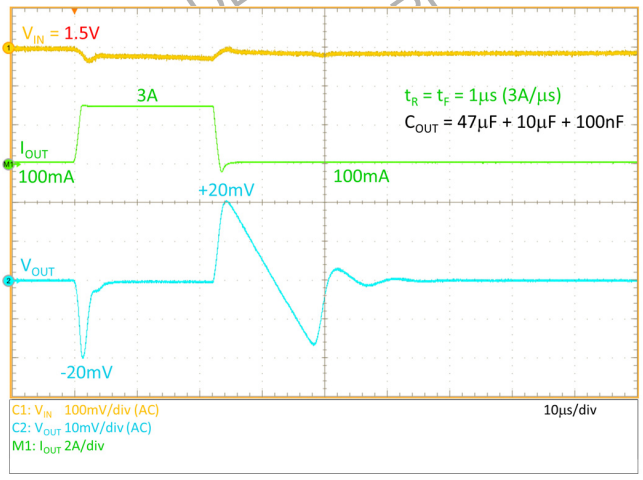


Figure 61. Load Transient Response, FIX−1.2V

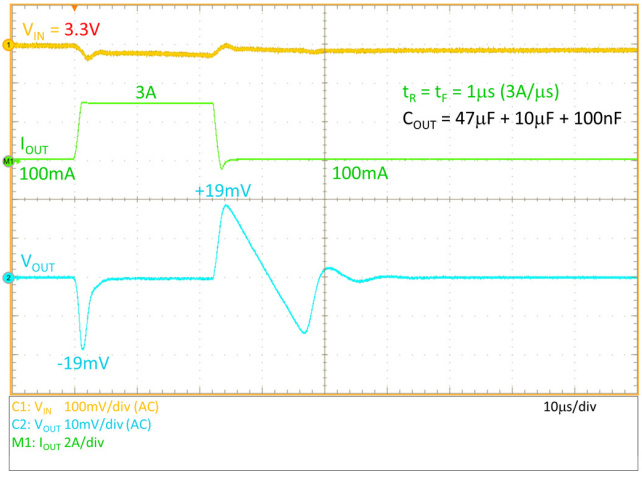


Figure 62. Load Transient Response, FIX−1.2V

Note A: The V_{OUT} cycling after transient going from high to idle (low) load current is not a feedback loop oscillation, it is just a combination of two different actions: small overshoot above $V_{OUT-NOM}$ (caused by limited error amp speed and light load condition at once) what is LDO related and slow C_{OUT} discharging by the light load current, what is related to C_{OUT} and idle I_{OUT} only. Bigger C_{OUT} capacitor value and lower idle state load current makes the cycling amplitude and count higher.

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

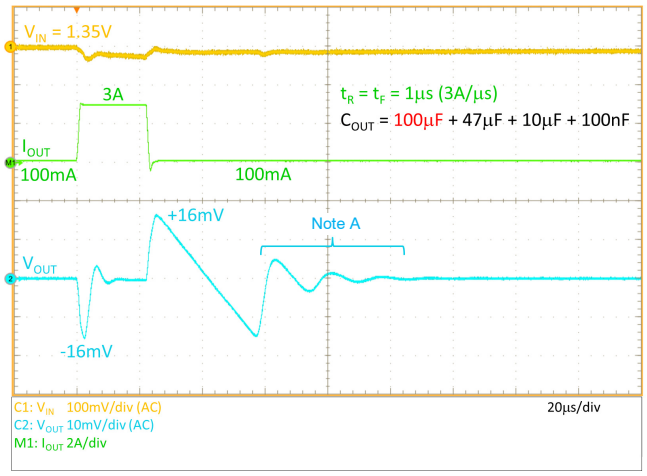


Figure 63. Load Transient Response, FIX−1.2V

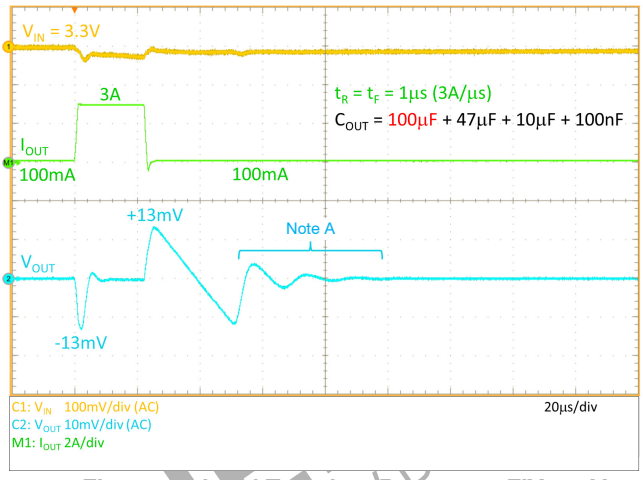


Figure 64. Load Transient Response, FIX−1.2V

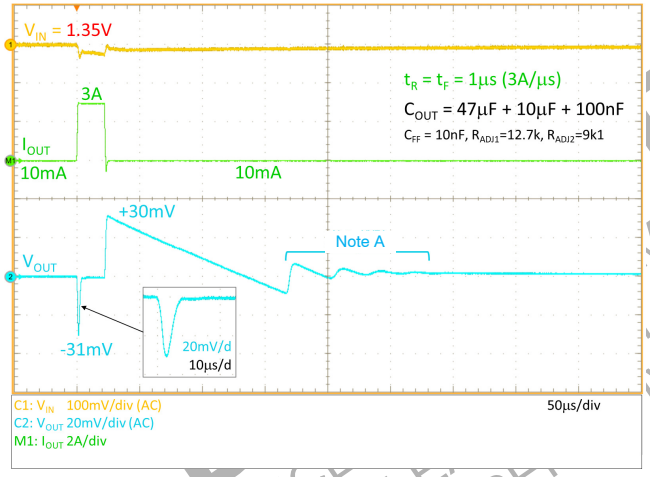


Figure 65. Load Transient Response, ADJ−0.5V set to 1.2V

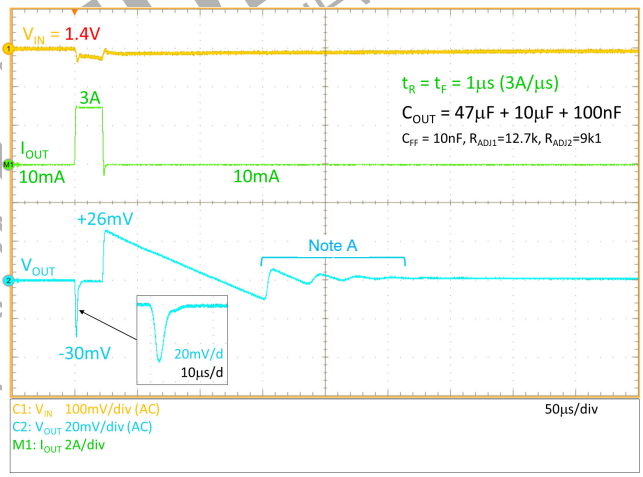


Figure 66. Load Transient Response, ADJ−0.5V set to 1.2V

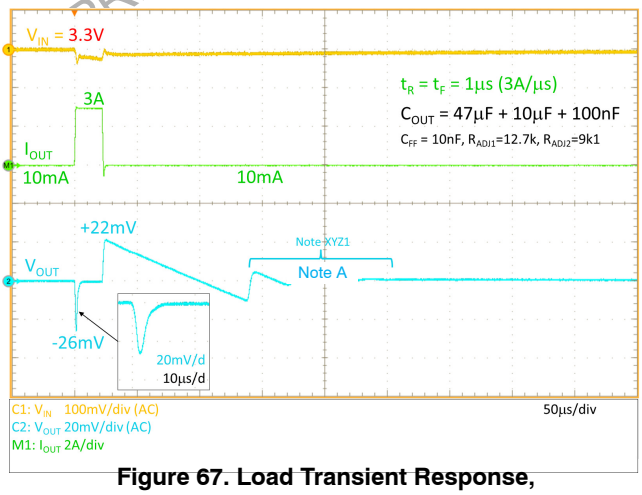


Figure 67. Load Transient Response, ADJ−0.5V set to 1.2V

Note A: The V_{OUT} cycling after transient going from high to idle (low) load current is not a feedback loop oscillation, it is just a combination of two different actions: small overshoot above $V_{OUT-NOM}$ (caused by limited error amp speed and light load condition at once) what is LDO related and slow C_{OUT} discharging by the light load current, what is related to C_{OUT} and idle I_{OUT} only. Bigger C_{OUT} capacitor value and lower idle state load current makes the cycling amplitude and count higher.

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

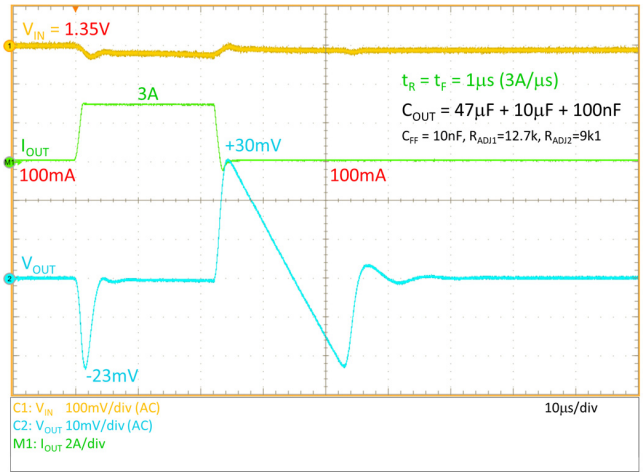


Figure 68. Load Transient Response, ADJ−0.5V set to 1.2V

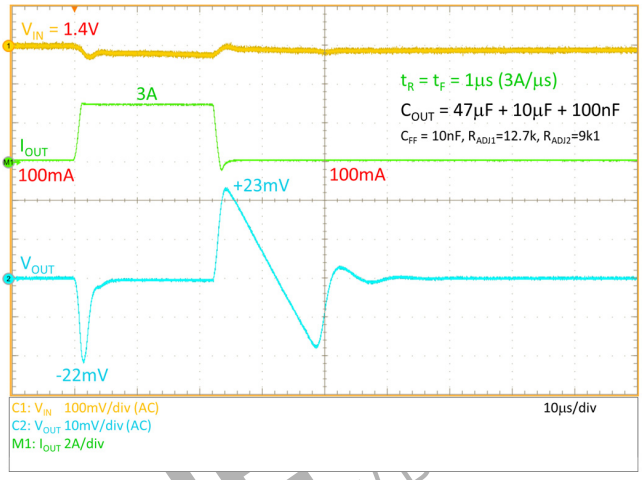


Figure 69. Load Transient Response, ADJ−0.5V set to 1.2V

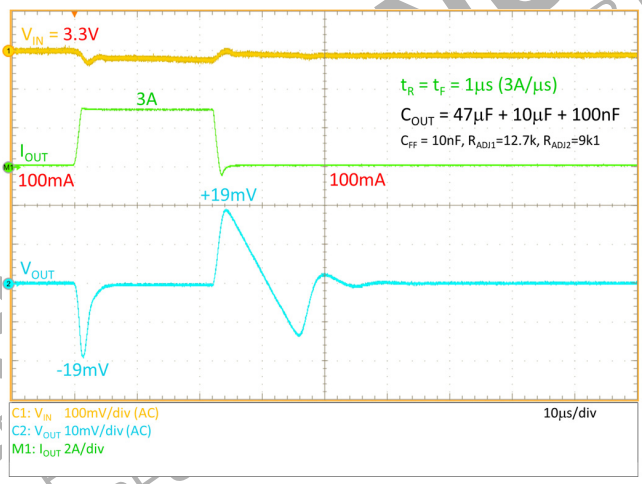


Figure 70. Load Transient Response, ADJ−0.5V set to 1.2V

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

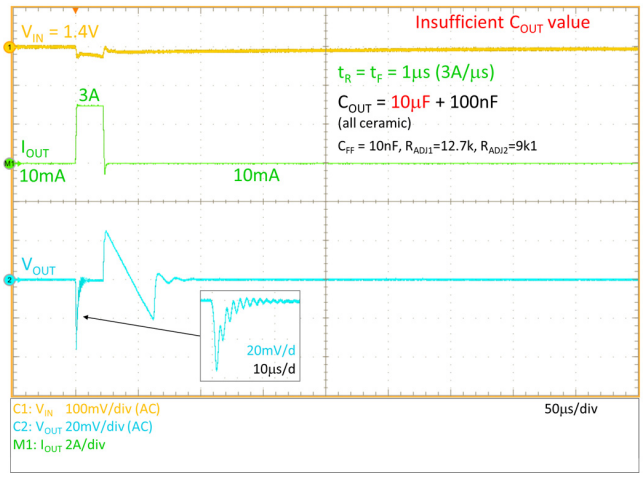


Figure 71. Load Transient Response, ADJ−0.5V set to 1.2V

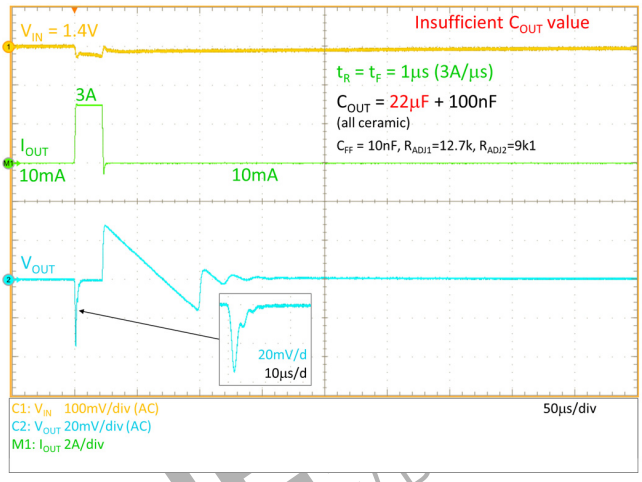


Figure 72. Load Transient Response, ADJ−0.5V set to 1.2V

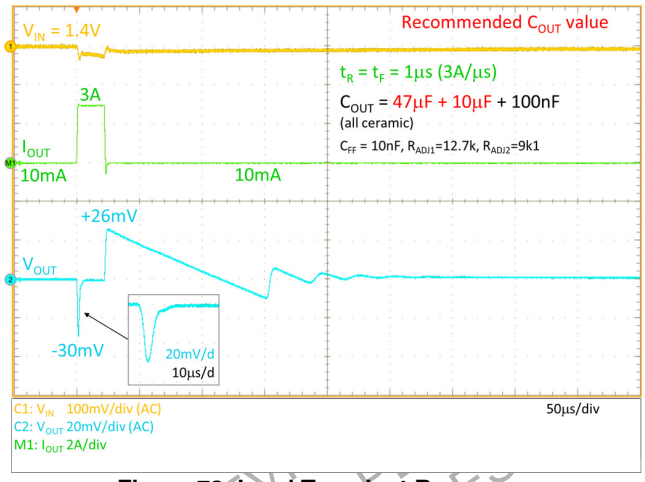


Figure 73. Load Transient Response, ADJ−0.5V set to 1.2V

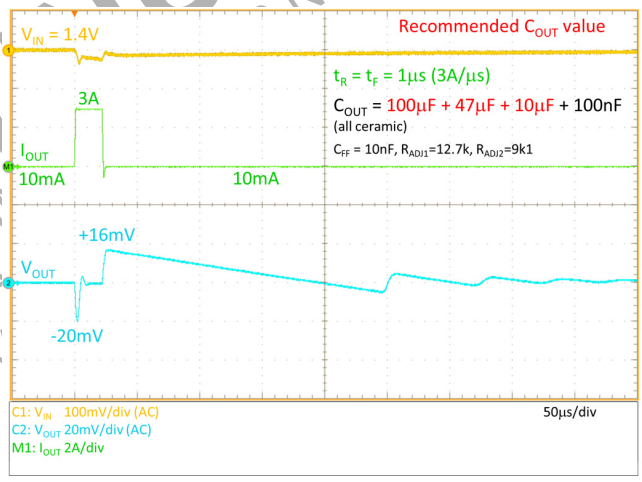


Figure 74. Load Transient Response, ADJ−0.5V set to 1.2V

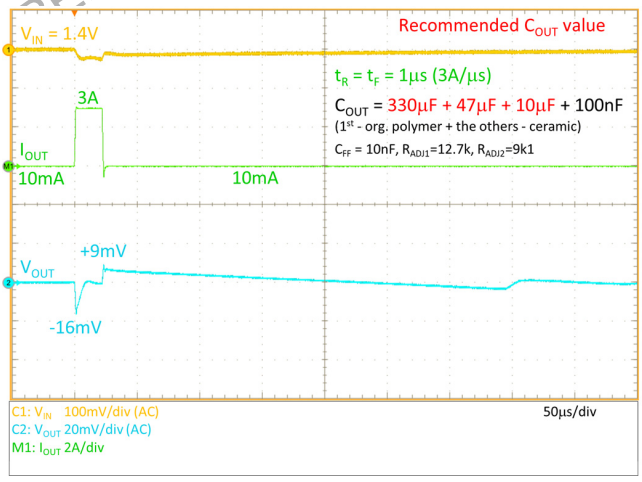


Figure 75. Load Transient Response, ADJ−0.5V set to 1.2V

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

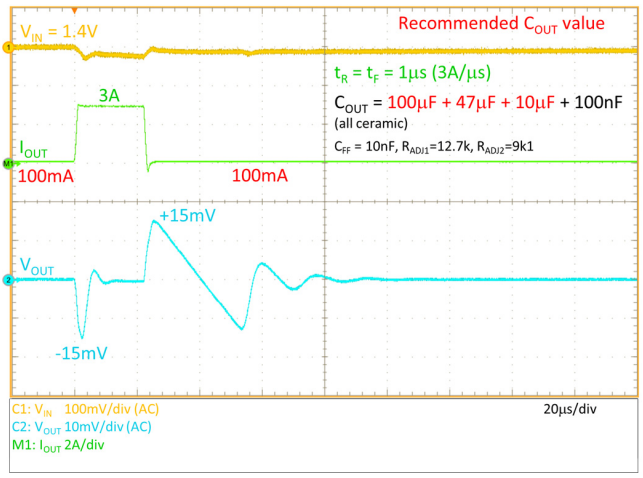


Figure 76. Load Transient Response, ADJ−0.5V set to 1.2V

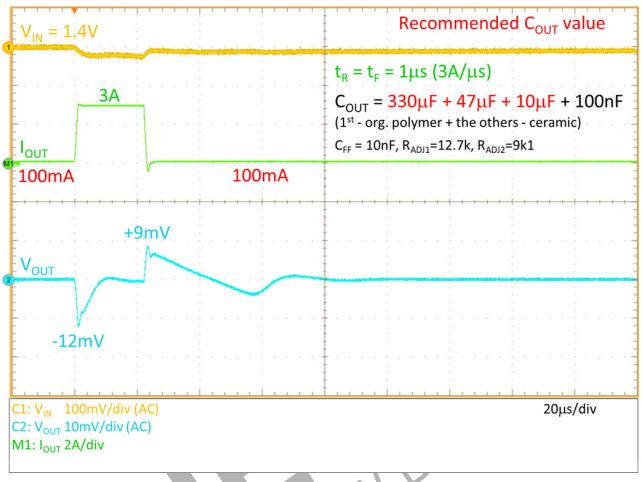


Figure 77. Load Transient Response, ADJ−0.5V set to 1.2V

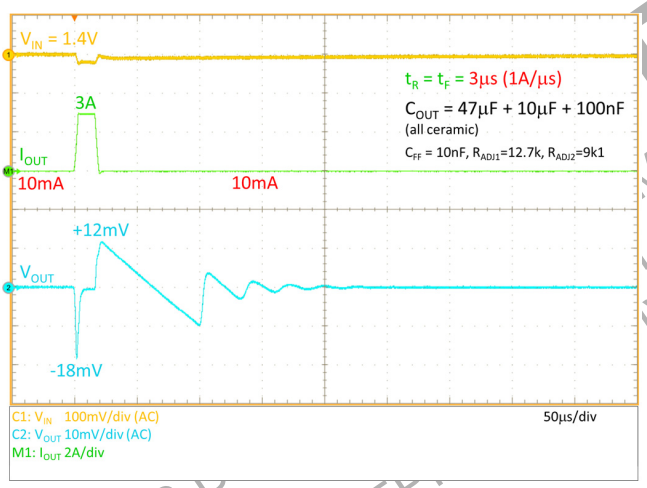


Figure 78. Load Transient Response, ADJ−0.5V set to 1.2V

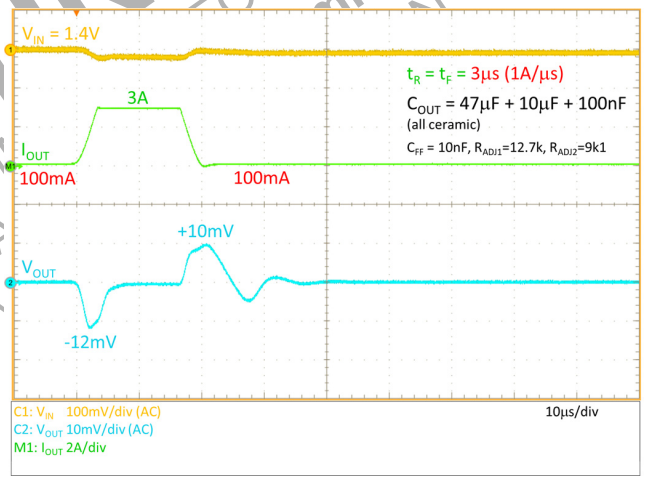


Figure 79. Load Transient Response, ADJ−0.5V set to 1.2V

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

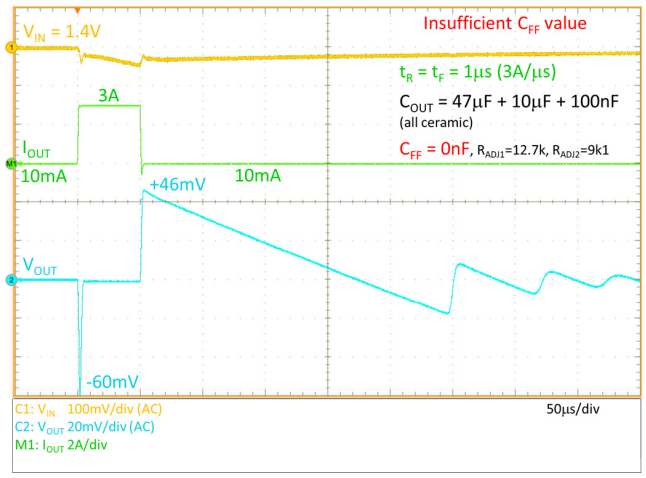


Figure 80. Load Transient Response, ADJ−0.5V set to 1.2V

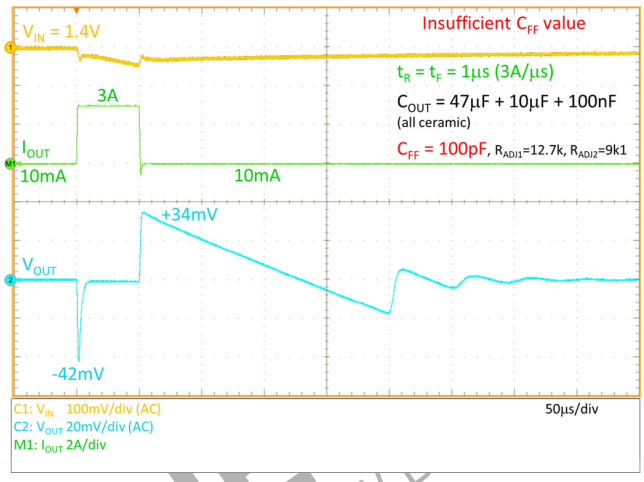


Figure 81. Load Transient Response, ADJ−0.5V set to 1.2V

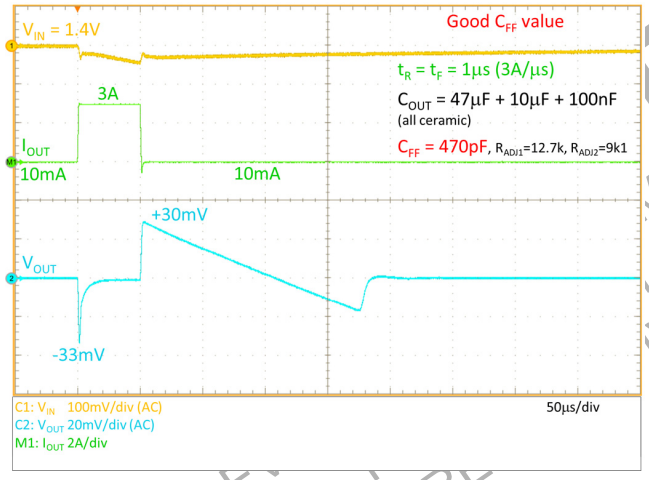


Figure 82. Load Transient Response, ADJ−0.5V set to 1.2V

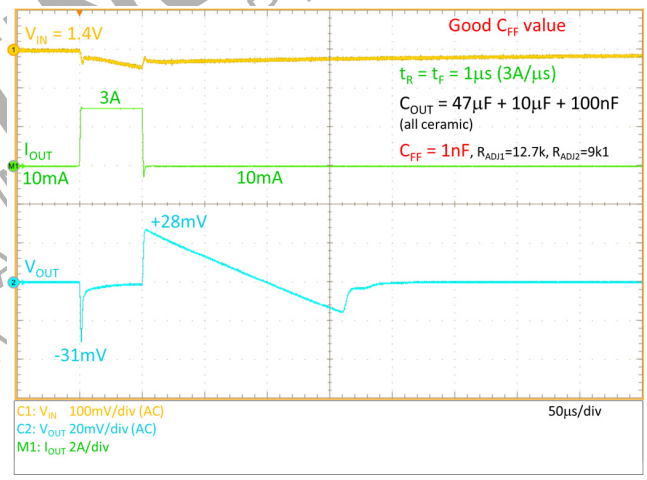


Figure 83. Load Transient Response, ADJ−0.5V set to 1.2V

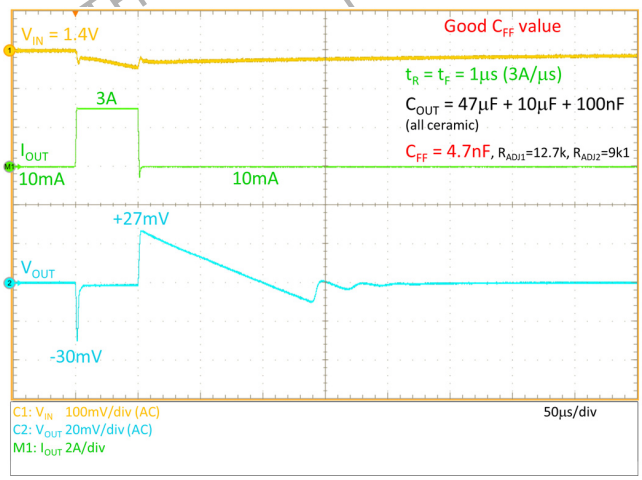


Figure 84. Load Transient Response, ADJ−0.5V set to 1.2V

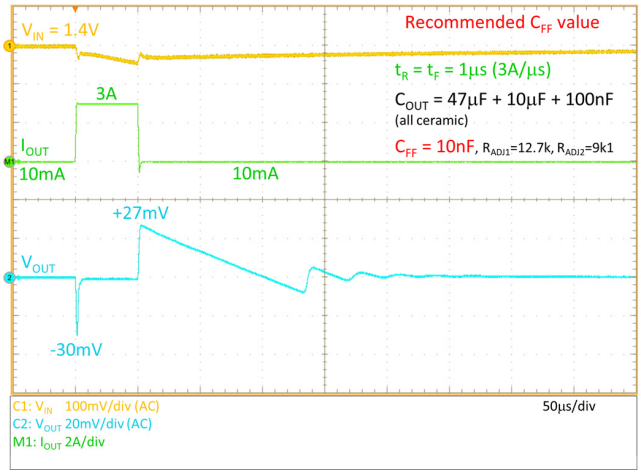


Figure 85. Load Transient Response, ADJ−0.5V set to 1.2V

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

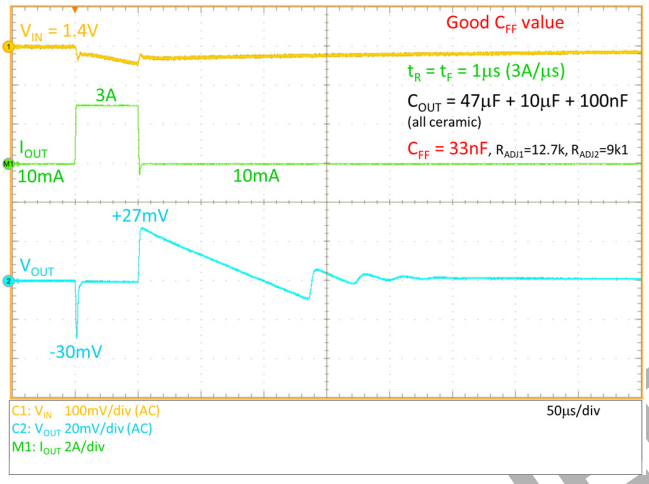


Figure 86. Load Transient Response, ADJ−0.5V set to 1.2V

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

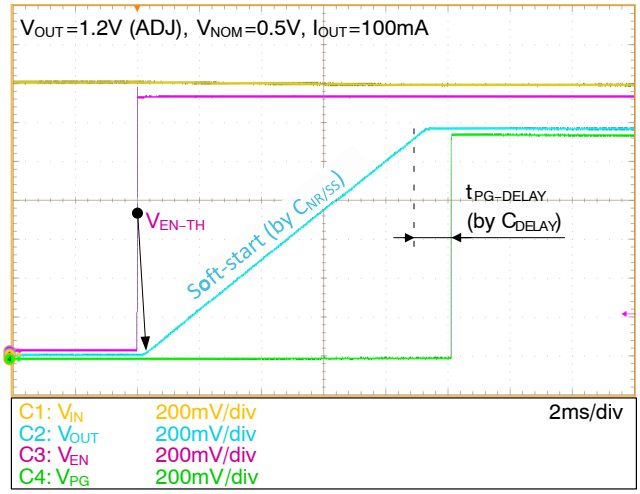


Figure 87. EN−pin Startup, Fast Ramp Up

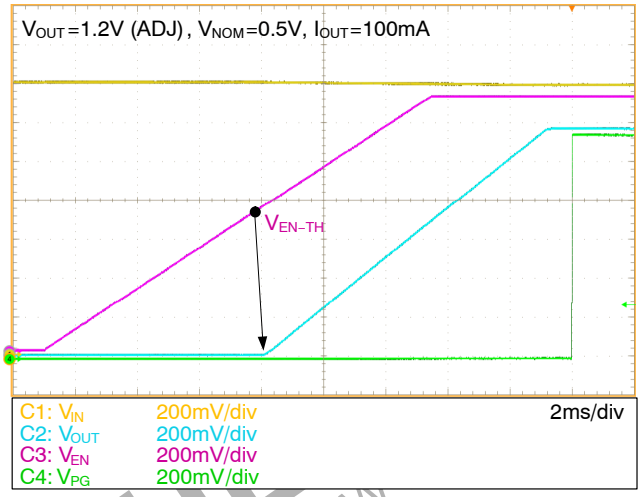


Figure 88. EN−pin Startup, Slow Ramp Up

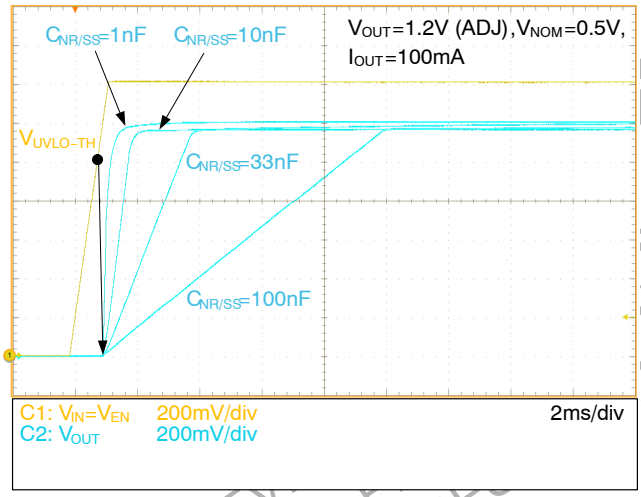


Figure 89. N−pin Startup for Different $C_{NR/SS}$, ADJ Application

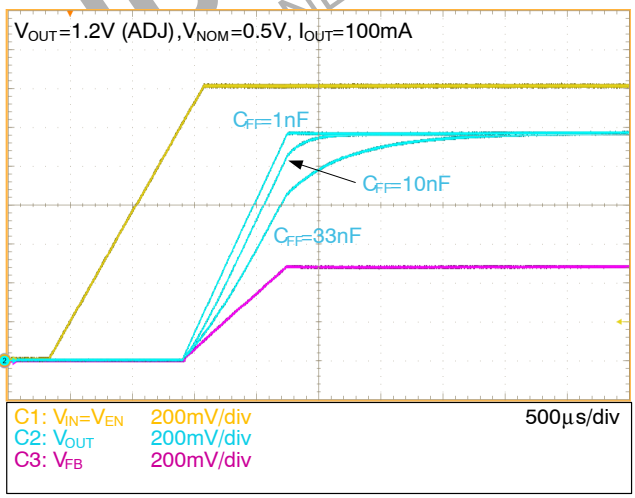


Figure 90. IN−pin Startup for Different C_{FF}, ADJ Application

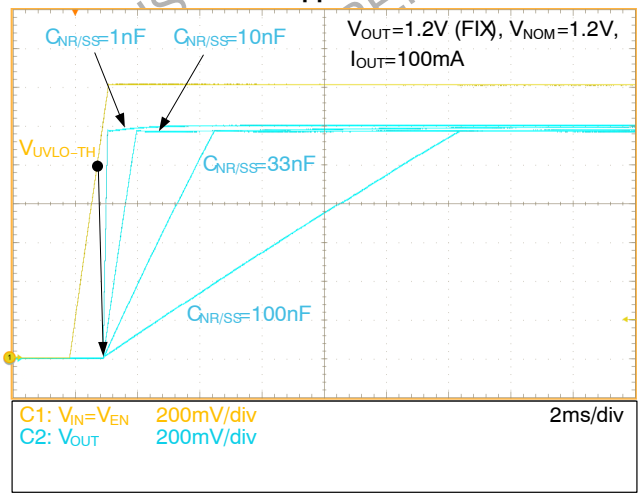


Figure 91. IN−pin Startup for Different $C_{NR/SS}$, FIX Application

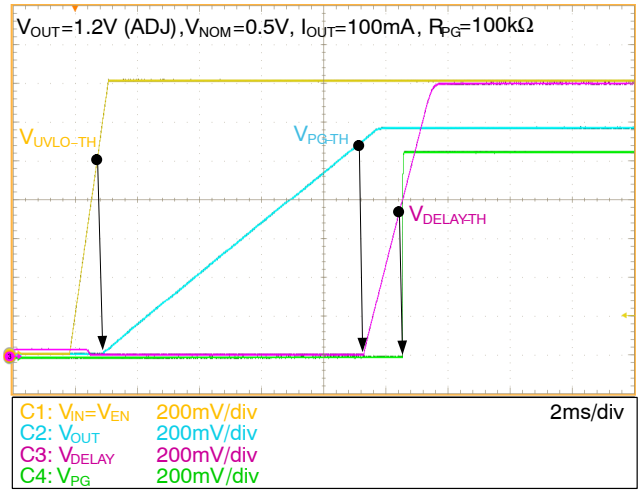


Figure 92. Startup DELAY and PG Behavior

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

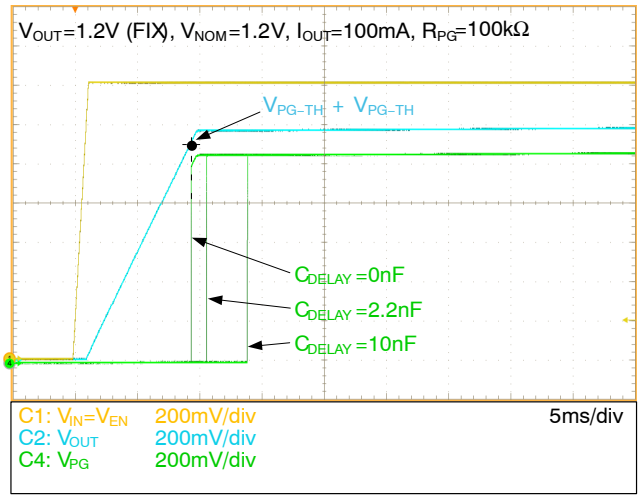


Figure 93. Startup PG Behavior for Different C_{DELAY}

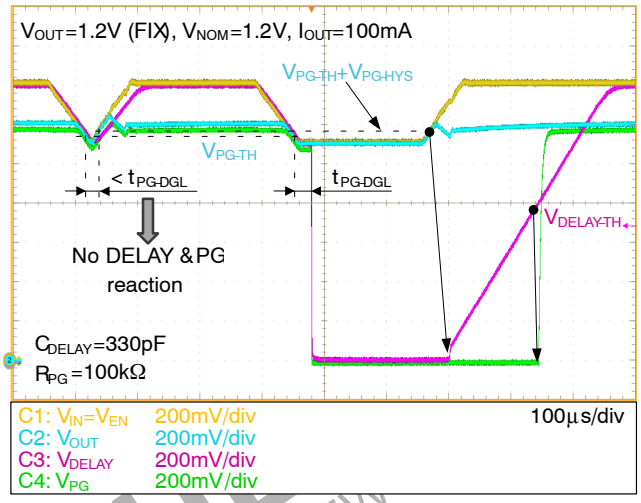


Figure 94. DELAY and PG Signals Behavior During V_{OUT} Drops

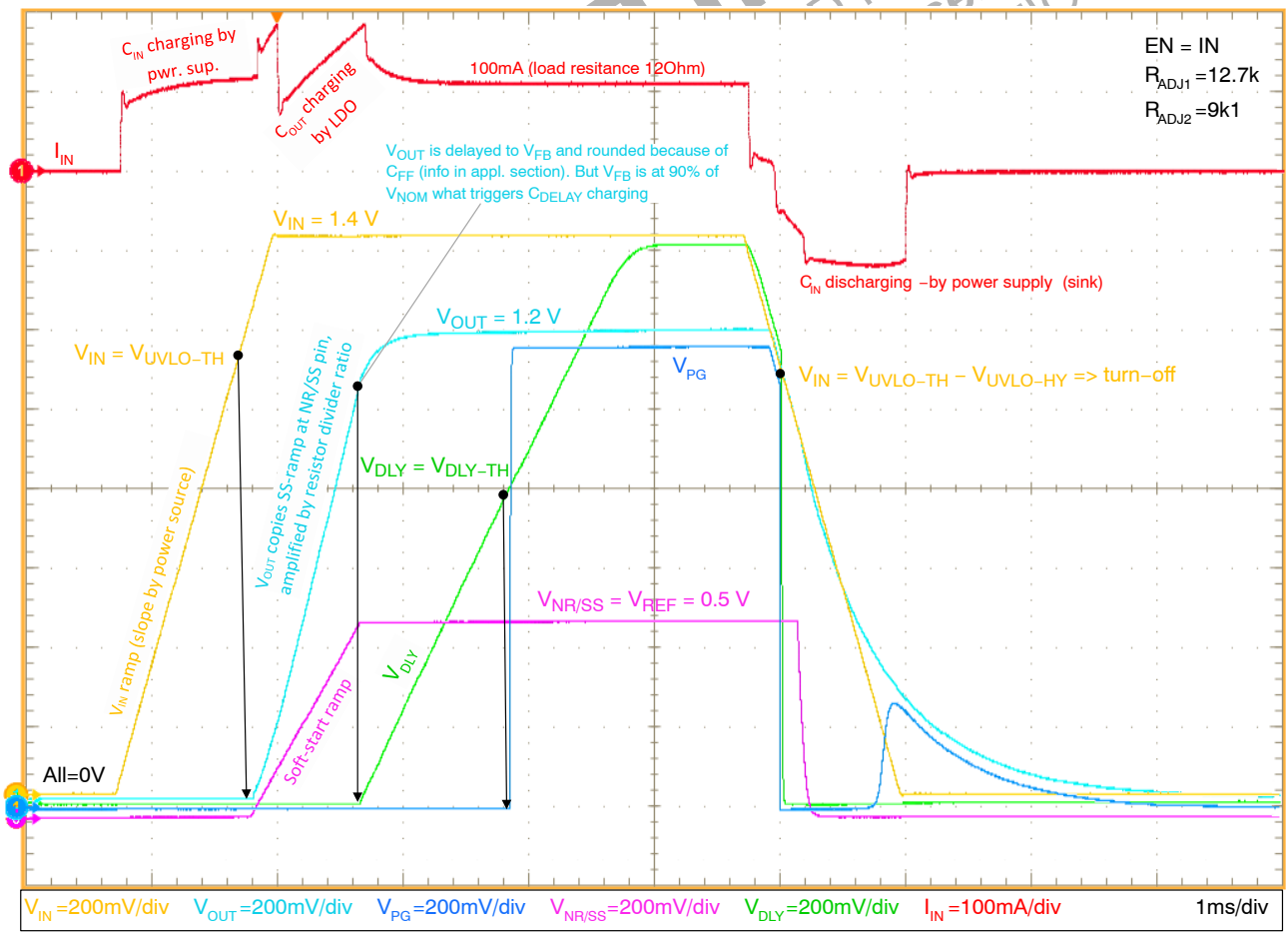


Figure 95. Start–up and Shut–down by V_{IN} Voltage, ADJ Application, V_{NOM} = 0.5 V, V_{OUT} = 1.2 V

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.4 V and V_{IN} ≥ 1.2 V, V_{EN} = 1.1 V, FB = OUT, I_{OUT} = 50 mA, C_{CF} = 10 nF, $C_{NR/SS}$ = 100 nF, C_{DELAY} = 2.2 nF, C_{FF} = 10 nF, C_{IN} = 1 mF (polymer) + 100 μF (C1210) + 10 μF + 100 nF, C_{OUT} = 47 μF (C1210) + 10 μF + 100 nF, T_J = 25°C, unless otherwise noted.

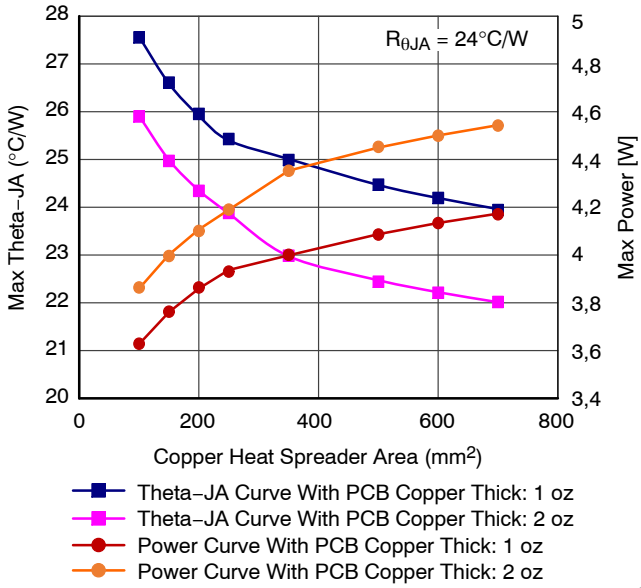


Figure 96. $R_{\theta JA}$ and $P_{DIS(MAX)}$ vs. Copper Area

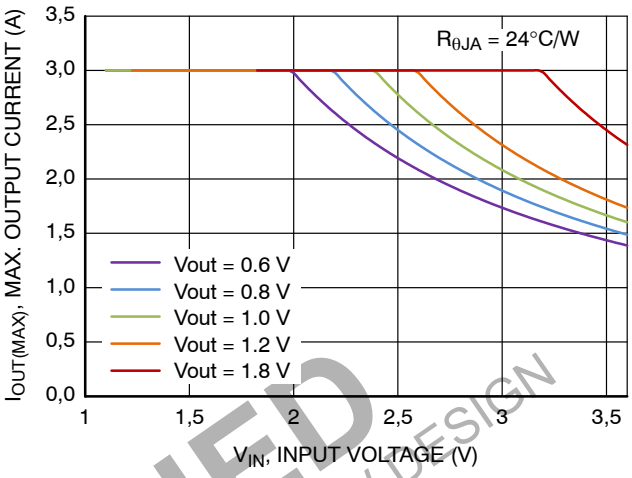


Figure 97. Max. Allowable Output Current vs. V_{IN}, FIX & ADJ Applications, T_A = 25°C

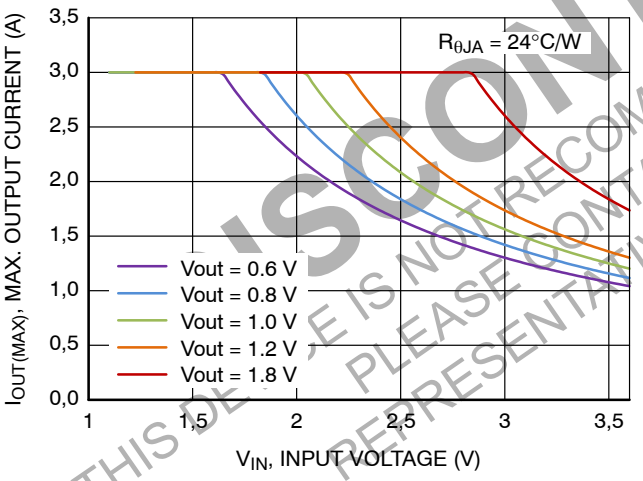


Figure 98. Max. Allowable Output Current vs. V_{IN}, FIX & ADJ Applications, T_A = 50°C

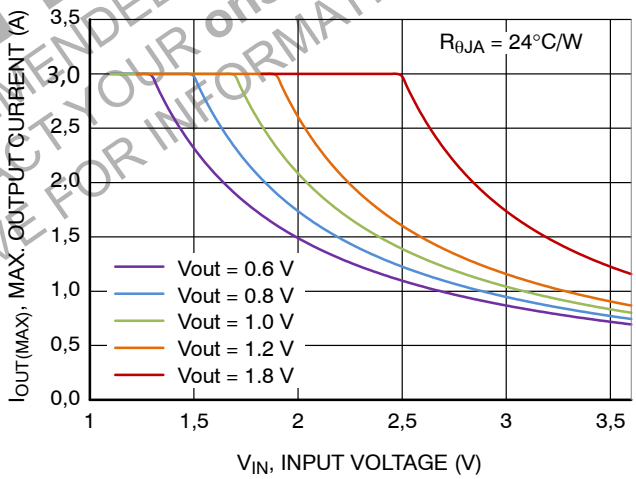


Figure 99. Max. Allowable Output Current vs. V_{IN}, FIX & ADJ Applications, T_A = 75°C

Additional Information to Figures on this Page

Thermal data are based on thermal simulation methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:

These data were generated with only a single device at the center of a high−K (2s2p) board which follows the JEDEC51.7 guidelines. Top and bottom layer 2 oz. copper, inner planes 1 oz. copper. The GND pad connected to the PCB inner GND plane layer through a 3x5 thermal via array. All the vias are 0.3 mm diameter, plated.

The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.

T_A = 25°C, T_J = $T_{J(MAX)}$ = 125°C, unless otherwise noted.

APPLICATIONS INFORMATION

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary to ensure device stability. The ceramic X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be at least 10 μF, recommended value is parallel combination of 47 μF + 100 nF. Maximum value is not limited and the higher means better for the LDO, as this capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitor for its low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes. When a large load transients (like 10 mA to 3 A) happens in the application the input power source of the LDO needs to provide enough power and the input voltage must not go below the level defined by this equation: $V_{IN} = V_{OUT-NOM} + V_{DO}$ otherwise the output voltage drop will be significantly higher (because LDO will enter the dropout state). In cases when LDO's input power supply has a poor load transient response or when there is a long connection between LDO and its power source then the input capacitor needs to be significantly bigger (in range of hundreds of μF).

Output Capacitor Selection (C_{OUT})

The LDO requires the output capacitor connected as close as possible to the output and ground pins. The LDO is designed to remain stable with output capacitor's effective capacitance in range from 40 μF to 1000 μF and ESR from 1 mΩ to 50 mΩ. The ceramic X5R or better type is recommended due to its low capacitance variations over the specified temperature range and low ESR. When selecting the output capacitor the value change with temperature and DC bias voltage needs to be taken into account. Especially for small package size capacitors such as 0805 or smaller the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details). Recommended is parallel combination of ceramic capacitors 47 μF (1210 package) + 10 μF (0805 package) + 100 nF (any small package like 0603, 0402 etc.).

Larger capacitance and lower capacitor ESR improves the load transient response, PSRR and output voltage noise.

Internal Supply Bypass Capacitor (C_{CF})

This capacitor is needed to stabilize the internal power rail generated by the on−chip high frequency charge pump. This charge pump generates a minimal amount of noise but is suppressed to almost zero with additional on−chip isolation and circuits. The C_{CF} capacitor should be 10 nF ceramic capacitor X5R, X7R, X8R, NP0 or similar type, 6.3 V_{DC} or more.

Output Voltage

NCP59763 part is available in several output voltage options (see OPNs table). All of these options could be used in fixed (non−adjustable) or adjustable application circuit. When adjustment of output voltage is not needed then simply connect the FB pin to OUT pin and the output voltage will be equal to the nominal output voltage specified by OPN: $V_{OUT} = V_{NOM}$. If the adjustment is important, connect the output voltage resistor divider between OUT, FB and GND pins. Then the output voltage can be computed by the following equation:

$$V_{OUT} = V_{NOM} \times \left(1 + \frac{R_{ADJ1}}{R_{ADJ2}}\right) + I_{FB} \times R_{ADJ1} \qquad \text{(eq. 1)}$$

Where:

V_{OUT} is output voltage of the circuit with resistor divider (adjustable application).

V_{NOM} is the LDO's nominal output voltage given by OPN.

I_{FB} is the LDO's FB pin input current.

R_{ADJ1} is the upper resistor in resistor divider.

R_{ADJ2} is the lower resistor in resistor divider.

Recommended values of R_{ADJ1} and R_{ADJ2} are in range from 1 kΩ to about 300 kΩ.

Both circuits of FIX (non−adjustable) and ADJ (adjustable) applications are shown at the following figures.

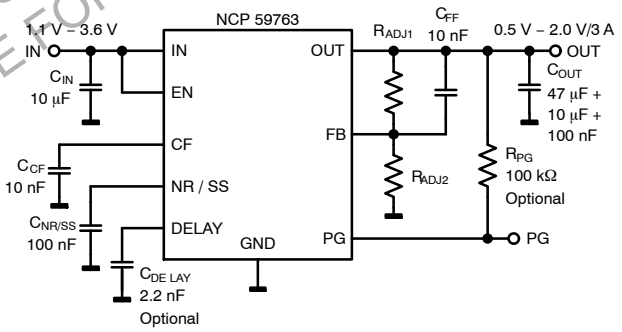


Figure 100. ADJ (Adjustable) Application Schematic

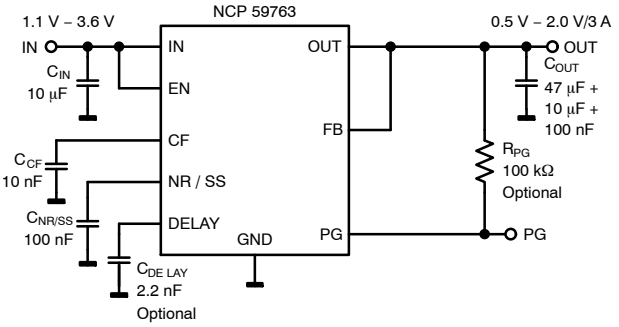


Figure 101. FIX (Non−adjustable) Application Schematic

At the ADJ application, the external resistor divider with input FB pin capacity and FB pin PCB trace capacity to GND makes a low pass filter what negatively affects the dynamic behavior of the LDO. This unwanted dynamic performance degradation could be compensated by adding of feed−forward capacitor C_{FF} across R_{ADJ1} resistor. Recommended value is 10 nF and its influence to several parameters is shown at figures in Typical characteristics section.

The C_{FF} capacitor on one hand improves dynamic behavior of LDO in ADJ application but on the other hand it rounds and delays the V_{OUT} voltage at the startup. Next picture shows V_{OUT} voltage for three different C_{FF} capacitors. It can be seen that for none C_{FF} capacitor the V_{OUT} perfectly follows the V_{FB} voltage while with C_{FF} capacitor it doesn't. The different shape and small delay is probably not an issue. But when the PG is needed in the application, then this phenomenon causes troubles with timing. Because the internal PG comparator checks FB voltage (not OUT voltage) and compares it to the internal thresholds then the PG rises during startup when V_{FB} reaches 93% of V_{NOM} (typ). Without C_{FF} the V_{OUT} rises the same as V_{FB} so PG indicates also 93% of the V_{OUT}. But when C_{FF} is used, V_{OUT} is delayed to V_{FB} which reaches the threshold sooner than V_{OUT}. This results too early rise of the PG signal and it looks like the threshold related to V_{OUT} is false (but it is just the effect of the V_{OUT} delay). It is needed to be told that such behavior is common for all ADJ LDOs with PG, not just for NCP59763.

To overcome this C_{FF} delay issue we can simply tune the value of the C_{DELAY} capacitor and postpone the PG reaction for the same or longer delay time. This is shown at the next picture as V_{PG} curves.

Of course this situation needs care only at the ADJ application when C_{FF} is used (as C_{FF} is not applicable at FIX application).

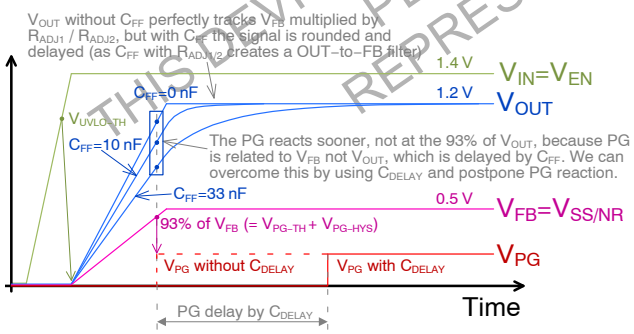


Figure 102. PG Reaction Influenced by C_{FF} Capacitor, ADJ Application, V_{NOM} = 0.5 V, V_{OUT} = 1.2 V

Next table shows recommended feedback part values (R_{AD1}, R_{AD2} and C_{FF}) selected from E24 (resistors) and E6 (capacitor) series. Higher output voltages can be created by several combinations of OPN and divider. It is recommended to select the part with the nearest nominal voltage do desired output voltage for the best dynamic performance. For example, the part with V_{NOM} = 0.5 V set to V_{OUT} = 1.8 V has slightly worse output voltage noise than part with V_{NOM} = 1.2 V, set to the same V_{OUT} = 1.8 V, see Typical characteristics section for details.

Table 6. RECOMMENDED FEEDBACK PART VALUES

V_{OUT} [V]	Part (OPN)	V_{NOM} [V]	R_{ADJ1} [kΩ]	R_{ADJ2} [kΩ]	V_{OUT2} [V]	Diff [%]
0.5	NCP59763AMN050	0.5	Short	None	0.500	0.0
0.6	NCP59763AMN050	0.5	15	75	0.600	0.0
0.7	NCP59763AMN050	0.5	12	30	0.700	0.0
0.8	NCP59763AMN050	0.5	12	20	0.800	0.0
	NCP59763AMN080	0.8	Short	None	0.800	0.0
0.9	NCP59763AMN050	0.5	12	15	0.900	0.0
	NCP59763AMN080	0.8	15	120	0.900	0.0
1.0	NCP59763AMN050	0.5	10	10	1.000	0.0
	NCP59763AMN080	0.8	7.5	30	1.000	0.0
	NCP59763AMN100	1.0	Short	None	1.000	0.0
1.1	NCP59763AMN050	0.5	12	10	1.100	0.0
	NCP59763AMN080	0.8	9.1	24	1.103	0.3
	NCP59763AMN100	1.0	10	100	1.100	0.0
1.2	NCP59763AMN050	0.5	51	36	1.208	0.7
	NCP59763AMN080	0.8	10	20	1.200	0.0
	NCP59763AMN100	1.0	15	75	1.200	0.0
	NCP59763AMN120	1.2	Short	None	1.200	0.0
1.5	NCP59763AMN050	0.5	20	10	1.500	0.0
	NCP59763AMN080	0.8	16	18	1.511	0.7
	NCP59763AMN100	1.0	10	20	1.500	0.0
	NCP59763AMN120	1.2	9.1	36	1.503	0.2
1.8	NCP59763AMN050	0.5	39	15	1.800	0.0
	NCP59763AMN080	0.8	15	12	1.800	0.0
	NCP59763AMN100	1.0	12	15	1.800	0.0
	NCP59763AMN120	1.2	11	22	1.800	0.0
2.0	NCP59763AMN050	0.5	30	10	2.000	0.0
	NCP59763AMN080	0.8	15	10	2.000	0.0
	NCP59763AMN100	1.0	10	10	2.000	0.0
	NCP59763AMN120	1.2	10	15	2.000	0.0

Where:

V_{OUT} [V] is desired output voltage.

V_{NOM} [V] is selected part nominal voltage.

V_{OUT2} [V] is calculated output voltage.

Diff [%] is difference between desired and calculated output voltage.

Of course the table above is just an example and other values of output voltage divider parts are possible.

Startup and Shutdown

In the NCP59763 device there are two main internal signals which triggers the startup process, the under−voltage lockout (UVLO) signal and enable signal. The first one comes from UVLO comparator, which monitors if the IN pin voltages is high enough, while the second one comes from EN pin comparator. Both comparators have embedded hysteresis to be insensitive to input noise.

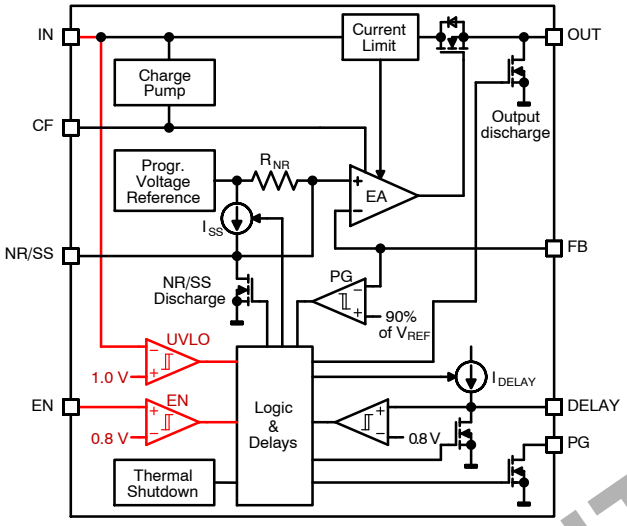


Figure 103. Internal Block Diagram (UVLO and EN Blocks Highlighted)

Next figures show three startup/shutdown cases, initiated by input, enable or both signals assertion.

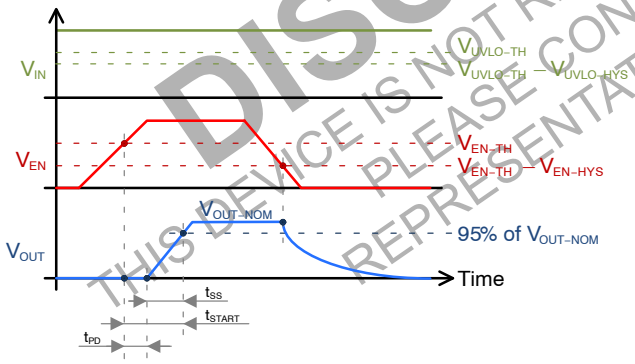


Figure 104. EN Pin Initiated Startup/Shutdown

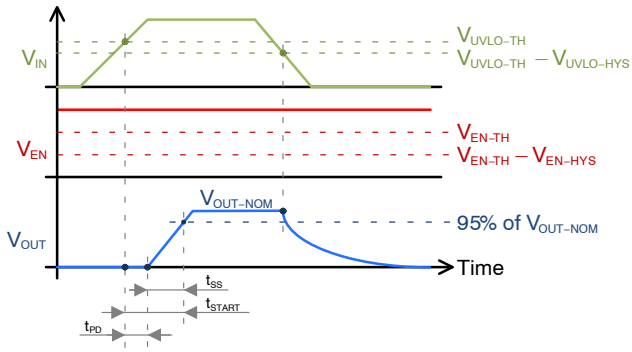


Figure 105. IN Pin Initiated Startup/Shutdown

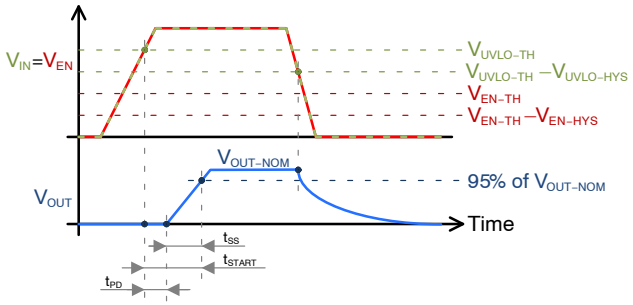


Figure 106. IN & EN Pins Initiated Startup/Shutdown

Where:

t_{SS} is the soft−start time (described below)

t_{START} is the overall startup time

t_{PD} is the internal propagation delay (170 μs typ.)

PG Output

NCP59763 device contains PG circuit for the output voltage level monitoring. Internally it is combined from PG comparator, DELAY comparator, logic block with deglitch timer, DELAY pin current source and discharge NMOS transistor and PG output NMOS transistor (all highlighted by red color at the following picture). The PG comparator compares internal feedback signal voltage (V_{FB}) with the 90% of V_{REF} voltage what means that the V_{OUT} drop below 90% is detected. Output signal from this comparator is blanked by deglitch timer (typ. 20 μs) to filter out possible short spikes at the output voltage. This means that only pulses longer than about 20 μs and lower than 90% of set V_{OUT} are detected. When the PG comparator output signal passes through this deglitch timer it turns ON the DELAY pin discharge NMOS which discharges external delay capacitor (C_{DELAY}) and also turns ON the PG output NMOS.

For proper operation the PG output needs external pull−up resistor which defines the voltage level at the non−fault time. Recommended values range is from 3.9 kΩ to 100 kΩ.

When the output drop event disappears, the DELAY pin discharge NMOS is turned back OFF and the external delay capacitor is charged by internal I_{DELAY} current source. When the DELAY voltage reaches 0.8 V (typ.), what is the internal DELAY comparator threshold voltage, the PG output NMOS transistor is turned OFF to indicate normal condition. This DELAY capacitor charging time is in fact a C_{DELAY} capacitor programmable delay time, what could be needed by external monitoring circuit (for example MCU connected to PG). In case very short delay is acceptable for the application the C_{DELAY} capacitor could be omitted. Then the delay between rising edges of PG to V_{OUT} is about 30 μs.

At adjustable application when C_{FF} capacitor is used, the output voltage settling time could be several times longer than FB voltage settling time (caused by C_{FF} with R_{ADJ1} and R_{ADJ2}). And because the PG comparator monitors the FB voltage, it could indicate “power ok” state based on settled FB voltage at a time when output voltage is still too low. At such case the PG delay must be set by C_{DELAY} capacitor to a longer value than output voltage settling time is.

When the overall PG function is not needed than both C_{DELAY} capacitor and R_{PG} resistor could be omitted.

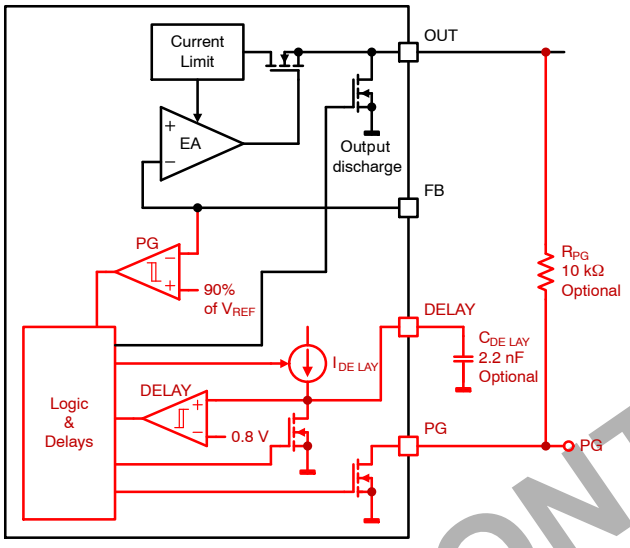


Figure 107. Internal Block Diagram (PG Circuit Highlighted)

Delay time could be computed by the following equation:

$$t_{DELAY} = t_{DELAY-MIN} + \frac{V_{DELAY-TH}}{I_{DELAY}} \times C_{DELAY} = = 30\ \mu + \frac{0.8}{1.8\ \mu} \times C_{DELAY} = 30 + 444 \times C_{DELAY}\ [\mu s; nF] \quad \text{(eq. 2)}$$

Where:

$t_{DELAY-MIN}$ is minimum delay time without capacitor (about 30 μs)

$V_{DELAY-TH}$ is DELAY pin threshold voltage

I_{DELAY} is DELAY capacitor charging current

Soft−start and Noise Reduction

The NR/SS pin has two functions – program LDO’s output voltage rise time and reduce the output voltage noise – both by the same externally connected $C_{NR/SS}$ capacitor.

Startup situation very often needs a special care, because the charge currents of capacitors connected to power rails could cause used power supplies overcurrent events. Generally, any capacitor voltage change generates charge current flowing into this capacitor, given by the following equation:

$$I_C(t) = C \times \frac{dV_C(t)}{dt} \quad \text{(eq. 3)}$$

The $dV_C(t)/dt$ is the slope of capacitor voltage change. The higher V_C voltage change or the higher capacitor value, the bigger capacitor charge current.

In LDO application, there are two capacitors used, C_{IN} and C_{OUT}, and both of them are charged during power−up what could generate very high input current, which is caller inrush current.

Inrush current of LDO application consist of the sum of:

- C_{IN} charge current (can’t be influenced by the LDO, could be influenced by previous power stage only by setting of LDO’s V_{IN} slope)
- C_{OUT} charge current (influenced by the LDO)
- LDO’s ground current (negligible)
- LDO’s load current $I_{LOAD}(t)$

This relations could be written in equation:

$$I_{INRUSH}(t) = I_{CIN}(t) + I_{COUT}(t) + I_{LOAD}(t) \quad \text{(eq. 4)}$$

$$I_{INRUSH}(t) = C_{IN} \times \frac{dV_{IN}(t)}{dt} + C_{OUT} \times \frac{dV_{OUT}(t)}{dt} + I_{LOAD}(t) \quad \text{(eq. 5)}$$

Where:

$dV_{IN}(t)/dt$ is the slope of V_{IN} ramp

$dV_{OUT}(t)/dt$ is the slope of V_{OUT} ramp

From the equation above we can see that in reel application we need to care about both C_{IN} and C_{OUT} capacitor values and about both V_{IN} and V_{OUT} voltage slopes. Only the V_{OUT} slope is influenced by the LDO while the V_{IN} slope is influenced by previous power stage (defined by its soft−start time). The last part of the equation, the $I_{LOAD}(t)$ current, could be dependent to the immediate value of rising V_{OUT} voltage and generally it could vary in time. Because it is part of the inrush current, the LDO should care about it as well and it does by load current limiting during start−up by the current limit feature to I_{CL} level (see Electrical characteristics table).

Back to the soft−start feature, the externally connected $C_{NR/SS}$ capacitor is charged by internal current source I_{SS}. The $C_{NR/SS}$ value and size of the I_{SS} current together define the V_{OUT} voltage rise time. The voltage at the $C_{NR/SS}$ capacitor rises linearly in time and is followed by the LDO’s output voltage.

When the NR/SS pin voltages reaches the internal voltage reference value the I_{SS} current source is turned OFF and the $C_{NR/SS}$ capacitor in combination with internal R_{NR} resistor behaves as an internal reference filter. The bigger $C_{NR/SS}$ value the lower LDO’s output voltage noise.

Recommended range of $C_{NR/SS}$ capacitor is from 10 nF to 100 nF. See the Typical characteristics section for $C_{NR/SS}$ capacitor influence to output voltage noise and startup time as well.

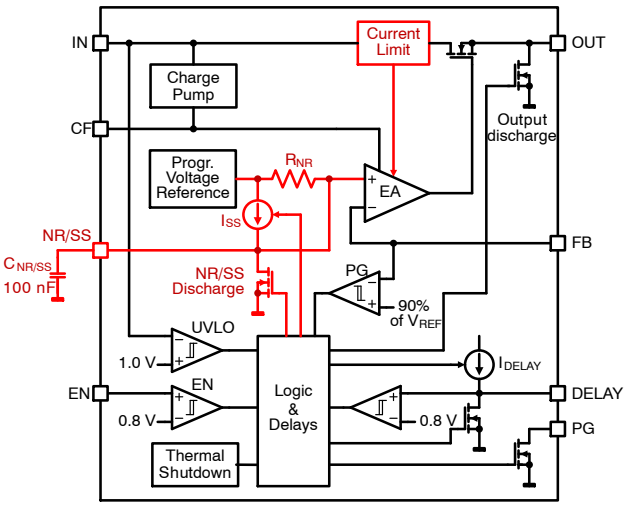


Figure 108. Internal Block Diagram (Startup Circuit Highlighted)

Soft−start time (t_{SS}) represents the length of the output voltage rise time at the startup (not the overall startup time from UVLO or EN assertion). It could be computed by the following equation:

$$t_{SS} = t_{SS-MIN} + \frac{V_{NOM}}{I_{SS}} \times C_{NR/SS} \quad \text{(eq. 6)}$$

Where:

t_{SS-MIN} is minimum soft−start time without $C_{NR/SS}$ capacitor (about 50 μs)

V_{NOM} is nominal LDO's output voltage

I_{SS} is soft−start capacitor charging current

Note that the t_{START} parameter listed in the Electrical characteristics table is not the same time as t_{SS-MIN} mentioned here. t_{START} is overall minimum startup time measured from EN rising edge to a point where V_{OUT} reaches 95% of V_{NOM} while t_{SS-MIN} time is just an output voltage rise time (it means it is a part of t_{START}).

Active Output Discharge

Active output discharge function discharges the output capacitor when the LDO is disabled by EN pin.

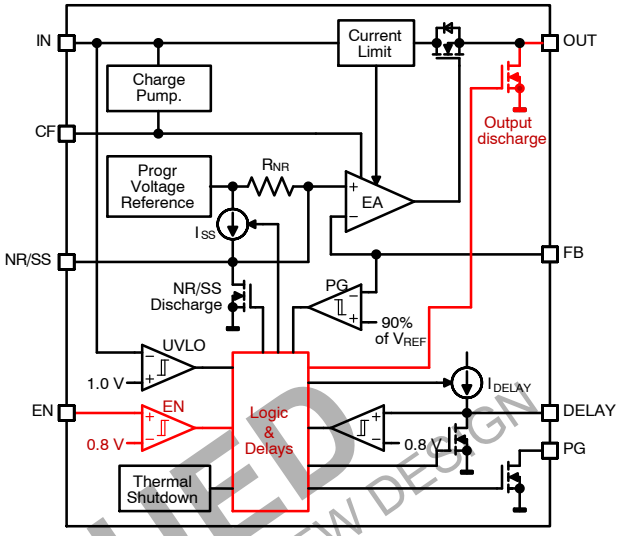


Figure 109. Internal Block Diagram (Output Discharge Related Blocks Highlighted)

When EN pin is turned to low state (when V_{IN} is still present), the output voltage is discharged continuously for the whole EN pin low level period. The slope and shape of discharged output voltage is given by resistance of internal discharge NMOS transistor, load resistance and total output capacitance.

Output voltage during the discharge period could be described by:

$$V_{OUT}(t) = V_{NOM} \times e^{-t/\tau} \quad \text{(eq. 7)}$$

$$\tau = (R_{ACT} + R_{LOAD}) \times C_{OUT} \quad \text{(eq. 8)}$$

Where:

$V_{OUT}(t)$ is immediate voltage at desired time point

V_{NOM} is the nominal output voltage

t is the desired time

τ is the RC time constant

R_{ACT} is resistance of int. active discharge NMOS

R_{LOAD} is load resistance

From time perspective, we can say that after one RC time constant (τ), the output voltage is discharged to 36.6%, after two τ to 13.5%, after four τ to 1.8% etc.

Next picture shows waveforms for discussed situation.

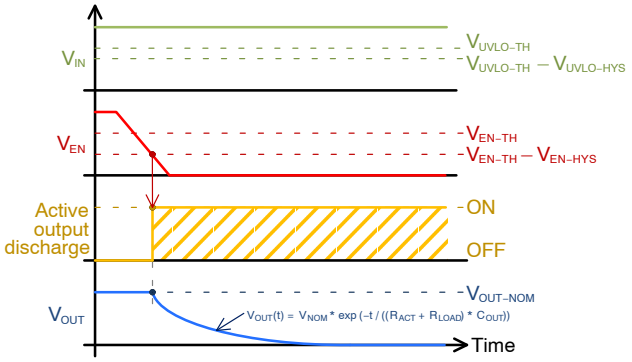


Figure 110. Active Output Discharge Activated by EN Pin

It is important to mention a different situation, when LDO is not disabled by EN pin, but turned off by input voltage (EN pin held high or connected to IN pin and V_{IN} is forced low). At this case the output discharge function is also activated but just for a short period of time, starting when input voltage falls below the low UVLO threshold (0.9 V typ.) and ending when falls below the minimum discharge block operational level ($V_{AOD-MIN}$, 0.8 V typ.). We can see that there is a small input voltage window where the discharge function is active (0.9 V – to – 0.8 V). Based on this fact the proper output voltage discharge to 0V is not possible. Simply, LDO's active output discharge block can't be functional because the LDO's power supply is turned off. The situation is shown at the next picture.

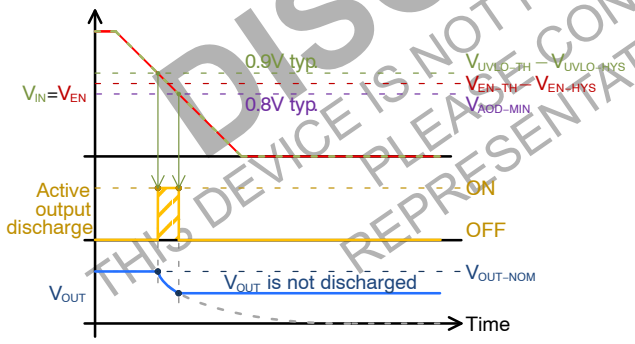


Figure 111. Active Output Discharge Activated by Falling V_{IN}

At a situation of the high falling input voltage slope, it could happen that the activated output discharge function theoretical time window is shorter than internal delays, resulting the discharge function will not be activated (fast falling V_{IN} slope means no output discharge).

Thermal protection

When the LDO's die temperature exceeds the thermal shutdown threshold value, the device is internally disabled. The IC will remain in disabled state until the die temperature decreases by the thermal shutdown hysteresis value. Then the LDO is back enabled.

The thermal shutdown feature provides the protection against overheating due to application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by one of the following equations:

$$P_{DIS} = \frac{T_J - T_A}{R_{\theta JA}} [W] \quad \text{(eq. 9)}$$

Or

$$P_{DIS} = \frac{T_J - T_B}{R_{\theta JB}} [W] \quad \text{(eq. 10)}$$

Where:

T_J is the desired junction temperature

T_A is the ambient temperature

T_B is the board temperature (on the trace within 1 mm of the package body)

$R_{\theta JA}$ is junction to ambient thermal resistance

$R_{\theta JB}$ is junction to board thermal resistance

If we enter the maximum junction temperature value (125°C) as a T_J, we obtain a maximum allowable power dissipation $P_{DIS(MAX)}$. Then, when applying higher power dissipation to this max. power dissipation ($P_{DIS} > P_{DIS(MAX)}$), the device will be overheated ($T_J > T_{J(MAX)}$).

We can substitute for the power dissipation the following equation:

$$P_{DIS} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad \text{(eq. 11)}$$

To obtain equation for the output current:

$$I_{OUT} = \frac{P_{DIS}}{V_{IN} - V_{OUT}} = \frac{T_J - T_X}{R_{\theta JX} \times (V_{IN} - V_{OUT})} \quad \text{(eq. 12)}$$

Where:

T_X is T_A resp. T_B

$R_{\theta JX}$ is $R_{\theta JA}$ resp. $R_{\theta JB}$

And similarly, if we enter the maximum junction temperature value (125°C) as a T_J, we obtain a maximum allowable load current $I_{OUT(MAX)}$. Then, when applying higher load current to this max. load current ($I_{OUT} > I_{OUT(MAX)}$), the device will be overheated ($T_J > T_{J(MAX)}$).

Maximum power dissipation and maximum allowable output currant charts are shown at figures 96 to 99.

PCB Layout Recommendations

To obtain good LDO's stability and the best transient, PSRR and output voltage noise performance, place both C_{IN} and C_{OUT} capacitors as close as possible to the device pins, make the PCB traces wide and short and place capacitors to the same PCB Cu layer as the LDO is (avoid connections through vias). The same rules should be applied to the connections between C_{OUT} and the load – the less parasitic impedance the better dynamic performance at the point of load.

Regarding high impedance ADJ pin, prevent capacitive coupling of this trace to any switching signals in the circuitry.

The same applies to high impedance NR/SS pin, which is very sensitive to coupled noise. Therefore make the trace to $C_{NR/SS}$ as short as possible.

When routing the trance to C_{CF} capacitor, use also as short as possible connection.

Other traces like PG, DELAY and EN don't need any special care.

Demo Board Quick Overview

First it should be noted that more detailed evaluation board information are provided in separate documents on company web pages.

Below are schematic and board pictures of the NCP59763AMN050TBGEVB evaluation board. The board has been used during product evaluation to capture the data shown in this datasheet (transients, PSRR, noise, startups etc.).

By the solder jumper JP6 (label FIX) the application circuit could be changed from the default adjustable type (trimmer resistor RT1 sets the V_{OUT}) to fixed. By default the board is supplied with LDO NCP59763AMN050 (V_{NOM} = 0.5 V) but it can handle any other OPN (on request).

There is also a picture showing the layout in detail, which could be taken as a recommended layout.

Generally, when testing LDOs dynamic performance on evaluation board connected to laboratory power supply typically by long cables, the device would need additional input capacitor. This capacitor will cover voltage drops created at the long connection cables impedance by the load current transients (note that this is different situation to normal application where the distance of the LDO to its power source is short so it need special care). In such case it is recommended to assemble low ESR electrolytic input capacitor to the spare place (C4) on the evaluation board (recommended is aluminum organic polymer capacitor 560 μF to 2.2 mF for 6.3V or higher with ESR about 10 – 30 mΩ, 10 mm of diameter, through−hole with 5 mm pin pitch to fit the PCB, for example Kemet A750MV108M1EAAE014).

Besides the main LDO application circuit, evaluation board includes some supporting staff:

- Two positions for optional through−hole SMB connectors for IN and OUT signals, mainly for line/load transients, PSRR and noise testing (recommended connectors are Molex 73100−0258 or compatible).
- Edge connector where all these signal leads to (the appropriate receptacle type is SAMTEC MECF−20−01−L−DV−WT).
- Three diodes as temperature sensors.

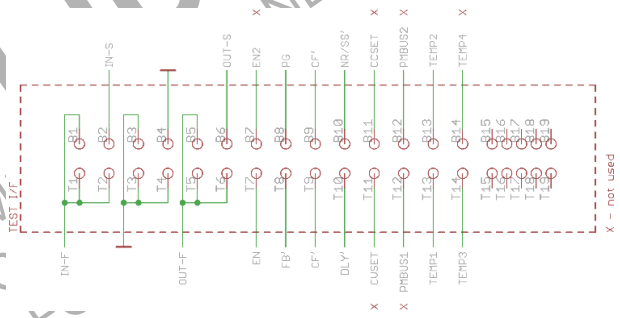


Figure 112. NCP59763AMN050TBGEVB Schematic (Edge Connector Pinout)

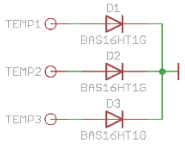


Figure 113. NCP59763AMN050TBGEVB Schematic (Three Diodes as Temperature Sensors)

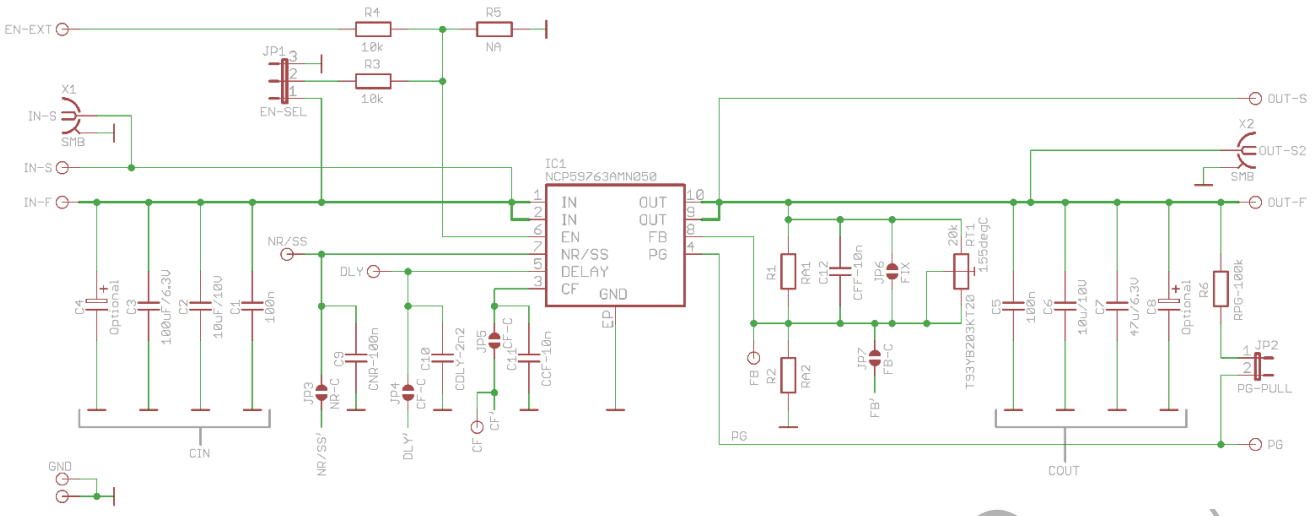


Figure 114. NCP59763AMN050TBGEVB Schematic (Main Part)

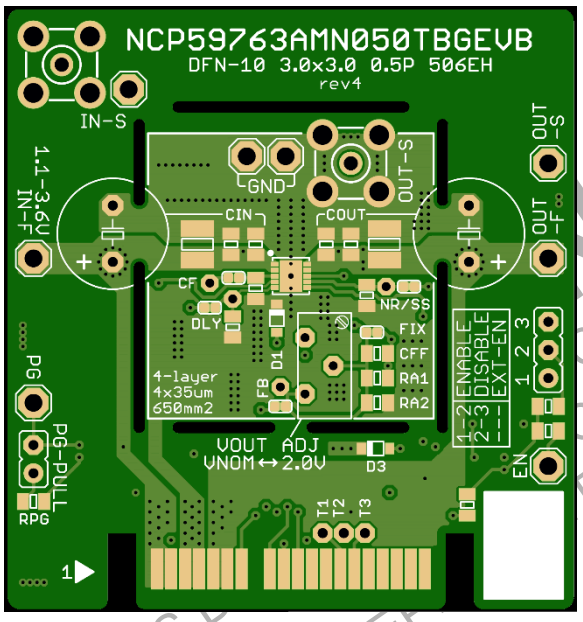


Figure 115. NCP59763AMN050TBGEVB Board

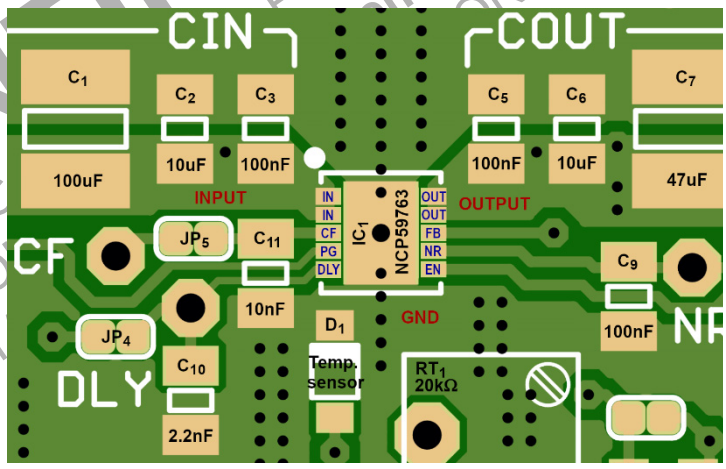


Figure 116. NCP59763AMN050TBGEVB Board Center Detail

ORDERING INFORMATION

Device	Output Voltage (V_{NOM})	Marking	Package	Shipping†
NCP59763AMN050TBG	0.5 V	59763 P050A	DFN10 3x3, 0.5P (Pb−Free)	3000 Tape & Reel
NCP59763AMN080TBG	0.8 V	59763 P080A		
NCP59763AMN100TBG	1.0 V	59763 P100A		
NCP59763AMN120TBG	1.2 V	59763 P120A		

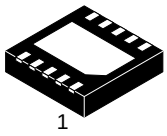
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

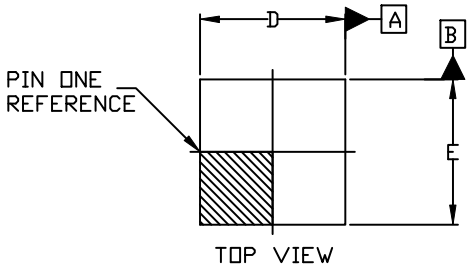
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

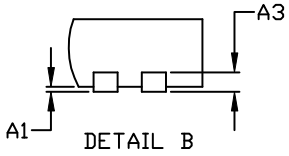
ON Semiconductor®

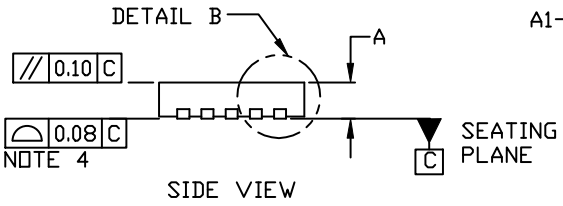
DFN10 3x3, 0.5P
CASE 506EH
ISSUE O

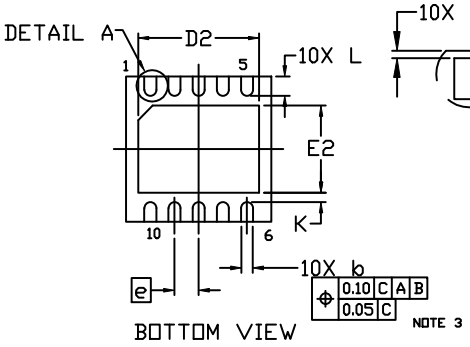
DATE 24 JUL 2018

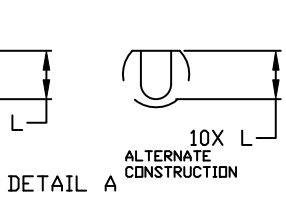








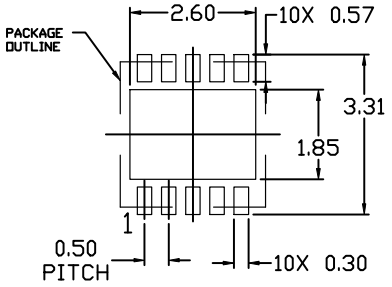




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e	0.50 BSC		
K	0.20 REF		
L	0.30	0.40	0.50
L1	---	---	0.10



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON94098G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN10 3x3, 0.5P**	**PAGE 1 OF 1**

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