NCP6336

Product Preview

Configurable 5.0 A Step Down Converter - Transient Load Helper

The NCP6336 is a synchronous buck converter optimized to supply the different sub systems of portable applications powered by one cell Li−Ion or three cell Alkaline/NiCd/NiMH batteries. The device is able to deliver up to 5.0 A, with programmable output voltage from 0.6 V to 1.5 V. It can share the same output rail with another DC−to−DC converter and works as a transient load helper. Operation at a 3 MHz switching frequency allows the use of small components. Synchronous rectification and automatic PWM/PFM transitions improve overall solution efficiency. The NCP6336 is in a space saving, low profile 2.0 x 1.6 mm CSP−20 package.

Features

- Input Voltage Range from 2.3 V to 5.5 V: Battery and 5 V Rail Powered Applications
- Programmable Output Voltage: 0.6 V to 1.5 V in 10 mV Steps
- 3 MHz Switching Frequency with On Chip Oscillator
- Uses 330 nH Inductor and 47 μF Capacitors for Optimized Footprint and Solution Thickness
- PFM/PWM Operation for Optimum Increased Efficiency
- Low 35 μA Quiescent Current
- I^2C Control Interface with Interrupt and Dynamic Voltage Scaling Support
- Enable Pins, Power Good / Fail Signaling
- Thermal Protections and Temperature Management
- Transient Load Helper: Share the Same Rail with Another Rail
- Small 2.0 x 1.6 mm / 0.4 mm Pitch CSP Package
- These are Pb−Free Devices

Typical Applications

- Smartphones
- Tablets

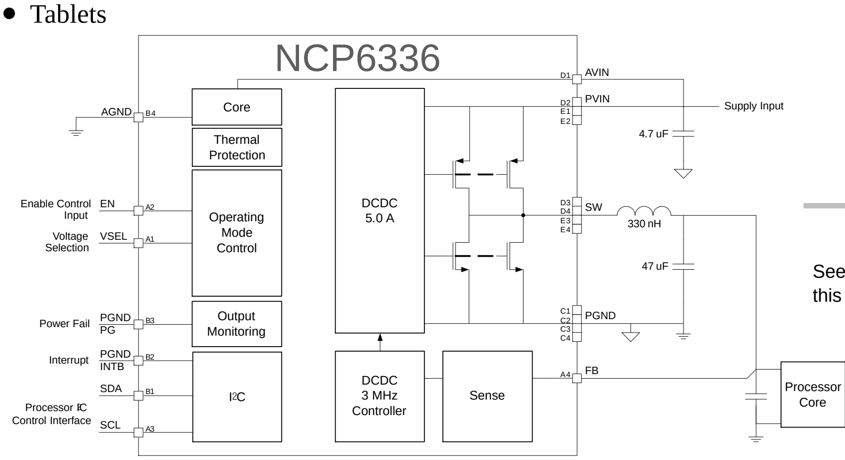

Figure 1. Typical Application Circuit

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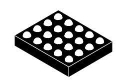
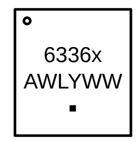


WLCSP20
CASE 568AG

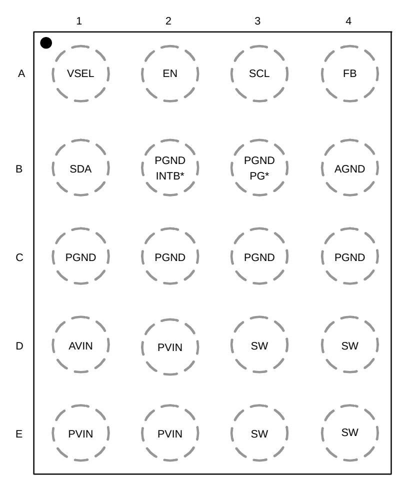
MARKING DIAGRAM



x = P: Prototype
  = blank: Production
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

Pb−Free indicator, G or microdot (▪), may or may not be present

PIN OUT



(Top View)
*Optional

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

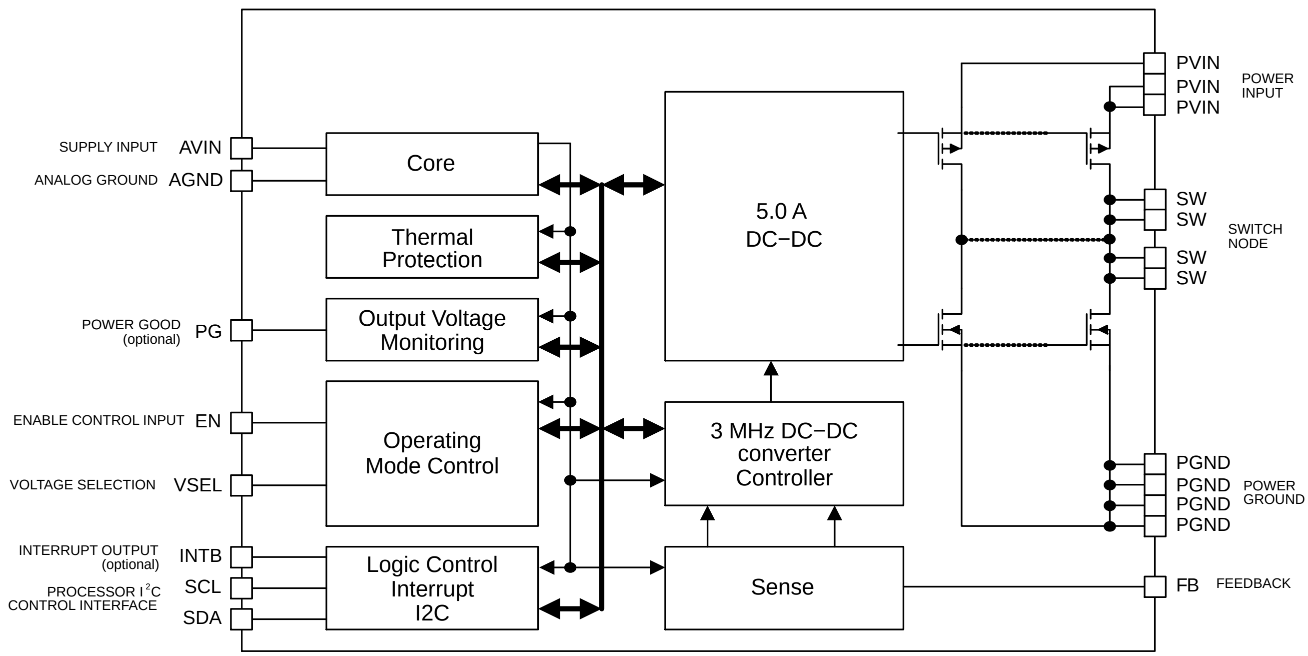


Figure 2. Simplified Block Diagram

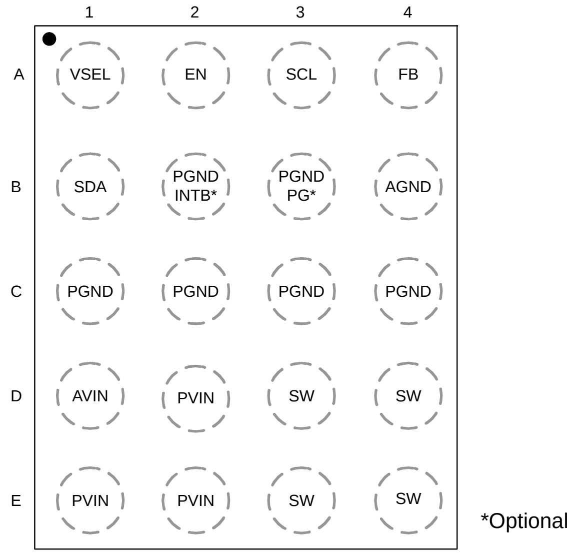


Figure 3. Pin Out (Top View)

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
REFERENCE			
D1	AVIN	Analog Input	**Analog Supply.** This pin is the device analog and digital supply. Could be connected directly to the VIN plane just next to the 4.7 μF PVIN capacitor or to a dedicated 1.0 μF ceramic capacitor.
B4	AGND	Analog Ground	**Analog Ground.** Analog and digital modules ground. Must be connected to the system ground.
CONTROL AND SERIAL INTERFACE			
A2	EN	Digital Input	**Enable Control.** Active high will enable the part. There is an internal pull down resistor on this pin.
A1	VSEL	Digital Input	**Output voltage / Mode Selection.** The level determines which of two programmable configurations to utilize (operating mode / output voltage). There is an internal pull down resistor on this pin; could be left open if not used.
A3	SCL	Digital Input	I^2C interface **Clock** line. There is an internal pull down resistor on this pin; could be left open if not used
B1	SDA	Digital Input/Output	I^2C interface Bi−directional **Data** line. There is an internal pull down resistor on this pin; could be left open if not used
B3	PGND PG	Digital Output Analog Ground	**Power Good** open drain output. If not used has to be connected to ground plane
B2	PGND INTB	Digital Output Analog Ground	**Interrupt** open drain output. If not used has to be connected to ground plane
DC to DC CONVERTER			
D2, E1, E2	PVIN	Power Input	**Switch Supply.** These pins must be decoupled to ground by a 4.7 μF ceramic capacitor. It should be placed as close as possible to these pins. All pins must be used with short heavy connections.
D3, D4, E3, E4	SW	Power Output	**Switch Node.** These pins supply drive power to the inductor. Typical application uses 0.33 μH inductor; refer to application section for more information. All pins must be used with short heavy connections.
C1, C2, C3, C4	PGND	Power Ground	**Switch Ground.** This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane that connects all PGND pins together is recommended. Analog and power grounds should only be connected together in one location with a trace.
A4	FB	Analog Input	**Feedback Voltage input.** Must be connected to the output capacitor positive terminal with a trace, not to a plane. This is the positive input to the error amplifier.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog and power pins: AVIN, PVIN, SW, PG, INTB, FB (Note 1)	V_A	−0.3 to + 6.0	V
Digital pins: SCL, SDA, EN, VSEL, Pin: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A + 0.3 ≤ 6.0 10	 V mA
Human Body Model (HBM) ESD Rating (Note 2)	ESD HBM	2500	V
Charged Device Model (CDM) ESD Rating (Note 2)	ESD CBM	1250	V
Latch Up Current: (Note 3) Digital Pins All Other Pins	I_{LU}	 10 100	mA
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series contains ESD protection and passes the following ratings:
   Human Body Model (HBM) ± 2.5 kV per JEDEC standard: JESD22−A114.
   Charged Device Model (CDM) ± 1250 V per JEDEC standard: JESD22−C101 Class IV
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN}, PV_{IN}	Power Supply		2.3		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range (Note 6)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 7)	CSP−20 on Demo−board	−	55	−	°C/W
P_D	Power Dissipation Rating (Note 8)	T_A ≤ 85°C	−	727	−	mW
P_D	Power Dissipation Rating (Note 8)	T_A = 65°C	−	1090	−	mW
L	Inductor for DC to DC converter (Note 5)		0.26	0.33	0.56	μH
Co	Output Capacitor for DC to DC Converter (Note 5)		30	−	150	μF
Cin	Input Capacitor for DC to DC Converter (Note 5)		4.7	−	−	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Including de−ratings (Refer to the Application Information section of this document for further details)
6. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
7. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a NCP6336EVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board.
8. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

ELECTRICAL CHARACTERISTICS (Notes 10 and 11)
Min and Max Limits apply for T_A = −40°C to +85°C, AVIN = PVIN = 3.6 V and default configuration, unless otherwise specified.
Typical values are referenced to T_A = +25°C, AVIN = PVIN = 3.6 V and default configuration, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS AVIN – PVINx						
$I_{Q\ PWM}$	Operating quiescent current PWM	DCDC active in Forced PWM no load	−	15	25	mA
$I_{Q\ PFM}$	Operating quiescent current PFM	DCDC active in Auto mode no load − minimal switching	−	35	70	μA
I_{SLEEP}	Product sleep mode current	EN high, DCDC off or EN low and (VSEL high or Sleep_Mode high) V_{IN} = 2.5 V to 5.5 V	−	7	15	μA
I_{OFF}	Product in off mode	EN, VSEL and Sleep_Mode low V_{IN} = 2.5 V to 5.5 V	−	0.8	5	μA
DC to DC CONVERTER						
PV_{IN}	Input Voltage Range		2.3	−	5.5	V
I_{OUTMAX}	Maximum Output Current	Ipeak[1..0] = 00 (Note 12)	3.5	−	−	A
		Ipeak[1..0] = 01 (Note 12)	4.0	−	−	
		Ipeak[1..0] = 10 (Note 12)	4.5	−	−	
		Ipeak[1..0] = 11 (Note 12)	5.0	−	−	
Δ_{VOUT}	Output Voltage DC Error	Forced PWM mode, No load	−1	−	1	%
		Forced PWM mode, V_{IN} range, I_{OUT} up to I_{OUTMAX} (Note 12)	−1	−	1	
		Auto mode, V_{IN} range, I_{OUT} up to I_{OUTMAX} (Note 12)	−1	−	2	
F_{SW}	Switching Frequency		2.70	3	3.30	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PVIN to SW V_{IN} = 5.0 V	−	23	40	mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW to PGND V_{IN} = 5.0 V	−	12	20	mΩ
I_{PK}	Peak Inductor Current	Open loop – Ipeak[1..0] = 00 (Note 12)	−	5.2	−	A
		Open loop – Ipeak[1..0] = 01 (Note 12)	−	5.8	−	
		Open loop – Ipeak[1..0] = 10 (Note 12)	−	6.2	−	
		Open loop – Ipeak[1..0] = 11	6.1	6.8	7.8	
DC_{LOAD}	Load Regulation	I_{OUT} from 0 A to I_{OUTMAX} (Note 12) Forced PWM mode	−	−0.2	−	%/A
DC_{LINE}	Line Regulation	I_{OUT} = 3 A 2.3 V ≤ V_{IN} ≤ 5.5 V (Note 12) Forced PWM mode	−	0	−	%
AC_{LOAD}	Transient Load Response	tr = ts = 100 ns Load step 1.2 A (Note 12)	−	±40	−	mV
D	Maximum Duty Cycle		−	100	−	%
t_{START}	Turn on time	Time from EN transitions from Low to High to 90% of Output Voltage (DELAY[2..0] = 000b)	−	90	110	μs
$R_{DISDCDC}$	DCDC Active Output Discharge	V_{OUT} = 1.15 V	−	25	35	Ω

9. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Refer to the Application Information section of this data sheet for more details.
11. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
12. Guaranteed by design and characterized.

ELECTRICAL CHARACTERISTICS (Notes 10 and 11)
Min and Max Limits apply for T_A = −40°C to +85°C, AVIN = PVIN = 3.6 V and default configuration, unless otherwise specified.
Typical values are referenced to T_A = +25°C, AVIN = PVIN = 3.6 V and default configuration, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EN, VSEL						
V_{IH}	High input voltage		1.05	−	−	V
V_{IL}	Low input voltage		−	−	0.4	V
T_{FTR}	Digital input X Filter	EN, VSEL rising and falling DBN_Time = 01 (Note 12)	0.5	−	4.5	μs
I_{PD}	Digital input X Pull−Down (input bias current)		−	0.05	1.00	μA
PG (Optional)						
V_{PGL}	Power Good Threshold	Falling edge as a percentage of nominal output voltage	86	90	94	%
V_{PGHYS}	Power Good Hysteresis		0	3	5	%
T_{RT}	Power Good Reaction Time for DCDC	Falling (Note 12) Rising (Note 12)	− 3.5	3.5 −	− 14	μs
V_{PGL}	Power Good low output voltage	I_{PG} = 5 mA	−	−	0.2	V
PG_{LK}	Power Good leakage current	3.6 V at PG pin when power good valid	−	−	100	nA
V_{PGH}	Power Good high output voltage	Open drain	−	−	5.5	V
INTB (Optional)						
V_{INTBL}	INTB low output voltage	I_{INT} = 5 mA	0	−	0.2	V
V_{INTBH}	INTB high output voltage	Open drain	−	−	5.5	V
$INTB_{LK}$	INTB leakage current	3.6 V at INTB pin when INTB valid	−	−	100	nA
I^2C						
V_{I2CINT}	High level at SCL/SCA line		1.7	−	5.0	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Note 11, 12)	−	−	0.5	V
V_{I2CIH}	SCL, SDA high input voltage	SCL, SDA pin (Note 11, 12)	0.8 * V_{I2CINT}	−	−	V
V_{I2COL}	SDA low output voltage	I_{SINK} = 3 mA (Note 12)	−	−	0.4	V
F_{SCL}	I^2C clock frequency	(Note 12)	−	−	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	−	−	2.3	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	−	200	mV
T_{SD}	Thermal Shut Down Protection		−	150	−	°C
$T_{WARNING}$	Warning Rising Edge		−	135	−	°C
T_{PWTH}	Pre − Warning Threshold	I^2C default value	−	105	−	°C
T_{SDH}	Thermal Shut Down Hysteresis		−	30	−	°C
$T_{WARNINGH}$	Thermal warning Hysteresis		−	15	−	°C
$T_{PWTH\ H}$	Thermal pre−warning Hysteresis		−	6	−	°C

9. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Refer to the Application Information section of this data sheet for more details.
11. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
12. Guaranteed by design and characterized.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6$ V, $T_J = +25°C$, DCDC = 1.15 V, Ipeak = 3.9 A (Unless otherwise noted). L = 0.33 μH PIFE25201B – $C_{OUT} = 47$ μF 0603, $C_{IN} = 4.7$ μF 0603

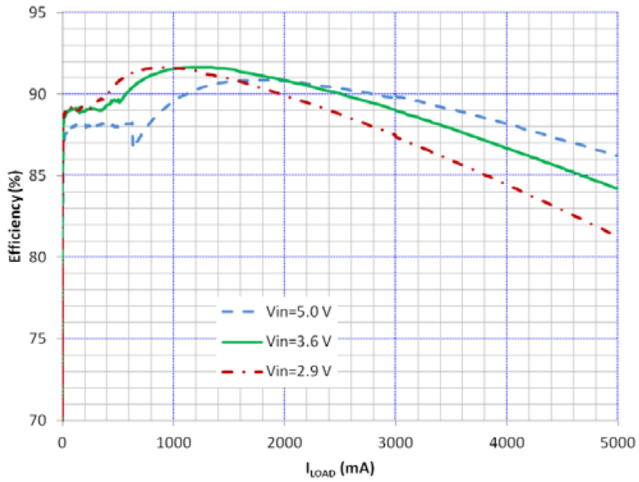


Figure 4. Efficiency vs I_{LOAD} and V_{IN}
$V_{OUT} = 1.50$ V, SPM5030 Inductor

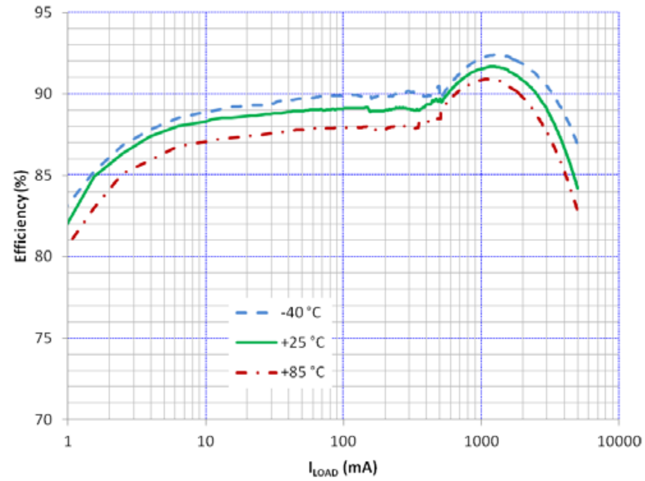


Figure 5. Efficiency vs I_{LOAD} and Temperature
$V_{OUT} = 1.50$ V, SPM5030 Inductor

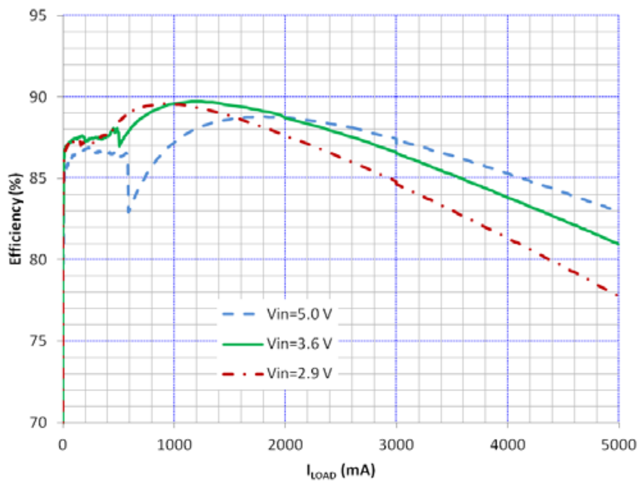


Figure 6. Efficiency vs I_{LOAD} and V_{IN}
$V_{OUT} = 1.15$ V, SPM5030 Inductor

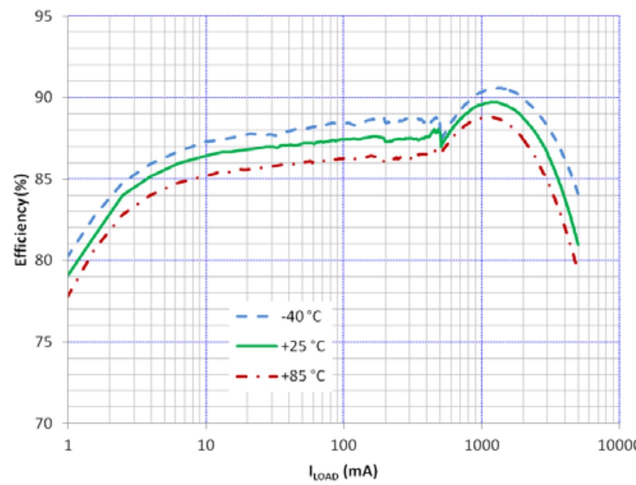


Figure 7. Efficiency vs I_{LOAD} and Temperature
$V_{OUT} = 1.15$ V, SPM5030 Inductor

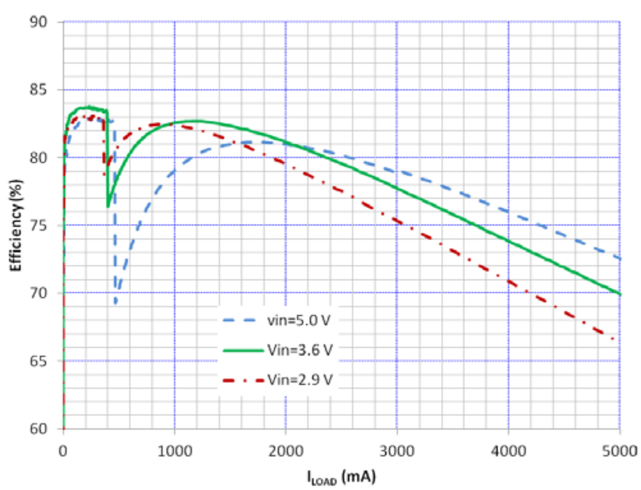


Figure 8. Efficiency vs I_{LOAD} and V_{IN}
$V_{OUT} = 0.60$ V, SPM5030 Inductor

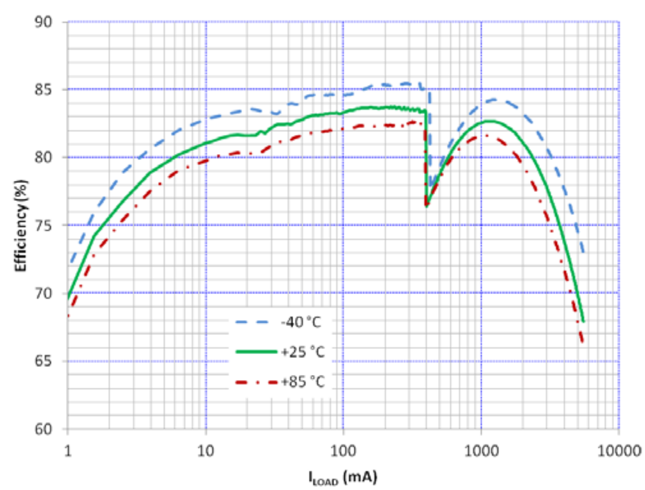


Figure 9. Efficiency vs I_{LOAD} and Temperature
$V_{OUT} = 0.60$ V, SPM5030 Inductor

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN}$ = 3.6 V, T_J = +25°C, DCDC = 1.15 V, Ipeak = 3.9 A (Unless otherwise noted). L = 0.33 μH PIFE25201B – C_{OUT} = 47 μF 0603, C_{IN} = 4.7 μF 0603

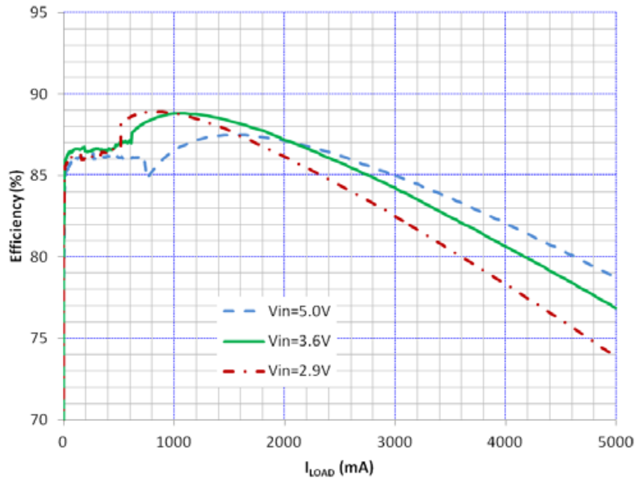


Figure 10. Efficiency vs I_{LOAD} and V_{IN} V_{OUT} = 1.15 V

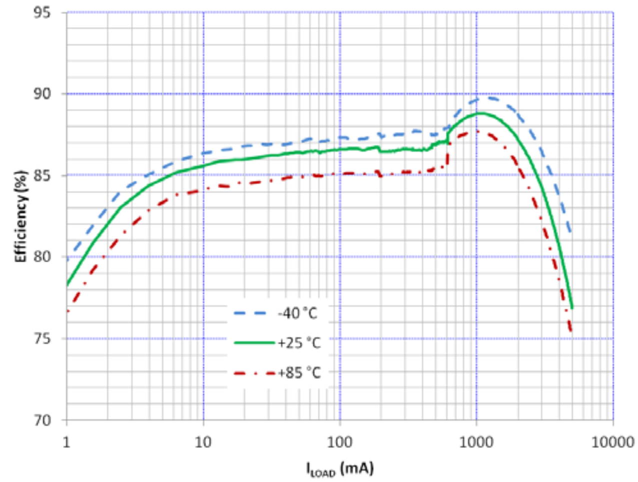


Figure 11. Efficiency vs I_{LOAD} and Temperature V_{OUT} = 1.15 V

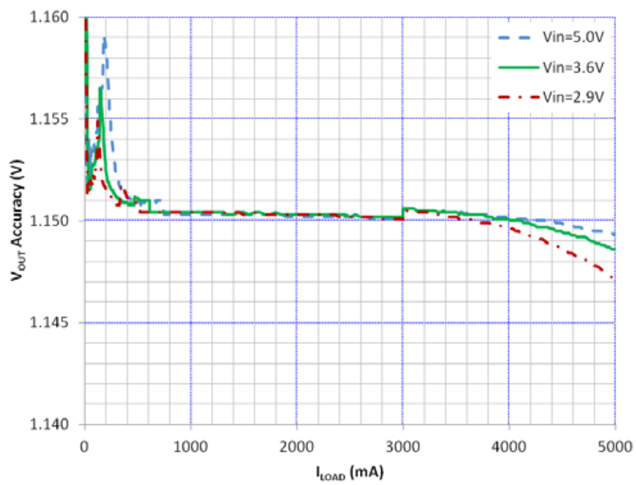


Figure 12. V_{OUT} Accuracy vs I_{LOAD} and V_{IN} V_{OUT} = 1.15 V

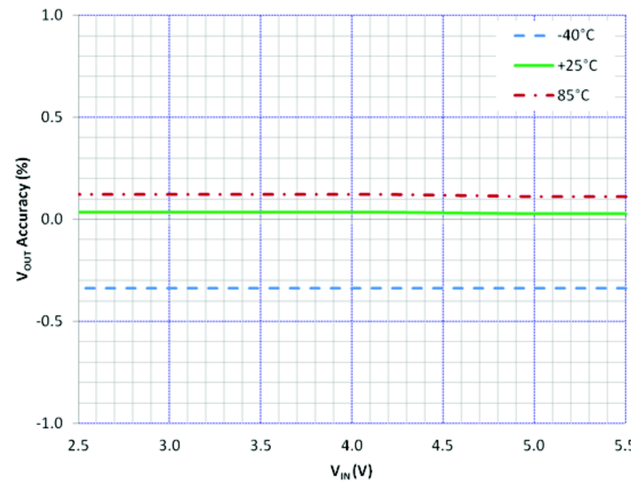


Figure 13. V_{OUT} Accuracy vs V_{IN} and Temperature, V_{OUT} = 1.15 V

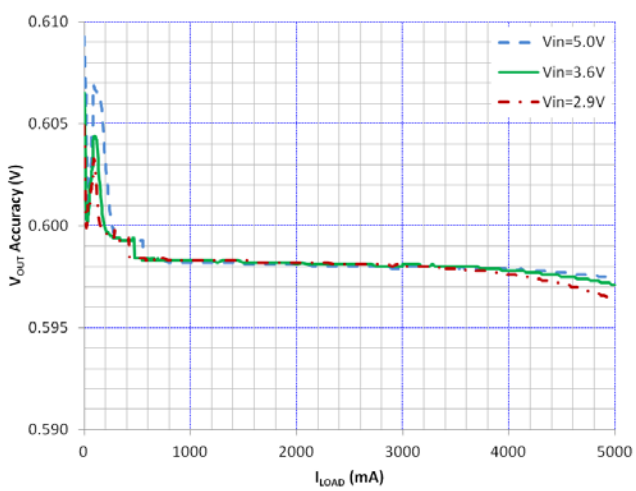


Figure 14. V_{OUT} Accuracy vs I_{LOAD} and V_{IN} V_{OUT} = 0.60 V

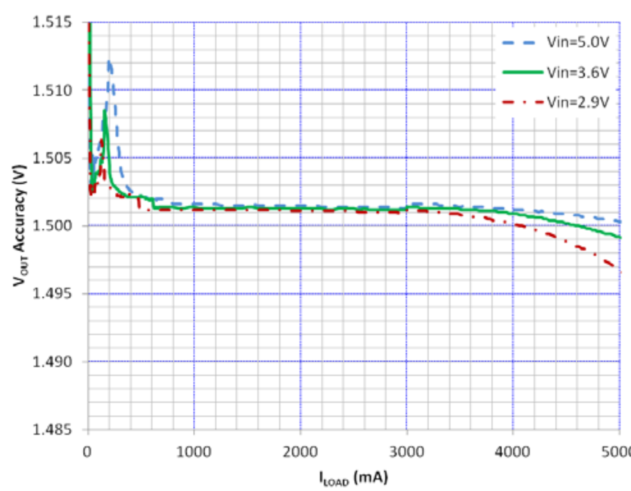


Figure 15. V_{OUT} Accuracy vs I_{LOAD} and V_{IN} V_{OUT} = 1.50 V

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6$ V, $T_J = +25°C$, DCDC = 1.15 V, Ipeak = 3.9 A (Unless otherwise noted). L = 0.33 μH PIFE25201B – $C_{OUT} = 47$ μF 0603, $C_{IN} = 4.7$ μF 0603

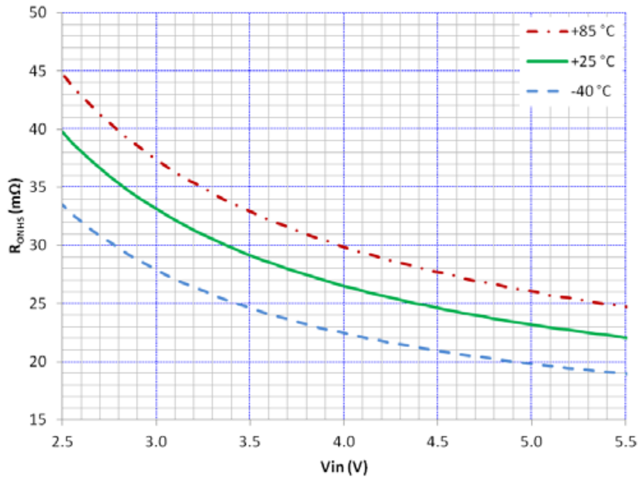


Figure 16. HSS R_{ON} vs V_{IN} and Temperature

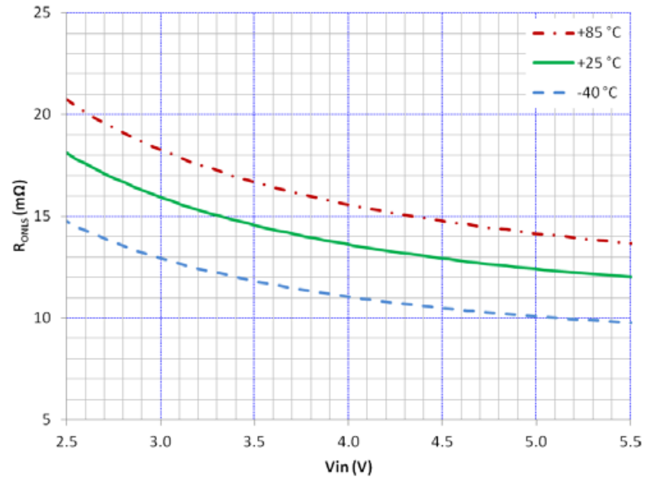


Figure 17. LSS R_{ON} vs V_{IN} and Temperature

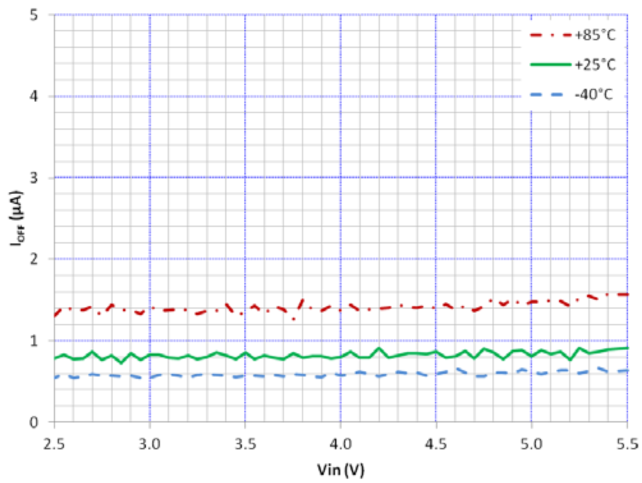


Figure 18. I_{OFF} vs V_{IN} and Temperature

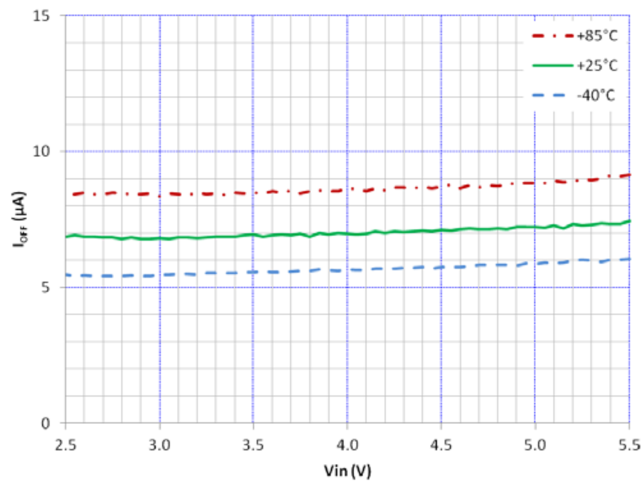


Figure 19. I_{SLEEP} vs V_{IN} and Temperature

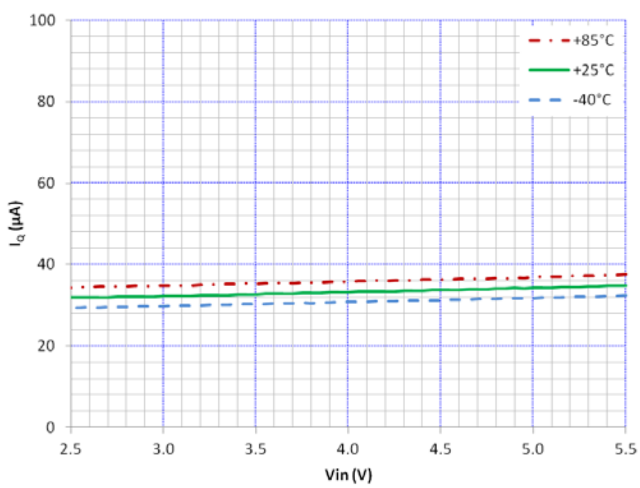


Figure 20. $I_{Q\ PFM}$ vs V_{IN} and Temperature

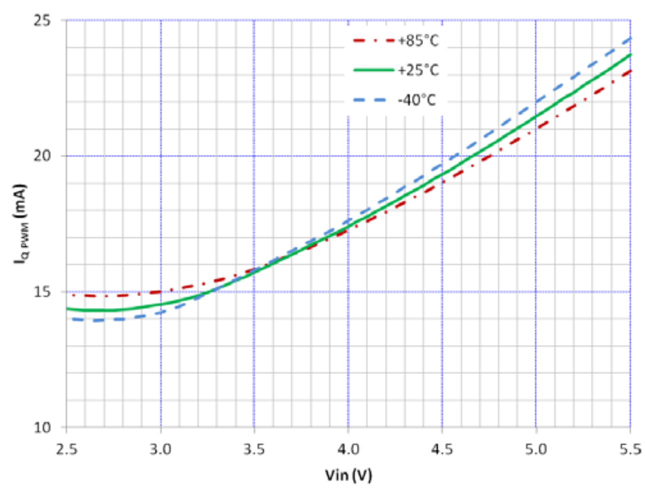


Figure 21. $I_{Q\ PWM}$ vs V_{IN} and Temperature

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN} = 3.6$ V, $T_J = +25°C$, DCDC = 1.15 V, Ipeak = 3.9 A (Unless otherwise noted). L = 0.33 μH PIFE25201B – C_{OUT} = 47 μF 0603, C_{IN} = 4.7 μF 0603

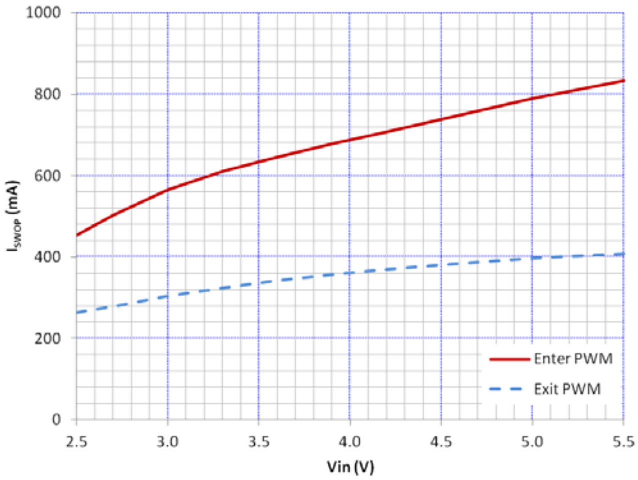


Figure 22. Switchover Point V_{OUT} = 1.15 V

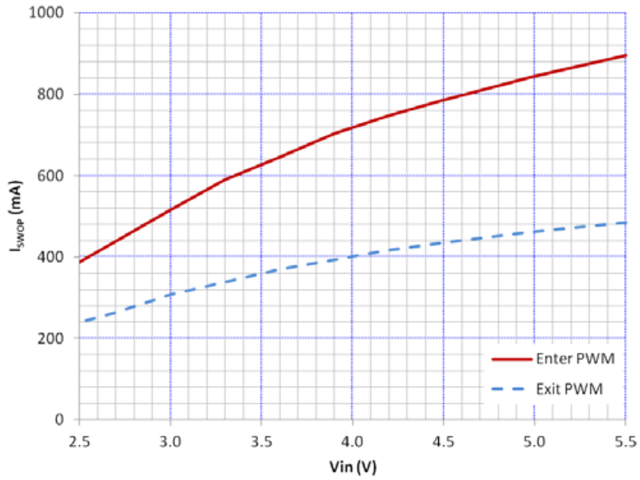


Figure 23. Switchover Point V_{OUT} = 1.50 V

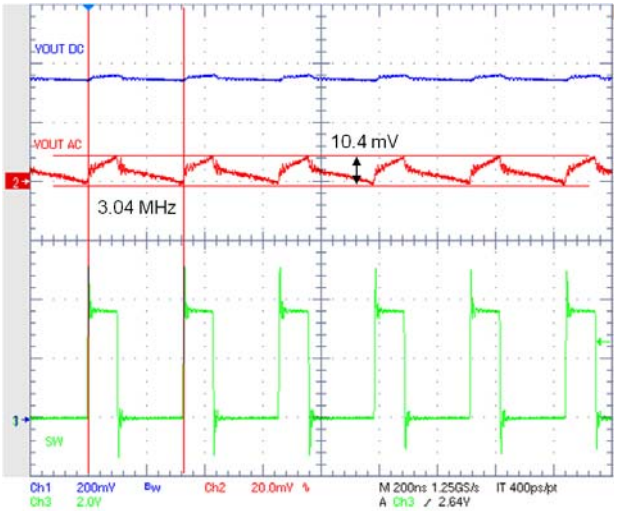


Figure 24. PWM Ripple

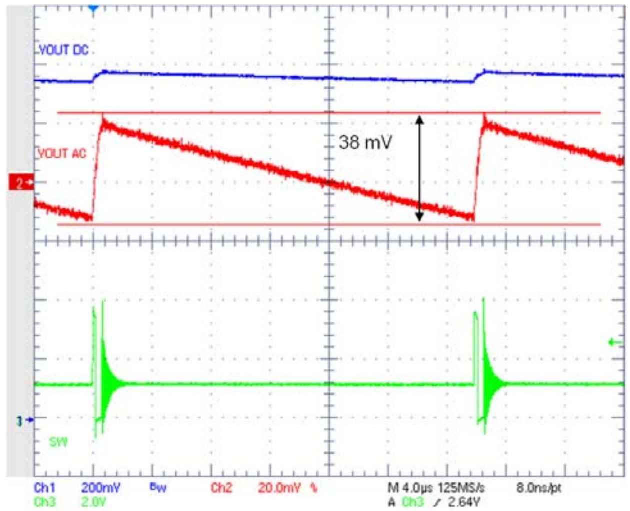


Figure 25. PFM Ripple

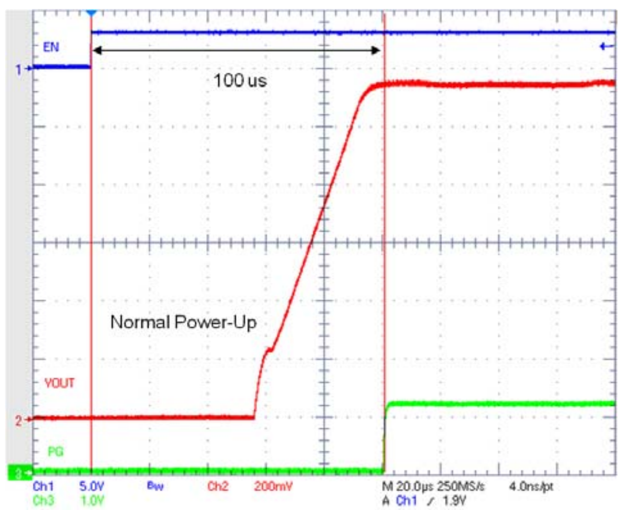


Figure 26. Normal Power Up, V_{OUT} = 1.15 V

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN}$ = 3.6 V, T_J = +25°C, DCDC = 1.15 V, Ipeak = 3.9 A (Unless otherwise noted). L = 0.33 μH PIFE25201B – C_{OUT} = 47 μF 0603, C_{IN} = 4.7 μF 0603

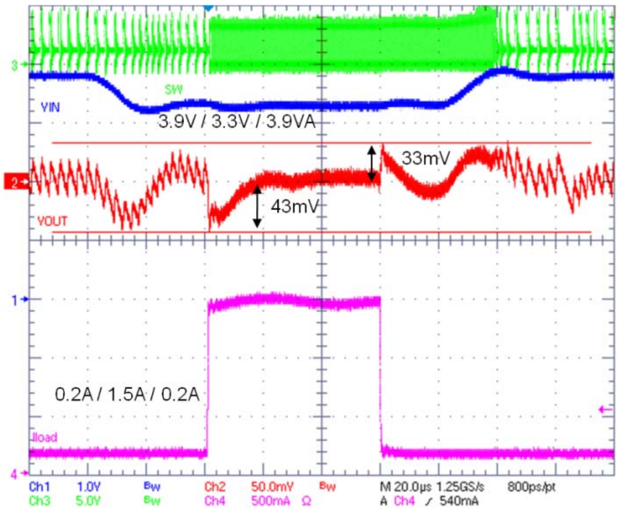


Figure 27. Transient Load 0.2 to 1.5 A Transient Line 3.9 − 3.3 V Auto Mode

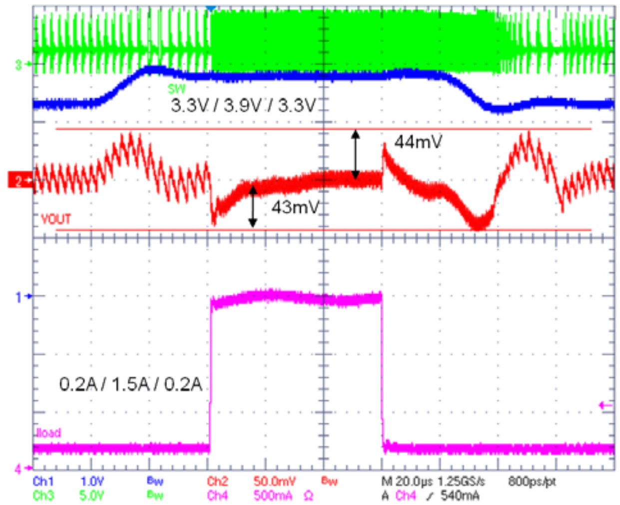


Figure 28. Transient Load 0.2 to 1.5 A Transient Line 3.3 − 3.9 V Auto Mode

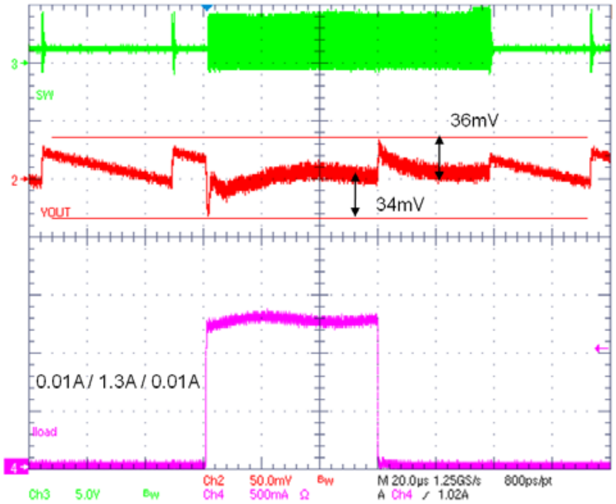


Figure 29. Transient Load 0.01 to 1.3 A Auto Mode

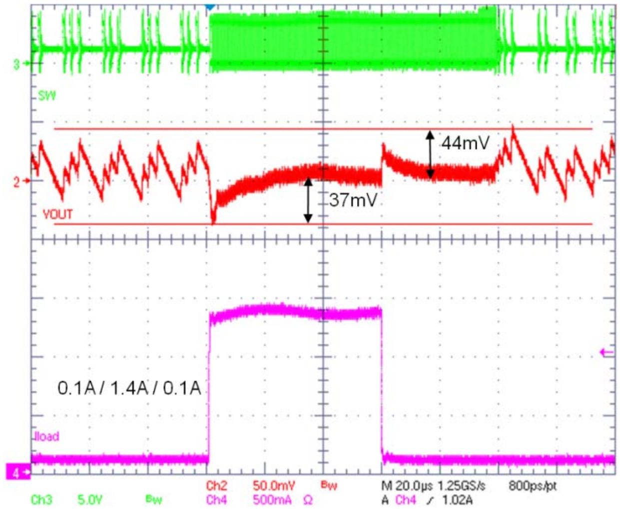


Figure 30. Transient Load 0.1 to 1.4 A Auto Mode

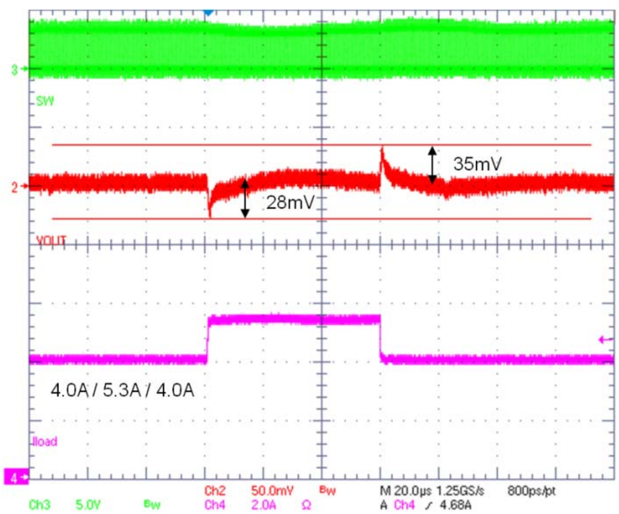


Figure 31. Transient Load 4 to 5.3 A Auto Mode

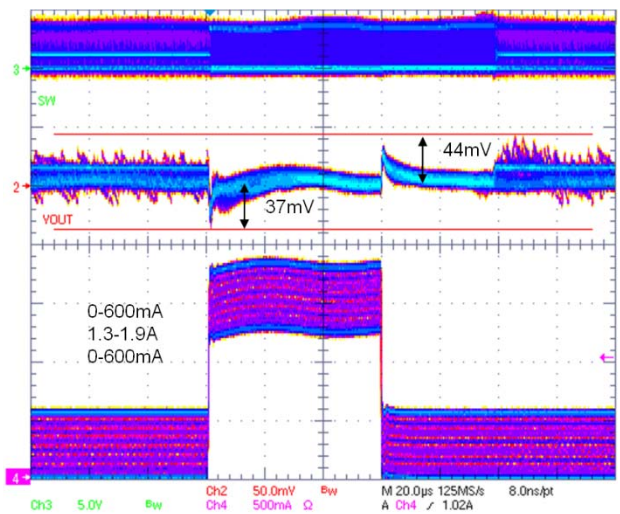


Figure 32. Transient Load 0 mA – 600 mA to 1.3 A − 1.9 A Auto Mode

DETAILED OPERATING DESCRIPTION

Detailed Descriptions

The NCP6336 is voltage mode stand−alone synchronous DC to DC converter optimized to supply different sub systems of portable applications powered by one cell Li−Ion or three cells Alkaline/NiCd/NiMh. The IC can deliver up to 5 A at an I^2C selectable voltage ranging from 0.6 V to 1.50 V. It can share the same output rail with another DC to DC converter and works as a transient load helper without sinking current on shared rail. A 3 MHz switching frequency allows the use of smaller output filter components. Synchronous rectification and automatic PWM/PFM transitions improve overall solution efficiency. Forced PWM is also configurable. Operating modes, configuration, and output power can be easily selected either by using digital I/O pins or by programming a set of registers using an I^2C compatible interface capable of operation up to 3.4 MHz. Default I^2C settings are factory programmable.

DC to DC Converter Operation

The converter is a synchronous rectifier type with both high side and low side integrated switches. Neither external transistor nor diodes are required for NCP6336 operation. Feedback and compensation network are also fully integrated. The converter can operate in two different modes: PWM and PFM. The transition between PWM/PFM modes can occur automatically or the switcher can be placed in forced PWM mode by I^2C programming (PWMVSEL0 / PWMVSEL1 bits of COMMAND register).

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, NCP6336 operates in PWM mode from a fixed clock and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM. The internal N−MOSFET switch operates as synchronous rectifier and is driven complementary to the P−MOSFET switch. In CCM, the lower switch (N−MOSFET) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the NCP6336 operates in PFM mode as the inductor current drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N−MOSFET operates as synchronous rectifier after each P−MOSFET on−pulse. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM mode.

Forced PWM

The NCP6336 can be programmed to only use PWM and disable the transition to PFM if so desired.

Output Stage

NCP6336 is a 3.5 A to 5.0 A output current capable integrated DC to DC converter. To supply such a high current, the internal MOSFETs need to be large.

Inductor Peak Current Limitation

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrain inductor power. The user can select peak current to keep inductor within its specifications. The peak current can be set by writing IPEAK[1..0] bits in LIMCONF register.

Table 1. IPEAK VALUES

IPEAK[1..0]	Inductor Peak Current (A)
00	5.2 − for 3.5 output current
01	5.8 − for 4.0 output current
10	6.2 − for 4.5 output current
11	6.8 − for 5.0 output current

Output Voltage

Output voltage is set internally by integrated resistor bridge and error amplifier that drives the PWM/PFM controller. No extra component is needed to set output voltage. However, writing in the VoutVSEL0[6..0] bits of the PROGVSEL0 register or VoutVSEL1[6..0] bits of the PROGVSEL1 register will change settings. Output voltage level can be programmed in the 0.6 V to 1.5 V range by 10 mV steps.

The VSEL pin and VSELGT bit will determine which register between PROGVSEL0 and PROGVSEL1 will set the output voltage.

- If VSELGT = 1 AND VSEL=0 → Output voltage is set by VoutVSEL0[6..0] bits (PROGVSEL0 register)
- Else → Output voltage is set by VoutVSEL1[6..0] bits (PROGVSEL1 register)

Under Voltage Lock Out (UVLO)

NCP6336 core does not operate for voltages below the Under Voltage Lock Out (UVLO) level. Below UVLO threshold, all internal circuitry (both analog and digital) is held in reset.

NCP6336 operation is guaranteed down to VUVLO when battery voltage is dropping off. To avoid erratic on / off behavior, a maximum 200 mV hysteresis is implemented. Restart is guaranteed at 2.5 V when VBAT voltage is recovering or rising.

Thermal Management

Thermal Shutdown (TSD)

The thermal capability of IC can be exceeded due to step down converter output stage power level. A thermal protection circuitry is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shut down, output voltage is turned off.

When NCP6336 returns from thermal shutdown, it can re−start in 2 different configurations depending on REARM bit in the LIMCONF register (see register description section):

- If REARM = 0 then NCP6336 does not re−start after TSD. To restart, an EN pin toggle is required.
- If REARM = 1, NCP6336 re−starts with register values set prior to thermal shutdown.

A Thermal shut down interrupt is raised upon this event.

Thermal shut down threshold is set at 150°C (typical) when the die temperature increases and, in order to avoid erratic on / off behavior, a 30°C hysteresis is implemented. After a typical 150°C thermal shut down, NCP6336 will resume to normal operation when the die temperature cools to 120°C.

Thermal Warnings

In addition to the TSD, the die temperature monitoring will flag potential die over temperature. A thermal warning and thermal pre−warning sensor and interrupts are implemented. These can inform the processor that NCP6336 is closed to its thermal shutdown, so preventive measures to cool down die temperature can be taken by software.

The Warning threshold is set by hardware to 135°C typical when the die temperature increases. The Pre−Warning threshold is set by default to 105°C, but can be changed by user by setting the TPWTH[1..0] bits in the LIMCONF register.

Active Output Discharge

To make sure that no residual voltage remains in the power supply rail when disabled, an active discharge path can ground the NCP6336 output voltage.

For maximum flexibility, this feature can be easily disabled or enabled with DISCHG bit in PGOOD register. By default the discharge path is enabled.

However the discharged path is activated during the first 100 μs after battery insertion.

Enabling

The EN pin controls NCP6336 start up. EN pin Low to High transition starts the power up sequencer. If EN is made low, the DC to DC converter is turned off and device enters:

- In Sleep Mode if Sleep_Mode I^2C bit is high or VSEL is high,
- In Off Mode if Sleep_Mode I^2C bit and VSEL are low.

When EN pin is set to a high level, the DC to DC converter can be enabled / disabled by writing the ENVSEL0 or ENVSEL1 bit of the PROGVSEL0 and PROGVSEL1 registers: If ENx I^2C bit is high, DC to DC converter is activated, If ENx I^2C is low the DC to DC converter is turned off and device enters in Sleep Mode

A built in pull down resistor disables the device when this pin is left unconnected or not driven. EN pin activity does not generate any digital reset.

Power Up Sequence (PUS)

In order to power up the circuit, the input voltage AVIN has to rise above the VUVLO threshold. This triggers the internal core circuitry power up which is the “Wake Up Time” (including “Bias Time”).

This delay is internal and cannot be bypassed. EN pin transition within this delay corresponds to the “Initial power up sequence” (IPUS):

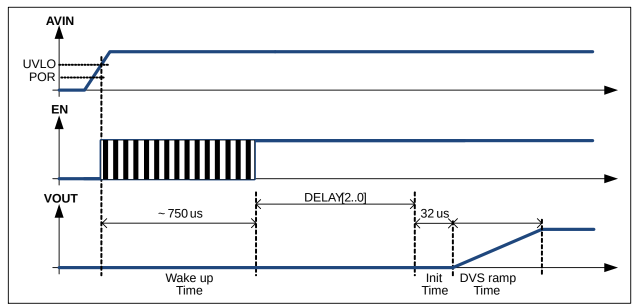


Figure 33. Initial Power Up Sequence

In addition a user programmable delay will also take place between end of Core circuitry turn on (Wake Up Time and Bias Time) and Init time: The DELAY[2..0] bits of TIME register will set this user programmable delay with a 2 ms resolution. With default delay of 0 ms, the NCP6336 IPUS takes roughly 900 μs, means DC to DC converter output voltage will be ready within 1 ms.

The power up output voltage is defined by VSEL state.

NOTE: During the Wake Up time, the I^2C interface is not active. Any I^2C request to the IC during this time period will result in a NACK reply.

Normal, Quick and Fast Power Up Sequence

The previous description applies only when the EN transitions during the internal core circuitry power up (Wake up and calibration time). Otherwise 3 different cases are possible:

- Enabling the part by setting EN pin from Off Mode will result in “Normal power up sequence” (NPUS, with DELAY;[2..0]).
- Enabling the part by setting EN pin from Sleep Mode will result in “Quick power up sequence” (QPUS, with DELAY;[2..0]).

- Enabling the DC to DC converter, whereas EN is already high, either by setting ENVSEL0 or ENVSEL1 bits or by VSEL pin transition will results in “Fast power up sequence” (FPUS, without DELAY[2..0]).

Sleep mode is when VSEL is high and EN low, or when Sleep_Mode I^{2}C bit is set and EN is low, or finally when DC to DC converter is off and EN high.

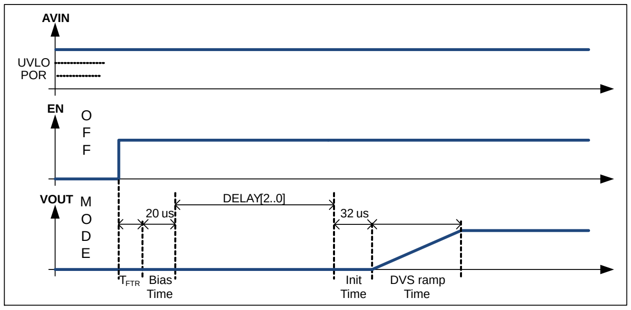


Figure 34. Normal Power Up Sequence

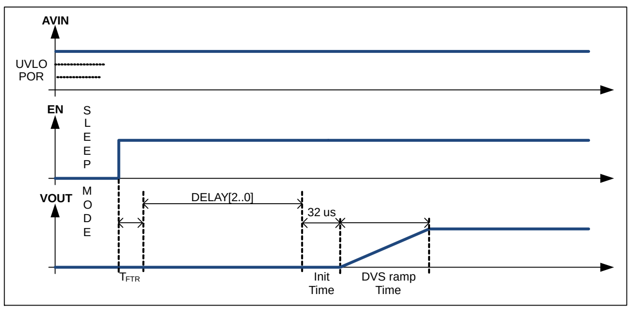


Figure 35. Quick Power Up Sequence

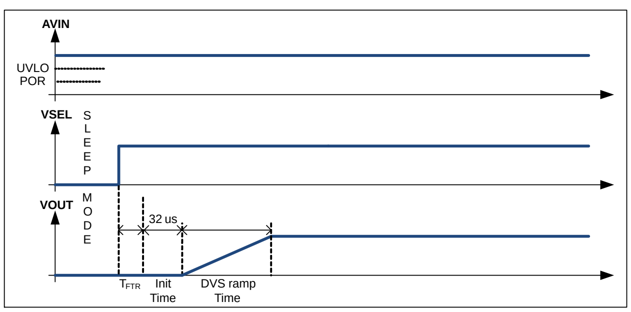


Figure 36. Fast Power Up Sequence

In addition the delay set in DELAY[2..0] bits in TIME register will apply only for the EN pins turn ON sequence (NPUS and QPUS).

The power up output voltage is defined by VSEL state.

Note that the sleep mode needs about 150 μs to be established.

DC to DC Converter Shut Down

When shutting down the device, no shut down sequence is required. Output voltage is disabled and, depending on the DISCHG bit state of PGOOD register, output may be discharged.

DC to DC converter shutdown is initiated by either grounding the EN pin (Hardware Shutdown) or, depending on the VSEL internal signal level, by clearing the ENVSEL0 or ENVSEL1 bits (Software shutdown) in PROGVSEL0 or PROGVSEL1 registers.

In hardware shutdown (EN = 0), the internal core is still active and I^{2}C accessible.

NCP6336 shuts internal core down when AVIN falls below UVLO.

Dynamic Voltage Scaling (DVS)

This converter supports dynamic voltage scaling (DVS) allowing the output voltage to be reprogrammed via I^{2}C commands and provides the different voltages required by the processor. The change between set points is managed in a smooth fashion without disturbing the operation of the processor.

When programming a higher voltage, output raises with controlled dV/dt defined by DVS[1..0] bits in TIME register. When programming a lower voltage the output voltage will decrease accordingly.

The DVS step is fixed and the speed is programmable.

DVS sequence is automatically initiated by changing output voltage settings. There are two ways to change these settings:

- Directly change the active setting register value (VoutVSEL0[6..0] of PROGVSEL0 register or VoutVSEL1[6..0] of the PROGVSEL1 register) via I^{2}C command
- Change the VSEL internal signal level by toggling VSEL pin.

The second method eliminates the I^{2}C latency and is therefore faster.

The DVS transition mode can be changed with the DVSMODE bit in COMMAND register:

- In forced PWM mode when accurate output voltage control is needed.

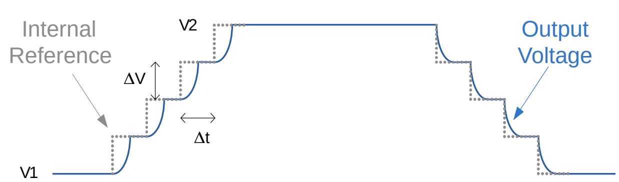


Figure 37. DVS in Forced PWM Mode Diagram

- In Auto mode when output voltage has not to be discharged. Note that approximately 30 μs is needed to transition from PFM mode to PWM mode.

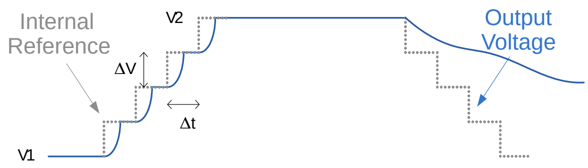


Figure 38. DVS in Auto Mode Diagram

Digital IO Settings

VSEL Pin

By changing VSEL pin levels, the user has a latency free way to change NCP6336 configuration: operating mode (Auto or PWM forced), the output voltage as well as enable.

Table 2. VSEL PIN PARAMETERS

Parameter VSEL Pin Can Set	REGISTER VSEL = LOW	REGISTER VSEL = HIGH
ENABLE	ENVSEL0 PROGVSEL0[7]	ENVSEL1 PROGVSEL1[7]
VOUT	VoutVSEL0[6..0]	VoutVSEL1[6..0]
OPERATING MODE (Auto / PWM Forced)	PWMVSEL0 COMMAND[7]	PWMVSEL1 COMMAND[6]

VSEL pin action can be masked by writing 0 to the VSELGT bit in the COMMAND register. In that case I^2C bit corresponding to VSEL high will be taken into account.

EN Pin

The EN pin can be gated by writing the ENVSEL0 or ENVSEL1 bits of the PROGVSEL0 and PROGVSEL1 registers, depending on which register is activated by the VSEL internal signal.

Power Good Pin (Optional)

To indicate the output voltage level is established, a power good signal is available.

The power good signal is low when the DC to DC converter is off. Once the output voltage reaches 95% of the expected output level, the power good logic signal becomes high and the open drain output becomes high impedance.

During operation when the output drops below 90% of the programmed level the power good logic signal goes low (and the open drain signal transitions to a low impedance state) which indicates a power failure. When the voltage rises again to above 95% the power good signal goes high again.

During a positive DVS sequence, when target voltage is higher than initial voltage, the Power Good logic signal will be set low during output voltage ramping and transition to high once the output voltage reaches 95% of the target voltage. When the target voltage is lower than the initial voltage, Power Good pin will remain at high level during transition.

Power Good signal during normal operation can be disabled by clearing the PGDCDC bit in PGOOD register.

Power Good operation during DVS can be controlled by setting / clearing the bit PGDVS in PGOOD register

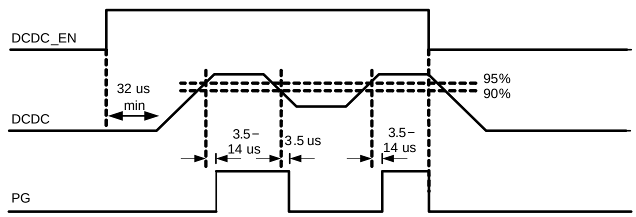


Figure 39. Power Good Signal

Power Good Delay

In order to generate a Reset signal, a delay can be programmed between the output voltage gets 95% of its final value and Power Good pin is released to high level.

The delay is set from 0 ms to 64 ms through the TOR[1..0] bits in the TIME register. The default delay is 0 ms.

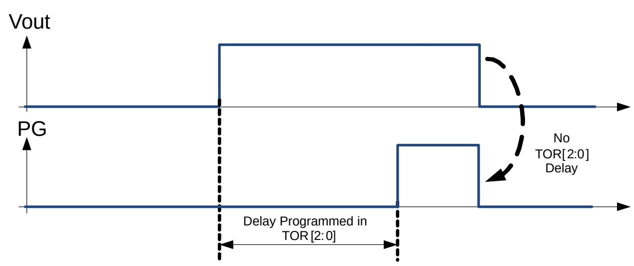


Figure 40. Power Good Operation

Interrupt Pin (Optional)

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring).

Table 3. INTERRUPT SOURCES

Interrupt Name	Description
TSD	Thermal Shut Down
TWARN	Thermal Warning
TPREW	Thermal Pre Warning
UVLO	Under Voltage Lock Out
IDCDC	DC to DC converter current Over / below limit
PG	Power Good

Individual bits generating interrupts will be set to 1 in the INT_ACK register (I^2C read only registers), indicating the interrupt source. INT_ACK register is automatically reset by an I^2C read. The INT_SEN register (read only register) contains real time indicators of interrupt sources.

All interrupt sources can be masked by writing in register INT_MSK. Masked sources will never generate an interrupt request on INTB pin.

The INTB pin is an open drain output. A non masked interrupt request will result in INTB pin being driven low.

When the host reads the INT_ACK registers the INTB pin is released to high impedance and the interrupt register INT_ACK is cleared.

Figure 41 is UVLO event example: INTB pin with INT_SEN/INT_MSK/INT_ACK and an I^2C read access behavior.

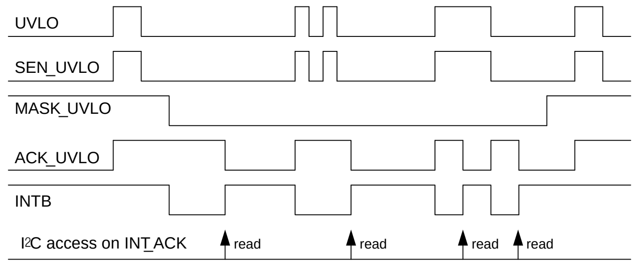


Figure 41. Interrupt Operation Example

INT_MSK register is set to disable INTB feature by default.

Configurations

Default output voltages, enables, DCDC modes, current limit and other parameters can be factory programmed upon request. Below is the default configurations pre−defined:

Configuration	NCP6336 − 5.0 A
Default I^2C address PID product identification RID revision identification FID feature identification	0x1C 14h xxh 00h
Default VOUT – VSEL=1	1.15 V
Default VOUT – VSEL=0	1.15 V
Default MODE – VSEL=1	Auto mode − ON
Default MODE – VSEL=0	Auto mode − ON
Default IPEAK	6.8 A
OPN	NCP6336FCCT1G
Marking	6336

I²C Compatible Interface

NCP6336 can support a subset of I²C protocol Detailed below.

I²C Communication Description

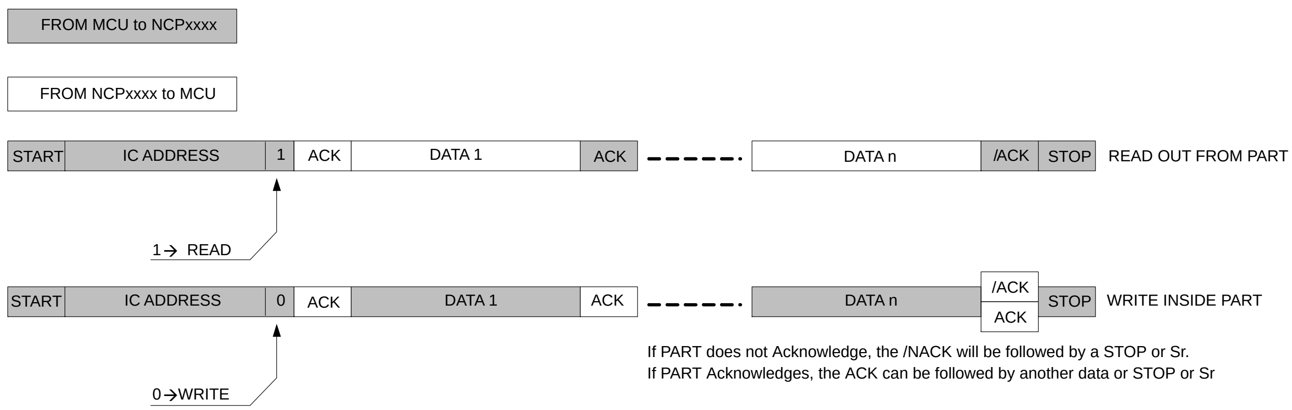


Figure 42. General Protocol Description

The first byte transmitted is the Chip address (with the LSB bit set to 1 for a read operation, or set to 0 for a Write operation). The following data will be:

- In case of a Write operation, the register address (@REG) pointing to the register we want to write in followed by the data we will write in that location. The writing process is auto−incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1 …, etc.
- In case of read operation, the NCP6336 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto−incremental.

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has pointed to:

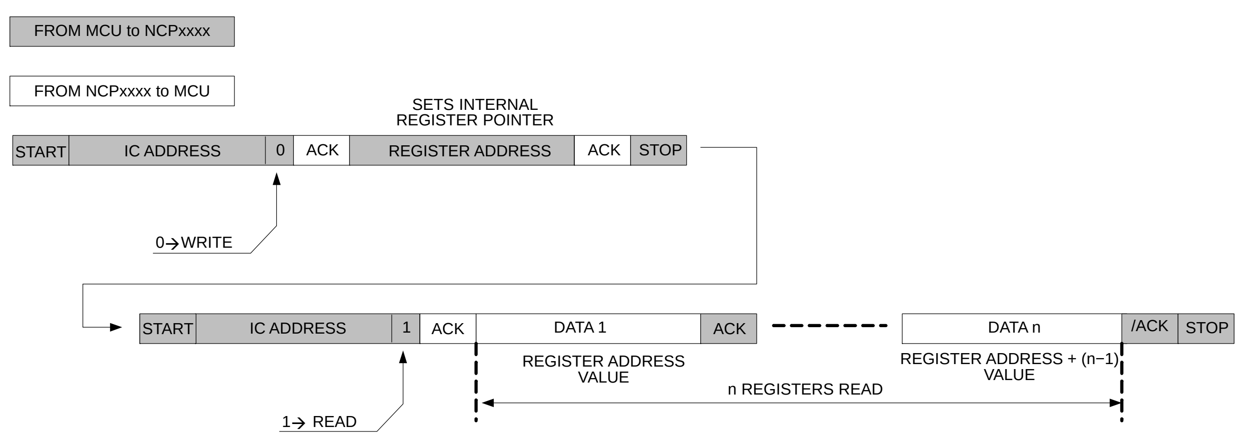


Figure 43. Read Out from Part

The first WRITE sequence will set the internal pointer to the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

With Stop Then Start

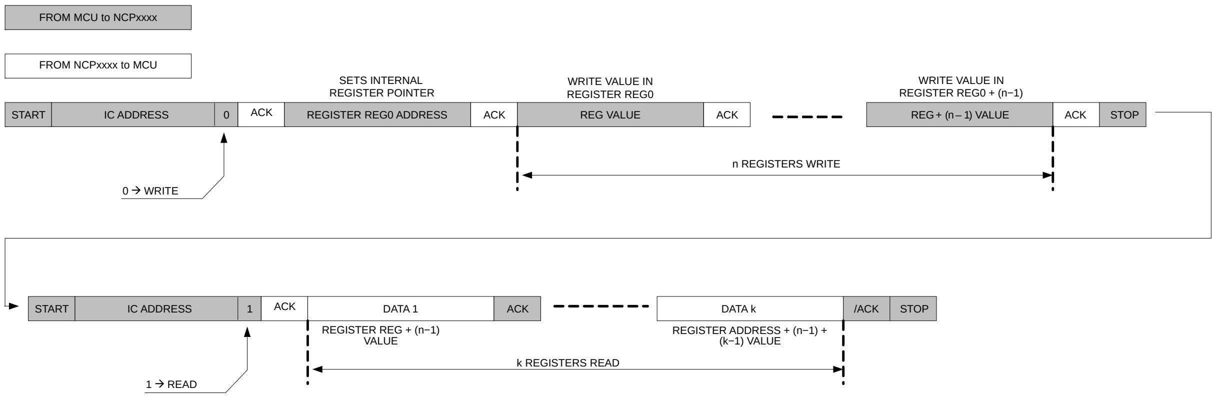


Figure 44. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, …, Reg +n.

Write n Registers:

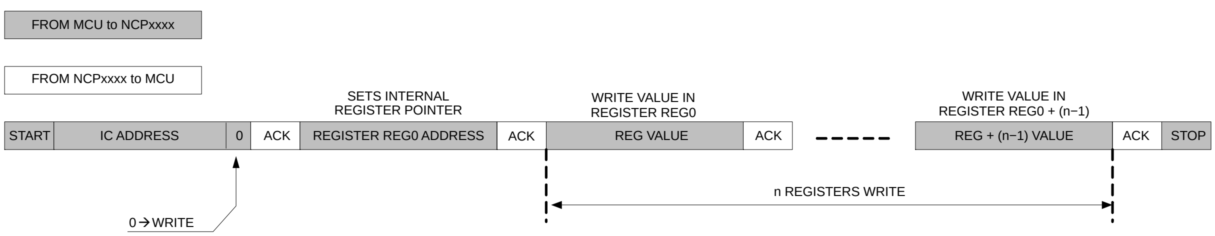


Figure 45. Write in n Registers

I²C Address

NCP6336 has four available I²C address selectable by factory settings (ADD0 to ADD3). Different address settings can be generated upon request to ON Semiconductor. The default address is set to 38h / 39h since the NCP6336 supports 7−bit address only and ignores A0.

Table 4. I²C ADDRESS

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0	W 0x20 R 0x21	0	0	1	0	0	0	0	R/W
	Add	0x10							−
ADD1	W 0x28 R 0x29	0	0	1	0	1	0	0	R/W
	Add	0x14							−
ADD2	W 0x30 R 0x31	0	0	1	1	0	0	0	R/W
	Add	0x18							−
ADD3 (default)	W 0x38 R 0x39	0	0	1	1	1	0	0	R/W
	Add	0x1C							−

Register Map

Table 5 describes I²C registers.

Registers / bits can be:

R	Read only register
RC	Read then Clear
RW	Read and Write register
Reserved	Address is reserved and register/bit is not physically designed
Spare	Address is reserved and register/bit is physically designed

Table 5. I²C REGISTERS MAP 5 A CONFIGURATION (NCP6336)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK	RC	00h	Interrupt register
01h	INT_SEN	R	00h	Sense register (real time status)
02h	INT_MSK	RW	FFh	Mask register to enable or disable interrupt sources (trim)
03h	PID	R	14h	Product Identification
04h	RID	R	Metal	Revision Identification
05h	FID	R	00h	Features Identification (trim)
06h to 0Fh	–	–	–	Reserved for future use
10h	PROGVSEL1	RW	B7h	Output voltage settings and EN for VSEL pin = High (trim)
11h	PROGVSEL0	RW	B7h	Output voltage settings and EN for VSEL pin = Low (trim)
12h	PGOOD	RW	10h	Power good and active discharge settings (trim)
13h	TIME	RW	09h	Enabling and DVS timings (trim)
14h	COMMAND	RW	01h	Enabling and Operating mode Command register (trim)
15h	MODULE	RW	80h	Active module count settings (test)
16h	LIMCONF	RW	E3h	Reset and limit configuration register (trim)
17h to 1Fh	–	–	–	Reserved for future use
20h to FFh	–	–	–	Reserved. Test Registers

Registers Description

Table 6. INTERRUPT ACKNOWLEDGE REGISTER

Name: INTACK				**Address: 00h**			
Type: RC				**Default: 00000000b (00h)**			
Trigger: Dual Edge [D7..D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ACK_TSD	ACK_TWARN	ACK_TPREW	Spare = 0	Spare = 0	ACK_UVLO	ACK_IDCDC	ACK_PG

Bit	Bit Description
ACK_PG	Power Good Sense Acknowledgement 0: Cleared 1: DCDC Power Good Event detected
ACK_IDCDC	DCDC Over Current Sense Acknowledgement 0: Cleared 1: DCDC Over Current Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected
ACK_TPREW	Thermal Pre Warning Sense Acknowledgement 0: Cleared 1: Thermal Pre Warning Event detected
ACK_TWARN	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 7. INTERRUPT SENSE REGISTER

Name: INTSEN				**Address: 01h**			
Type: R				**Default: 00000000b (00h)**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_TSD	SEN_TWARN	SEN_TPREW	Spare = 0	Spare = 0	SEN_UVLO	SEN_IDCDC	SEN_PG

Bit	Bit Description
SEN_PG	Power Good Sense 0: DCDC Output Voltage below target 1: DCDC Output Voltage within nominal range
SEN _IDCDC	DCDC over current sense 0: DCDC output current is below limit 1: DCDC output current is over limit
SEN _UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold
SEN _TPREW	Thermal Pre Warning Sense 0: Junction temperature below thermal pre−warning limit 1: Junction temperature over thermal pre−warning limit
SEN _TWARN	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN _TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 8. INTERRUPT MASK REGISTER

Name: INTMASK				**Address: 02h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MASK_TSD	MASK_TWARN	MASK_TPREW	Spare = 1	Spare = 1	MASK_UVLO	MASK_IDCDC	MASK_PG

Bit	Bit Description
MASK_PG	Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MASK _IDCDC	DCDC over current interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MASK _UVLO	Under Voltage interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MASK _TPREW	Thermal Pre Warning interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MASK _TWARN	Thermal Warning interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MASK _TSD	Thermal Shutdown interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 9. PRODUCT ID REGISTER

Name: PID				**Address: 03h**			
Type: R				**Default: 00010100b (14h)**			
Trigger: N/A				**Reset on N/A**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Table 10. REVISION ID REGISTER

Name: RID				**Address: 04h**			
Type: R				**Default: Metal**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Bit	Bit Description
RID[7..0]	Revision Identification 00000000: First silicon

Table 11. FEATURE ID REGISTER

Name: FID				Address: 05h			
Type: R				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare	Spare	Spare	Spare	FID_3	FID_2	FID_1	FID_0

Bit	Bit Description
FID[3..0]	Feature Identification 00000000: NCP6336 5.0 A configuration

Table 12. DC TO DC VOLTAGE PROG (VSEL = 1) REGISTER

Name: PROGVSEL1				Address: 10h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ENVSEL1	VoutVSEL1[6..0]						

Bit	Bit Description
VoutVSEL1[6..0]	Sets the DC to DC converter output voltage when VSEL pin = 1 and VSEL pin function is enabled in register COMMAND.D0, or when VSEL pin function is disabled in register COMMAND.D0 0000000b = 600 mV – 1011010b = 1500 mV (steps of 10 mV) 1011011b to 1111111b Reserved
ENVSEL1	EN Pin Gating for VSEL internal signal = High 0: Disabled 1: Enabled

Table 13. DC TO DC VOLTAGE PROG (VSEL = 0) REGISTER

Name: PROGVSEL0				Address: 11h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ENVSEL0	VoutVSEL0[6..0]						

Bit	Bit Description
VoutVSEL0[6..0]	Sets the DC to DC converter output voltage when VSEL pin = 0 and VSEL pin function is enabled in register COMMAND.D0 0000000b = 600 mV – 1011010b = 1500 mV (steps of 10 mV) 1011011b to 1111111b Reserved
ENVSEL0	EN Pin Gating for VSEL internal signal = Low 0: Disabled 1: Enabled

Table 14. POWER GOOD REGISTER

Name: PGOOD				Address: 12h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	Spare = 0	Spare = 0	DISCHG	TOR[1..0]		PGDVS	PGDCDC

Bit	Bit Description
PGDCDC	Power Good Enabling 0 = Disabled 1 = Enabled
PGDVS	Power Good Active On DVS 0 = Disabled 1 = Enabled
TOR[1..0]	Time out Reset settings for Power Good 00 = 0 ms 01 = 8 ms 10 = 32 ms 11 = 64 ms
DISCHG	Active discharge bit Enabling 0 = Discharge path disabled 1 = Discharge path enabled

Table 15. TIMING REGISTER

Name: TIME				Address: 13h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
DELAY[2..0]			DVS[1..0]		Spare = 0	DBN_Time[1..0]	

Bit	Bit Description
DBN_Time[1..0]	EN and VSEL debounce time 00 = No debounce 01 = 1−2 μs 10 = 2−3 μs 11 = 3−4 μs
DVS[1..0]	DVS Speed 00 = 10 mV step / 0.333 μs 01 = 10 mV step / 0.666 μs 10 = 10 mV step / 1.333 μs 11 = 10 mV step / 2.666 μs
DELAY[2..0]	Delay applied upon enabling (ms) 000b = 0 ms − 111b = 14 ms (Steps of 2 ms)

Table 16. COMMAND REGISTER

Name: COMMAND				**Address: 14h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PWMVSEL0	PWMVSEL1	DVSMODE	Sleep_Mode	Spare = 0	Spare = 0	Spare = 0	VSELGT

Bit	Bit Description
VSELGT	VSEL Pin Gating 0 = Disabled 1 = Enabled
Sleep_Mode	Sleep mode 0 = Low Iq mode when EN and VSEL low 1 = Force product in sleep mode (when EN and VSEL are low)
DVSMODE	DVS transition mode selection 0 = Auto 1 = Forced PWM
PWMVSEL1	Operating mode for VSEL internal signal = High 0 = Auto 1 = Forced PWM
PWMVSEL0	Operating mode for VSEL internal signal = Low 0 = Auto 1 = Forced PWM

Table 17. OUTPUT STAGE MODULE SETTINGS REGISTER

Name: MODULE				**Address: 15h**			
Type: RW				**Default: 10000000b (80h)**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MODUL[3..0]				Spare = 0	Spare = 0	Spare = 0	Spare = 0

Bit	Bit Description
MODUL [3..0]	Number of modules 0000 = 1 Module 0001 = 2 Modules 0010 ~ 1111 = 9 Modules

Table 18. LIMITS CONFIGURATION REGISTER

Name: LIMCONF				**Adress: 16h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IPEAK[1..0]		TPWTH[1..0]		Spare = 0	Spare = 0	RSTSTATUS	REARM

Bit	**Bit Description**
REARM	Rearming of device after TSD 0: No re−arming after TSD 1: Re−arming active after TSD with no reset of I^2C registers: new power−up sequence is initiated with previously programmed I^2C registers values
RSTSTATUS	Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)
TPWTH[1..0]	Thermal pre−Warning threshold settings 00 = 83°C 01 = 94°C 10 = 105°C 11 = 116°C
IPEAK	Inductor peak current settings 00 = 5.2 A (for 3.5 A output current) 01 = 5.8 A (for 4.0 A output current) 10 = 6.2 A (for 4.5 A output current) 11 = 6.8 A (for 5.0 A output current)

APPLICATION INFORMATION

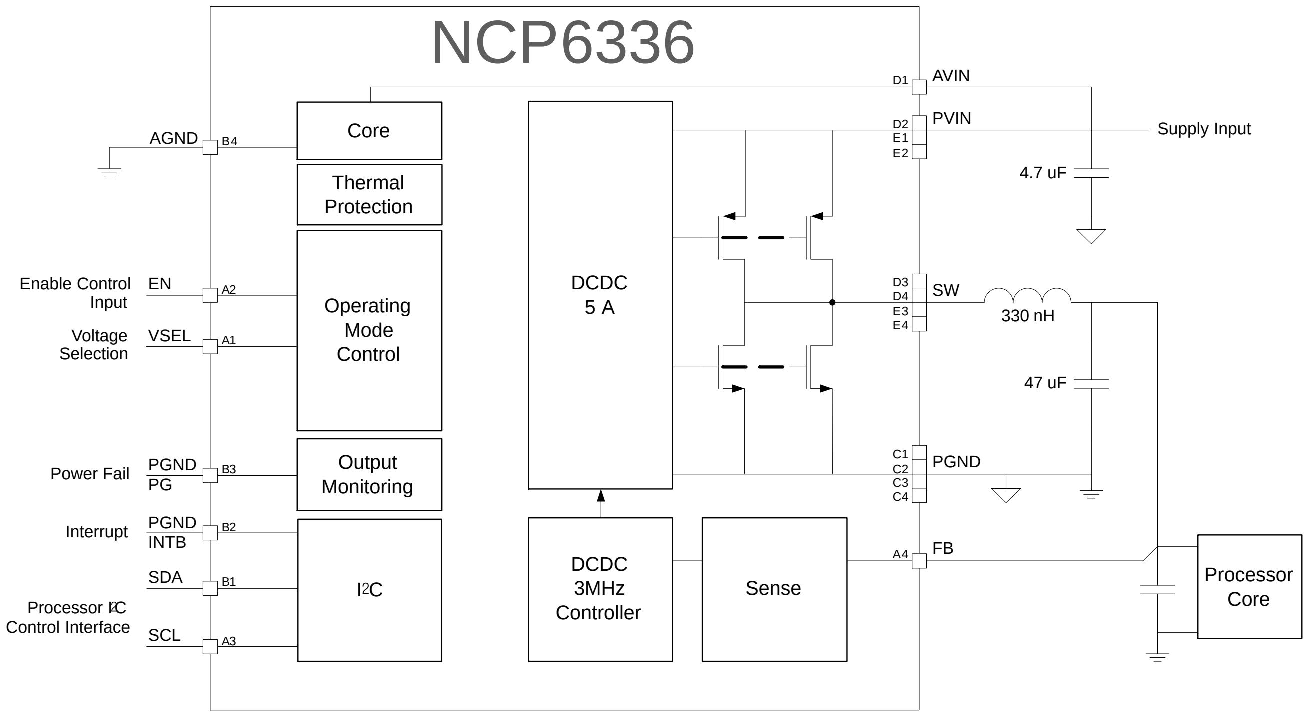


Figure 46. Typical Application Schematic

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of:

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \qquad \text{(eq. 1)}$$

The NCP6336 internal compensation network is optimized for a typical output filter comprising a 330 nH inductor and 47 μF capacitor as described in the basic application schematic shown in Figure 46.

Voltage Sensing Considerations

In order to regulate power supply rail, NCP6336 should sense its output voltage. Thanks to the FB pin, the IC can support two sensing methods:

- Normal case: the voltage sensing is achieved close to the output capacitor. In that case, FB is connected to the output capacitor positive terminal (voltage to regulate).
- Remote sensing: In remote sensing, the power supply rail sense is made close to the system powered by the NCP6336. The voltage to system is more accurate, since PCB line impedance voltage drop is within the regulation loop. In that case, we recommend connecting the FB pin to the system decoupling capacitor positive terminal.

Components Selection

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current I_{L_PP} of approximately 20% to 50% of the maximum output current I_{OUT_MAX} for a trade−off between transient response and output ripple. The inductance corresponding to the given current ripple is:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L\_PP}} \qquad \text{(eq. 2)}$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2} \qquad \text{(eq. 3)}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 19 shows recommended.

Table 19. INDUCTOR SELECTION

Supplier	Part #	Value (μH)	Size (mm) (L x l x T) (mm)	Saturation Current Max (A)	DCR Max at 25°C (mΩ)
Cyntec	PIFE20161B−R33MS−11	0.33	2.0 x 1.6 x 1.2	4.0	33
Cyntec	PIFE25201B−R33MS−11	0.33	2.5 x 2.0 x 1.2	5.2	17
Cyntec	PIFE32251B−R33MS−11	0.33	3.2 x 2.5 x 1.2	6.5	14
TOKO	DFE201612P−H−R30M	0.30	2.0 x 1.6 x 1.2	4.8	29
TOKO	DFE252012P−H−R33M	0.33	2.5 x 2.0 x 1.2	5.2	24
TOKO	FDSD0412−H−R33M	0.33	4.2 x 4.2 x 1.2	7.5	19
TDK	VLS252012HBX−R33M	0.33	2.5 x 2.0 x 1.2	5.3	25
TDK	SPM5030T−R35M	0.35	7.1 x 6.5 x 3.0	14.9	4

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be used. For a given peak−to−peak ripple current I_{L_PP} in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as below.

$$V_{OUT\_PP} \approx V_{OUT\_PP(C)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(ESL)}, \quad \text{(eq. 4)}$$

Where $V_{OUT\_PP(C)}$ is a ripple component by an equivalent total capacitance of the output capacitors, $V_{OUT\_PP(ESR)}$ is a ripple component by an equivalent ESR of the output capacitors, and $V_{OUT\_PP(ESL)}$ is a ripple component by an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUT\_PP(C)} = \frac{I_{L\_PP}}{8 \cdot C \cdot f_{SW}}, \quad \text{(eq. 5)}$$

and

$$V_{OUT\_PP(ESR)} = I_{L\_PP} \cdot ESR \quad \text{(eq. 6)}$$

$$V_{OUT\_PP(ESL)} = \frac{ESL}{ESL + L} \cdot V_{IN} \quad \text{(eq. 7)}$$

and the peak−to−peak ripple current is

$$I_{L\_PP} \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot L} \quad \text{(eq. 8)}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT\_PP(C)}$. So that the minimum output capacitance can be calculated regarding to a given output ripple requirement V_{OUT_PP} in PWM operation mode.

$$C_{MIN} = \frac{I_{L\_PP}}{8 \cdot V_{OUT\_PP} \cdot f_{SW}} \quad \text{(eq. 9)}$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding to the input ripple voltage V_{IN_PP} is

$$C_{IN\_MIN} = \frac{I_{OUT\_MAX} \cdot \left(D - D^2\right)}{V_{IN\_PP} \cdot f_{SW}} \quad \text{(eq. 10)}$$

where

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 11)}$$

In addition, the input capacitor needs to be able to absorb the input current, which has a RMS value of

$$I_{IN\_RMS} = I_{OUT\_MAX} \cdot \sqrt{D - D^2} \quad \text{(eq. 12)}$$

The input capacitor also needs to be sufficient to protect the device from over voltage spike, and normally at least 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC. All PGNDs are connected together to the ground terminal of the input cap which then connects to the ground plane. All PVIN are connected together to the Vbat terminal of the input cap which then connects to the Vbat plane.

Electrical Layout Considerations

Good electrical layout is a key to ensuring proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as PVIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper, but compact because it is also a noise source.

- It would be good to have separated ground planes for PGND and AGND and connect the two planes at one point. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense, and make it surrounded by a ground plane.

Thermal Layout Considerations

Good PCB layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Use two layers for the high current paths (PVIN, PGND, SW) in order to split current in two different paths and limit PCB copper self heating.

(See demo board example Figure 48)

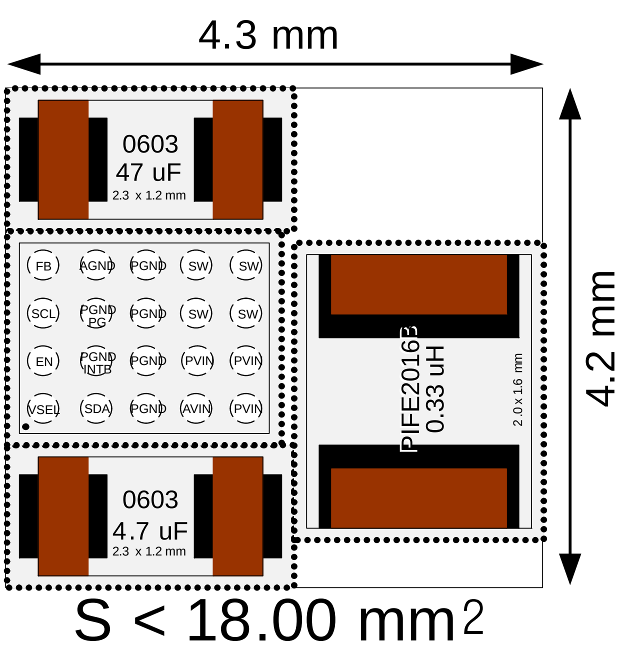


Figure 47. Layout Recommendation

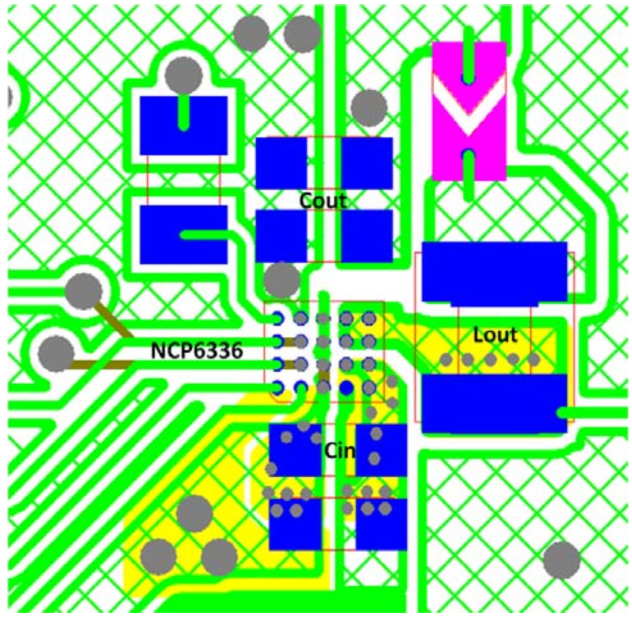


Figure 48. Demo Board Example

Input capacitor placed as close as possible to the IC.

PVIN directly connected to Cin input capacitor, and then connected to the Vin plane. Local mini planes used on the top layer (green) and layer just below top layer (yellow) with laser vias.

AVIN connected to the Vin plane just after the capacitor.

AGND directly connected to the GND plane.

PGND directly connected to Cin input capacitor, and then connected to the GND plane: Local mini planes used on the top layer (green) and layer just below top layer (yellow) with laser vias.

SW connected to the Lout inductor with local mini planes used on the top layer (green) and layer just below top layer (yellow) with laser vias.

Legend:
In green are top layer planes and wires
In yellow are layer1 plane and wires (just below top layer)
Big circles gray are normal vias
Small circles gray are top to layer1 vias

ORDERING INFORMATION

Device	Marking	Configuration	Package	Shipping†
NCP6336FCCT1G	6336	5 A 1.15 V	WLCSP20 2.02 x 1.62 mm (Pb–Free)	3000 / Tape & Reel

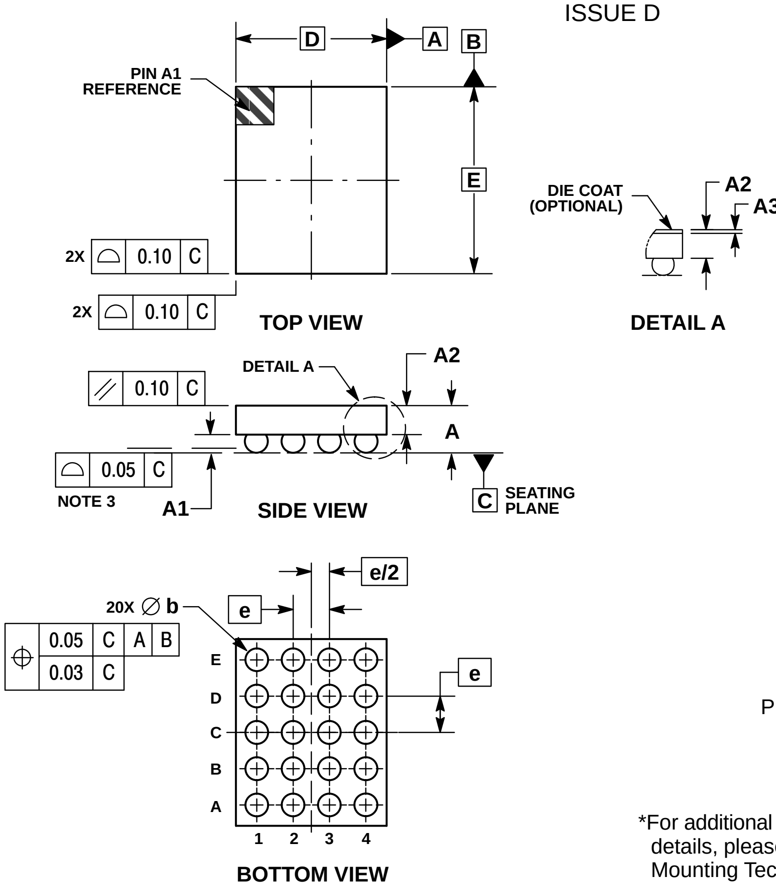
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Demo Board Available:

The NCP6336GEVB/D evaluation board that configures the device in typical application to supply constant voltage.

PACKAGE DIMENSIONS

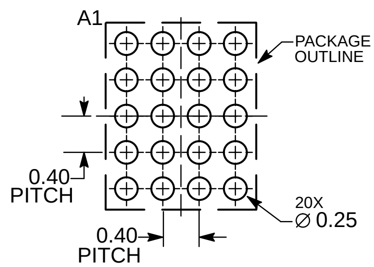
WLCSP20, 1.62x2.02
CASE 568AG
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.17	0.23
A2	0.33	0.39
A3	0.02	0.04
b	0.24	0.28
D	1.62 BSC	
E	2.02 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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