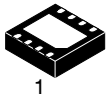
LDO Regulator, 500 mA, Low Iq, Wide Input with Power Good and Programmable Delay

Product Preview

NCP734



DFNW8
CASE 507AD

The NCP734 offers ideal combination of high performance and reach feature set which make this LDO suitable for various industrial applications. The wide input voltage up to 38 V and output voltage up to 35 V is very useful for powering device from low power MCUs up to high performance motor drivers. Low quiescent current 13 μA allows to extend device battery life and design more efficient always−on devices. The power good feature with programmable delay brings additional safety for industrial applications. The NCP734 is available in thermal enhanced 3 mm x 3 mm DFN8 package. The device is stable with small 4.7 μF MLCC output capacitor.

Features

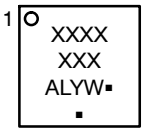
- Operating Input Voltage Range: 2.7 V to 38 V
- Available in Adjustable Voltage Option: 1.2 V to 35 V
- Available in Fixed Voltage Option: 3.3 V, 5 V
- Typ. ±1 % Accuracy
- Ultra−Low Quiescent Current Typ. 13 μA
- Standby Current 1 μA
- Very Low Dropout: 300 mV at 500 mA
- Operating Temperature: −40°C to 125°C
- Stable with a 4.7 μF Small Case Size Ceramic Capacitors
- Available in DFNW8 3 mm x 3 mm with EP
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Test and Measurement Equipment
- Battery Power Tools
- IoT, Wireless Devices
- Smart Metering, Smart Grid
- Home Appliances

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

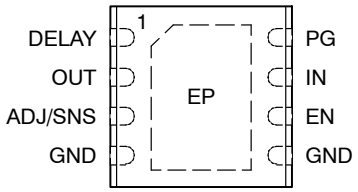
MARKING DIAGRAM



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

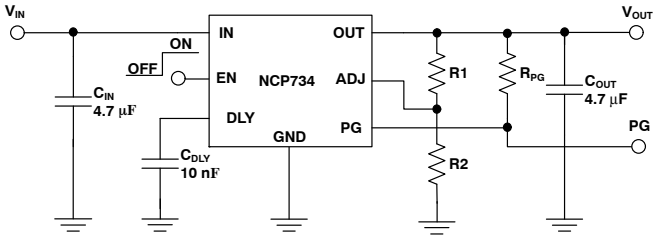
PIN CONNECTONS



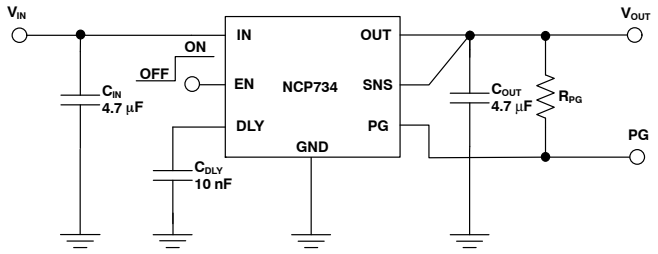
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

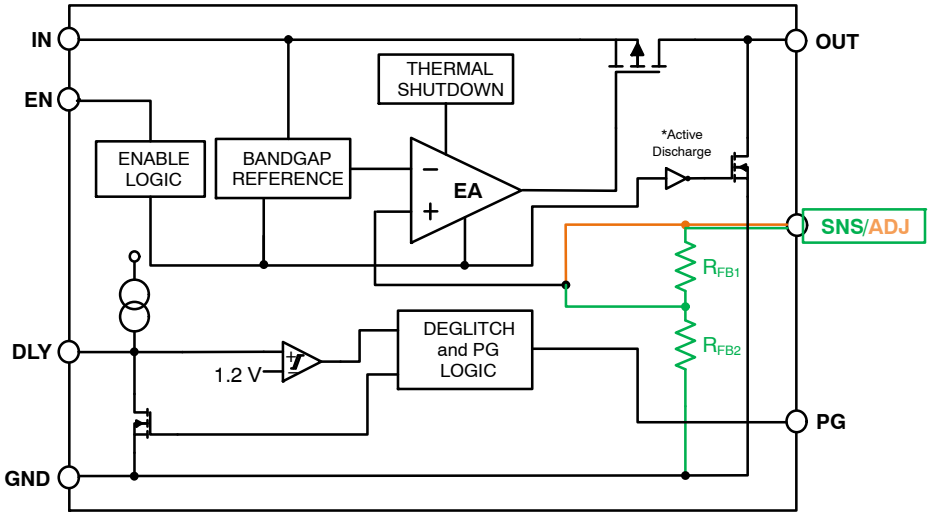


Adjustable voltage output



Fixed voltage output

Figure 1. Typical Application Schematics



*Active Discharge – Only A version

Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	DELAY	Delay pin. Connect a capacitor to GND to adjust power good delay or leave it unconnected to use default delay time – typ. 350 μs.
2	OUT	Regulated output voltage. Connect at least 4.7 μF ceramic capacitor to ensure stability.
3	SNS	Feedback pin. Connect to output. (Fixed)
	ADJ	Adjust pin. Connect resistor divider to set output voltage. (Adjustable)
4, 5	GND	Common ground connection
6	EN	Chip enable: Applying V_{EN} < 0.4 V disables the regulator, Pulling V_{EN} > 1.7 V enables the LDO.
7	IN	Input voltage supply pin
8	PG	Power Good. Open drain output – should be connected via pull−up resistor to V_{OUT}. This pin is pulled down when V_{OUT} goes under PG threshold limit
EP	EPAD	Expose pad can be tied to ground plane for better power dissipation or can be left floating.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 40	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 40	V
Chip Enable Input	V_{EN}	−0.3 to V_{IN} + 0.3, max. 40	V
Delay	V_{DELAY}	−0.3 to 2.4	V
Sense and Adjust Pin	V_{SNS}, V_{ADJ}	−0.3 to 6	V
Power Good Pin	V_{PG}	−0.3 to V_{IN} + 0.3, max. 40	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	TBD	°C/W
Thermal Resistance, Junction−to−Case (bottom)	$R_{\theta JC(bot)}$	TBD	°C/W
Thermal Resistance, Junction−to−Board (top)	$R_{\theta JB(top)}$	TBD	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	$\Psi_{JC(top)}$	3.5	°C/W
Thermal Characterization Parameter, Junction−to−Board (FEM)	Ψ_{JB}	8.9	°C/W

3. Measured according to JEDEC board specification, 2S2P board, 1 oz. copper. Detailed description of the board can be found in JESD51−7.

Table 4. ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 μF, C_{DLY} = 10 nF, V_{EN} = 1.2 V, unless otherwise noted. Typical values are at T_J = +25°C (Note 4))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.7		38	V
Under−Voltage Lockout	V_{IN} Falling until device turn−off		UVLO		2.55	2.6	V
UVLO Hysteresis			$UVLO_{HYS}$		50		mV
Output Voltage Accuracy	T_J = 25°C		V_{OUT}		1		%
	$V_{IN} = V_{OUT(NOM)}$ + 1 V to 38 V, 100 μA ≤ I_{OUT} ≤ 500 mA	$-40°C \le T_J \le 125°C$		−1.5		+1.5	
Reference voltage			V_{REF}		1.2		V
Output voltage range − Adjustable			V_{RANGE}	V_{REF}		35	V
ADJ Input Current	V_{ADJ} = 1.2 V		I_{ADJ}		0.01	TBD	μA
Line Regulation	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 38 V		$Line_{Reg}$		0.01	0.2	%Vout
Load Regulation	I_{OUT} = 1 mA to 500 mA		$Load_{Reg}$		0.15	0.4	%Vout
Dropout Voltage (Note 5)	I_{OUT} = 500 mA	V_{OUT} = 3.3 V	V_{DO}		300	TBD	mV
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	550	700	850	mA
Quiescent Current	V_{IN} = 2.7 V to 38 V, no load		I_Q		13	25	μA
Shutdown Current	V_{EN} = 0 V, V_{IN} = 38 V		I_{DIS}		1	TBD	μA
EN Pin Threshold Voltage	EN Input Voltage “L”		V_{ENL}			0.4	V
	EN Input Voltage “H”		V_{ENH}	1.2			
EN Pull Down Current	V_{EN} = 38 V, V_{IN} = 38 V		I_{EN}			1	μA
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$		t_{ON}		TBD		μs
Power Supply Rejection Ratio	I_{OUT} = 100 mA	f = 100 Hz	PSRR		75		dB
		f = 1 kHz			80		
		f = 100 kHz			45		
Output Voltage Noise	f = 10 Hz to 100 kHz		V_N		70		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		175		°C
	Temperature falling		T_{SDL}		160		
Active output discharge resistance	V_{EN} < 0.4 V, Version A only		R_{DIS}		100		Ω
PG Threshold	V_{OUT} falling		V_{PG-TH}	90	93	96	%
PG Hysteresis	V_{OUT} rising		$V_{PG-HYST}$		2		%
PG Delay Time	C_{DELAY} = floating		t_{PG-DLY}		350		μs
	C_{DELAY} = 10 nF		t_{PG-DLY_10nF}	8	10	12	ms
PG Deglitch Time			t_{PG_DG}		200		μs
PG Output Low Level Voltage	I_{OL} = 1 mA		V_{PG-OL}		0.2	0.4	V
PG leakage current	PG is pulled to V_{OUT} by 10 kΩ resistor		I_{PG-LK}		0.01	TBD	μA
C_{DELAY} charging current			$I_{CAP-CHRG}$		1.2		μA
DLY pin Threshold	DLY pin Voltage rising		V_{DLY_TH}	1.1	1.2	1.3	V
DLY pin Hysteresis	DLY pin Voltage falling		V_{DLY_HYST}		0.1		V
DLY pin voltage clamp	DLY pin floating		V_{DLY_CLAMP}		2.4		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

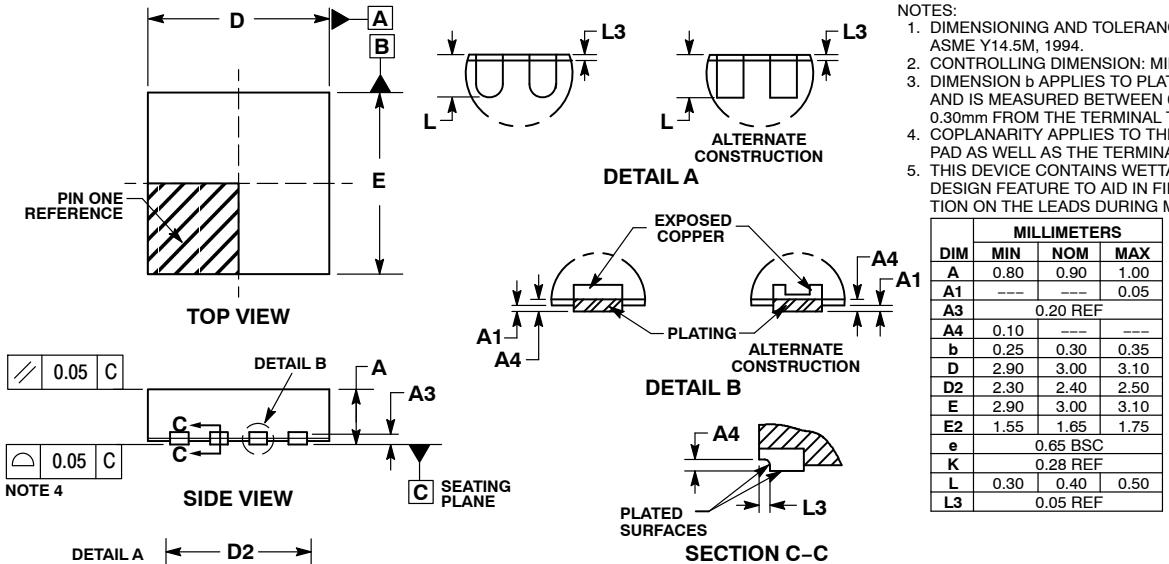
4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls -100 mV below $V_{OUT(NOM)}$.

ORDERING INFORMATION

Device	Output Voltage	Description	Marking	Package	Shipping
NCP734AML330TCG	3.3 V	500 mA, Active Discharge	TBD	DFNW8 CASE 507AD (Pb−Free)	TBD
NCP734AML500TCG	5.0 V		TBD		
NCP734AMLADJTCG	Adjustable		TBD		

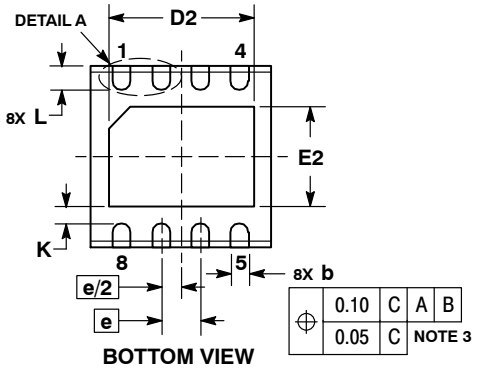
PACKAGE DIMENSIONS

DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

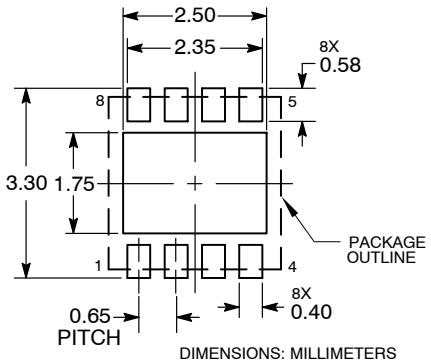


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	2.30	2.40	2.50
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
e		0.65 BSC	
K		0.28 REF	
L	0.30	0.40	0.50
L3		0.05 REF	



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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