NCP81031

Product Preview

Low Voltage Synchronous Buck Controller with Power Saving and Transient Enhancement Features

The NCP81031 is a simple single phase solution with differential phase current sensing, low current power saving mode of operation, and on board gate drivers to provide accurately regulated power. It can be set up to synchronize to an external clock or PWM signal within certain frequency range.

The adaptive non overlap gate drive and power saving operation circuit provide a low switching loss and high efficiency solution for server, notebook, and desktop systems. A high performance operational error amplifier is provided to simplify compensation of the system. The NCP81031 features include soft−start sequence, accurate overvoltage and over current protection, UVLO for VCC and VCCP, and thermal shutdown.

Features

- High Performance Operational Error Amplifier
- Internal Soft−Start/Stop
- ±0.5% internal Voltage Accuracy, 0.8 V voltage reference
- OCP accuracy, Four Re−entry Times Before Latch
- “Lossless” Differential Inductor Current Sensing
- Internal high precision current sensing amplifier
- Oscillator Frequency Range of 100 kHz − 1000 kHz
- 20 ns Adaptive FET Non−overlap Time of internal Gate Driver
- 5.0 V to 12 V Operation
- Support 1.5 V to 19 V V_{in}
- V_{out} from 0.8 V to 3.3 V (5 V with 12 V_{CC})
- Chip enable through OSC pin
- Latched Over Voltage Protection (OVP)
- Internally fixed OCP Threshold
- Guaranteed Startup Into Pre−Charged Loads
- Thermally Compensated Current Monitoring
- Thermal Shutdown Protection
- Integrated MOSFET Drivers
- Integrated BOOST diode with internal R_{bst} = 2.2 Ω
- Automatic Power Saving Mode to Maximize Efficiency During Light Load Operation
- Sync Function
- Remote Ground Sensing
- Enhanced Transient Protection
- This is a Pb−Free Device

Applications

- Desktop and Server Systems

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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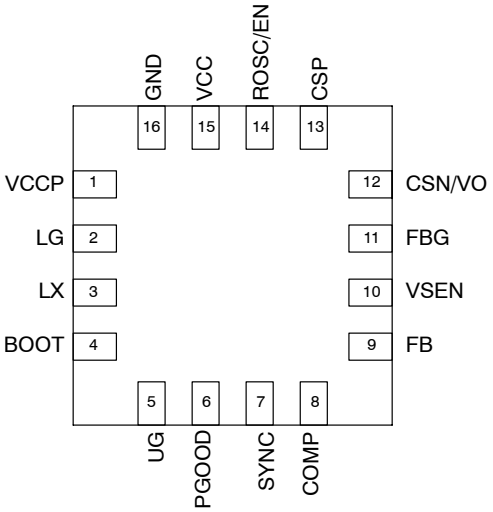
MARKING DIAGRAMS

QFN16
CASE 485G

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

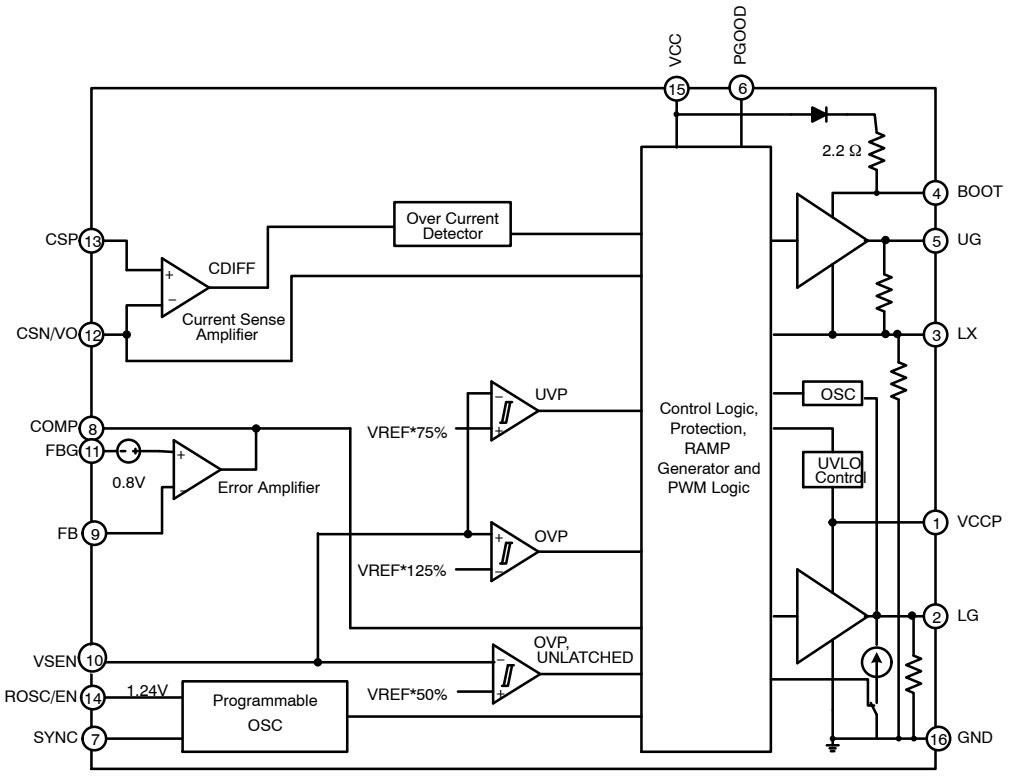


Figure 1. NCP81031 BLOCK DIAGRAM

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	VCCP	Power supply for MOSFET drivers
2	LG	Bottom gate MOSFET driver pin.
3	LX	Switch node
4	BOOT	Supply rail for the floating top gate drier.
5	UG	Top gate MOSFET driver pin.
6	PGOOD	Power Good. It is an open−drain output set free after SS (with 3x clock delay) as long as the output voltage monitored through VSEN is within specifications.
7	SYNC	Synchronization Pin. The controller synchronizes on the falling edge of a square wave provided to this pin. Short to GND if not used.
8	COMP	Output of the error amplifier. The device cannot be disabled by grounding this pin
9	FB	Inverting input to the error amplifier
10	VSEN	Output Voltage Sensing
11	FBG	Remote Ground Sense
12	CSN/VO	Inductor differential sense inverting input
13	CSP	Inductor differential sense non−inverting input
14	ROSC/EN	Programs the switching frequency; EN: Pull−low to disable the device
15	VCC	Supply rail for the controller internal circuitry.
16	GND	Ground reference
	THERMAL PAD	Connects with the Silicon substrate for good thermal contact with the PCB. Connect to GND plane

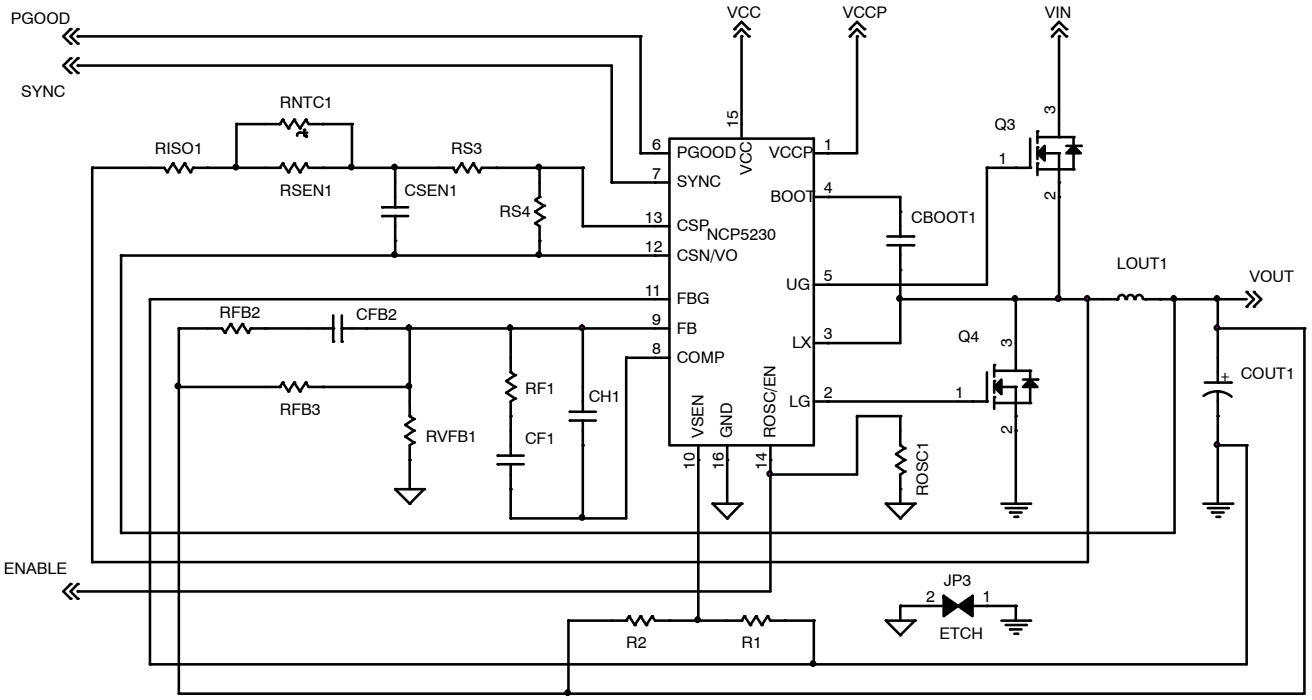


Figure 2. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	V_{MAX}	V_{MIN}	Unit
Controller Power Supply Voltages to GND	VCC, VCCP	15	−0.3	V
Boost Supply Voltage Input	BOOT	35V wrt/GND 40 V <100 ns wrt/GND 15 wrt/LX	−0.3	V
High−Side Driver Output (Top Gate)	UG	35 V 40 V ≤ 50 ns wrt/GND 15 wrt/LX	−0.3 wrt/LX −5 V < 200 ns	V
Switching Node (Bootstrap Supply Return)	LX	35 40 < 100 ns	−5 −10 V < 200 ns	V
Low−Side Driver Output (Bottom Gate)	LG	15 V	−0.3 −5 V < 200 ns	V
Logic Inputs	V_{LOGIC}	6	−0.3	V
All Other Pins		6	−0.3	V
PGOOD	PGOOD	7.0	−0.3	V
SYNC	SYNC	7.0	−0.3	V
Current Sense Amplifier	CSP, CSN/VO with V_{CC} = 12 V	10	−0.3	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Rating	Symbol	Typ	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	60	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	18	°C/W
Operating Junction Temperature Range	T_J	−40 to 125	°C
Operating Ambient Temperature Range	T_A	0 to 85	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	−

ELECTRICAL CHARACTERISTICS Unless otherwise stated: 0°C < T_A < 85°C; 4.5 V < VCC < 13.2 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY OPERATING CONDITIONS					
VCC Voltage Range		4.5		13.2	V
VCCP Voltage Range		4.5		13.2	V
dV/dt on VCC (Note 1)		−10		10	V/μs
dV/dt on VCCP (Note 1)		−10		10	V/μs
VCC AND BOOT INPUT SUPPLY CURRENT					
VCC Operating Current	V_{CC} = 5 V, EN = High V_{CC} = 12 V, EN = High			5.0	mA
VCC Quiescent Supply Current (low power mode)	V_{CC} = 5 V, EN = Low V_{CC} = 12 V, EN = Low			200	uA
VCCP INPUT SUPPLY CURRENT					
VCCP Operating Current UG and LG Open	V_{CCP} = 5 V, EN = High V_{CCP} = 12 V, EN = High		3.5	5.0	mA
VCCP Operating Current	V_{CCP} = 5 V, EN = Low V_{CCP} = 12 V, EN = Low			200	μA
VCC SUPPLY VOLTAGE					
VCC UVLO Start Threshold	V_{CC} Rising			4.45	V
VCC UVLO Hysteresis	V_{CC} Rising or Falling		300		mV
VCCP SUPPLY VOLTAGE					
VCCP UVLO Start Threshold				4.1	V
VCCP UVLO Hysteresis			200		mV
ERROR AMPLIFIER COMP					
Open Loop DC Gain (Note 1)			120		dB
Open Loop Unity Gain Bandwidth (Note 1)		15	18		MHz
Slew Rate (Note 1)	COMP pin to GND with 100 pF load		8		V/μs
VREF					
Internal Reference Voltage			0.800		V
Output Voltage Accuracy	Reference and Error Amplifier excluding external resistive divider tolerance, V_{out} to FBG	−0.5		0.5	%
CURRENT SENSE AMPLIFIERS					
Common Mode Input Voltage Range(Note 1, GNG, output within 10mV)	$V_{CC} \leq$ 7.5 V	−0.3	−	3.5	V

1. Guaranteed by design.
2. For propagation delays, ”tpdh” refers to the specified signal going high ”tpdl” refers to it going low. Reference Gate Timing Diagram.

ELECTRICAL CHARACTERISTICS Unless otherwise stated: 0°C < T_A < 85°C; 4.5 V < VCC < 13.2 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIERS					
Common Mode Input Voltage Range (Note 1, GNG, output within 10 mV)	V_{CC} > 7.5 V	−0.3	–	5.5	V
OSCILLATOR (with no ROSC Resistor Defaults to 200 kHz)					
Switching Frequency Accuracy	R_{OSC} open	−10	–	10	%
OSC Gain (Note 1)			10	–	kHz / μA
Disable threshold	R_{OSC}/EN pin, V_{dis_th}	–	–	0.75	V
MODULATORS (PWM Comparators)					
Minimum Pulse Width	F_{sw} = 200 kHz, OSC open		80		ns
Minimum Turn Off Time (LG on)	F_{sw} = 200 kHz, OSC open	250	300	400	ns
Magnitude of the PWM Ramp	V_{IN} = 5 V or 12 V		1.50		V
Maximum Duty Cycle	OSC/EN = OPEN	80	–	95	%
Minimum Skip mode frequency	In light load, maximum time for LG to turn on after HG turns off	30	–	–	kHz
SOFT−START					
Soft Start Time @ 200 kHz	1024 clock cycles, OSC/EN open		5.12		ms
SOFT−OFF					
Soft OFF bleeding resistor	R_{dis}		200		Ω
OVER CURRENT PROTECTION					
First Over Current Threshold	CSP−CSN, 4xMasking	17	20	23	mV
Second Over Current Threshold	CSP−CSN, Immediate action		30		mV
SYNC PIN					
Synchronization Input	VIL, square wave			1.0	V
Synchronization Input	VIH, square wave	2.5			V
PROTECTION AND PGOOD					
Output Voltage	Logic Low, Sinking 4 mA			0.4	V
OVP Threshold	VSEN rising above 1.25 * V_{ref}	120	125	130	%
UVP Threshold	VSEN falling below 0.75 * V_{ref}	70	75	80	%
Unlatched Overvoltage Threshold	V_{th_disoff} with respect to 0.5 V_{ref}	40	50	60	%
ZERO CURRENT DETECTION (LX Pin)					
Blanking Time before Zero Current Detection (Note 1)	Blanking Time after LG is < 1.0 V			40	ns
Capture Time for LX Voltage (Note 1)	Time to capture LX voltage once LG is < 1.0 V (must be within dead time limits)			20	ns
Negative LX detection voltage	V_{bdls}	200	300	400	mV
Positive LX detection voltage	V_{bdhs}	0.2	0.5	1	V
Time for V_{th} adjustment and settling time (Note 1)	300 kHz	3	–	3.7	μs
Initial Negative Current Detection Threshold Voltage Set Point (Note 1)	LX−GND, Includes ± 2 mV Offset Range	−6.0	−4.0	−2.0	mV
V_{th} adjustable Range (Note 1)		−16	0	15	mV

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ELECTRICAL CHARACTERISTICS Unless otherwise stated: 0°C < T_A < 85°C; 4.5 V < VCC < 13.2 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
HIGH SIDE DRIVER UG					
R_{H_TG} Output Resistance, Sourcing	V_{BOOT} − V_{LX} = 12 V, C_{load} = 3 nF		2.5	5	Ω
R_{H_TG} Output Resistance, Sinking	V_{BOOT} − V_{LX} = 12V		2	2.5	Ω
Tr_{DRVH} Transition Time	C_{LOAD} = 3 nF	–	16	–	ns
Tf_{DRVH} Transition Time	C_{LOAD} = 3 nF	–	11	–	
$Tpdh_{DRVH}$ Propagation Delay (Notes 1, 2)	Driving High, C_{LOAD} = 3 nF, V_{CC} = 12 V, V_{CCP} =12 V	10	20	30	ns
UG Internal Resistor to LX	Unbiased, BOOT − LX = 0		45		kΩ
LOW SIDE DRIVER LG					
R_{H_BG} Output Resistance, Sourcing	V_{LX} = GND, C_{load} = 3 nF		2	3	Ω
R_{L_BG} Output Resistance, Sinking	V_{LX} = V_{CC}		1	1.5	Ω
Tr_{DRVL} Transition Time	C_{LOAD} = 3 nF	–	16	–	ns
Tf_{DRVL} Transition Time	C_{LOAD} = 3 nF	–	11	–	
$Tpdh_{DRVL}$ Propagation Delay (Notes 1, 2)	Driving High, C_{LOAD} = 3 nF, V_{CCP} = 12 V, V_{CCP} = 12 V	TBD	18	TBD	ns
LX Internal Resistor to GND			45		kΩ
THERMAL SHUTDOWN					
T_{sd} Thermal Shutdown	(Note 1)	150	180	–	°C
T_{sdhys} Thermal Shutdown Hysteresis	(Note 1)		50		°C

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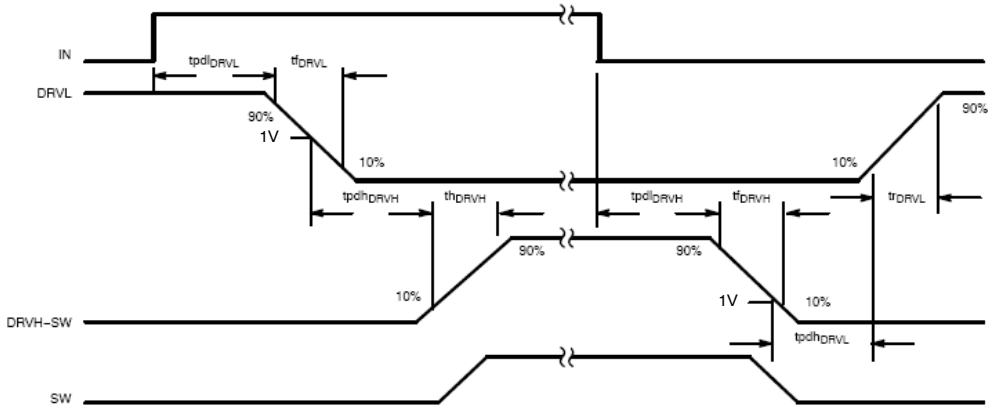


Figure 3. Gate Timing Diagram

Switching Frequency

Connecting a resistor from ROSC/EN to external voltage source V_{pu} will configure the frequency. Normal range would be 100 kHz to 1 MHz. With no resistor connected to the pin, the oscillator frequency is 200 kHz. The switching frequency will follow the relationship:

$$F_{SW} = 200\ kHz - \frac{V_{pu} - 1.240}{R_{OSC}} \cdot 10\frac{kHz}{\mu A} \qquad \text{(eq. 1)}$$

When R_{osc} = infinity (no resistor connected), F_{sw} = 200 kHz; when V_{pu} = ground, the frequency programmed will be higher than 200 kHz.

Soft−Start

Soft−Start will begin if VCC, VCCP are both above their UVLO threshold and EN pin is set free. IC initially waits a fixed delay time and then ramping−up the reference in 1024 clock cycles in closed−loop regulation. After digital soft start, PGOOD signal will be released with three clock cycles delay.

Protection active during soft−start:

- Overvoltage Protection always enabled;
- Undervoltage Protection is enabled after reference voltage ramps up to 80% of the final value. In soft−start, a UVP fault will directly restart a complete soft−start.

Synchronization Function

Synchronize through the SYNCH pin. Synchronization function allows different converters to share the same input filter reducing the resulting Irms and reducing the need for total caps to sustain the load. Synchronized systems also exhibits higher noise immunity and better regulation.

The device synchronizes the high−side MOSFET turn−on with the falling edge of the SYNCH pin input signal. In order for internal switching to track the external signal, the external signal has to fall within 0−40% frequency window above the internal frequency set by the OSC pin. SYNCH pin can be connected to other regulators' PWM, phase node, gate signals according to the desired phase−shift with proper voltage scaling.

Protection Scheme

- PGOOD
- Overvoltage Protection (OV)
- Undervoltage Protection (UV)
- PreOVP Protection, monitor CSN/VO when IC is disabled.
- V_{in} detection: If UV is triggered during SS, it will restart SS after a fixed delay.

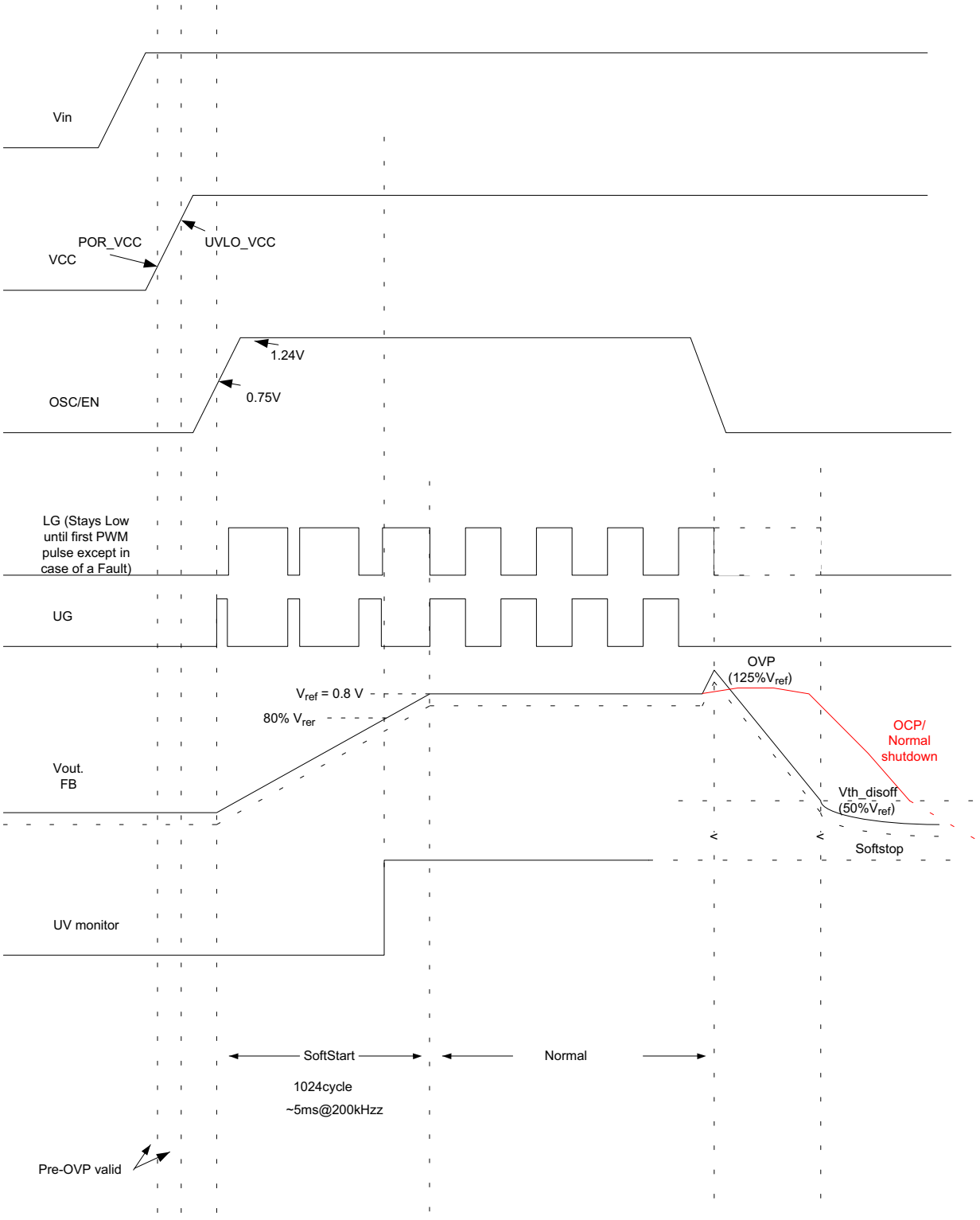


Figure 4. Start Up and Shutdown Timing Diagram

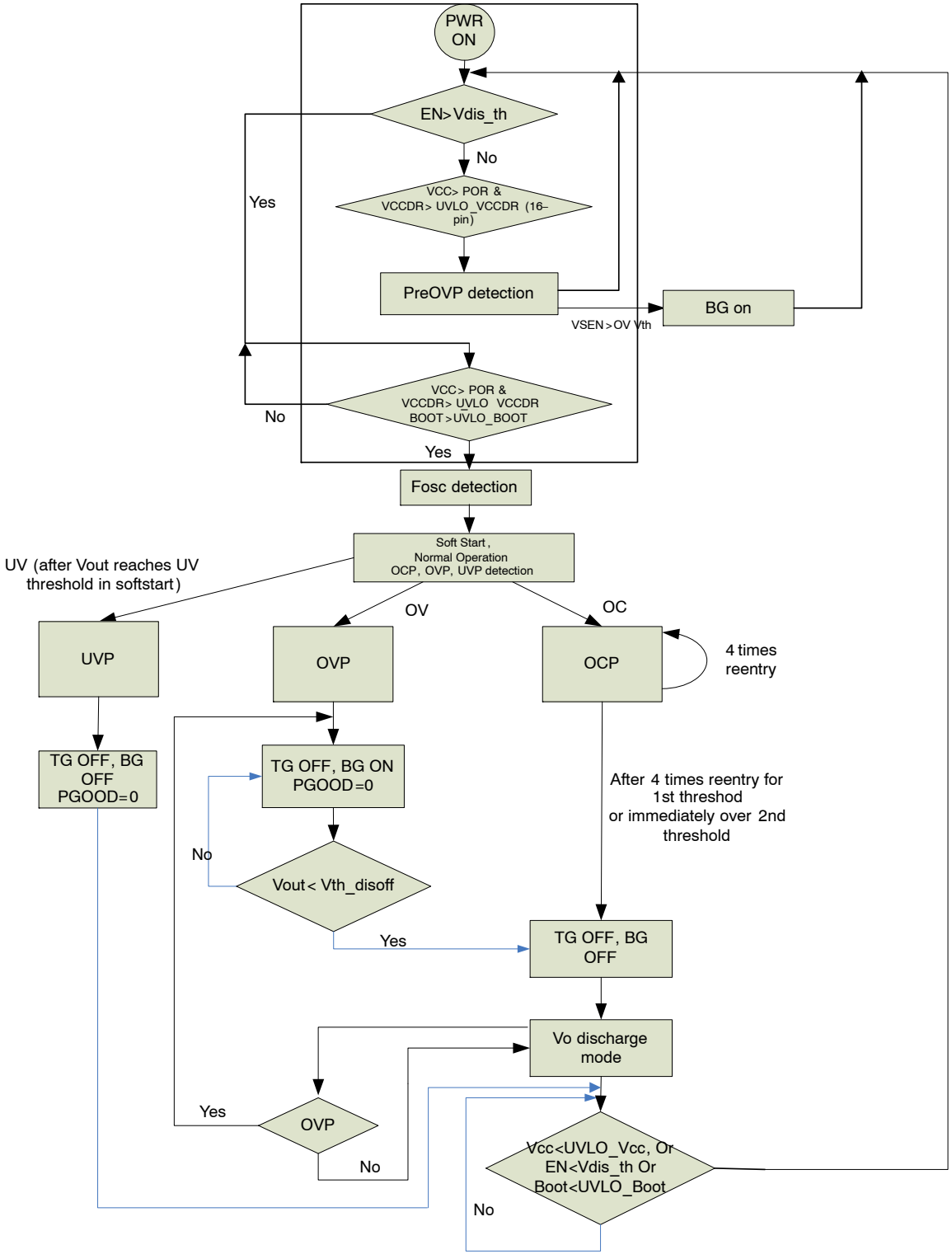


Figure 5. State Diagram

During Soft−start, UV is active once V_{out} reaches the UVP threshold and OVP is always active. In normal operating conditions, a UVP Fault will latch off the UG and LG. Requires a VCC or EN cycle to recover.

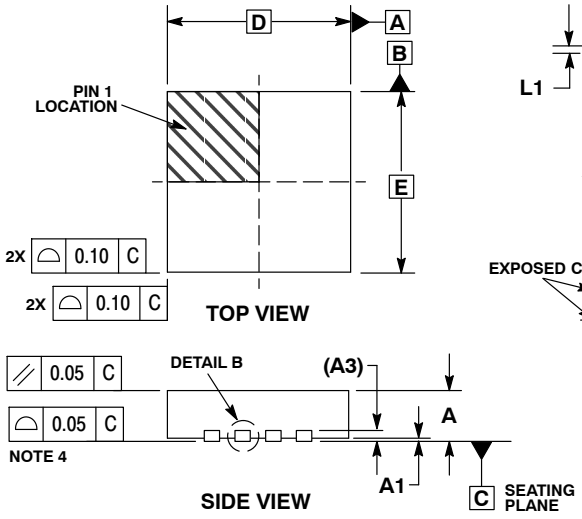
ORDERING INFORMATION

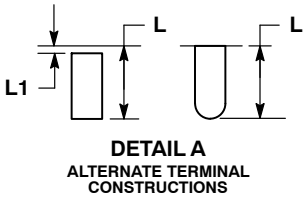
Device	Package	Tape & Reel Size†
NCP81031MNTWG	QFN16 (Pb−Free)	3000 / Tape & Reel

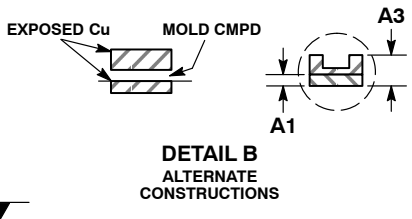
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G−01
ISSUE E

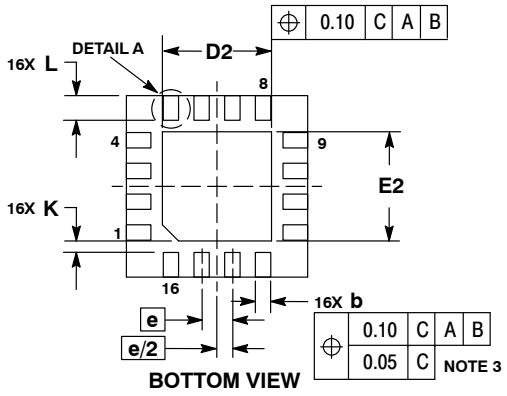




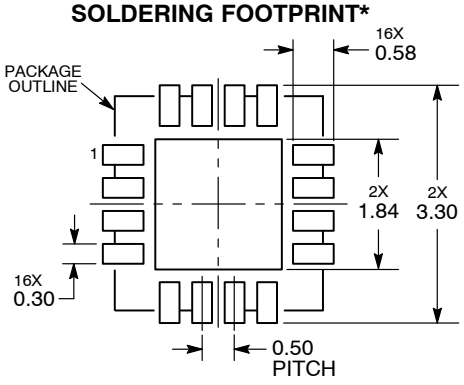


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50
L1	0.00	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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