NCP81111

3 Phase VR12.5-6 High Speed Digital Controller with SVID and I²C Interfaces for 5 MHz Desktop, Notebook CPU Applications

The NCP81111 is a high performance digital single output three phase VR12.5−6 compatible buck solution optimized to operate at frequencies up to 5 MHz for Intel CPU applications. The NCP81111 and can also work as a general purpose I²C controlled multiphase voltage regulator. The NCP81111 is designed to support the NCP81163 digital phase doubler IC which expands the capability of the part to 6 phases for high current handling. The controller includes true differential voltage sensing, differential current sensing, digital input voltage feed−forward, DAC feed forward, and adaptive voltage positioning. These features combine to provide an accurately regulated dynamic voltage system. The control system makes use of digital constant on time modulation and is combined with an analog and digital current sensing system. This system provides the fastest initial response to dynamic load events to reduced system cost. On board user programmable memory is included for configuring the controller's parameters. User programmable voltage and droop compensation is internally integrated to minimize the total board space used. The NCP81111 is optimized for use with DRMOS.

Features

- Meets Intel®'s VR12.5 Specifications
- On Board EEPROM for User Configuration
- High Performance Digital Architecture
- Dynamic Reference Injection
- Fully Differential Voltage Current Sense Amplifiers
- "Lossless" DCR Current Sensing for Current Balancing
- Thermally Compensated Inductor Current Sensing for Droop
- User Adjustable Internal Compensation
- Switching Frequency Range of 250 kHz − 5.0 MHz
- Input Voltage Feed−forward
- Startup into Pre−Charged Loads
- Power Saving Phase Shedding
- Supports Lower Power Operation in PS3
- This is a Pb−Free Device

Applications

- Desktop, Notebook Processors, and General Purpose I²C Controlled Multiphase Regulators.

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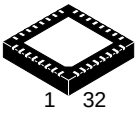
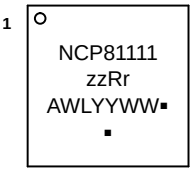
MARKING DIAGRAM



QFN32
CASE 485CE



NCP81111 = Specific Device Code
zz = Configuration Option
Rr = Revision Number
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device*	Package	Shipping†
NCP81111MNDFTXG	QFN32 (Pb−Free)	2500 / Tape & Reel
NCP81111MNzzTXG	QFN32 (Pb−Free)	2500 / Tape & Reel

*zz = Configurable Option, please contact Sales for additional information.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

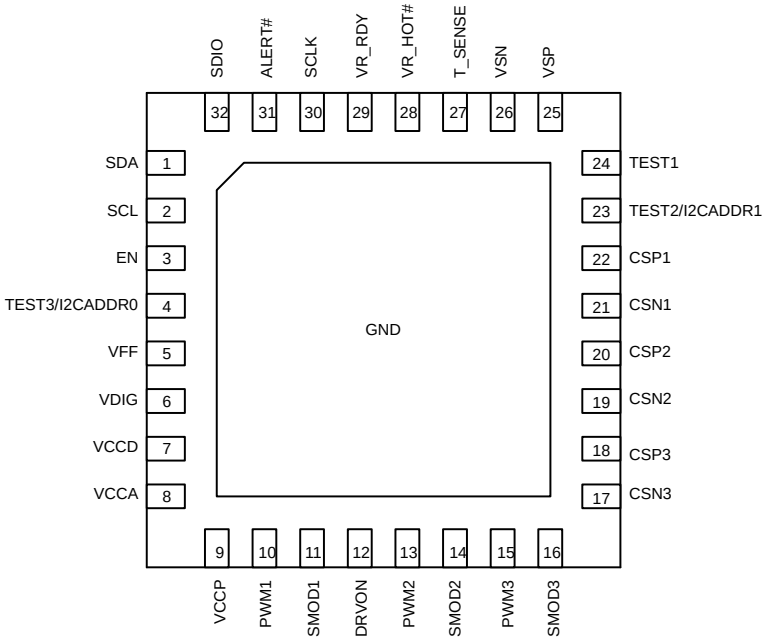


Figure 1. Pinout Diagram

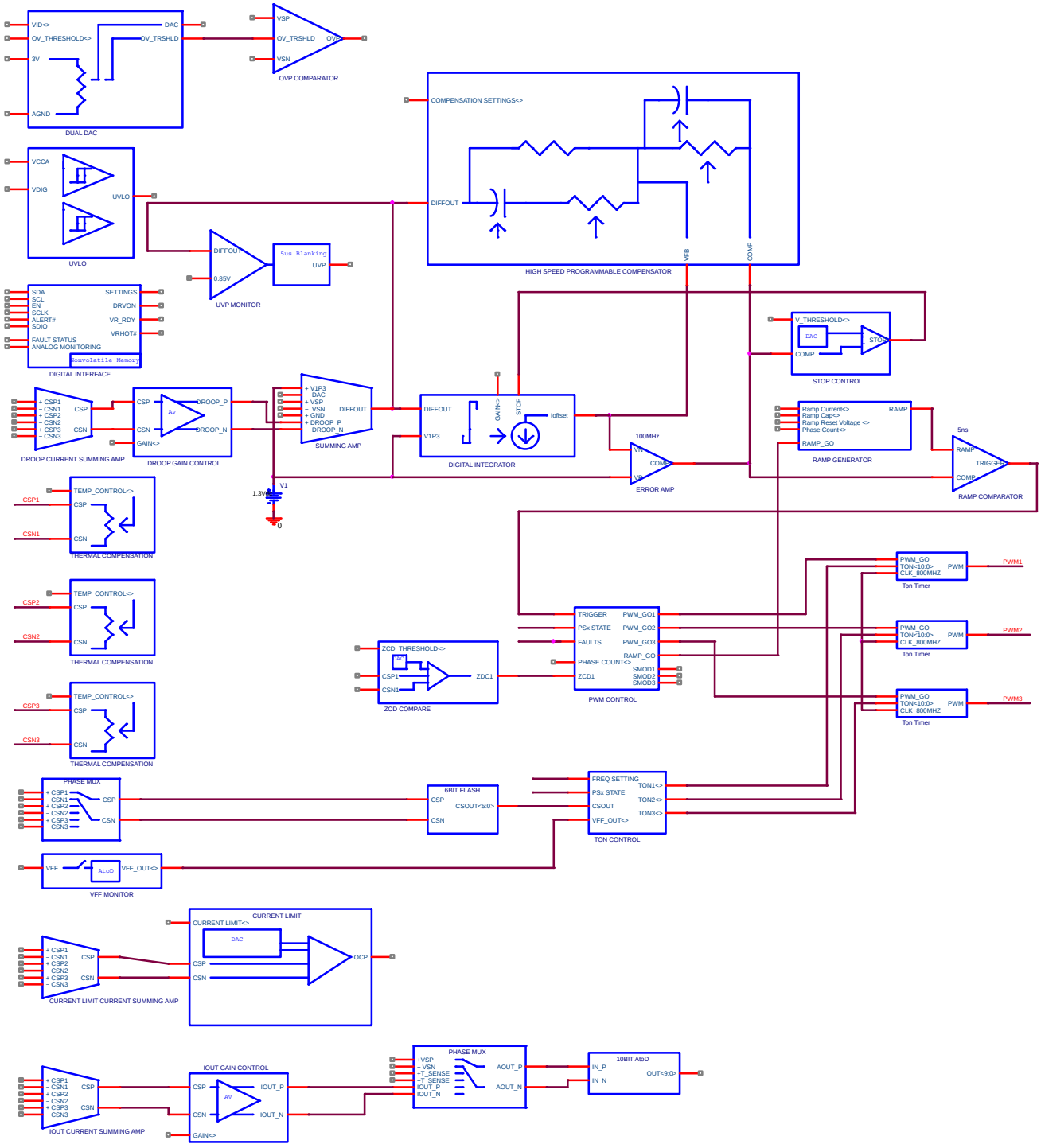


Figure 2. Block Diagram

PIN LIST DESCRIPTION

Pin No.	Symbol	Description
1	SDA	Serial Data Configuration Port
2	SCL	Serial Clock Configuration Port
3	EN	Logic input. Logic high enables output.
4	TEST3/I2CCADR0	Debug and monitor port / I^2C Programming Address Offset 0
5	VFF	Input voltage monitor
6	VDIG	Digital power filter pin. Internally regulated
7	VCCD	5V digital VCC
8	VCCA	5V analog VCC
9	VCCP	5V driver VCC
10	PWM1	Phase 1 PWM output.
11	SMOD1	Low side FET enable signal
12	DRON	Gate driver enable
13	PWM2	Phase 2 PWM output
14	SMOD2	PWM 2 low side FET enable signal
15	PWM3	Phase 3 PWM output
16	SMOD3	PWM3 low side FET enable signal
17	CSN3	Inverting input to current balance sense amplifier for phase 2
18	CSP3	Non−Inverting input to current balance sense amplifier for phase 2
19	CSN2	Inverting input to current balance sense amplifier for phase 2
20	CSP2	Non−inverting input to current balance sense amplifier for phase 2
21	CSN1	Inverting input to current balance sense amplifier for phase 1
22	CSP1	Non−inverting input to current balance sense amplifier for phase 1
23	TEST2/ADDR1	Monitor port / I^2C Programming Address Offset 1
24	TEST1	Debug and monitor port
25	VSP	Non−inverting input to the core differential remote sense amplifier.
26	VSN	Inverting input to the core differential remote sense amplifier.
27	T_SENSE	Temp sense for the single phase converter
28	VR_HOT#	Thermal logic output for over temperature.
29	VR_RDY	Open drain output. High indicates that the core output is regulating.
30	SCLK	Serial VID clock.
31	ALERT#	Serial VID ALERT#.
32	SDIO	Serial VID data interface.
FLAG	GND	Power supply return (QFN Flag)

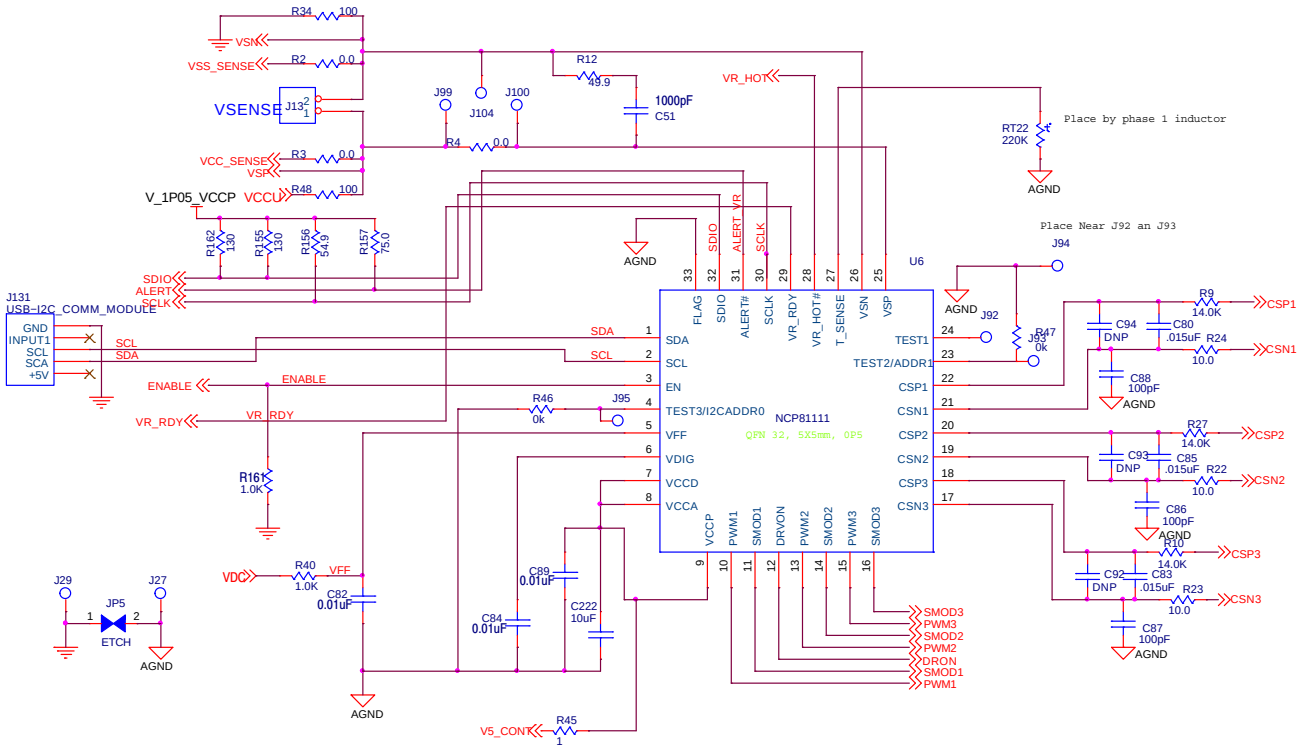


Figure 3. Three Phase Application Control Circuit

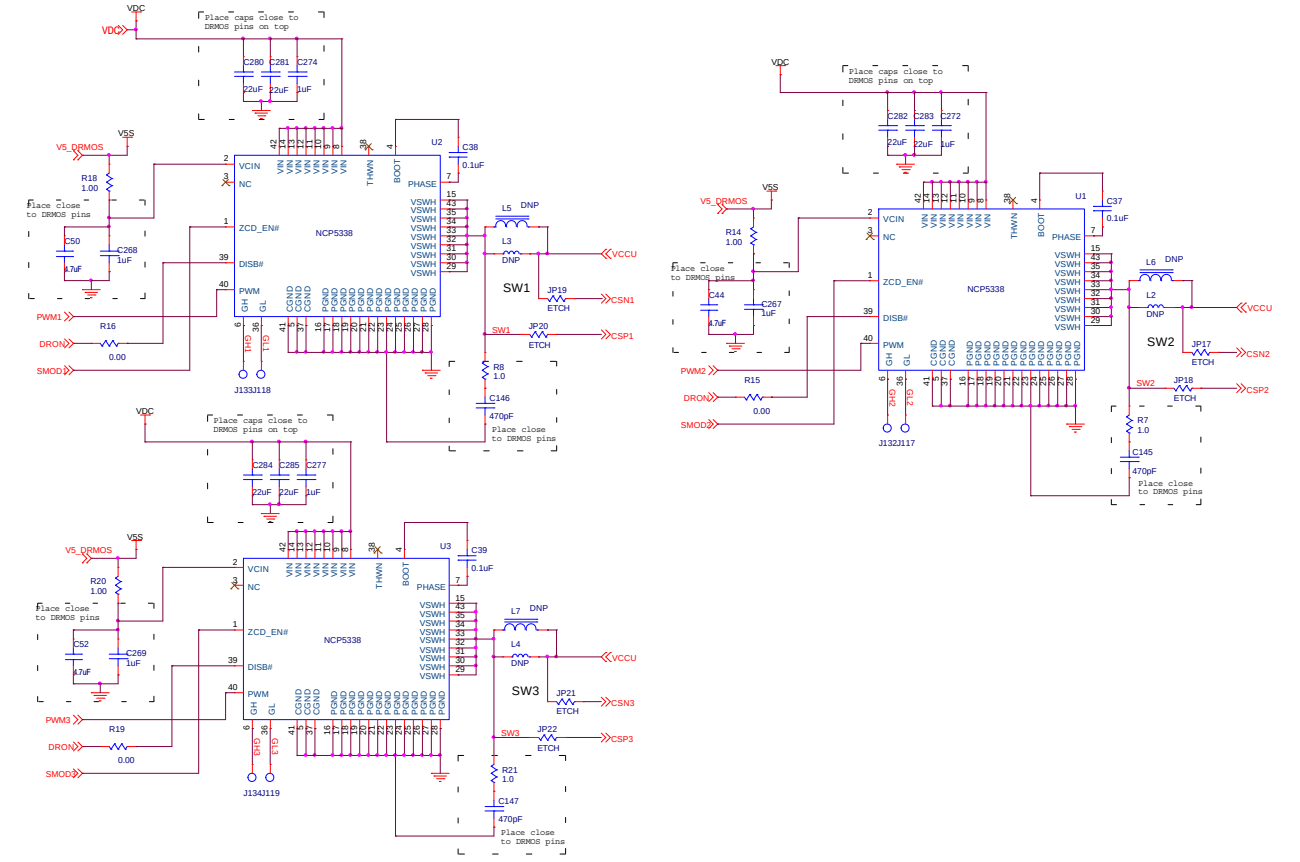


Figure 4. Three Phase Applications Power Stage Circuit

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
VFF	30 V	−0.3 V	N/A	N/A
VDIG	3.3 V			
All Other Pins	6.5 V	−0.3 V	N/A	N/A

*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic, QFN Package (Note 1)	$R_{\theta JA}$	44	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−10 to 125	°C
Operating Ambient Temperature Range		−10 to 100	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Quiescent Current	EN = high	30	40	50	mA
	EN = low		10		μA
	PS3		40		mA
VCCA UVLO Threshold	VCC rising		4.4	4.55	V
	VCC falling	4.1	4.2		V
VCCA UVLO Hysteresis			200		mV
VDIG UVLO Threshold	VDIG rising		1.65	1.8	V
	VDIG falling	1.27	1.45		V
VDIG UVLO Hysteresis			200		mV
ENABLE INPUT					
Enable High Input Leakage Current	External 1k pull−up to 3.3 V			1.0	μA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.4	V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$		100		mV
Enable Delay Time	Measure time from Enable transitioning HI to when DRON goes high, Vboot is not 0 V			1	ms
DIFFERENTIAL VOLTAGE SENSE					
Input Bias Current		−400		400	nA
VSP Input Voltage Range		−0.3		3.0	V
VSN Input Voltage Range		−0.3		0.3	V

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
DRVON					
Output High Voltage	Sourcing 500 μA	3.5			V
Output Low Voltage	Sinking 500 μA			0.1	V
Rise/Fall Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%		10		ns
Internal Pull Down Resistance	EN = Low		70		kΩ
IOUT MONITOR					
Analog Gain Accuracy		−3%		+3%	
Analog Gain Range		16		1024	
Analog Gain Step Size			Binary weigh ted		
Analog IOUT Offset Accuracy	Gain = 64, CSx sum = 40 mV, Digital Gain = 1			3	LSB
Digital Gain Step Size	Digital gain is 2.8 format		0.4%		
Digital Gain Range		0.004		4	
ADC Voltage Range		0		2.56	V
ADC Total Unadjusted Error (TUE)	Max % error of the ideal value	−1		+1	%
ADC Differential Nonlinearity (DNL)	Highest 8−bits			1	LSB
ADC Conversion Time			10		μs
ADC Conversion Rate	Per Channel		33		kHz
INTERNAL RAMP					
Ramp Slope Accuracy		−5		5	%
Ramp Reset Voltage Step Size			8		mV
Maximum Ramp Reset Step		486	512	538	mV
Ramp Slope Maximum	Single Phase Mode		4000		mV/μs
Ramp Slope Minimum	Single Phase Mode		5.6		mV/μs
Ramp Slope Step Size	Single Phase Mode Typical	5.3	5.6	5.88	mV/μs
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Set Point Accuracy	Threshold is programmable	−20		20	mV
Over Voltage Max Capability			3		V
Over Voltage Delay	VSP(A) rising to PWMx low		400		ns
Under Voltage Threshold Below DAC−DROOP	VSP(A) falling	415	450	475	mV
Under Voltage Hysteresis	VSP(A) rising		100		mV
Under Voltage Delay			150		ns
DROOP					
Gain Accuracy	Guaranteed by Design	−2		+2	%
Programmable Gain Range	CSx sum to Diffout	0,0.3		16.5	
Gain Step Size			1.2		%
Offset Accuracy	CSx input referred from 1.0 V to 2.0 V	−2.5		2.5	mV
Common Mode Rejection	CSx input referred from 1.0 V to 2.0 V	60	80		db
OVERCURRENT PROTECTION					
ILIM Threshold Accuracy	Sum of CSx inputs	−3.5		3.5	mV

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
OVERCURRENT PROTECTION					
Step Size			2		mV
Maximum Setting	Sum of CSx inputs		126		mV
ILIM Delay			1000		ns
ZCD COMPARATOR					
Offset Accuracy		−1.5		1.5	mV
Offset Programmable Range	Guaranteed by Design	−6.2		6.2	mV
Offset Step Size	Guaranteed by Design		0.2		mV
VR_HOT#					
Output Low Resistance	I_{VRHOT} = −10 mA			13	Ω
Output Leakage Current	High Impedance State	−1.0		1.0	μA
TSENSE					
Temperature Accuracy	(0°C and 125°C) Using Murata thermistor NCP18WM224J03RB (220 kΩ)	−4		4	°C
Internal Resistance Hot Range	50°C to 125°C	9.8	11.5	13.2	kΩ
Internal Resistance Cold Range	0°C to 50°C	146	172.5	198	kΩ
Bias Current Hot Range	50°C to 125°C	49.3	58	66.7	μA
Bias Current Cold Range	0°C to 50°C	4.1	4.83	5.6	μA
6 BIT CURRENT SHARE ADC					
Voltage Range		−24		39	mV
Differential Nonlinearity (DNL)				2	LSB
Step Size			1		mV
Conversion Time			550		ns
Common Mode Range		0.5		2.5	V
VR_RDY (Power Good)					
Output Low Saturation Voltage	$I_{VR\_RDY(A)}$ = 4 mA,			0.3	V
Rise Time	External pull−up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%		100		ns
Fall Time	External pull−up of 1 kΩ to 3.3V, C_{TOT} = 45 pF, ΔVo = 90% to 10%		10		ns
Output Voltage at Power−up	VR_RDY pulled up to 5 V via 2 kΩ			1.0	V
Output Leakage Current when High	VR_RDY = 5.0 V	−1.0		1.0	μA
VR_RDY Delay (rising)	DAC=TARGET to VR_RDY		5	6	μs
VR_RDY Delay (falling)	UVP response time		5		μs
VR_RDY Delay (falling)	OCP response time		1000		ns
VR_RDY Delay (falling)	OVP response time		250		ns
VR_RDY Delay (falling)	SetVID 0 V if register 34h is set to respond			500	ns
VR_RDY Delay (falling)	Time after Enable transitions low		1.3	1.5	μs
PWM					
Output High Voltage	No Load		VCC		V
Output Low Voltage	No Load		GND		V

ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
PWM					
Rise and Fall Time	CL (PCB) = 25 pF, ΔVo = GND to VCC		1		ns
Ton Accuracy		−5		5	%
Ton Step Size			1.25		ns
Ton Range		15		2559	ns
SMOD					
Output High Voltage	No Load		VCC		V
Output Low Voltage	No Load		GND		V
Rise and Fall Time	CL (PCB) = 25 pF, ΔVo = GND to VCC		1		ns
VFF ADC / VFF UVLO Note: UVLO threshold is programmable					
Step Size			200		mV
Maximum Tracking Slew Rate			2.5		V/us
Maximum Input			25.5		V

General

The NCP81111 is a single output three phase digital controller designed to meet the Intel VR12.5 specifications with a serial SVID control interface. The NCP81111 implements VR12.5 or VR12.6 depending on the device configuration.

I2C USER COMMANDS

These commands operate on a subset range of address space and are primarily for use by end users during application configuration.

USER_REG_READ

This command can read one or more bytes from the working register set. The address (USER_ADDR) specified with this command is a working set address from the user address range (refer to the USER column in the Register Map). Only registers which have read access (shown as (R) or (RW) in the USER column) can be read with this command. If the command is specified with an address that does not have read access the device will respond with NA (not−acknowledge).

However, if a block of registers are read which start from a valid address, then via the auto−incrementing address point to an address that does not have read access, then for those invalid registers the return value will be 00h (zeros). The invalid registers do not stop the command, and the device will respond with an A (acknowledge). This allows a single USER_REG_READ command to read a contiguous block of data even if it spans addresses that are not valid. Note that this command requires a repeated START sequence to change the data direction. Also, for the final byte received by the master it must signal end of data to the device by responding with a NA (not−acknowledge). This allows the device to release the data line so the master can send the STOP sequence. If a long sequence of data is read, which due to the auto−incrementing address exceeds the allowable address range, then the device will return zero values (00h) for bytes beyond the address boundary.

For a single−byte read the sequence is as follows:

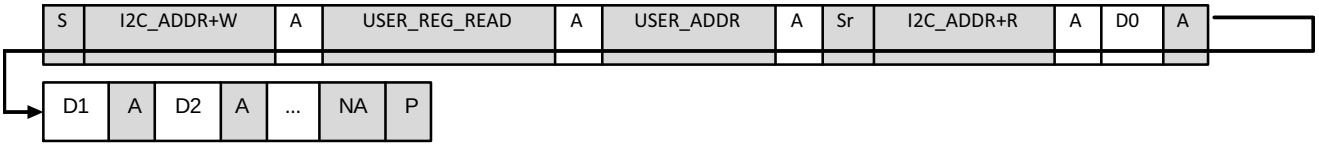
S	I2C_ADDR+W	A	USER_REG_READ	A	USER_ADDR	A	Sr	I2C_ADDR+R	A	D0	NA	P

This will read the data from the working register map as shown:

Working Registers

Data	Address
D0	USER_ADDR

For a multi−byte read command the sequence is as follows:



This will read the data from the working registers as shown:

Working Registers

Data	Address
D0	USER_ADDR
D1	USER_ADDR+1
D2	USER_ADDR+2
...	...

USER_REG_WRITE

This command will write one or more bytes into the working register set. The address (USER_ADDR) specified with this command is a working set address from the user address range (refer to the USER column in the Register Map). Only registers which have write access (shown as (RW) in the USER column) can be written with this command. If the command is specified with an address that does not have write access the device will respond with NA (not−acknowledge). However, if a block of registers are written which start from a valid address, then via the auto−incrementing address point to an address that does not have write access, then for those invalid registers the input data will be ignored. The invalid registers do not stop the command, and the device will respond with an A (acknowledge). This allows a single USER_REG_WRITE command to write a contiguous block of data even if it spans addresses that are not valid. If a long sequence of data is written which exceeds the allowable address range then the command will automatically terminate when the end of the address range is reached. Attempting to write past this point will result in NA (not−acknowledge) responses from the device.

For a single−byte write the sequence is as follows:

S	I2C_ADDR+W	A	USER_REG_WRITE	A	USER_ADDR	A	D0	A	P

This will insert data into the register as shown:

Working Registers

Data	Address
D0	USER_ADDR

For a multi−byte write command the sequence is as follows:

S	I2C_ADDR+W	A	USER_REG_WRITE	A	USER_ADDR	A	D0	A	D1	A	D2	A	...	A	P

This will insert a block of data into the registers as shown:

Working Registers

Data	Address
D0	USER_ADDR
D1	USER_ADDR+1
D2	USER_ADDR+2
...	...

USER_NVM_RELOAD

This command will reload the User NVM settings from the NVM into the working registers.

The sequence is as follows:

S	I2C_ADDR+W	A	USER_NVM_RELOAD	A	P

The command will reload all the registers at once and should complete in less than **50 µs** (worst case). This can be used to restore User settings after altering the working registers via the I2C interface. The reload is forced and does not require the settings to be configured.

USER_NVM_WRITE

This is the primary method for writing the User NVM settings into the NVM.

The sequence is as follows:

S	I2C_ADDR+W	A	USER_NVM_WRITE	A	P

The command will write all the current User settings from the working registers into the NVM. It should complete in less than **988 ms** (worst case, 380 ms typical case).

I2C USER_POWER CONTROL

Due to the internal construction of the device, when the EN pin goes low the internal regulators will turn off and the device will lose its working state. Subsequently if the EN pin goes high the device will reinitialize its state from the NVM configuration. For purposes of test and application configuration it is useful to power cycle the device without necessarily losing state. In addition, preserving state allows the device to optionally skip NVM load and/or auto−calibration sequences resulting in a faster startup time. To accomplish this, the USER_POWER command was added which allows the user to Enable/Disable the device without power−cycling the part. It also allows the NVM, working registers, and auto−calibration behavior to be modified when exiting the DISABLED state. The key to this command is the concept of a “Virtual Enable” signal. This virtual−EN signal can be controlled via the USER_POWER command and will behave in a similar way to the actual EN−pin, however when the virtual−EN is set low it will not completely power off the device. The internal regulators and clocks will continue running in order to preserve device state. Note, the EN−pin must remain high at all times when using the device in this way.

The command sequence is as follows:

S	I2C_ADDR+W	A	USER_POWER	A	POWER_SETTING	A	P

Where the POWER_SETTING byte is mapped as follows:
POWER_SETTING:

0	0	0	RESET_TEST	RESET_MEM	RESET_AUTOCAL	RESTART	ENABLE

- **ENABLE** − This bit is the “Virtual Enable” signal. When the device is in the DISABLED state, sending the USER_POWER command with this bit set to “1” will cause the device to exit the DISABLED state and begin the power−up sequence. The exact power−up sequence followed will depend on the other bit settings. If the device is in an operational state (not DISABLED) and the command is issued with this bit set to “0” then the device will stop operation and enter the DISABLED state.
- **RESTART** − This bit is used in conjunction with the ENABLE bit. It is used to immediately restart the device when the DISABLED state has been entered. So when the device is in an operational state, if the USER_POWER command is issued with this bit set to “1” and the ENABLE bit set to “0”, the device will stop operation, enter the DISABLED state, and then immediately power−up again. It is in essence a fast toggle on the Virtual Enable signal, used to quickly cycle the device through its power−up sequence.
- **RESET_AUTOCAL** − When this bit is set to “1”, upon exiting the DISABLED state, the device will reset its auto−calibration state and proceed to recalibrate during power−up. Normally auto−calibration is only required if the device has lost its state (thus it will occur anytime the actual EN−pin is toggled), however the procedure takes a few milliseconds to complete. Since the device can retain state using this command, if this bit is set to “0”, the auto−calibration settings will be retained and the procedure will be skipped. A “0” setting will allow the device to power−up several milliseconds faster than normal.
- **RESET_MEM** − This bit controls the behavior of the working registers and the NVM during power−up. If the bit is set to “1” then upon exiting the DISABLED state the working registers will be reinitialized − first the POR settings will be applied, then the NVM will be read and those settings will be applied. Any changes to the working registers that were not programmed to the NVM will be lost. If the bit is instead set to “0” then the device will retain all the settings that are currently in the working registers. A “0” setting is useful for testing minor changes to device settings without needing to program them to NVM.
- **RESET_TEST** − If the bit is set to “1” then upon exiting the DISABLED state, the test registers will be reset to their POR defaults. A “1” setting is useful for quickly clearing all test modes when cycling through a power−up sequence. If the bit is set to “0” then the test registers will be unaffected by the power−up sequence.

Example command sequences:
Starting from a normal operational state, issuing the following command:

S	I2C_ADDR+W	A	USER_POWER	A	00000000b	A	P

Will cause the part to exit to the DISABLED state and remain there. The test interface can then be used to modify the working registers and adjust settings prior to re−enabling the part.

Starting from the DISABLED state, issuing the following command:

S	I2C_ADDR+W	A	USER_POWER	A	00000001b	A	P

Will cause the part to exit the DISABLED state and begin power−up. The working registers will not be affected during power−up, and auto−calibration will be skipped (Note: this is only true if auto−cal has completed its sequence at least once.

Starting from any state, issuing the following command:

S	I2C_ADDR+W	A	USER_POWER	A	00000110b	A	P

Will cause the part to exit to the DISABLED state, then immediately begin power−up. The working registers will not be affected during power−up, however the part will recalibrate.

Starting from any state, issuing the following command:

S	I2C_ADDR+W	A	USER_POWER	A	00011010b	A	P

Will cause the part to exit to the DISABLED state, then immediately power−up again. On power−up it will clear the test registers and reload the NVM into the working registers. It will skip the auto−calibration sequence. This is very similar to toggling the EN−pin, but with a faster powerup time.

Starting from any state, issuing the following command:

S	I2C_ADDR+W	A	USER_POWER	A	00011110b	A	P

Will cause the part to exit to the DISABLED state, then immediately power−up again. On power−up the controller will clear the test registers and reload the NVM into the working registers. It will recalibrate during power−up. This is exactly the same as toggling the EN−pin, but with a slightly faster power−up time (due to regulators and clocks already being powered up and running).

DEVICE CONFIGURATION

The following sections describe the configuration of certain device register groups based on function.

External Address Offset

There is an external address offset circuit which can be used to allow otherwise identically programmed devices to be placed on a common bus. The address that the devices will respond to can be altered via an external resistor network. The address offset circuit can offset both the I2C and SVID addresses by an offset range of +0 to +15. The address system is controlled by the following registers:

Table 1. I2C / SVID ADDRESS REGISTERS

Register (I2C Addr)	R/W	Purpose	Description
43 Bits<2:0>	RW	Address Offset Configuration	This register has bit flags as follows: 0 | 0 | 0 | 0 | 0 | apply_svid_addr_offset | apply_i2c_addr_offset | en_addr_offset These bit flags control whether the External Address Offset function is enabled, and if so how the offset is applied. apply_svid_addr_offset = When set the address offset will be applied to the SVID Address (Default enabled) apply_i2c_addr_offset = When set, the address offset will be applied to the I2C Address (Default enabled) en_addr_offset = Controls if the address offset circuit is enabled (Default enabled)
50 Bits<6:0>	RW	I2C Address	This settings holds the base I2C address. The value should be between 8 to 119. Default is 68 (44h). 0−7 = Invalid (I2C reserved) 8−119 = Valid (08h − 77h) 120−127 = Invalid (I2C reserved)
51 Bits<3:0>	RW	SVID Address	This setting holds the base SVID address. The value can be between 0 to 15 (0h − Fh). Default is 0 (0h).

The address offset circuit is enabled by default on an unprogrammed device. It can be disabled by writing a zero into **en_addr_offset** (Register 43, Bit 0) when programming the device. When enabled, the device will sense resistors attached to the TEST2 and TEST3 pins during powerup and will add the resulting offset to the SVID and I2C base addresses as defined by the bit flag settings above.

Addresses that exceed the maximum address will wrap around. For instance:

The address offset that is generated is determined by the resistors placed between the TEST2/TEST3 pins and GND. The system uses 20 kΩ increments per step, and both the highest and lowest settings will give an address offset of zero (this is to allow the TEST pins to be either shorted or open on a single−VR application or during device evaluation).

The following tables list the resultant offsets versus resistance for the TEST2 and TEST3 pins. The individual offsets are added to give a total offset.

Table 2. TEST2 ADDRESS OFFSET

Address Offset	Resistance (kΩ)
0	0−60
+8	80−140
0	>160

Table 3. TEST3 ADDRESS OFFSET

Address Offset	Resistance (kΩ)
0	0
+1	20
+2	40
+3	60
+4	80
+5	100
+6	120
+7	140
0	>160

The address offset value is latched during power−up as part of NVM initialization. It will be retained for the duration of device operation. Enabling/Disabling the device via USER_POWER commands will not cause the address offset value to be relatched. The only way to relatch the address offset value is to either power cycle the device or use a USER_POWER command with the RESET_MEM flag set. After power−up the resulting address offset value can be read via I2C (Note: if I2C address offset is enabled, this requires knowing the offset in advance, if this is not the case, then the hardwired addressing mode can be used):

Table 4. ADDRESS OFFSET READBACK

Register (I2C Addr)	R/W	Purpose	Description
219 Bits<3:0>	R	Address Offset	Readback of the latched address offset

DAC FEED FORWARD

A DAC Feed Forward (abbreviated DACFF) function has been added to the device. The purpose of this circuit is to counteract the transient response of the output pole given by the droop resistance and the output load capacitance. In order to do this the DACFF circuit adds a counteracting zero which cancels the pole.

This is illustrated below, where $\omega_z = \omega = 1/RC$, with R = droop resistance and C = output load capacitance:

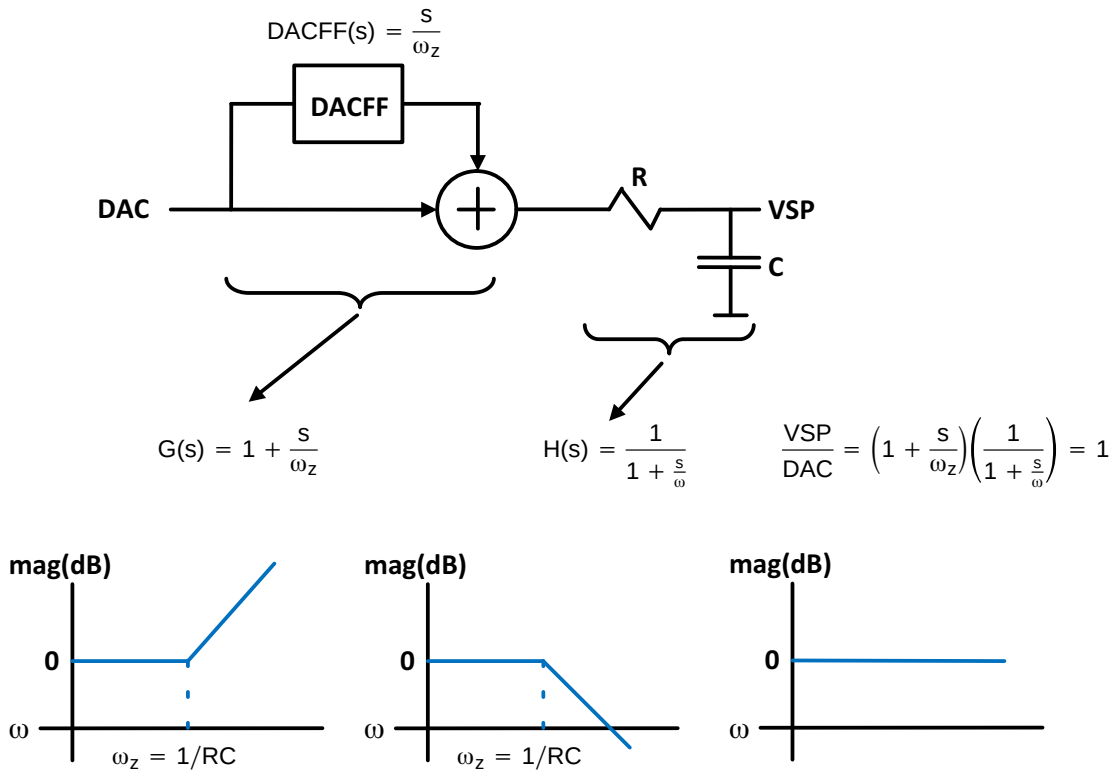


Figure 5.

There are some important things to note about the DACFF system:

- This effect is only applied in the VID UP direction, and allows the DAC to closely follow the ideal ramp slope behavior. The effect is not applied in the VID DOWN direction to prevent potential voltage undershoot.
- For the effect to work properly the internal DACFF coefficients (given below) must be set properly with respect to the actual droop resistance and output load capacitance. Improperly setting the coefficients may yield a lagging voltage response (under−compensated) or overshoot artifacts (over−compensated). **For this reason the feature is disabled by default and must be explicitly enabled via end−user configuration.**
- The above representation is a theoretical idealized model. In practice due to the digital nature and internal clock frequency of the VID controller an additional high−frequency pole is introduced. The actual transfer function of the DACFF circuit is given below. From a transient perspective this pole will have an effect on the leading and trailing response of the DACFF function (the transition from VID up to VID stable, or vice−versa), and it's effect will be discussed more in the coefficient calculation section below.

$$DACFF(s) = \frac{\frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \qquad \text{(eq. 1)}$$

There are two DACFF coefficients, a 16−bit A−coefficient and an 8−bit B−coefficient. They can be calculated with the following equations and procedure.

$$A[15:0] = \frac{\frac{2}{T \cdot \omega_z}}{\left(1 + \frac{2}{T \cdot \omega_p}\right)} \cdot 128 \qquad B[7:0] = \frac{\left(\frac{2}{T \cdot \omega_p} - 1\right)}{\left(1 + \frac{2}{T \cdot \omega_p}\right)} \cdot 256 \qquad \text{(eq. 2)}$$

where:

$$\omega_z = \frac{1}{RC}$$

$$\omega_p = 2\pi \cdot f_p \text{ where } f_p < 3.18 \text{ MHz}$$

T = 100 ns = $1 \bullet 10^{-7}$
R = droop resistance
C = output load capacitance
Calculation procedure:

1. Calculate ω_z and choose initial ω_p. Use those parameters to calculate A/B−coefficients.
2. Program the device with the coefficients, and enable the DACFF function. Observe the transient behavior.
3. Adjust A/B−coefficients directly as needed to modify the transient behavior as shown below.
4. Program the new coefficients and iterate as needed until satisfactory transients are obtained.

To the first−order the magnitude of the DACFF function will be controlled by the A−coefficient and the frequency response will be controlled by the B−coefficient. This is illustrated below and can be used as a guideline when adjusting the coefficients to obtain the desired response.

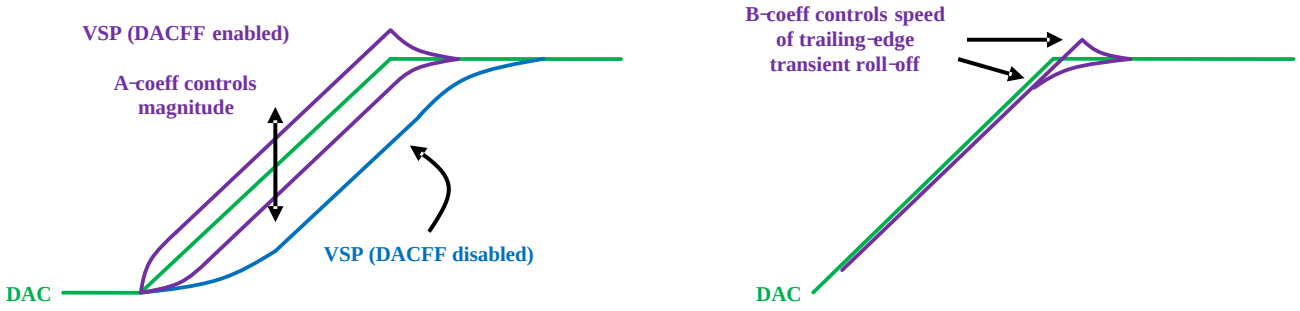


Figure 6.

IOUT Gain Programming

The NCP81111 has a high accuracy 10 bit A/D to monitor the total output current. The IOUT gain and the ICCMAX register are user programmed and stored in the nonvolatile memory. The IOUT gain consists of two analog gain stages and one digital gain stage for fine gain adjustment. When setting the IOUT gain the user must be care not to exceed the maximum input A/D signal capability using the analog gain. Set the digital gain to unity and then adjust the analog gain to get the maximum signal into the A/D without exceeding FFh at ICCMAX load in the IOUT register. Then fine tune the digital gain to achieve FFh in the IOUT register under the ICCMAX load condition. IOUT Offset can be adjusted after the A/D conversion via register 84d.

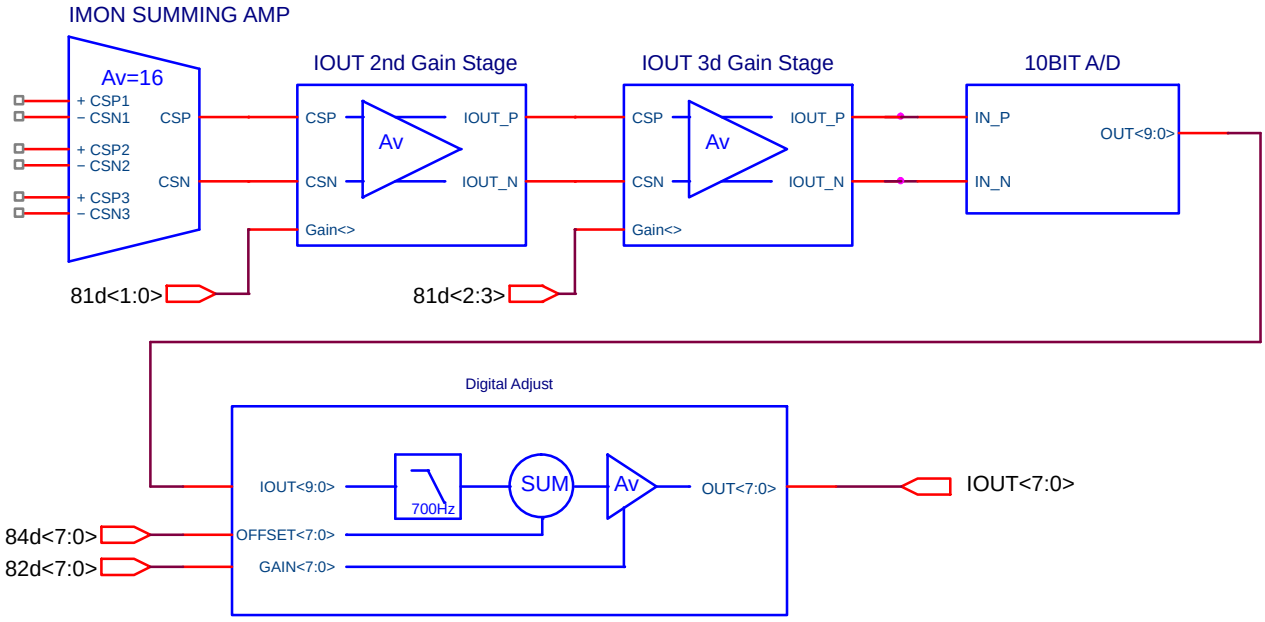


Figure 7. IOUT Signal Chain

IOUT CONFIGURATION TABLE

Function	Register	Value
Stage2 IOUT Gain Stage3 IOUT Gain	81d<1:0> 81d<3:2>	0: 1 1: 2 2: 4 3: 8
Digital Gain	82d<7:0>	absolute 2.8 format (2 integer, 8 fractional), 0.00390625 per step Example 100h = 256d ≥ Gain = 1
Iout Offset PS0	84d<7:0>	2's complement format
Imon Offset PS1	115d<7:0>	2's complement format
Imon Offset PS23	116d<7:0>	2's complement format
Imon Settling time	110d<1:0>	99% Settle in => 00b=840 μs, 01b=1.68 ms, 10b=3.36 ms, 11b:6.72 ms

The equation for Iout tuning is as follows.

$$2.5\ V = G_1 \cdot G_2 \cdot DCR \cdot 0.75 \cdot G_{Digital} \cdot I_{CC\_MAX} \qquad \text{(eq. 3)}$$

When tuning the Iout Analog gain G1 and G1 need to be set such that the Iout is between 80h and FFh but the voltage at the A/D should not exceed 2.5V at Icc_max or the Iout signal will saturate the A/D converter. The offset can also be adjusted.

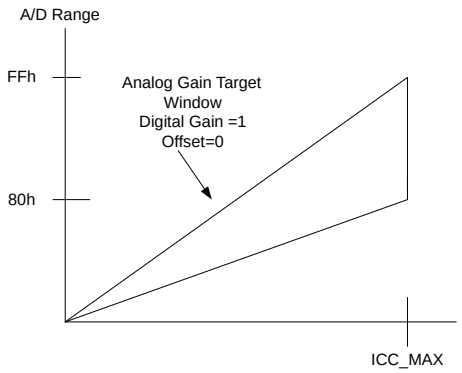


Figure 8.

The internal offset of the Iout signal chain is auto−calibrated and has very low offset. The current sense RC filter itself has some nonlinear behavior when using thick film resistors. This creates a positive offset on Iout that can be observed to follow the input supply voltage, Vout, and phase count. Using physically larger thick film 0805 resistors or two 0603 resistors in series can reduce but not eliminate this effect. The system provides the IOUT offset adjust registers to help compensate for this effect. For best performance using a metal film resistor is required in the cs filter network.

OCP Current Limit Programming

The NCP81111 uses a latching total current limit function. If the current limit is exceeded the controller will tri−state the output stage. There is an adjustable filter speed for the OCP function. The filter can be disabled for the fastest response. The OCP has three user settings to accommodate different current limits in separate power states.

The current limit is a total current limit and is digitally programmable in 2 mV steps to a maximum of 126 mV referred to the total CS input sum.

Table 5. OCP CONFIGURATION TABLE

Function	Register	Value
OCP PS0	85d<5:0>	2 mV per step 0d = 0 mV to 63d = 126 mV
OCP PS1	86d<5:0>	2 mV per step 0d = 0 mV to 63d = 126 mV
OCP PS23	87d<5:0>	2 mV per step 0d = 0 mV to 63d = 126 mV
OCP Filter Bandwidth	85d<7:6>	00b:250 kHz , 01b:125 kHz, 10b:75 kHz, 11b:50 kHz
OCP Filter Enable	86d<6>	0:Use Filter, 1:No Filter

Compensator Tuning

The NCP81111 uses a hybrid compensator. The high frequency performance is provided by a 100 MHz BW op−amp. The digital integrator allows better control of the low frequency transient response. R1 and can be adjusted for power states PS0 and PS1,2,3 to optimize the loop gain based on the number of phases running.

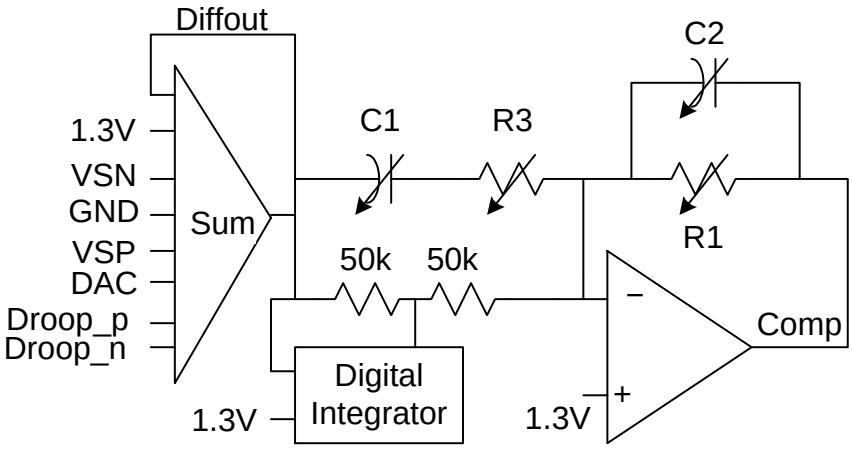


Figure 9. Hybrid Compensator Diagram

Equation 4 − Compensator Transfer Function

$$\frac{\text{Comp(s)}}{\text{Diffout(s)}} = \frac{-\left(\frac{Ai \cdot gm}{2 \cdot C_{cap} \cdot Divisor \cdot V_{ramp} \cdot s} + \frac{1}{R3 + \frac{1}{C3 \cdot s}} + \frac{1}{100k}\right)}{\frac{1}{R1} + C2 \cdot s} \quad \text{(eq. 4)}$$

ANALOG COMPENSATION CONFIGURATION TABLE

Function	Register	Value
R1 (PS0) R1 (PS123)	95d<3:0> 95d<7:4>	0:33k, 1:50k, 2:75k, 3:100k, 4:150k, 5:200k, 6:250k, 7:300k, 8:350k, 9:400k, 10:450k
R3	96d<5:3>	0:10k, 1:20k, 2:30k, 3:40k, 4−7:50k
C1	96d<2:0>	0:0pF, 1:1.23pF, 2:3.48pF, 3:8.02pF, 4:17.12pF, 5:35.8pF, 6−7:24.3pF
C2	97d<2:0>	0:0fF, 1:185fF, 2:90fF,3:522fF,4−7:1.373pF

Digital Integrator

The digital integrator allows for independent tuning of the load step and load release response time and allows the user to change the offset during power state changes to smooth the transition of the power state changes. The current DAC step size controls the working range/ resolution of the digital integrator.

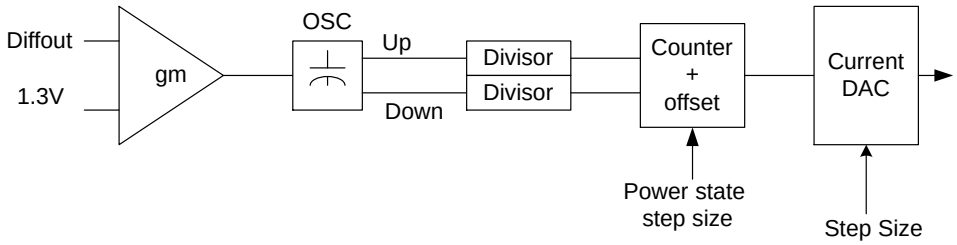


Figure 10.

The digital integrator is a voltage to current function. The gm is approximately 180 μs, Vramp is ~50 mVm and Ccap in the oscillator is 2 pF. The step size Ai for the current DAC is user adjustable. The digital integrator transfer function can be

approximated with the following equation below. The current gain Ai is the integrator current step multiplied by the size multiplier.

$$\frac{I(s)}{Verror(s)} = \frac{Ai \cdot gm}{Divisor \cdot V_{ramp} \cdot C_{cap} \cdot s} \qquad \text{(eq. 5)}$$

The digital integrator also includes a stop function that can be adjusted to improve some aspects of the dynamic response such as load release. If the output of the error amplifier falls below the integrator stop threshold the digital integrator counter will be stopped to limit the integrator windup effect. In some cases the range of the integrator is sufficient to stop the windup effect.

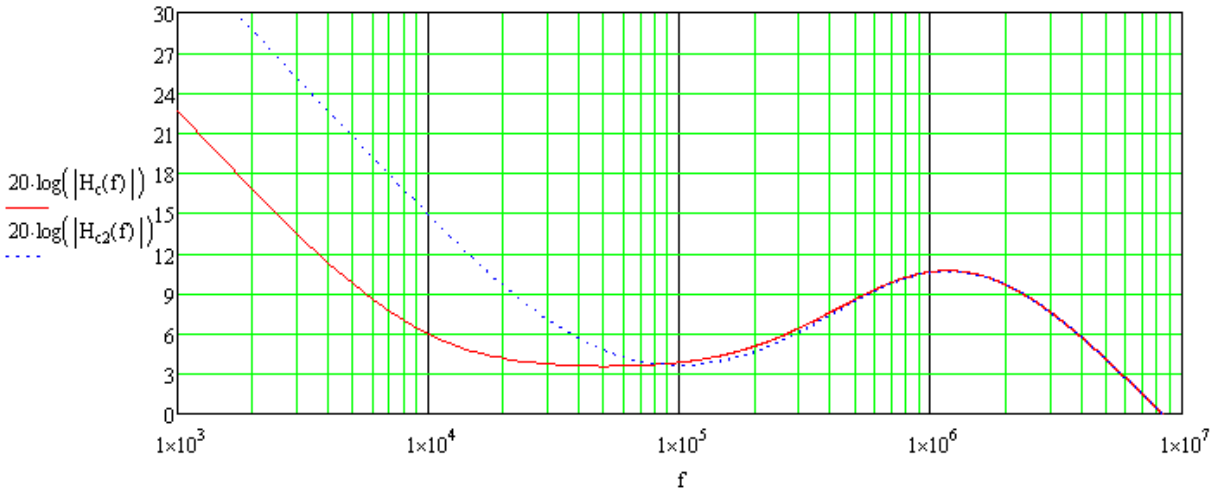


Figure 11. Example Compensator Gain Transfer Function with Mismatched Increment and Decrement Gains

DIGITAL INTEGRATOR CONFIGURATION TABLE

Function	Register	Value
Integrator Step Size Multiplier Integrator Current Step	88d:<7> 89d:<4:3>	0: 100% step size 1: 75% step size 0: 5nA, 1:10nA, 2:15nA, 3:20nA
Integrator Decrement Divisor PS0 PS1 PS23	 90d<5:3> 91d<5:3> 92d<5:3>	0:1, 1:2, 2:4, 3:8, 4:16, 5:32, 6:64, 7:128
Integrator Increment Divisor PS0 PS1 PS23	 90d<2:0> 91d<2:0> 92d<2:0>	0:1, 1:2, 2:4, 3:8, 4:16, 5:32, 6:64, 7:128
Integrator Offset PS1 Step	93d<7:0>	2's compliment format
Integrator Offset PS23 Step	94d<7:0>	2's compliment format
Integrator Stop Threshold PS0 PS1 PS23	 88d<0:2> 88d<5:3> 89d<2:0>	0:0.90V, 1:0.95V, 2:1.00V, 3:1.05V, 4:1.10V, 5:1.15V, 6:1.20V, 7:1.25V

Phase Shedding Threshold

When a power state command alters the phase count the controller will automatically reduce the current in the phases that are to be shed to the threshold level set by the user and then shutdown the phase. This allows the controller to minimize the voltage deviation during phase shedding operation.

PHASE SHED THRESHOLD CONFIGURATION TABLE

Function	Register	Value
Phase Shed Threshold	73d<5:0>	LSB = 1 mV 2's complement format

VBOOT Voltage Programming

The NCP81111 has a Vboot voltage register that can be configured to any valid VID value. If Vboot is configured to zero, the controller will wait for an initial SVID voltage command to begin soft start.

DAC Offset Voltage Programming

The NCP81111 has a user fine trim for the output voltage that is adjustable for each power state.

ZDC Offset Programming

The NCP81111 is optimized to work with the ON's HFVR high performance DRMOS drive stage. The ZCD detector is located in the controller and the offset is adjustable for optimization by the user. This allows for timing variations in the design

ZCD OFFSET CONFIGURATION TABLE

Function	Register	Value
ZDC Offset Trim	114d<5:0>	0.2 mV per LSB Sign magnitude format.

VFF Under-Voltage Protection Programming

The controller is protected against under−voltage on the VFF input pin. The threshold is user programmable.

VFF Under−Voltage Configuration Table

Function	Register	Value
VFF UVLO Threshold	93d<6:0>	200 mV per LSB Example 14h = 4.0 V

Programming the Phase Count

The phase count must be configured buy the user and stored in NVM before enabling the output.

PHASE COUNT CONFIGURATION TABLE

Function	Register	Value
VR Phase Count	64d<7:6>	1: 1phase 2: 2phase 3: 3phase

Programming the Minimum ON, Minimum OFF, and SMOD Skew Timing

The controller is designed to guarantee the timing in certain cases to protect the gate driver from very rapid signal changes that could potentially result is shoot though of the power stage. The user may select the setting for this based on the application selection of the power stage. The recommended values for the HFVR DRMOS are noted in the table.

MINIMUM ON AND OFF TIME AND SMOD SKEW CONFIGURATION TABLE

Function	Register	Value
Minimum On Time Phases 1	65d<5:0>	Minimum On time 1.25 ns per LSB Example 1Ah = 32.5 ns
Minimum On Time Phases 2 and 3	64d<5:0>	Minimum On time 1.25 ns per LSB Example 1Ah = 32.5 ns
Minimum Off Time	66d<4:0>	LSB = 2.5 ns Example 0Dh = 32.5 ns
SMOD Skew Time	69d<4:0>	LSB = 2.5 ns Example 06h = 15 ns

Programming the Period of Operation

The NCP81111 is designed to maintain a constant frequency in as many operating cases as possible. The On time of the controller varies based on many factors including VID setting, input voltage feed forward, load and power state. The frequency in continuous mode operations is controlled by the user period setting. Under some conditions including low VID and high Vin the frequency of operation may reduce due to reaching the minimum on time limits. The period setting is based on the

individual phase frequency desired. Example 134h = 770 ns for 1.3 MHz For this case the registers would be configured as follows. 72d = 34h with 73d<3:0> = 001b.

PERIOD CONFIGURATION TABLE

Function	Register	Value
USER Period low byte	71d<7:0>	2.5 ns per LSB
USER Period high byte	72d<3:0>	

Programming the Boost Cap Functions

Due to the high voltage operation of the output under some conditions the gate driver floating boost cap voltage may discharge to unacceptable levels, this is especially likely to occur when using 5 V gate drivers. The NCP81111 has several functions to maintain the charge on the boost capacitors such that the gate driver is ready to use when needed. These timers are user adjustable for custom optimization. The Tboost Period sets the time between recharge events for the phases that are shed. The Tboost Time sets the amount of time the switch node is pulled low to charge the boost cap. The Boost Loop Count is used at soft−start and sets the number of times the boost cap is charged before soft−start occurs.

BOOST CAP CONFIGURATION TABLE

Function	Register	Value
Tboost Period	67<7:4>	Default 1h = 81.92 μs
Tboost Time	68d<7:0>	2.5 ns per LSB Default 33h = 127.5 ns
Boost Loop Count	70d<3:0>	Default 8h for 8 loops.

Programming the Ramp Function

The ramp signal is user adjustable. This allows the user to maximize the performance of the controller. The ramp provides a synchronization function for the controller and stabilizes the loop gain as well as the phase angles. The ramp has a reset voltage for each phase and the slope automatically adjusts for the phase count during phase shedding. To achieve a wide verity of accurate settings both the current and the ramp capacitor are adjustable. The adjustable ramp reset voltage allow for fine tuning of the phase angles if the ripple feedback is not well balanced. The ramp descends to 1.3 V and remains there until reset again. Use the equation I = Cdv/dt the ramp current setting is based on single phase ramp operation. Figure x shows how to select the ramp cap and ramp slope. The design should target the trigger point near 1.31 V just above were the ramp goes flat at 1.3 V.

If the ramp intersects comp at high levels the load release response will be less aggressive and transitions into and out of DCM mode operation will be less smooth. If the ramp is too steep the comp will trigger on a flat ramp and the system will be less stable.

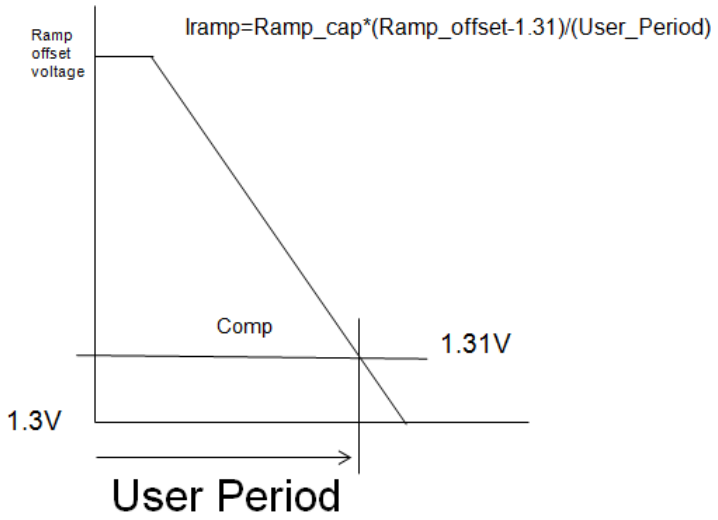


Figure 12.

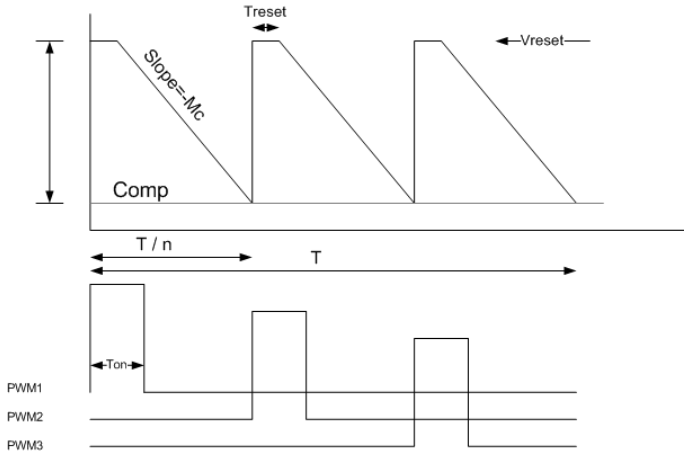


Figure 13. Multiphase Ramp Function

Modulator Gain Analysis

The NCP81111 modulator has an inherent non−linear transient response that varies depending on the ramp settings. The small signal modulator gain can be found by taking the derivative of the non linear curve at the operating point. The result is the equation for Am.

$$A_m := \frac{Mc \cdot Ton}{N \cdot \left(Vreset - comp_{opp} + Mc \cdot Treset\right)^2} \qquad comp_{opp} := \frac{\frac{Mc \cdot Ton}{D} - N \cdot Vreset - N \cdot Mc \cdot Treset}{-N} \qquad \text{(eq. 6)}$$

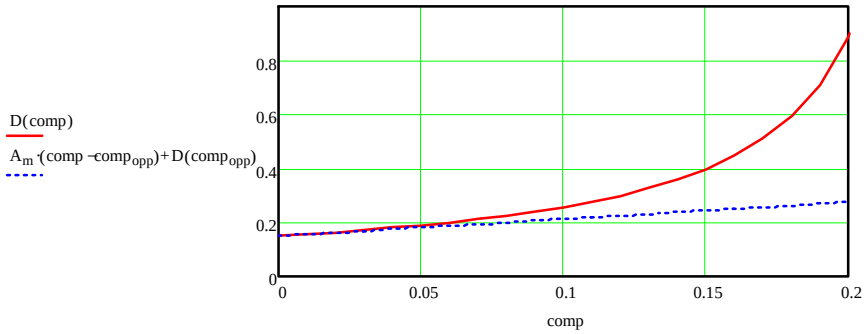


Figure 14. Modulator Gain Function

RAMP CONFIGURATION TABLE

Function	Register	Value
Ramp Cap Setting	77d<3:0>	0: 0 pF 1: 1 pF 2: 2 pF 3: 3 pF 4: 4 pF 5: 5 pF 6: 6 pF 7: 7 pF 8: 8 pF 9: 9 pF 10: 10 pF 11: 11 pF 12-15: 12 pF
Ramp Current Setting	78d<7:0>	0 to 4.2291 uA 33.3 nA per LSB
Phase 1 Reset Voltage	74d<7:0>	4 mV per LSB Example 3Fh = 63d = 1.556 V
Phase 2 Reset Voltage	75d<7:0>	4 mV per LSB

RAMP CONFIGURATION TABLE

Function	Register	Value
Phase 3 Reset Voltage	76d<7:0>	4 mV per LSB
Ramp Reset Time		

Control Loop Analysis

The NCP8111 control loop diagram can be modeled as shown below. The NCP81111 system is best described as voltage mode control with AVP. AVP does create a current feedback loop but the compensation signal does not directly control the current.

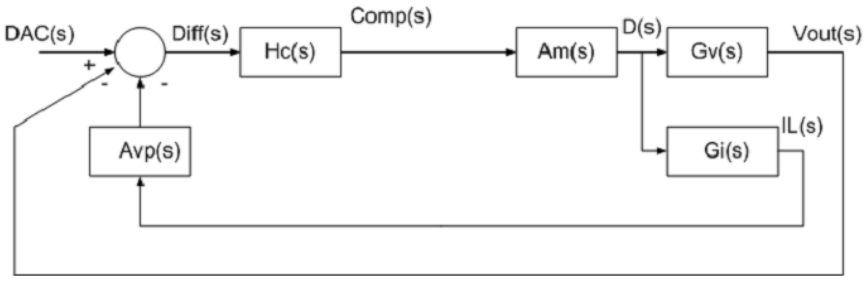


Figure 15. NCP81111 Control Loop

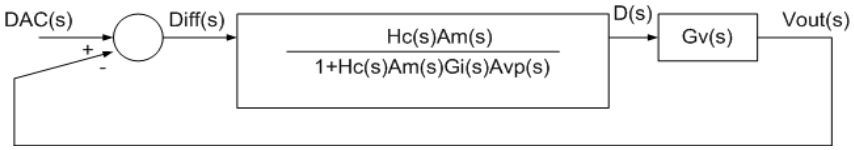


Figure 16. Current Loop Closed

Using the Test Ports for Debug

This controller has dedicated test ports for monitoring internal signals for debug purposes. Some of the more useful settings include access to the internal droop, IOUT, and comp signals. The test pins have some impedance. For proper monitoring please use 1 MQ or higher impedance probes.

Analog Application Notes Section

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points.

Differential Current Feedback Amplifiers

Each phase has a low offset differential amplifier to sense that phase current for current balance. Resistor RCSN must be 14 kΩ to work correctly with the internal thermal compensation. It is also recommended that the voltage sense element be no less than 0.5 mΩ for accurate current monitor and balance. The internal CS pin resistance forms a divider with the external CS filter resistor. Only 14 kΩ may be used for the external resistor. Fine tuning of the CS filter must be done by adjusting the capacitor values. Two parallel capacitors should be placed on each phase to allow for fine tuning of the time constant of the CS filter. The effective R in the RC time constant calculation will always be 10 kΩ. Select the C based on the L/(DCR * 10k) = CCSN. The internal thermal compensation resistor attenuates the signal from the inductor DCR. The thermal gain is approximately 0.75 at 25C for the inductor current sensing inputs. When calculating the droop gain the thermal gain effect must be included. For best droop and IMON offset performance RCSN should be of the metal film type resistor. Using a larger thick film 14 kΩ 0805 case size or two thick film 0603 case size resistors in series can offer improved current sense offset performance over a standard 0603 case size.

Equation 7 − Initial Estimate Equation for Ccs Total

$$\frac{L}{DCR \cdot 10k} = Ccs\_total \qquad \text{(eq. 7)}$$

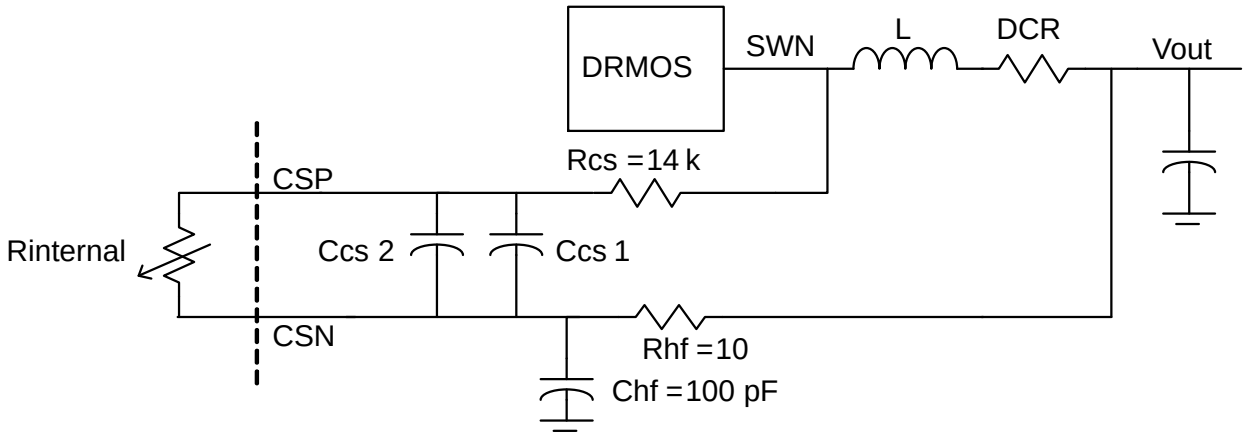


Figure 17. Phase Current Sense Network

TSENSE

One temperature sense input is provided which monitors both VR_HOT and Inductor temperature for thermal compensation. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. There are two internal networks that connect to the NTC depending on the measured temperature to extend the accuracy of the thermal measurement across a greater temperature range. The hot and cold range limits are controlled by the internal user registers. The voltage on the temperature sense input is sampled by the internal A/D converter and then digitally converted to temperature and stored in SVID register. A 220k NTC similar to the Murata NCP18WM224J03RB should be used.

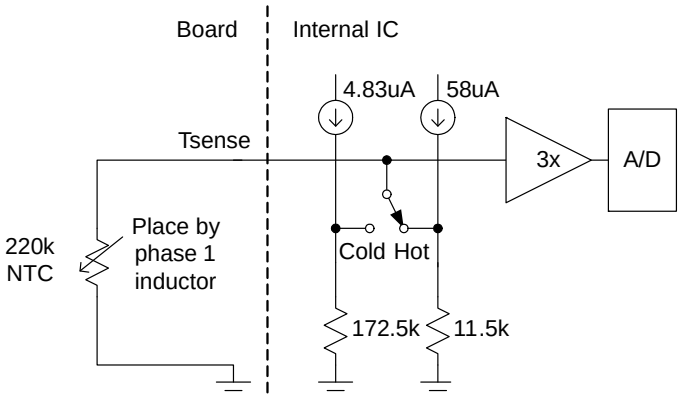


Figure 18. Thermal Sense Diagram

Equation 8 − Tsense Voltage Calculation

$$V_{ADC} = 3 \cdot I_{bias} \cdot \frac{\left(R_{NTC} \cdot R_{internal}\right)}{\left(R_{NTC} + R_{internal}\right)} \qquad \text{(eq. 8)}$$

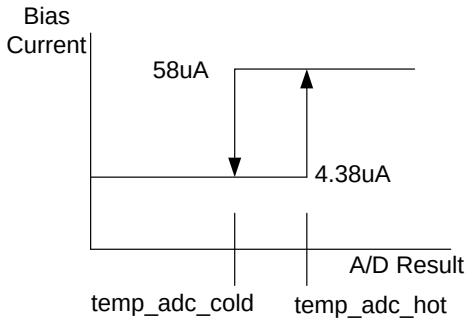


Figure 19. Thermal Bias Current Selection Function

The onboard A/D converter has 10 bits and the maximum DAC voltage is 2.56 V with 2.5 mV per step. The user enters two constants 1/M and C for both the thermal ranges this adjusts the temperature calculation reported for the temperature registers and for VR_HOT activation. C has an offset effect and M adjusts a slope effect. This allows the user to adjust the thermal gain. The conversion equation form the ADC result to the reported temperature is shown below.

Equation 9 − A/D Temperature Conversion Equation

$$\text{Temperature} = \frac{C - \text{Result}_{ADC}}{M} = \frac{C - 3 \cdot V_{Tsense}}{M} \qquad \text{(eq. 9)}$$

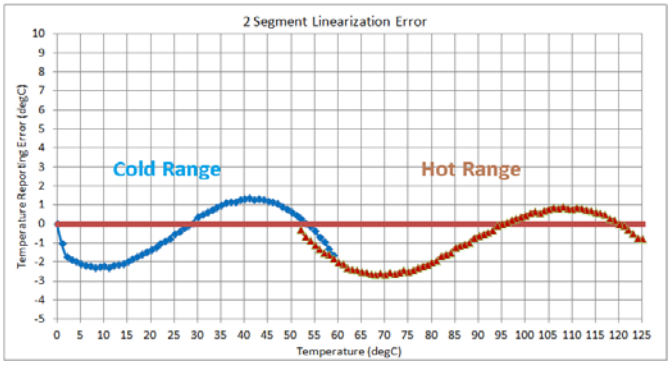


Figure 20. Example Results of the Thermal Sense Circuit

TSENSE CONFIGURATION TABLE

Function	Register	Notes
temp_adc_cold_low	100d<7:0>	Default value = DEh = 222d => 57C
temp_adc_cold_high	101d<1:0>	Default value = 0h
temp_adc_hot_low	105d<7:0>	Default value = A2h
temp_adc_hot_high	106d<1:0>	Default value = 2h 2A2h = 674 => 54C
temp_inv_m_cold	102d<7:0>	1/M used for the cold range temperature calculation. Default value = 18h = 24d
temp_inv_m_hot	107d<1:0>	1/M used for the hot range temperature calculation. Default value = 28h = 40d
Temp_c_cold_low	103d<7:0>	Default value = 3Ch
Temp_c_cold_high	104d<1:0>	Default value = 03h note 33Ch = 828d
Temp_c_hot_low	108d<7:0>	Default value = FDh
Temp_c_hot_high	109d<1:0>	Default value= 03h note 3Fdh = 1021d

VR_HOT Operation

The VR_HOT thresholds are controlled by the user setting for the Temp Max register. Calculate the voltage thresholds on the Tsense pin using the user settings for C and 1/M . See the equations below.

$$\text{Tsense\_VR\_HOT\_Assert\_Threshold} = \frac{\left(C_{HOT} - M_{HOT} \cdot \text{Temp\_Max}\right) \cdot 2.56\ \text{V}}{10243} \quad \text{(eq. 10)}$$

$$\text{Tsense\_VR\_HOT\_Deassert\_Threshold} = \frac{\left[C_{HOT} - M_{HOT} \cdot (\text{Temp\_ThermAlert})\right] \cdot 2.56\ \text{V}}{10243} \quad \text{(eq. 11)}$$

TEMP_MAX CONFIGURATION TABLE

Function	Register	Notes
vr_temp_max	18d<7:0>	1degC per LSB

INPUT UNDER-VOLTAGE PROTECTION

Under Voltage Protection

Under voltage protection will shut off the output similar to OCP to protect against short circuits. The threshold is specified in the parametric spec tables and is not adjustable. The controller is protected against under−voltage on the VCC and VFF pins.

Function	Register	Notes
disable_vff_uvlo	52d<2>	0:VFF UVLO Enabled 1: VFF UVLO Disabled
Vff_threshold	98d<6:0>	LSB = 200 mV Default = 0

Assigning Unused PWM and CS Pins

When using lower phase count arrangements always connect unused CSN and CSP pins together and to the nearest CSN signal. Unused PWM pins should be left floating.

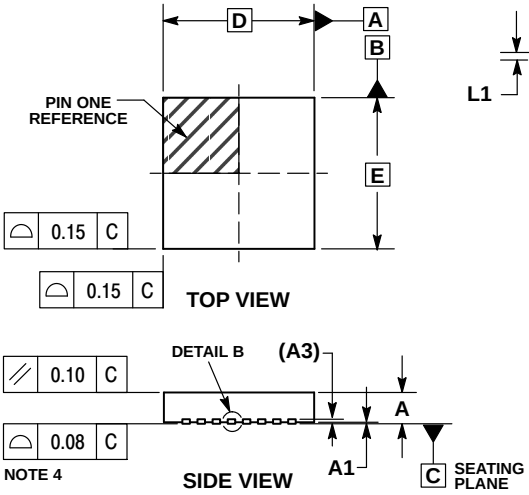
Phase Count	PWM1	PWM2	PWM3	CSP1	CSN1	CSP2	CSN2	CSP3	CSN3
3	Used	Used	Used	Used	Used	Used	Used	Used	Used
2	Used	Used	No Connect	Used	Used	Used	Used	Connect to CSN2	Connect to CSN2
1	Used	No Connect	No Connect	Used	Used	Connect to CSN1	Connect to CSN1	Connect to CSN1	Connect to CSN1

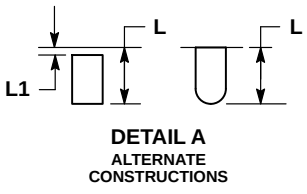
Layout Notes

The NCP81111 has differential voltage and current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To insure proper function there are some general rules to follow. Always place the inductor current sense RC filters as close to the CSN and CSP pins on the controller as possible. Place the V_{CC} decoupling caps as close as possible to the controller VCC pin.

PACKAGE DIMENSIONS

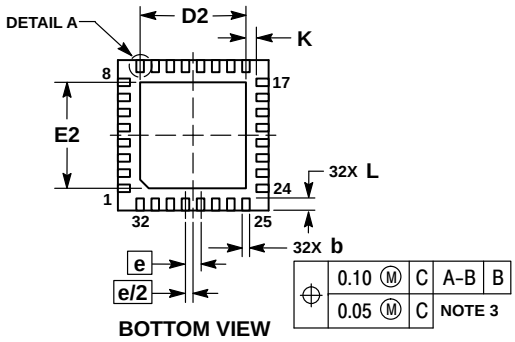
QFN32 5x5, 0.5P
CASE 485CE
ISSUE O



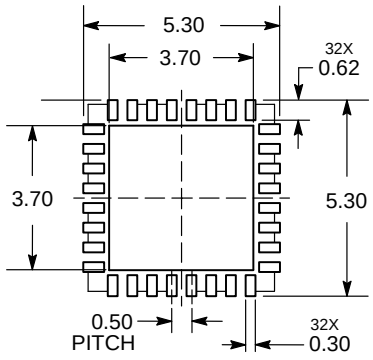


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	–––	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.50 BSC	
K	0.20	–––
L	0.30	0.50
L1	–––	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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