NCP9004

2.65 W Filterless Class-D Audio Power Amplifier

The NCP9004 is a cost−effective mono Class−D audio power amplifier capable of delivering 2.65 W of continuous average power to 4.0 Ω from a 5.0 V supply in a Bridge Tied Load (BTL) configuration. Under the same conditions, the output power stage can provide 1.4 W to a 8.0 Ω BTL load with less than 1% THD+N. For cellular handsets or PDAs it offers space and cost savings because no output filter is required when using inductive tranducers. With more than 90% efficiency and very low shutdown current, it increases the lifetime of your battery and drastically lowers the junction temperature.

The NCP9004 processes analog inputs with a pulse width modulation technique that lowers output noise and THD when compared to a conventional sigma−delta modulator. The device allows independent gain while summing signals from various audio sources. Thus, in cellular handsets, the earpiece, the loudspeaker and even the melody ringer can be driven with a single NCP9004. Due to its low 42 μV noise floor, A−weighted, a clean listening is guaranteed no matter the load sensitivity.

Features

- Optimized PWM Output Stage: Filterless Capability
- Efficiency up to 90%
  Low 2.5 mA Typical Quiescent Current
- Large Output Power Capability: 1.4 W with 8.0 Ω Load and THD+N < 1%
- Wide Supply Voltage Range: 2.5−5.5 V Operating Voltage
- High Performance, THD+N of 0.03% @ V_p = 5.0 V,
  R_L = 8.0 Ω, P_{out} = 100 mW
- Excellent PSRR (−65 dB): No Need for Voltage Regulation
- Surface Mounted Package 9−Pin Flip−Chip CSP (SnPb and Pb−Free)
- Fully Differential Design. Eliminates Two Input Coupling Capacitors
- Very Fast Turn On/Off Times with Advanced Rising and Falling Gain Technique
- External Gain Configuration Capability
- Internally Generated 250 kHz Switching Frequency
- Short Circuit Protection Circuitry
- “Pop and Click” Noise Protection Circuitry

Applications

- Cellular Phone
- Portable Electronic Devices
- PDAs and Smart Phones
- Portable Computer

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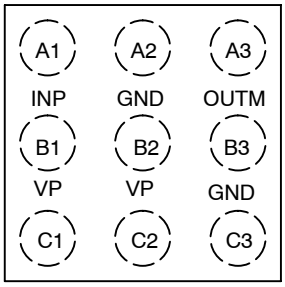
MARKING DIAGRAM

9−PIN FLIP−CHIP CSP
FC SUFFIX
CASE 499E

MAQ = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

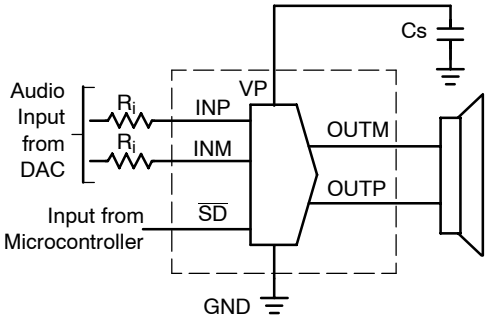
PIN CONNECTIONS
9−Pin Flip−Chip CSP

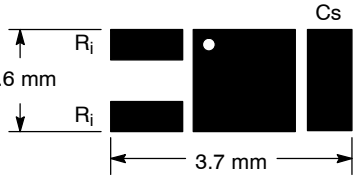


(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.





Solution Size

TYPICAL APPLICATION

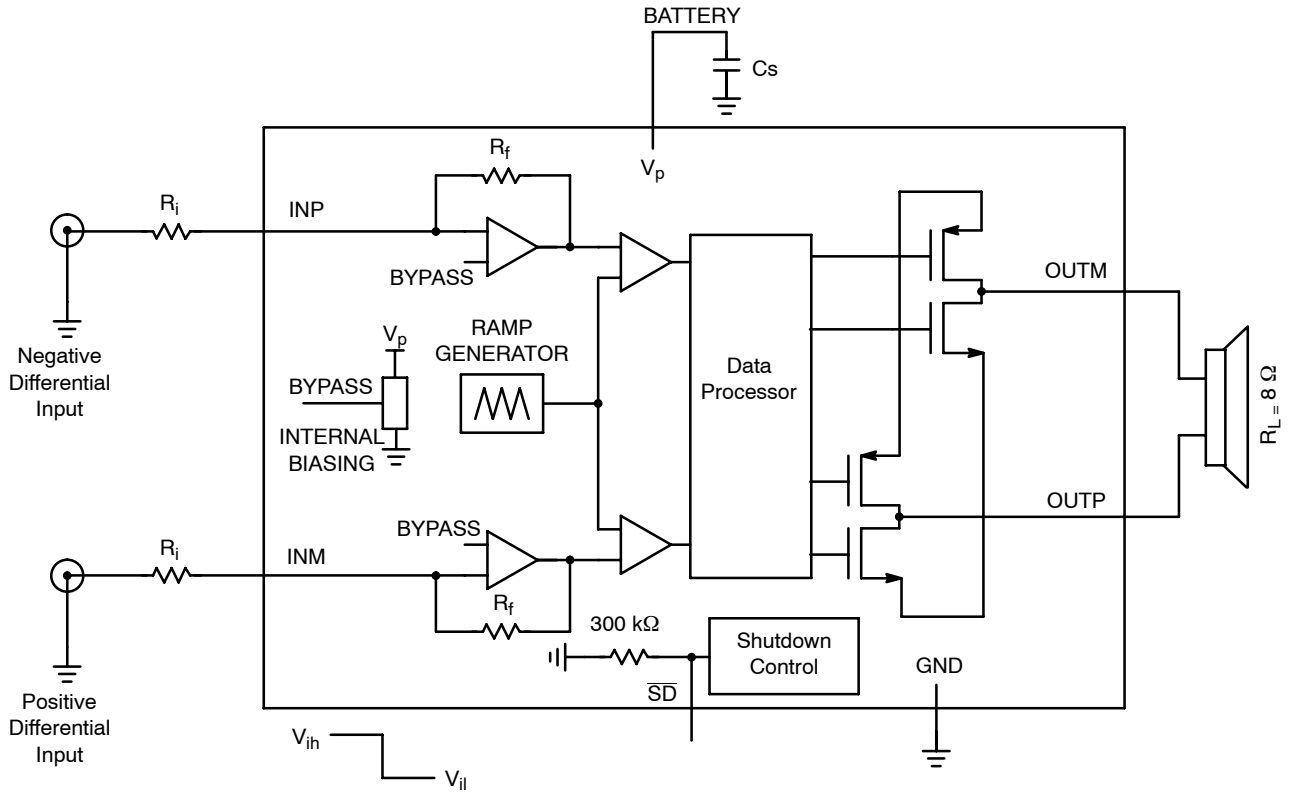


Figure 1. Typical Application

PIN DESCRIPTION

Pin No.	Symbol	Type	Description
A1	INP	I	Positive Differential Input.
A2	GND	I	Analog Ground.
A3	OUTM	O	Negative BTL Output.
B1	V_p	I	Power Analog Positive Supply. Range: 2.5 V – 5.5 V.
B2	V_p	I	Power Analog Positive Supply. Range: 2.5 V – 5.5 V.
B3	GND	I	Analog Ground.
C1	INM	I	Negative Differential Input.
C2	$\overline{SD}$	I	The device enters in Shutdown Mode when a low level is applied on this pin. An internal 300 kΩ resistor will force the device in shutdown mode if no signal is applied to this pin. It also helps to save space and cost.
C3	OUTP	O	Positive BTL Output.

MAXIMUM RATINGS

Symbol	Rating	Max	Unit
V_p	Supply Voltage Active Mode Shutdown Mode	6.0 7.0	V
V_{in}	Input Voltage	−0.3 to V_{CC} +0.3	V
I_{out}	Max Output Current (Note 1)	1.5	A
P_d	Power Dissipation (Note 2)	Internally Limited	–
T_A	Operating Ambient Temperature	−40 to +85	°C
T_J	Max Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	90 (Note 3)	°C/W
– –	ESD Protection Human Body Model (HBM) (Note 4) Machine Model (MM) (Note 5)	> 2000 > 200	V
–	Latchup Current @ T_A = 85°C (Note 6)	± 70	mA
MSL	Moisture Sensitivity (Note 7)	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The device is protected by a current breaker structure. See “Current Breaker Circuit” in the Description Information section for more information.
2. The thermal shutdown is set to 160°C (typical) avoiding irreversible damage to the device due to power dissipation.
3. For the 9−Pin Flip−Chip CSP package, the $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. When using ground and power planes, the value is around 90°C/W, as specified in table.
4. Human Body Model: 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114. B2 pin (Vp) qualified at 1500 V.
5. Machine Model: 200 pF discharged through all pins following specification JESD22/A115.
6. Latchup Testing per JEDEC Standard JESD78.
7. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (Limits apply for T_A = +25°C unless otherwise noted)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
V_p	Operating Supply Voltage	T_A = −40°C to +85°C	2.5	–	5.5	V
I_{dd}	Supply Quiescent Current	V_p = 3.6 V, R_L = 8.0 Ω	–	2.15	–	mA
		V_p = 5.5 V, No Load	–	2.61	–	
		V_p from 2.5 V to 5.5 V, No Load				
		T_A = −40°C to +85°C	–	–	4.6	
I_{sd}	Shutdown Current	V_p = 4.2 V				μA
		T_A = +25°C	–	0.42	0.8	
		T_A = +85°C	–	0.45	–	
		V_p = 5.5 V				μA
		T_A = +25°C	–	0.8	1.5	
		T_A = +85°C	–	0.9	–	
V_{sdih}	Shutdown Voltage High	–	1.2	–	–	V
V_{sdil}	Shutdown Voltage Low	–	–	–	0.4	V
F_{sw}	Switching Frequency	V_p from 2.5 V to 5.5 V T_A = −40°C to +85°C	190	250	310	kHz
G	Gain	R_L = 8.0 Ω	$\frac{285\ k\Omega}{R_i}$	$\frac{300\ k\Omega}{R_i}$	$\frac{315\ k\Omega}{R_i}$	$\frac{V}{V}$
Rs	Resistance from $\overline{SD}$ to GND	–	–	300	–	kΩ
Vos	Output Offset Voltage	V_p = 5.5 V	–	6.0	–	mV
Ton	Turn On Time	V_p from 2.5 V to 5.5 V	–	9.0	–	ms
Toff	Turn Off Time	V_p from 2.5 V to 5.5 V	–	5.0	–	ms
Tsd	Thermal Shutdown Temperature	–	–	160	–	°C
Vn	Ouput Noise Voltage	V_p = 3.6 V, f = 20 Hz to 20 kHz				μVrms
		no weighting filter	–	65	–	
		with A weighting filter	–	42	–	
		no weighting filter	–	70	–	μVrms
		with A weighting filter	–	48	–	
Po	RMS Output Power	R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 1%				W
		V_p = 2.5 V	–	0.32	–	
		V_p = 3.0 V	–	0.48	–	
		V_p = 3.6 V	–	0.7	–	
		V_p = 4.2 V	–	0.97	–	
		V_p = 5.0 V	–	1.38	–	
		R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 10%				W
		V_p = 2.5 V	–	0.4	–	
		V_p = 3.0 V	–	0.59	–	
		V_p = 3.6 V	–	0.87	–	
		V_p = 4.2 V	–	1.19	–	
		V_p = 5.0 V	–	1.7	–	
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 1%				W
		V_p = 2.5 V	–	0.49	–	
		V_p = 3.0 V	–	0.72	–	
		V_p = 3.6 V	–	1.06	–	
		V_p = 4.2 V	–	1.62	–	
		V_p = 5.0 V	–	2.12	–	
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 10%				W
		V_p = 2.5 V	–	0.6	–	
		V_p = 3.0 V	–	0.9	–	
		V_p = 3.6 V	–	1.33	–	
		V_p = 4.2 V	–	2.0	–	
		V_p = 5.0 V	–	2.63	–	

ELECTRICAL CHARACTERISTICS (Limits apply for T_A = +25°C unless otherwise noted)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
–	Efficiency	R_L = 8.0 Ω, f = 1.0 kHz				%
		V_p = 5.0 V, P_{out} = 1.2 W	–	91	–	
		V_p = 3.6 V, P_{out} = 0.6 W	–	90	–	
		R_L = 4.0 Ω, f = 1.0 kHz				%
		V_p = 5.0 V, P_{out} = 2.0 W	–	82	–	
		V_p = 3.6 V, P_{out} = 1.0 W	–	81	–	
THD+N	Total Harmonic Distortion + Noise	V_p = 5.0 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W	–	0.05	–	%
		V_p = 3.6 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W	–	0.09	–	
CMRR	Common Mode Rejection Ratio	V_p from 2.5 V to 5.5 V, V_{ic} = 0.5 V to V_p – 0.8 V	–	–62	–	dB
		V_p = 3.6 V, V_{ic} = 1.0 V_{pp}, f = 217 Hz	–	–56	–	
		f = 1.0 kHz	–	–57	–	
PSRR	Power Supply Rejection Ratio	$V_{p\_ripple\_pk-pk}$ = 200 mV, R_L = 8.0 Ω, Inputs AC Grounded, V_p = 3.6 V, f = 217 kHz	–	–62	–	dB
		f = 1.0 kHz	–	–65	–	

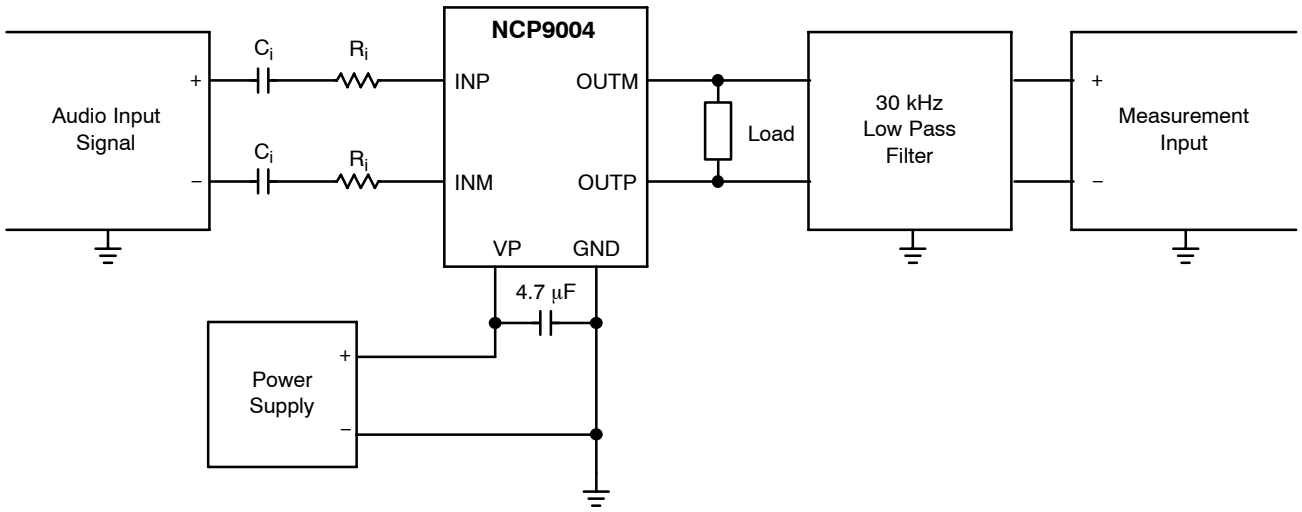


Figure 2. Test Setup for Graphs

NOTES:

1. Unless otherwise noted, C_i = 100 nF and R_i= 150 kΩ. Thus, the gain setting is 2 V/V and the cutoff frequency of the input high pass filter is set to 10 Hz. Input capacitors are shorted for CMRR measurements.
2. To closely reproduce a real application case, all measurements are performed using the following loads:
   R_L = 8 Ω means Load = 15 μH + 8 Ω + 15 μH
   R_L = 4 Ω means Load = 15 μH + 4 Ω + 15 μH
   Very low DCR 15 μH inductors (50 mΩ) have been used for the following graphs. Thus, the electrical load measurements are performed on the resistor (8 Ω or 4 Ω) in differential mode.
3. For Efficiency measurements, the optional 30 kHz filter is used. An RC low−pass filter is selected with (100 Ω, 47 nF) on each PWM output.

TYPICAL CHARACTERISTICS

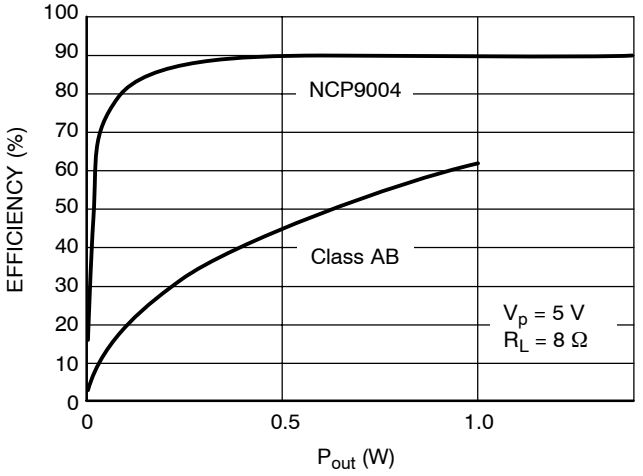


Figure 3. Efficiency vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz

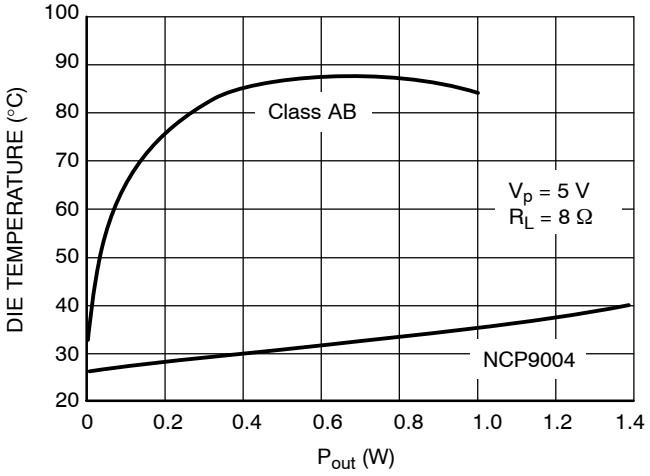


Figure 4. Die Temperature vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz @ T_A = +25°C

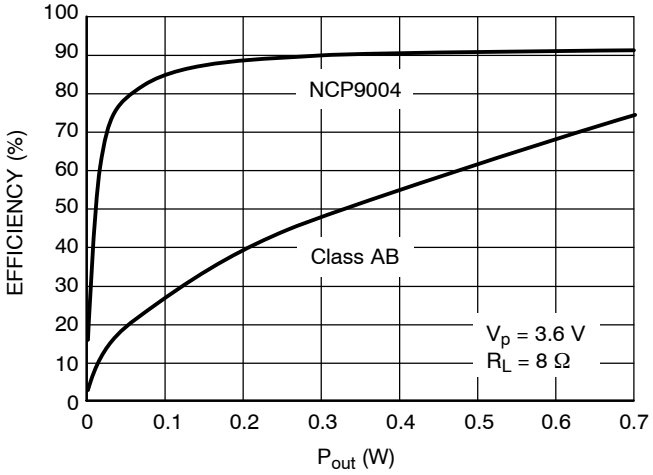


Figure 5. Efficiency vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz

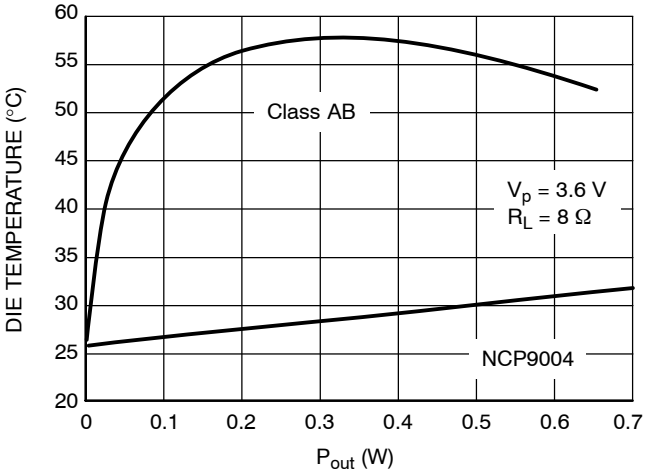


Figure 6. Die Temperature vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz @ T_A = +25°C

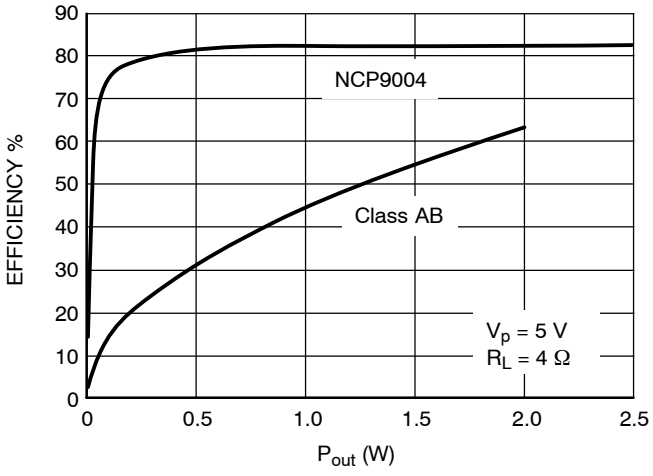


Figure 8. Efficiency vs. P_{out}
V_p = 5 V, R_L = 4 Ω, f = 1 kHz

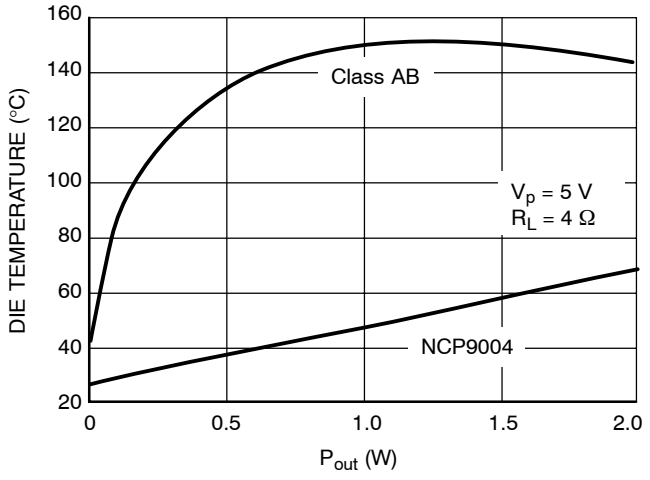


Figure 7. Die Temperature vs. P_{out}
V_p = 5 V, R_L = 4 Ω, f = 1 kHz @ T_A = +25°C

TYPICAL CHARACTERISTICS

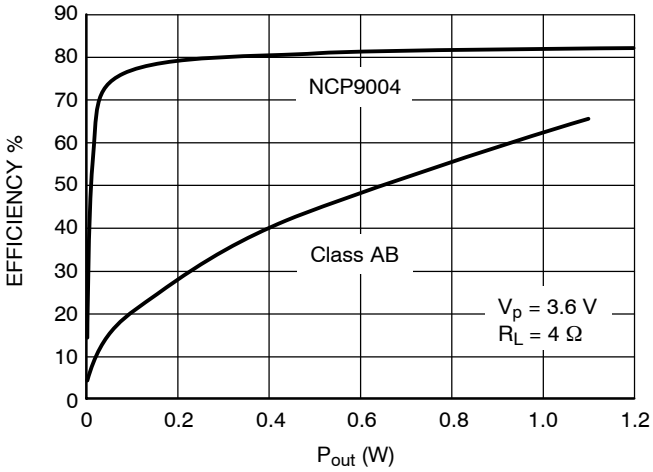


Figure 9. Efficiency vs. P_{out}
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz

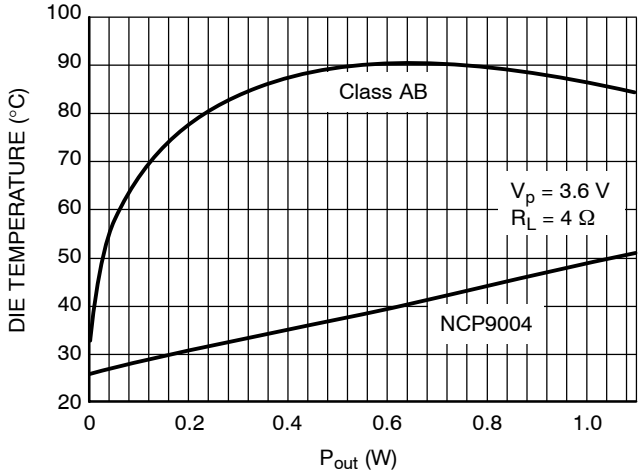


Figure 10. Die Temperature vs. P_{out}
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz @ T_A = +25°C

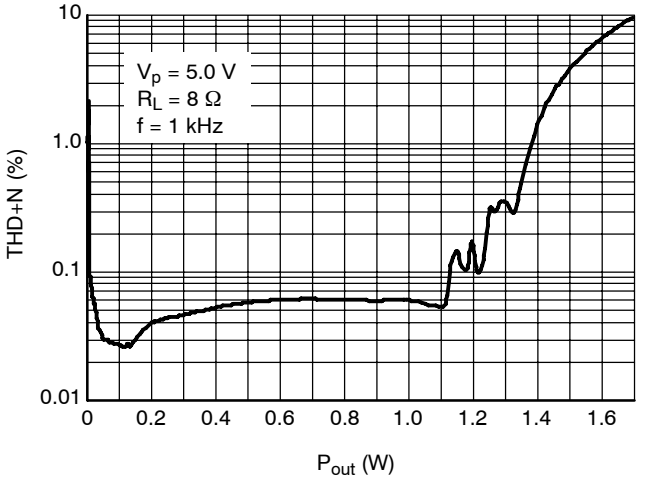


Figure 11. THD+N vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz

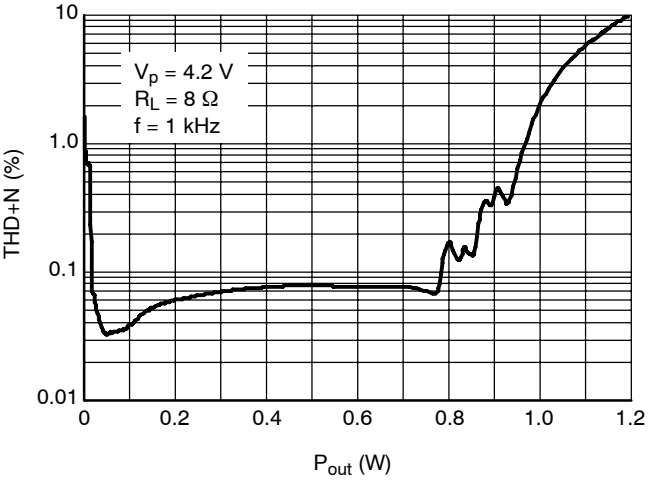


Figure 12. THD+N vs. P_{out}
V_p = 4.2 V, R_L = 8 Ω, f = 1 kHz

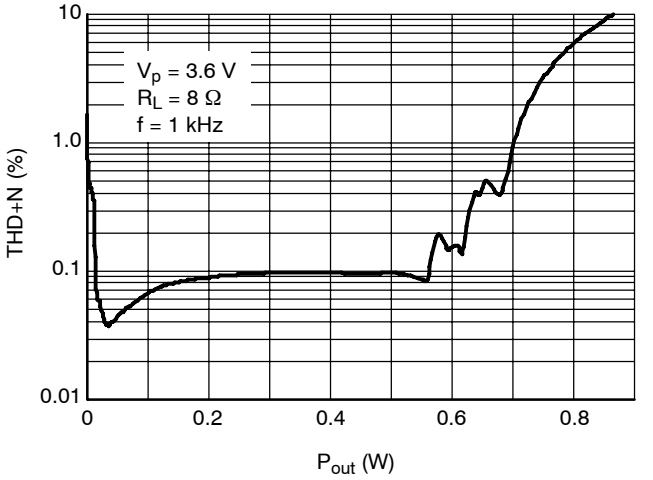


Figure 13. THD+N vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz

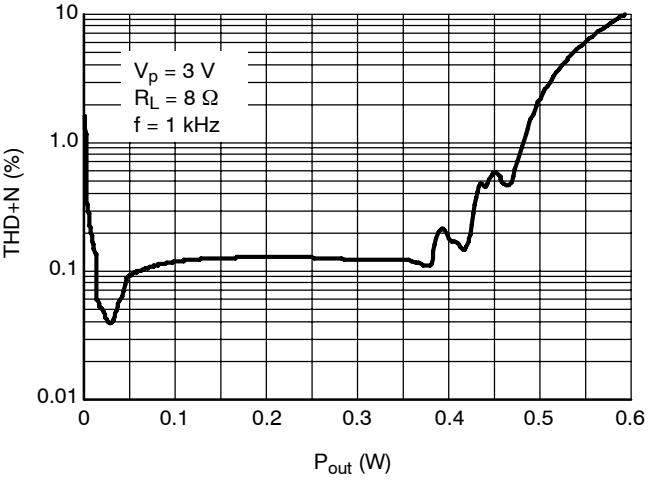


Figure 14. THD+N vs. P_{out}
V_p = 3 V, R_L = 8 Ω, f = 1 kHz

TYPICAL CHARACTERISTICS

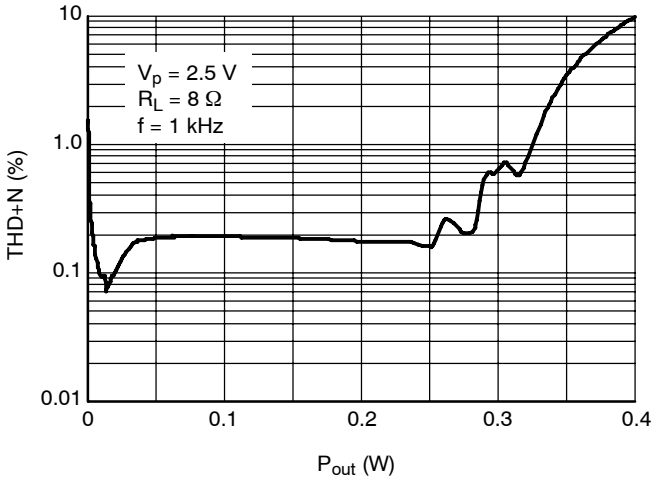


Figure 15. THD+N vs. Pout
V_p = 2.5 V, R_L = 8 Ω, f = 1 kHz

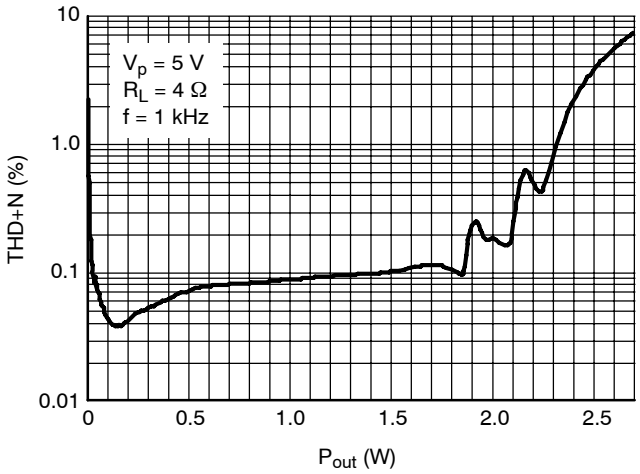


Figure 16. THD+N vs. Pout
V_p = 5 V, R_L = 4 Ω, f = 1 kHz

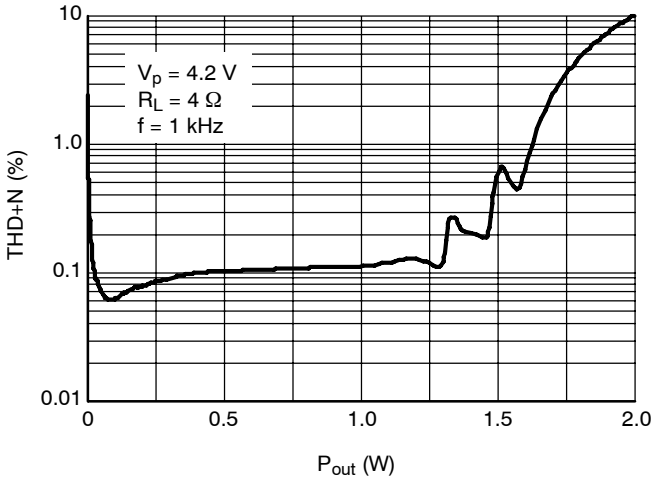


Figure 17. THD+N vs. Pout
V_p = 4.2 V, R_L = 4 Ω, f = 1 kHz

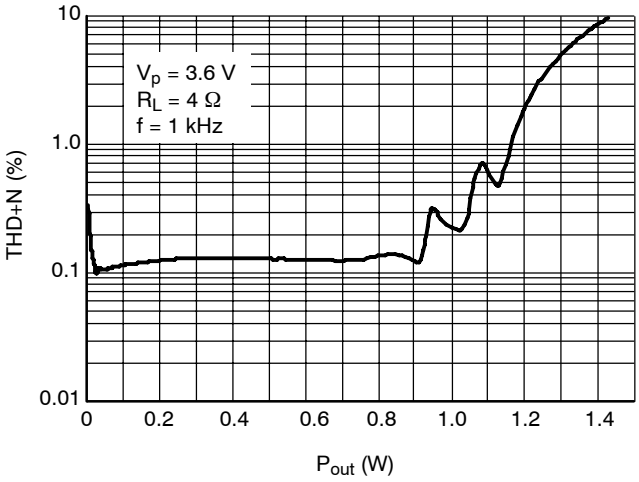


Figure 18. THD+N vs. Pout
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz

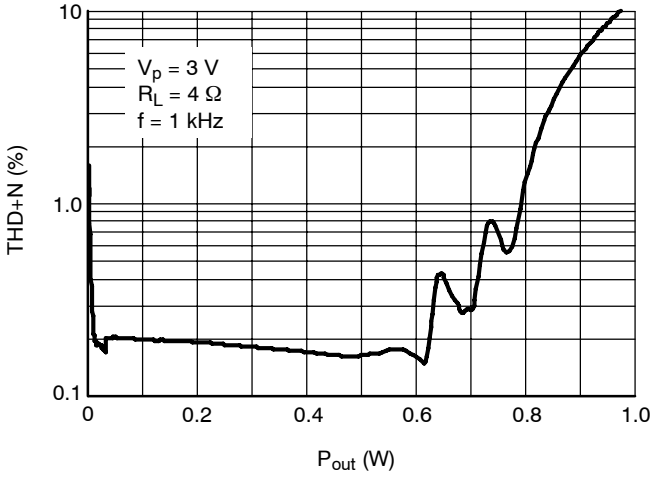


Figure 19. THD+N vs. Power Out
V_p = 3 V, R_L = 4 Ω, f = 1 kHz

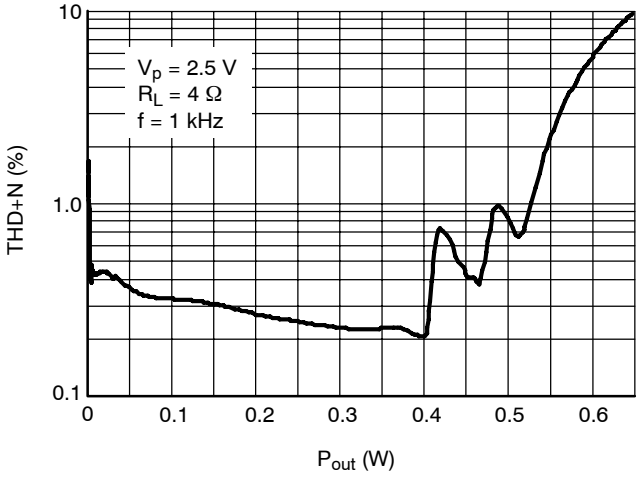


Figure 20. THD+N vs. Power Out
V_p = 2.5 V, R_L = 4 Ω, f = 1 kHz

TYPICAL CHARACTERISTICS

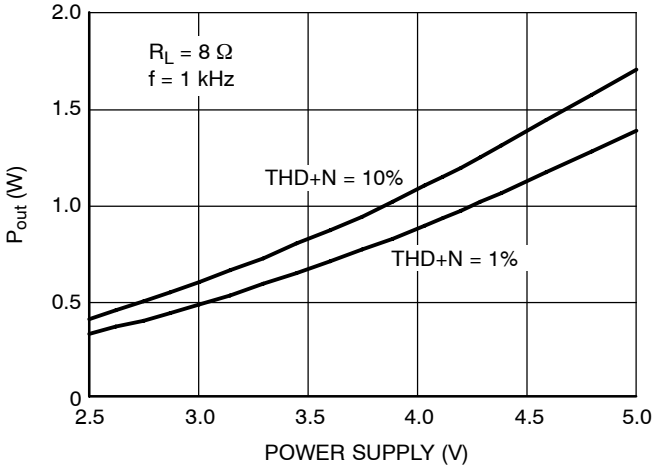


Figure 21. Output Power vs. Power Supply
R_L = 8 Ω @ f = 1 kHz

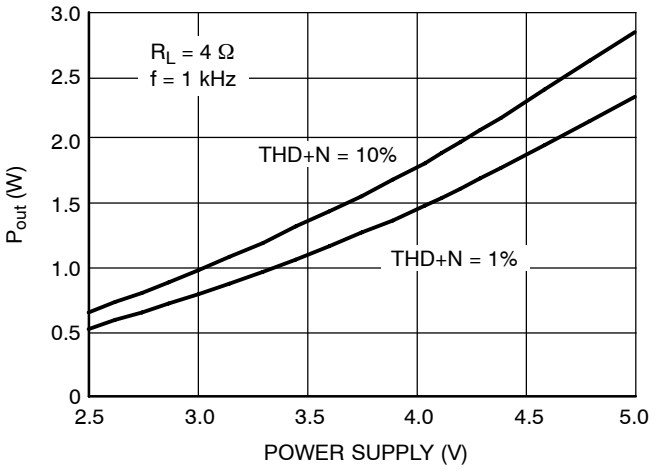


Figure 22. Output Power vs. Power Suppy
R_L = 4 Ω @ f = 1 kHz

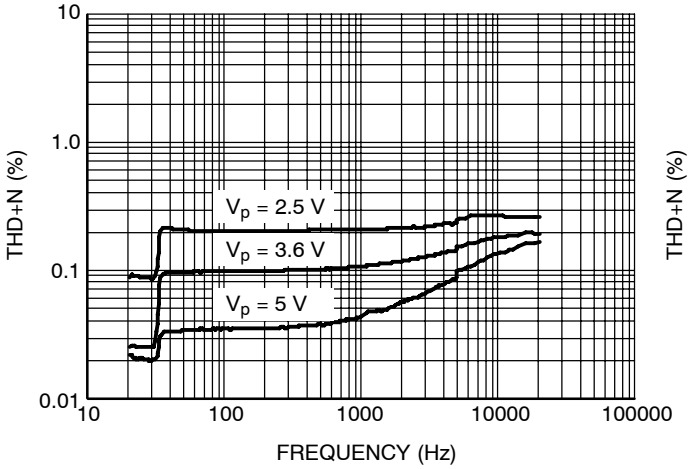


Figure 23. THD+N vs. Frequency
R_L = 8 Ω, P_{out} = 250 mW @ f = 1 kHz

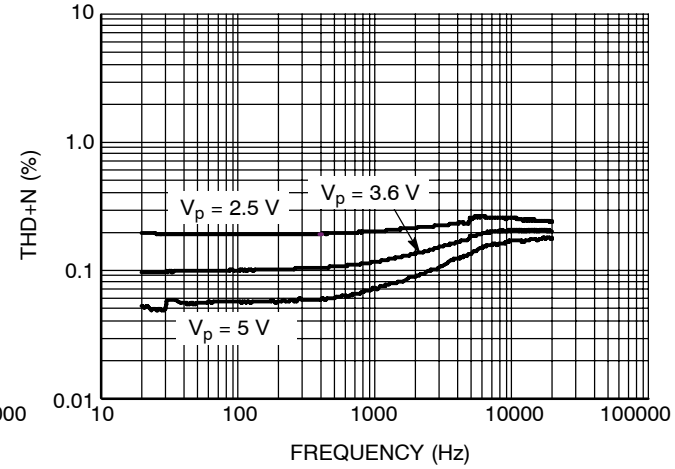


Figure 24. THD+N vs. Frequency
R_L = 4 Ω, P_{out} = 250 mW @ f = 1 kHz

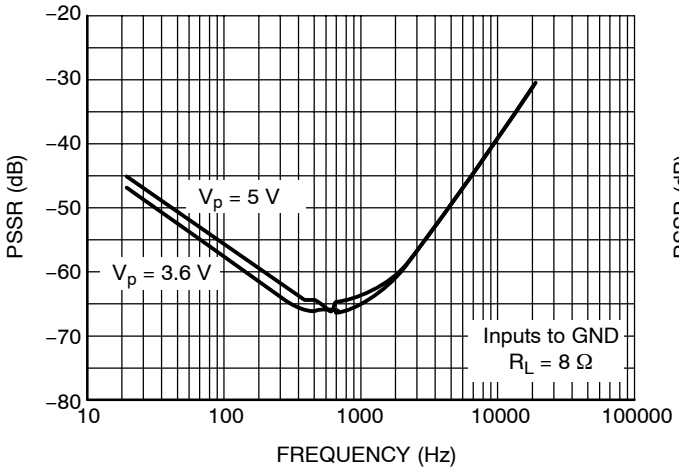


Figure 25. PSRR vs. Frequency
Inputs Grounded, R_L = 8 Ω, Vripple = 200 mvpkpk

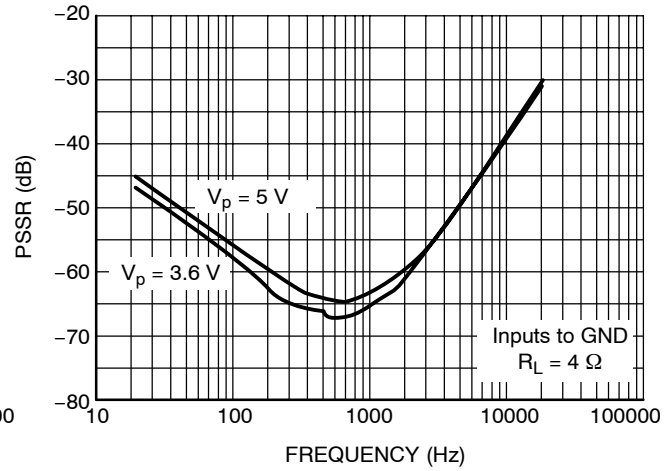


Figure 26. PSRR vs. Frequency
Inputs grounded, R_L = 4 Ω, Vripple = 200 mVpkpk

TYPICAL CHARACTERISTICS

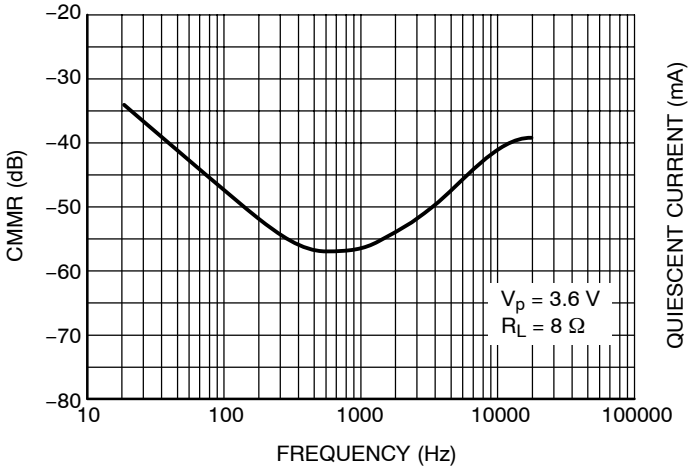


Figure 27. PSRR vs. Frequency
V_p = 3.6 V, R_L = 8 Ω, Vic = 200 mvpkpk

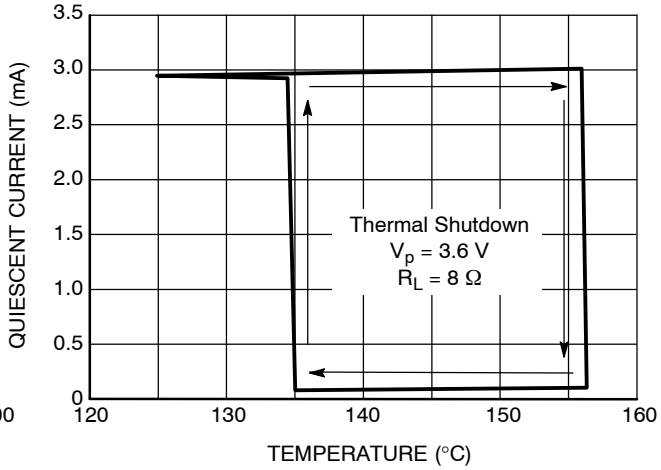


Figure 28. Thermal Shutdown vs. Temperature
V_p = 5 V, R_L = 8 Ω,

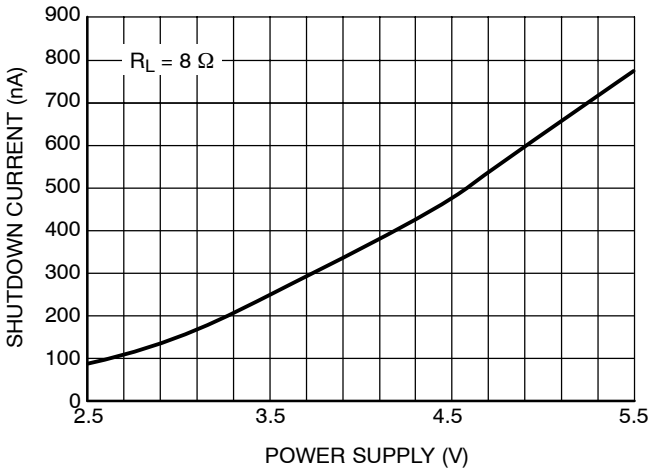


Figure 29. Shutdown Current vs. Power Supply
R_L = 8 Ω

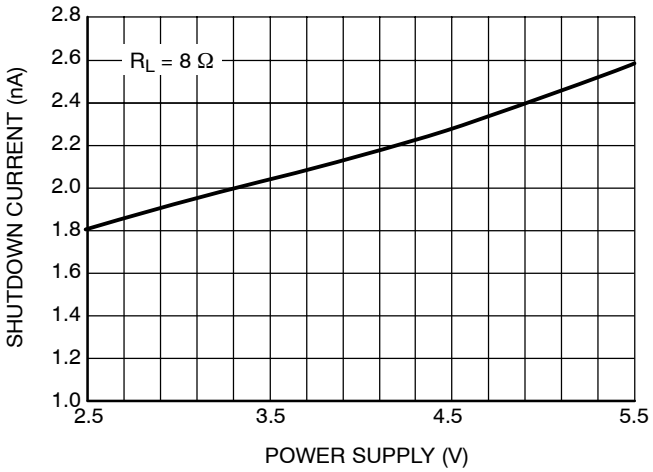


Figure 30. Quiescent Current vs. Power Supply
R_L = 8 Ω

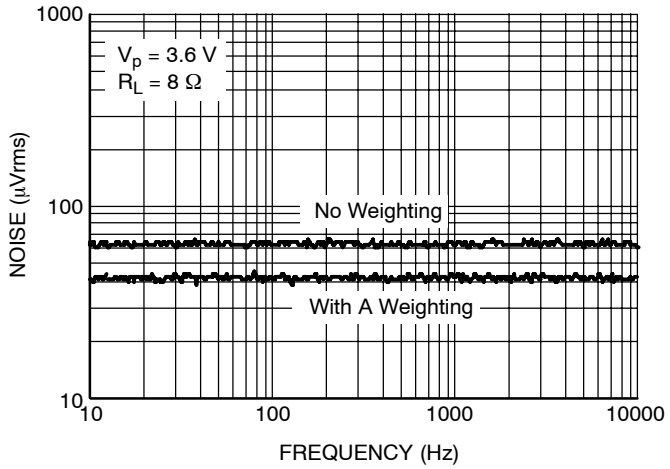


Figure 31. Noise Floor, Inputs AC Grounded
with 1 μF V_p = 3.6 V

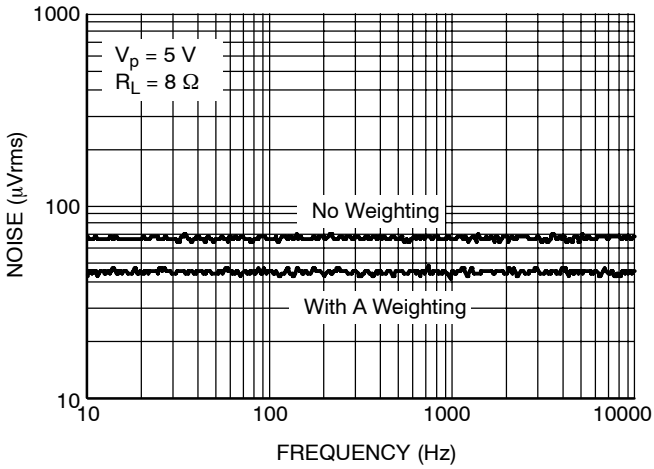


Figure 32. Noise Floor, Inputs AC Grounded
with 1 μF V_p = 5 V

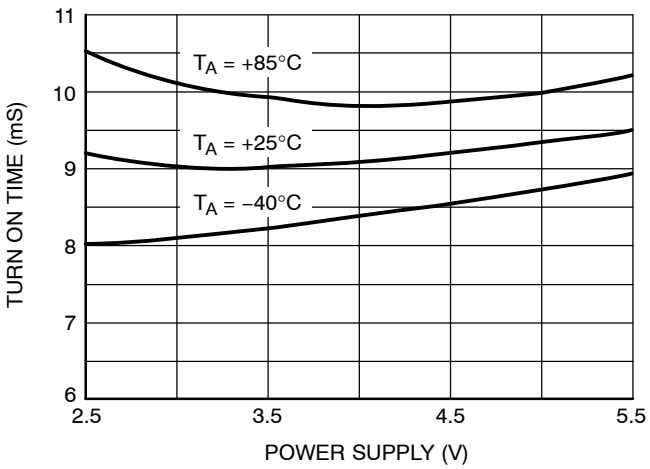


Figure 33. Turn on Time

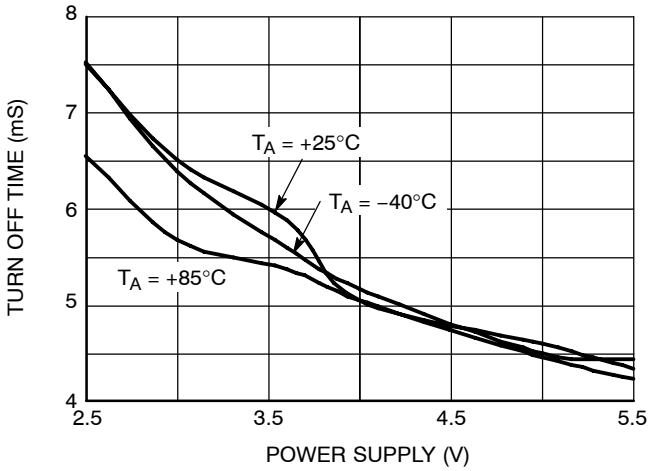


Figure 34. Turn off Time

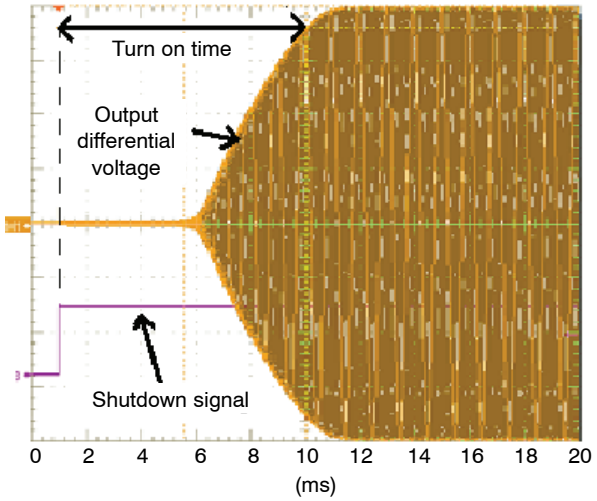


Figure 35. Turn on sequence
V_p = 3.6 V, R_L = 8 Ω

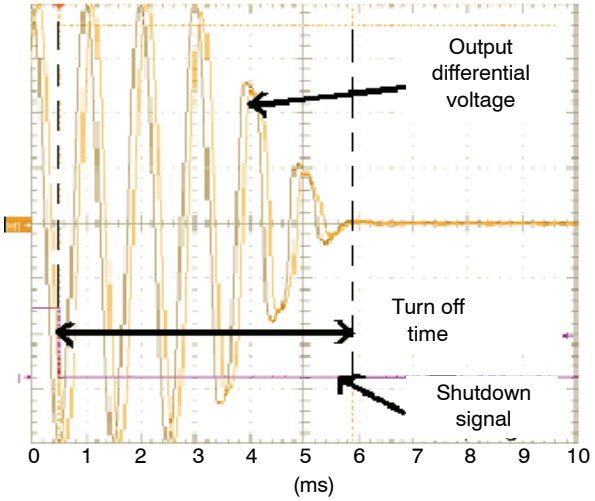


Figure 36. Turn off sequence
V_p = 3.6 V, R_L = 8 Ω

DESCRIPTION INFORMATION

Detailed Description

The basic structure of the NCP9004 is composed of one analog pre−amplifier, a pulse width modulator and an H−bridge CMOS power stage. The first stage is externally configurable with gain−setting resistor R_i and the internal fixed feedback resistor R_f (the closed−loop gain is fixed by the ratios of these resistors) and the other stage is fixed. The load is driven differentially through two output stages.

The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, the typical values of which are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors is typically 0.3 Ω.

Turn On and Turn Off Transitions

In order to eliminate “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When a logic high is applied to the shutdown pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly (5.0 ms). This method to turn on the device is optimized in terms of rejection of “pop and click” noises. Thus, the total turn on time to get full power to the load is 9 ms (typical) (see Figure 35).

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. No power is delivered to the load 5 ms after a falling edge on the shutdown pin (see Figure 36). Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

Shutdown Function

The device enters shutdown mode when the shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 1.5 μA.

Current Breaker Circuit

The maximum output power of the circuit corresponds to an average current in the load of 820 mA.

In order to limit the excessive power dissipation in the load if a short−circuit occurs, a current breaker cell shuts down the output stage. The current in the four output MOS transistors are real−time controlled, and if one current exceeds the threshold set to 1.5 A, the MOS transistor is opened and the current is reduced to zero. As soon as the short−circuit is removed, the circuit is able to deliver the expected output power.

This patented structure protects the NCP9004. Since it completely turns off the load, it minimizes the risk of the chip overheating which could occur if a soft current limiting circuit was used.

APPLICATION INFORMATION

NCP9004 PWM Modulation Scheme

The NCP9004 uses a PWM modulation scheme with each output switching from 0 to the supply voltage. If V_{in} = 0 V outputs OUTM and OUTP are in phase and no current is flowing through the differential load. When a positive signal is applied, OUTP duty cycle is greater than 50% and OUTM is less than 50%. With this configuration, the current through the load is 0 A most of the switching period and thus power losses in the load are lowered.

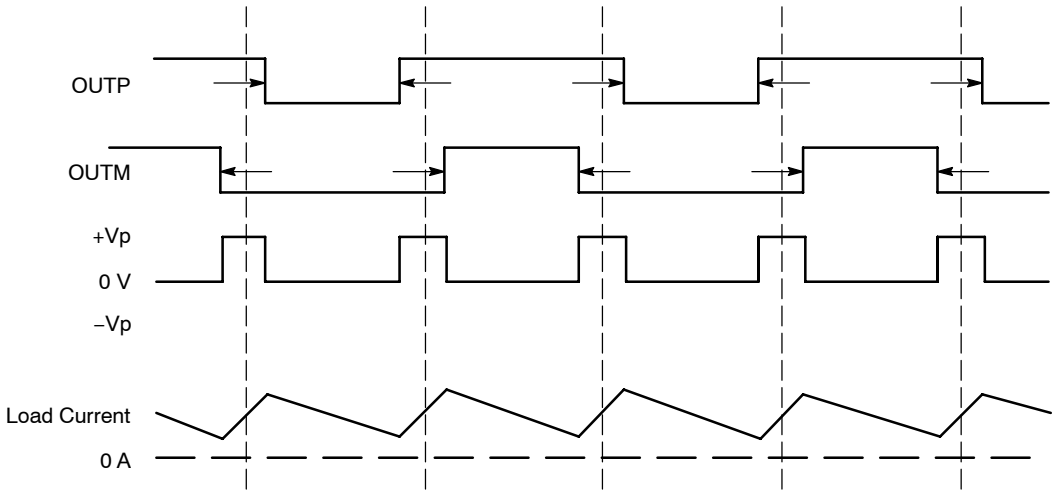


Figure 37. Output Voltage and Current Waveforms into an Inductive Loudspeaker DC Output Positive Voltage Configuration

Voltage Gain

The first stage is an analog amplifier. The second stage is a comparator: the output of the first stage is compared with a periodic ramp signal. The output comparator gives a pulse width modulation signal (PWM). The third and last stage is the direct conversion of the PWM signal with MOS transistors H−bridge into a powerful output signal with low impedance capability.

The total gain of the device is typically set to:

$$\frac{300\ k\Omega}{R_i}$$

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{in}, the cut−off frequency is given by $Fc = \frac{1}{2 \times \pi \times R_i \times C_i}$.

When using an input resistor set to 150 kΩ, the gain configuration is 2 V/V. In such a case, the input capacitor selection can be from 10 nF to 1 μF with cutoff frequency values between 1 Hz and 100 Hz. The NCP9004 also includes a built in low pass filtering function. It's cut off frequency is set to 20 kHz.

Optional Output Filter

This filter is optional due to the capability of the speaker to filter by itself the high frequency signal. Nevertheless, the high frequency is not audible and filtered by the human ear.

An optional filter can be used for filtering high frequency signal before the speaker. In this case, the circuit consists of two inductors (15 μH) and two capacitors (2.2 μF) (Figure 38). The size of the inductors is linked to the output power requested by the application. A simplified version of this filter requires a 1 μF capacitor in parallel with the load, instead of two 2.2 μF connected to ground (Figure 39).

Cellular phones and portable electronic devices are great applications for Filterless Class−D as the track length between the amplifier and the speaker is short, thus, there is usually no need for an EMI filter. However, to lower radiated emissions as much as possible when used in filterless mode, a ferrite filter can often be used. Select a ferrite bead with the high impedance around 100 MHz and a very low DCR value in the audio frequency range is the best choice. The MPZ1608S221A1 from TDK is a good choice. The package size is 0603.

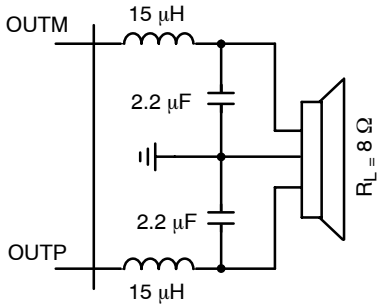


Figure 38. Advanced Optional Audio Output Filter

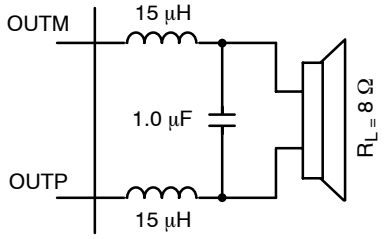


Figure 39. Optional Audio Output Filter

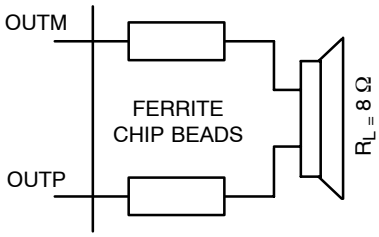


Figure 40. Optional EMI Ferrite Bead Filter

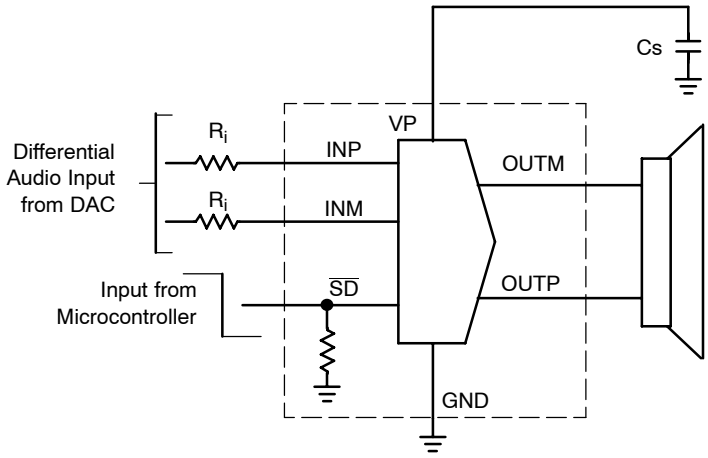


Figure 41. NCP9004 Application Schematic with Fully Differential Input Configuration

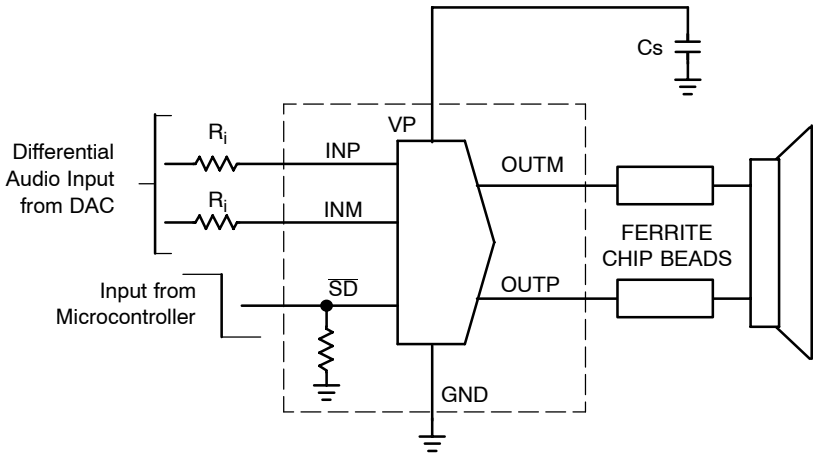


Figure 42. NCP9004 Application Schematic with Fully Differential Input Configuration and Ferrite Chip Beads as an Output EMI Filter

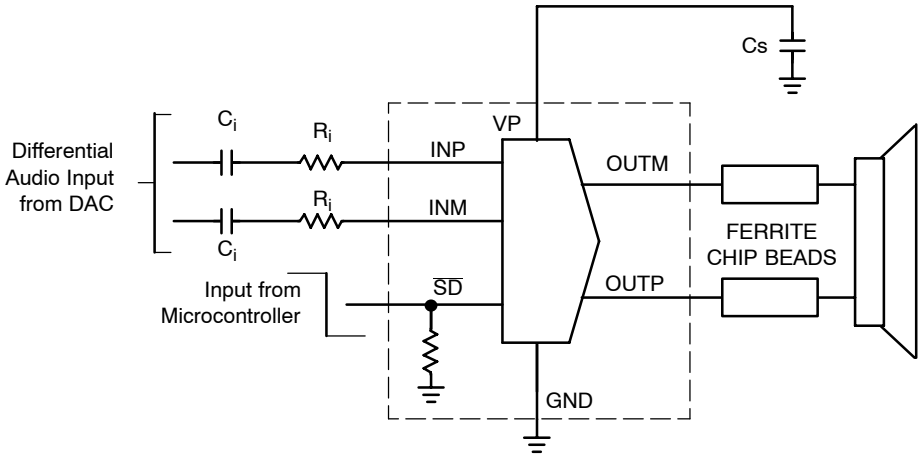


Figure 44. NCP9004 Application Schematic with Differential Input Configuration and High Pass Filtering Function

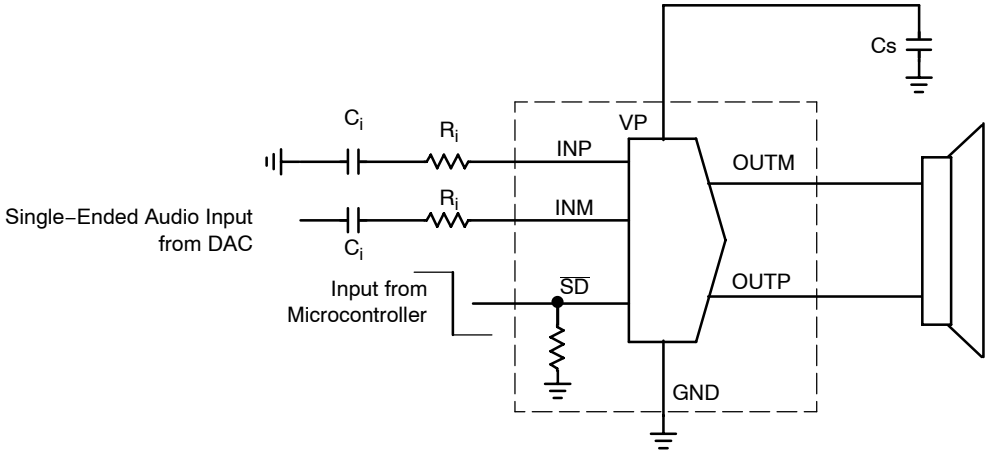


Figure 43. NCP9004 Application Schematic with Single Ended Input Configuration

PCB Layout Information

NCP9004 is suitable for low cost solution. In a very small package it gives all the advantages of a Class−D audio amplifier. Due to its fully differential capability, the audio signal can only be provided by an input resistor. If a low pass filtering function is required, then an input coupling capacitor is needed. The values of these components determine the voltage gain and the bandwidth frequency. The battery positive supply voltage requires a good decoupling capacitor versus the expected distortion.

When the board is using Ground and Power planes with at least 4 layers, a single 4.7 μF filtering ceramic capactior on the bottom face will give optimized performance.

A 1.0 μF low ESR ceramic capacitor can also be used with slightly degraded performances on the THD+N from 0.06% up to 0.2%.

In two layer application, if both V_p pins are connected on the top layer, two decoupling capacitors will improve the THD+N level. For example, a pair of capactors, 470 nF and 4.7 μF, are good choices for filtering the power supply.

The NCP9004 power audio amplifier can operate from 2.5 V until 5.5 V power supply. With less than 2% THD+N, it delivers 500 mW rms output power to a 8.0 Ω load at V_p =3.0 V and 1.0 W rms output power at V_p = 4.0 V.

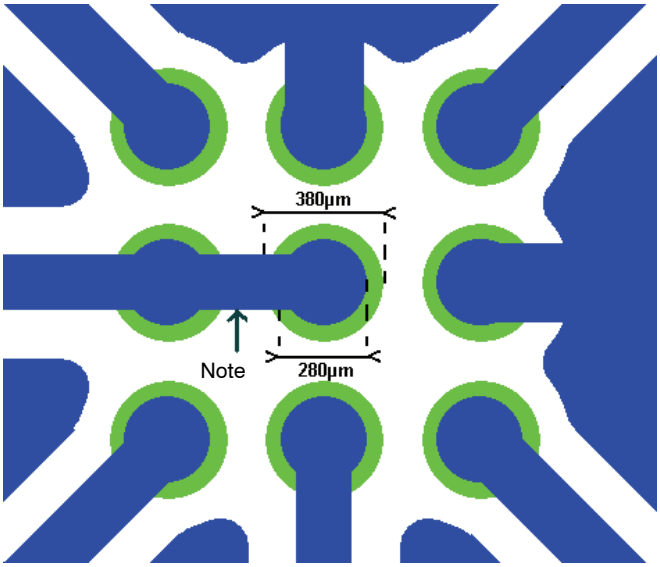


Figure 45. Top Layer

Note: This track between Vp pins is only needed when a 2 layers board is used. In case of a typical 4 or more layers, the use of laser vias in pad will optimize the THD+N floor.

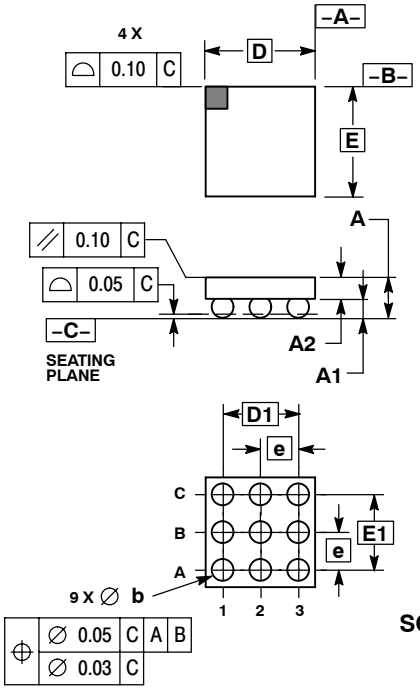
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP9004FCT1G	MAQ	9−Pin Flip−Chip CSP (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

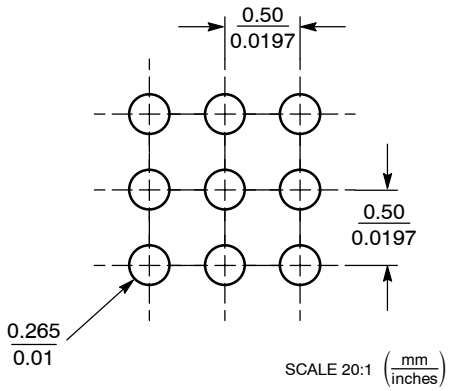
9−PIN FLIP−CHIP CSP
FC SUFFIX
CASE 499E
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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