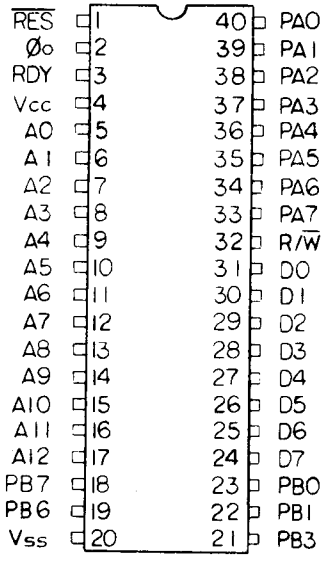
6518 SINGLE-CHIP MICROPROCESSOR WITH RAM AND I/O

PRELIMINARY

- 6507 CPU
  - 8-bit parallel processing
  - 13 addressing modes
  - Decimal and binary arithmetic modes
  - True indexing capability
  - 56 instructions
- 128 x 8 static RAM
- Two bidirectional TTL-compatible programmable I/O ports, one 8-bit, and one 5-bit
- Two programmable peripheral data direction registers
- 8-bit bidirectional data bus
- Programmable stack pointer
- Programmable interval timer with interrupt flag
- Variable length stack
- Addressable memory range of up to 8K bytes
- Bus compatible with M6800
- Pipeline architecture
- Use with any type or speed memory
- Up to 1.25 MHz clock frequency
- NMOS silicon gate, depletion load
- Single +5V power supply

The NCR 6518 is a low-cost microcomputer system capable of solving a broad range of small systems and peripheral control problems. It consists of a 6507 CPU; 128 bytes of RAM; two bidirectional I/O ports: one 8-bit and one 5-bit; and a programmable interval timer with interrupt flag. The internal processor architecture is software compatible with the 6502.

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The NCR 6518 has combined the functions of a 6507 microprocessor along with on-board RAM, I/O and timer logic. The functional block diagram shows the various elements of the device.

To understand the basic operation of the processor, we will briefly consider the register sections of the chip as follows:

- Input Data Latch
- Data Bus Buffers
- Accumulator
- Arithmetic Logic Unit
- Program Counter
- Index Registers X and Y
- Address Bus Latches
- Stack Pointer

At full operating frequency, data which comes into the microprocessor from program or data memory or from a peripheral device, appear on the data bus during one cycle and are transferred into the input data latch during the next cycle. After the data has been trapped on the data bus, it can then be transferred onto one of the internal busses and then into one of the internal registers.

As an example, data being moved from memory to the accumulator (A) will be put on the internal data bus and then transferred into the accumulator. If a logic operation or an arithmetic operation is to be performed using the contents of the accumulator and memory data, then the memory data in the input data latch will be transferred first onto the internal data bus and then into one input of the arithmetic logic unit (ALU). During the same instruction cycle, the contents of the accumulator will be transferred onto a bus and then into the second ALU input. The results of the operation will be transferred back to the accumulator via the bus on the next cycle.

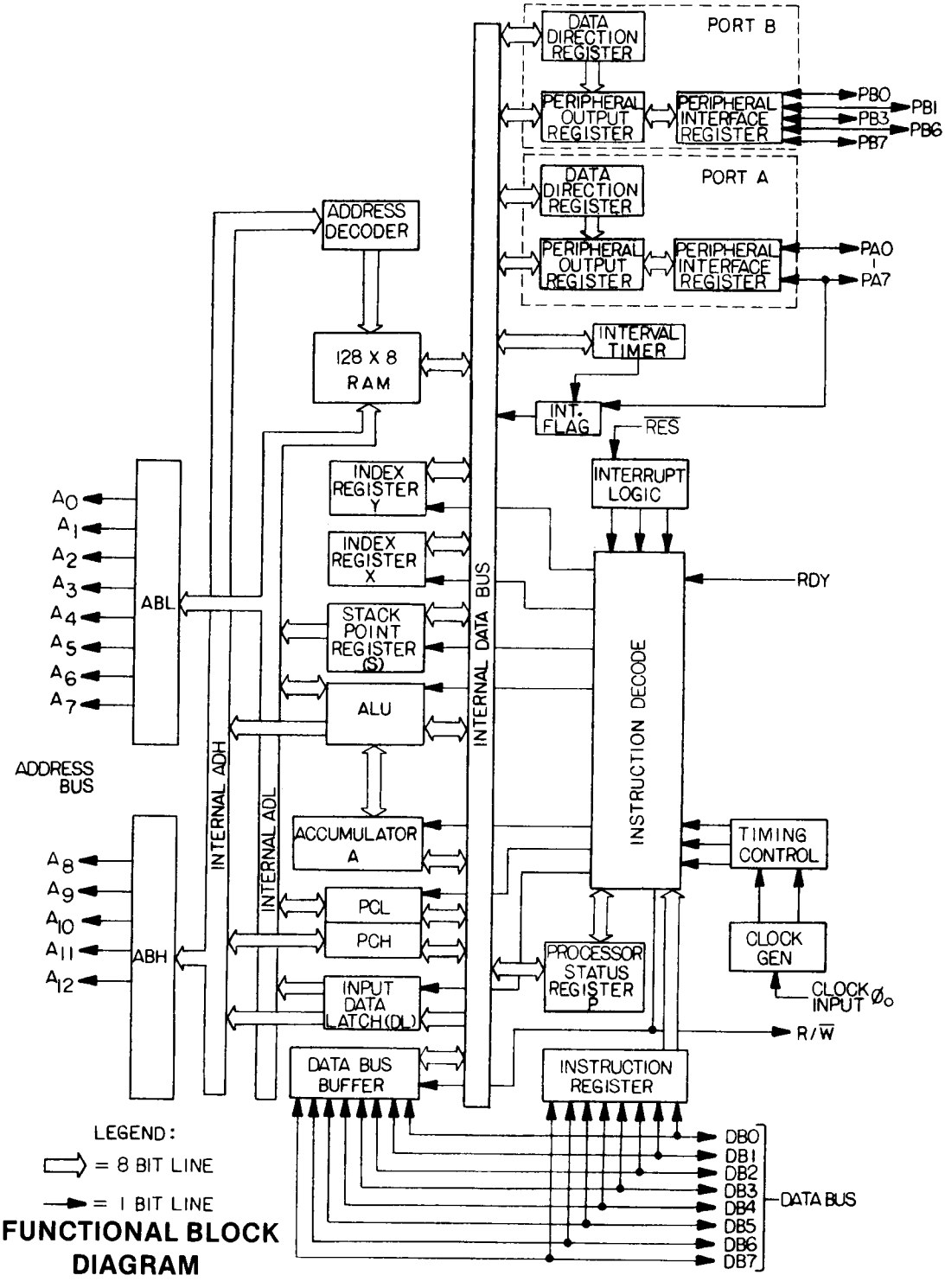
The microprocessor is sequenced through program instructions by the program counter (PCL,PCH) which provides the memory addresses. For each instruction fetch, the contents of PCL are placed on the low-order 8 bits of the address bus and the contents of PCH are placed onto the high order 8 bits. The program counter is automatically incremented with each instruction fetch.

The accumulator is a general purpose 8-bit register which is commonly used for storing the result of a logic or arithmetic operation. The accumulator is also often the source for one of the operands for these operations.

The arithmetic logic unit (ALU) is the site for all arithmetic and logic operations. By tying each of the ALU inputs to one of the several internal busses (or logic zero), various logic or arithmetic functions can be calculated. However, since the ALU cannot store data for more than one cycle, the result of each operation must be sent to one of the storage registers or external memory on the next cycle.

Three other device registers store data which are used for calculating addresses in memory. The X and Y index registers are each 8-bit latches whose values are used for various modes of data memory addressing. The stack pointer (S) is also an 8-bit latch which keeps track of the stack and allows for easy modification of program memory address.

The address bus latches (ABL,ABH) consist of 13 latches which can store the addresses used to access external ROM, RAM or I/O.



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

Pin	Description
$\overline{RES}$	The $\overline{RES}$ input is used to reset the microprocessor or initialize the device from a power-down condition. During the power up time, this line must be held low for at least two clock cycles after the power supply reaches minimum VCC. While that line is held low, writing to or from the processor is inhibited. When RES goes high, the microprocessor will delay 6 clock cycles and then load the program counter from memory vector locations FFFC and FFFD. This the starting location for the user's program.
ø0	TTL-Compatible single phase clock input.
RDY	The ready input delays execution of any cycle during which the RDY line is pulled low. The primary purpose of this line is to delay the execution of a program fetch cycle until data are available from memory. This allows the microprocessor to interface with both low and high speed memory.
VCC	Main power supply = 5V (+/− 5%)
A0-A12	TTL-Compatible address bus outputs, capable of driving one standard TTL load and 130 PF.
PB0-PB1 PB3 PB6-PB7	Peripheral data port B. I/O lines are each individually software programmable as either an input or output line. The pins are set as inputs by writing a "0" to the corresponding bit in the data direction register (DDRB). Writing a "1" to a bit in the DDRB will set the corresponding pin as an output. The outputs are capable of driving one standard TTL load and 130 PF. Note only 5 PB are available.
VSS	Signal Ground.
PA0-PA7	Peripheral data port A I/O lines. These pins function as do those in port B, but are controlled by a separate data direction register (DDRB). In addition to its function as an I/O line, PA7 can be used as an edge-detecting input.
R/$\overline{W}$	The read/$\overline{write}$ signal is generated by the microprocessor to control the direction of data transfers on the data bus. This line will be high except when the microprocessor is writing to memory, or to a peripheral device.
D0-D7	Bidirectional data bus. The outputs are tri-state buffers capable of driving one standard TTL load and 130 PF.

DEVICE OPERATION

CENTRAL PROCESSING UNIT (CPU)

The CPU is a 6507 configuration with standard 6502 instructions. It features an on-chip clock, 8-bit bidirectional data bus and 8K bytes of addressable memory.

RANDOM ACCESS MEMORY (RAM)

The 128 x 8 read/write memory acts as a conventional static RAM. Data can be written to memory by selecting the RAM (A7 = 1, A12 = 0) and setting A9 to a logic 0. Address lines A0 through A6 then select the desired byte in RAM.

INTERNAL PERIPHERAL REGISTERS

I/O port PA consists of eight lines each of which can be programmed to function as either an input or output. A logic zero in the corresponding bit of the data direction register (DDRA) sets up that line of the PA port as an input. Similarly, a logic one will configure that line as an output. If a line in PA is programmed as an output, the logic level of that output is determined by the corresponding bit in the output register (ORA).

Data is read directly from PA pins during any read operation. For any output pin, data transferred into the microprocessor will be the same as that contained in the output register if the voltage on the pin is allowed to go to a logic one. For input lines, the processor can write into the corresponding bit of the output register. This will not affect the polarity of the pin until the corresponding bit of the DDRA is set to a logic one, changing the pin to an output.

Along with its function as an I/O line, PA7 also can be used as an edge-detecting input. In this mode, an active transition on this pin will set the internal interrupt flag (Bit 6 of the Interrupt Flag Register). The edge-detecting mode of PA7 is controlled by writing to one of two addresses. The polarity of the transition is determined by the state of A0. Any data which is placed on the data bus during this operation is discarded and does not affect control of A7.

An active transition on PA7 will set the internal interrupt flag. Even if pin PA7 is being used as a normal I/O line. The reset signal (RES) will set the polarity of the active transition to negative (high to low). During system initialization, it is possible to set the interrupt flag by a negative transition. Clearing of the PA7 interrupt flag occurs when the interrupt flag register is read.

The second I/O port - PB, functions the same as the normal I/O operation of PA. The five lines (PB0, PB1, PB3, PB6, PB7) are controlled via the DDRB and ORB in similiar fashion to the control of PA.

INTERVAL TIMER

The interval timer can be programmed to count as many as 255 time intervals. Using the divide down, each interval can be T, 8T, 64T, or 1024T where T is the system clock period. When a full count down is complete, the interrupt flag is set and internal clock begins decrementing to a maximum of 255T. Therefore, after the interrupt flag is set, a read of the timer will tell how long it has been since the flag was set (up to a maximum of 255T).

The system data bus is used to transfer data to and from the interval timer. At the same time data is written to the timer, the preliminary divide down value (1, 8, 64, 1024) is decoded from the address lines A0 and A1. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read.

When the timer has counted down through 00 (00000000), an interrupt will occur on the next count and

the counter will read FF (11111111). After the interrupt, the counter will decrement at a divide by "1" rate of the system clock. If the timer is read after an interrupt and, for example, the value E4 (11100100) is obtained, the time elapsed since the interrupt is 27T.

The value read is in two's complement, but remembering that the interrupt occurred at FF (11111111), we simply take this difference.

Value at Interrupt	11111111
- Value Read	11100100
Elapsed Time	00011011 = 27

After the interrupt, when the timer is written to or read from, the interrupt flag is reset. However, reading the timer at the same time the interrupt occurs, will not reset the interrupt flag.

ADDRESS BUS DECODE FOR NCR 6518

FUNCTION	A9	A6	A5	A4	A3	A2	A1	A0	R/W	COMMENT
RAM ADDRESSING	0 (RAM ADDRESS SELECT) —									
I/O Addressing Read	1	—	—	—	—	0	0	0	1	PA Data
	1	—	—	—	—	0	0	1	1	PA Data Direction
	1	—	—	—	—	0	1	0	1	PB Data
	1	—	—	—	—	0	1	1	1	PB Data Direction
I/O Addressing Write	1	—	—	—	—	0	0	0	0	PA Data
	1	—	—	—	—	0	0	1	0	PA Data Direction
	1	—	—	—	—	0	1	0	0	PB Data
	1	—	—	—	—	0	1	1	0	PB Data Direction
Write Edge Detect Control	1	—	—	0	—	1	—	1	0	Positive Edge (PA7)
	1	—	—	0	—	1	—	0	0	Negative Edge (PA7)
Read and Clear Interrupt Flag	1	—	—	—	—	1	—	1	1	Bit 7 = Timer Flag Bit 6 = PA7 Flag
Read Interval Timer	1	—	—	—	—	1	—	0	1	
Write Count to Interval Timer	1	—	—	1	—	1	0	0	0	Divide by 1
	1	—	—	1	—	1	0	1	0	Divide by 8
	1	—	—	1	—	1	1	0	0	Divide by 64
	1	—	—	1	—	1	1	1	0	Divide by 1024

NOTE: FOR ALL OPERATIONS, A7 = 1, A12 = 0
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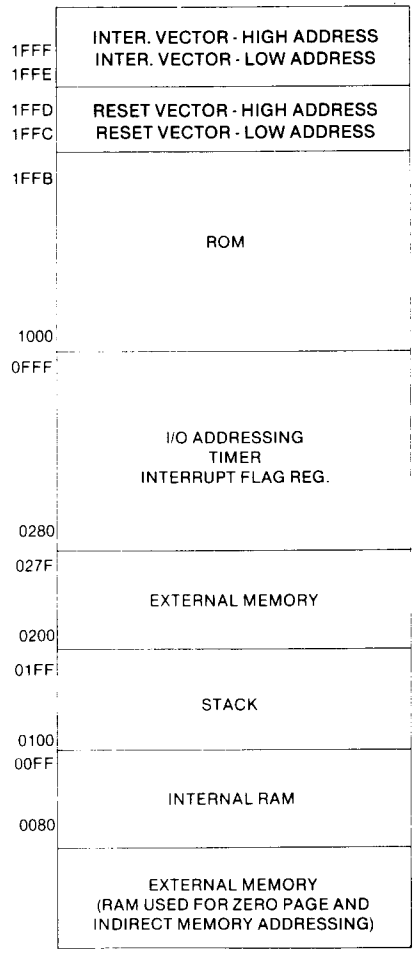
NCR 6518 MEMORY MAP



MAXIMUM RATINGS

PRELIMINARY

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input/Out Voltage	V_{IN}	−0.3 to 7.0	V
Operating Temperature Range	T_{op}	0 to 70	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside th specification range.

ELECTRICAL CHARACTERISTICS

D.C. Characteristics

T_A = 25°C, V_{CC} = 5.0V ± 5%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Test Conditions
	Capacitance at				
$C_{0\phi}$	Clock Input ϕ_o		15	pF	V_{in} = 0V f = 1.25 MHz
C_{OUT}	Address A0-A12, R/W		12	pF	
C_{IN}	Data Bus D0-D7		15	pF	
I_{IH}	Input High Current at Peripheral Data Ports				V_{in} = 2.4V
	PA0-PA7, PB (0,1,3,6,7)	—100		uA	
I_{IL}	Input Low Current at Peripheral Data Ports				V_{in} = 0.4V
	PA0-PA7, PB (0,1,3,6,7)		—1.6	mA	
I_{OL}	Output Low Current at Peripheral Data Ports				V_{OL} < 0.4V
	PA0-PA7, PB (0,1,3,6,7)	1.6		mA	
I_{OH}	Output High Current at Peripheral Data Ports				
	PA0-PA7, PB (0,1,3,6,7)	—100		uA	V_{OH} > 2.4V
	PB (0,1,3,6,7)	—3.0		mA	V_{OH} > 1.5V
C_{INP}	Input Capacitance at PA0-PA7, PB (0,1,3,6,7)		10	pF	
C_{OUTP}	Output Capacitance at PA0-PA7, PB (0,1,3,6,7)		10	pF	
V_{IH}	Input High Voltage	V_{SS} + 2.2	V_{CC} + 0.2.5	V	
V_{IL}	Input Low Voltage	V_{SS} —0.3	V_{SS} + 0.8	V	
I_{IN}	Input Leakage Current		2.5	uA	V_{in} = 0 to 5.25V
	for ϕ_o		10	uA	VCC = 0V

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Symbol	Parameter	Min.	Max	Units	Test Conditions
I_{TSI}	3-State Input Current		10	uA	V_{in} = 0.4 to 2.4V V_{CC} = 5.25V
V_{OH}	Output High Voltage D0-D7 A0-A12 R/W	V_{SS} + 2.4		V	I_{LOAD} = —100 uADC VCC = 4.75V
	PA0-PA7, PB (0,1,3,6,7)	V_{SS} + 2.4		V	I_{LOAD} = -100 uA
	PB (0,1,3,6,7)	V_{SS} + 1.5		V	I_{LOAD} = —3 mA
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V	I_{LOAD} = 1.6 mA VCC = 4.75V
I_{CC}	Maximum V_{CC} Current		70	mA	T_A = 25 °C
V_{ILC}	ϕ_0 Input Low Voltage	0	0.4	V	
V_{IHC}	ϕ_0 Input High Voltage	2.4	V_{CC} + 0.25	V	
$V_{IH}(\overline{RES})$	Reset Input High Voltage	V_{SS} + 2.19	V_{CC} + 0.25	V	For increasing V_{IN}
		V_{SS} + 1.20	V_{CC} + 0.25	V	For decreasing V_{IN}
$V_{IL}(\overline{RES})$	Reset Input Low Voltage	V_{SS} —0.3	V_{SS} + 1.87	V	For increasing V_{IN}
		V_{SS} —0.3	V_{SS} + 0.67	V	For decreasing V_{IN}

A.C. CHARACTERISTICS

T_A = 25°C, V_{CC} = 5.0V ± 5%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Test Conditions
T_{CYC}	Cycle Time	0.8	100	μs	
$TR\phi_o$, $TF\phi_o$	ϕ_o Rise, Fall Time		10	ns	
$PWH\phi_o$	ϕ_o Pulse Width	375	62000	ns	
T_{RWS}	R/$\overline{W}$ Setup Time		280	ns	Loading = 130pF + 1 TTL Load for D0-D7, A0-A12, R/$\overline{W}$
T_{ADS}	Address Setup Time		280	ns	
T_{ACC}	Memory Read Access Time		410	ns	
T_{ACP}	Data Read Access Time for from Internal Logic		375	ns	
T_{DSU}	Data Stability Time Period	110		ns	
T_{HR}	Data Hold Time-Read	50		ns	
T_{HW}	Data Hold Time-Write	50		ns	
T_{MDS}	Data Setup Time		240	ns	
T_{RDY}	Ready Setup Time	130		ns	
T_{HA}	Address Hold Time	50		ns	
T_{HRW}	R/$\overline{W}$ Hold Time	50		ns	
T_{CMOS}	Peripheral Data Valid (writing into CMOS load)		1.6	μs	
T_{CPW}	Peripheral Data Valid after Falling Edge of ϕ_o (Writing)		0.8	μs	Loading = 30pF + 1 TTL Load for PA0-PA7, PB (0,1,3,6,7)
T_{PCR}	Peripheral Data Valid after before Rising Edge of ϕ_o (Reading)	240		ns	
T_{IC}	External interrupt setup time	200		ns	

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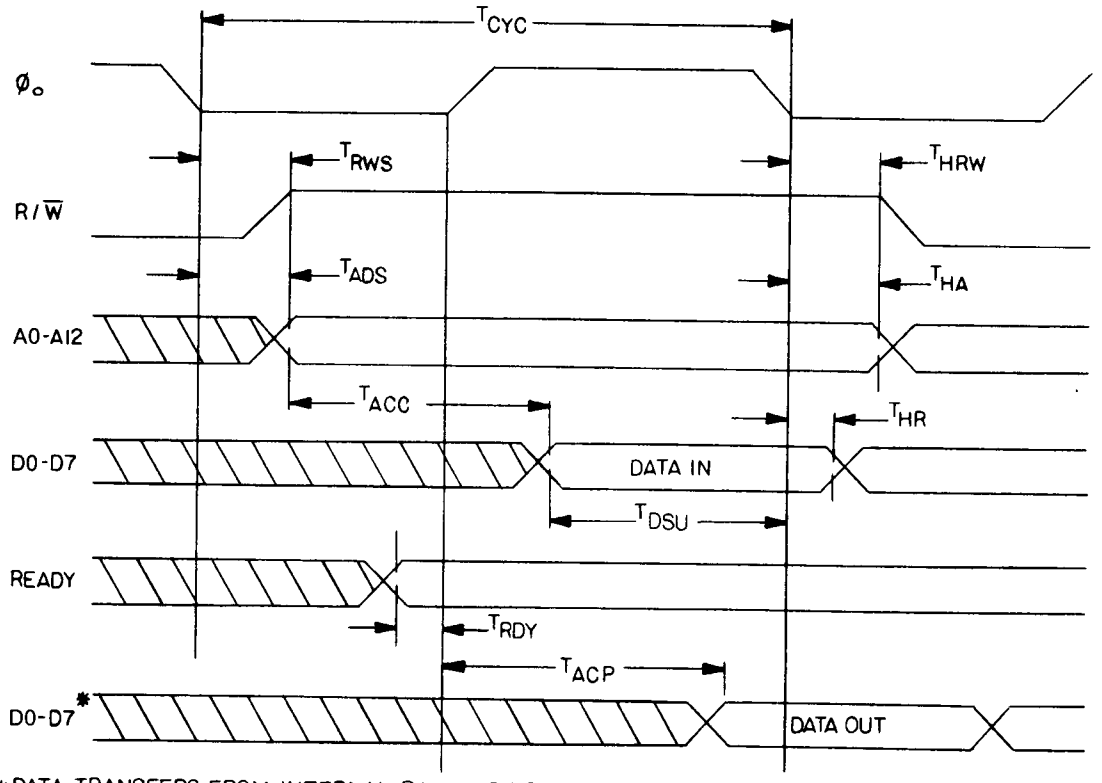
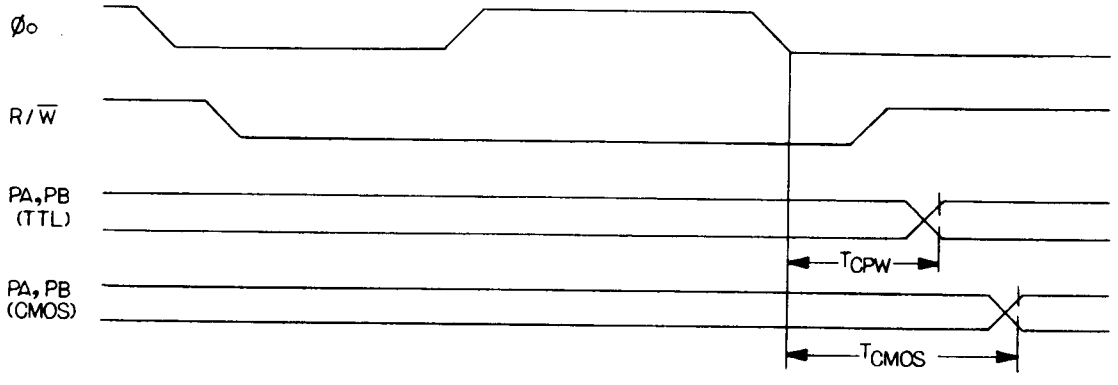
TIMING DIAGRAMS
Read Cycle Timing

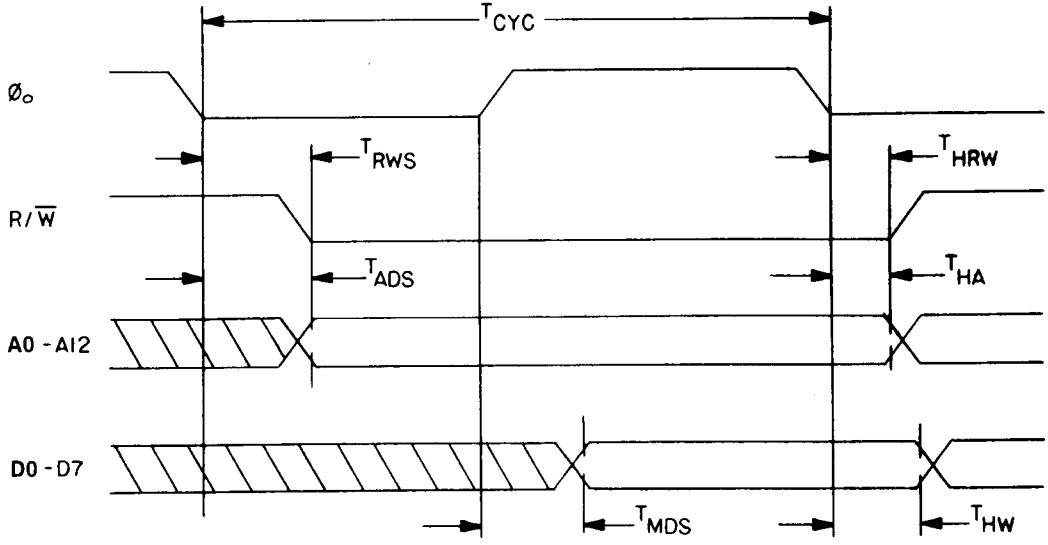


*DATA TRANSFERS FROM INTERNAL RAM, I/O LOGIC, TIMER OR INTERRUPT FLAG REGISTER ONLY.

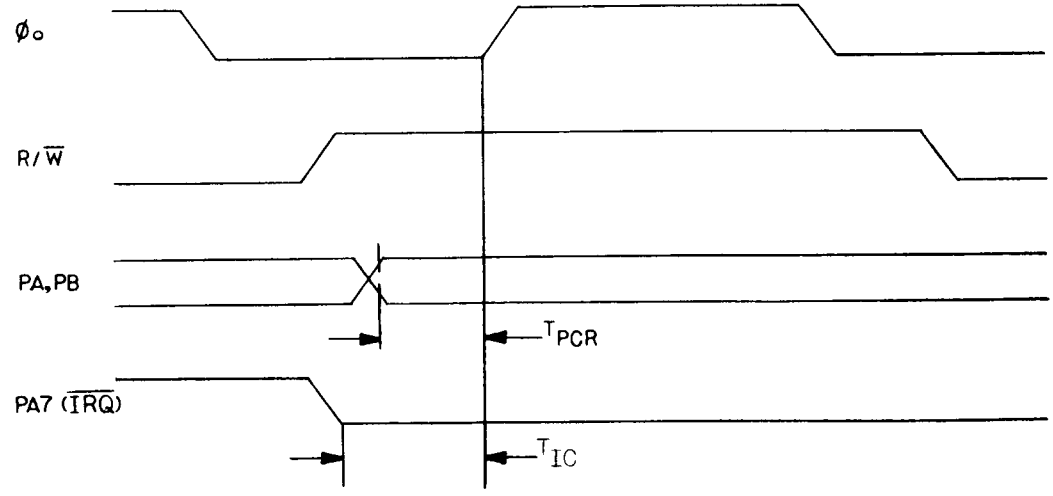
PA, PB Write Timing



Write Cycle Timing



PA, PB Read Timing



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