# Nuvoton
# DDR Termination Regulator
# NCT3107S

**DATE: NOVEMBER, 2011**

**Revision: A2**

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## 1. GENERATION DESCRIPTION

The NCT3107S is a sink/source linear regulator for DDR-SDRAM VTT bus termination. The device contains a high speed operational amplifier to provide excellent response to load transients and only requires a minimum output capacitance of 10uF. The NCT3107S also incorporates a remote sensing function (VSEN pin) to provide superior load regulation and a VREF output as a reference for the chipset and DIMMS. An additional feature found on the NCT3107S is an active low shutdown (SD# pin) that provides Suspend to RAM (STR) functionality. When SD# is pilled low, the VTT output voltage will be discharged to ground but VREF remains active. A power savings advantage can be obtained in this mode through lower quiescent current. NCT3107S is available in ESOP-8 package. It is specified from -40°C to 85°C.

## 2. FEATURES

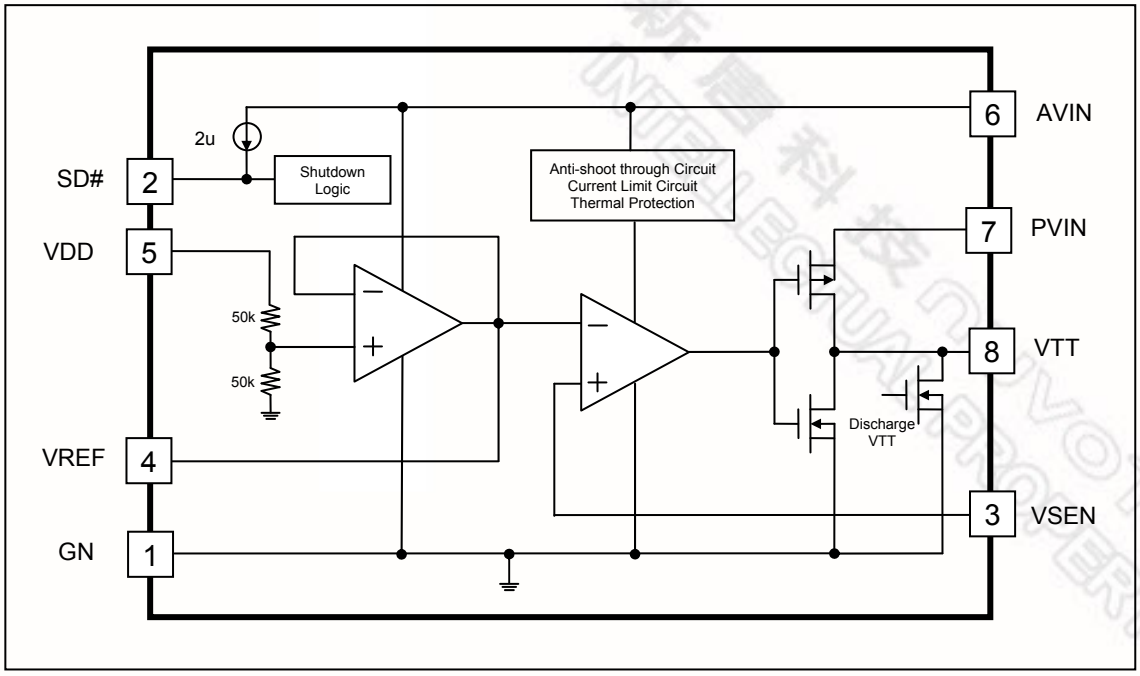
### General

- Sink and Source Current
- Low Output Voltage Offset
- No External Resistors Required
- Linear Topology
- Suspend to RAM (STR) Functionality
- Low External Component Count
- Required Minimum Output Capacitance of 10uF for Memory Termination Applications (DDR)
- Built-in Over Current Protection
- Thermal Shutdown
- Remote Sensing (VSEN)
- ±10mA Buffered Reference Output (VREF)
- Meets DDR2 Specifications; Support DDR3 VTT Applications
- ESOP-8 150mil with Exposed Pad Package
- Green Package (Lead Free and Halogen Free)

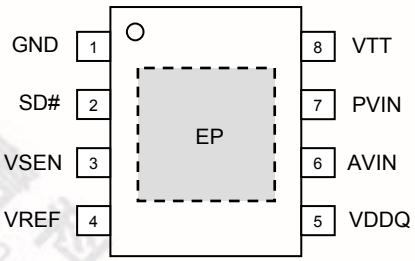
### Applications

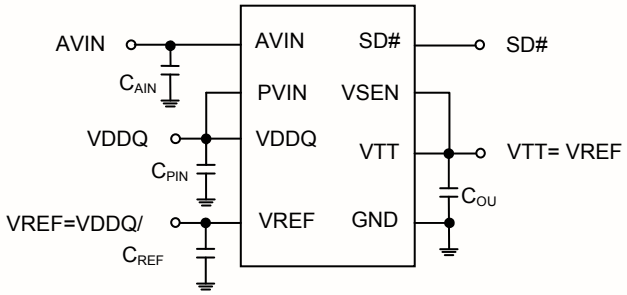
- Memory Termination Regulator for DDR2 and DDR3
- Motherboards
- LCD TV/PDP TV, Copier/Printer, Set Top Box

## 3. BLOCK DIAGRAM




## 4. PIN CONFIGURATION AND TYPICAL APPLICATION CIRCUIT




$C_{AIN}$=0.1uF, $C_{PIN}$=10uF, $C_{REF}$ = Reserved

$C_{OUT}$=10uF+100uF for worse case test condition

## 5. PIN DESCRIPTION

| PIN NAME | NO | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| GND | 1 | Ground | Ground |
| SD# | 2 | I | Shutdown VTT output voltage. |
| VSEN | 3 | AI | Feedback pin for regulating VTT. |
| VREF | 4 | AO | Buffered internal reference voltage of ½VDDQ. |
| VDDQ | 5 | AI | Input for internal reference equal to ½VDDQ. |
| AVIN | 6 | Power | Analog input pin for power source. |
| PVIN | 7 | AI | Analog input pin for internal power MOSFET source. |
| VTT | 8 | AO | Output voltage for connection to termination resistors. |
| EP | | | Exposed pad thermal connection. Connect to ground. |

| PIN TYPE | PIN Attribute |
|---|---|
| **AO** | Output pin (Analog) |
| **AI** | Input pin (Analog) |
| **I** | Input pin (Digital) |
| **POWER** | Positive power supply input |
| **GROUND** | Power supply ground |

## 6. FUNCTIONAL DESCRIPTION

### General Description

The NCT3107S is a sink/source linear regulator for DDR-SDRAM VTT bus termination. The device contains a high speed operational amplifier to provide excellent response to load transients and only requires a minimum output capacitance of 10uF. The NCT3107S also incorporates a remote sensing function (VSEN pin) to provide superior load regulation and a VREF output as a reference for the chipset and DIMMS. An additional feature found on the NCT3107S is an active low shutdown (SD# pin) that provides Suspend to RAM (STR) functionality. When SD# is pilled low, the VTT output voltage will be discharged to ground but, VREF remains active. A power savings advantage can be obtained in this mode through lower quiescent current.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The DDR-SDRAM memory termination structure determines the main characteristics of the VT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. Fig. 6-1 shows typical characteristics for a single memory cell.

When Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT
- VTT sinks current

When Q1 is off and Q2 is on:

- Current flows from VTT via the termination resistor to GND
- VTT sources current

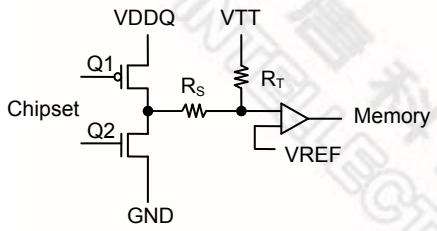



Fig. 6-1 DDR Physical Signal System Bi-Directional SSTL Signaling

**AVIN and PVIN**

AVIN and PVIN are the input supply voltage pins for NCT3107S. AVIN is used to supply the internal control circuitry and PVIN is used to provide the rail voltage for the output staged used to create VTT. AVIN has to be greater than or equal to PVIN in any applications. This prevents the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown threshold, the part will enter a shutdown state identical to the manual shutdown where VTT is tri-stated and VREF remains active. A lower rail can be used but it will reduce the maximum output current.

**VDDQ**

VDDQ is the input used to create the internal reference voltage for regulating VTT. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This guarantees that VTT will precisely track VREF. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the power rail at the DIMM instead of PVIN. This ensures that the reference voltage precisely tracks the DDR memory rails without a large voltage drop from the power lines.

**VREF**

VREF provides the buffered output of the internal reference voltage ½VDDQ. This output should be used to provide the reference voltage for chipset and memory. Typically, there is no necessary to place output capacitor. But for worse condition, an output bypass capacitor could be reserved, close to the pin, to secure a suitable phase margin. Insufficient capacitance may cause an oscillation. A ceramic capacitor in the range 0.01uF to 0.1uF is recommended. The output remains active during the shutdown state and thermal shutdown events for the Suspend to RAM functionality.

**VTT**

VTT is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VREF. If a transient is expected to last above the maximum continuous current rating for a significant amount of time, then the bulk output capacitor should be sized large enough to prevent an excessive voltage drop. If the NCT3107S is to operate in elevated temperatures for long durations, care should be taken to ensure the maximum operating junction temperature is not exceeded. Proper thermal de-rating

should always be used. If the junction temperature exceeds the thermal shutdown threshold, VTT will tri-state until the part returns below the temperature hysteresis trip-point.

**VSEN**

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications, the termination resistors will connect to VTT in a long plane. If the output voltage was regulated only at the output of the NCT3107S, then the long trace will cause a significant DC voltage drop resulting in a termination voltage lower at one end of the bus than the other. The VSEN pin can be used to improve this performance by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used, then the VSEN pin must be connected to VTT. Care should be taken when a long VSEN trace is implemented in close proximity to the memory. Noise pick up in the VSEN trace can cause problems with precise regulation of VTT. A small 0.1uF ceramic capacitor placed next to the VSEN pin can help filter any high frequency signals and prevent errors.

**Shutdown**

The NCT3107S contains an active low shutdown pin that can be used for Suspend to RAM functionality. In the condition, the VTT output voltage will be discharged to ground while the VREF output remains active and provides a constant reference signal for the memory and chipset. During shutdown, VTT should not be exposed to voltages that exceed PVIN. With the shutdown pin asserted low, the quiescent current of the NCT3107S will drop. However, VDDQ always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore, to calculate the total power loss in shutdown, both currents need to be considered. The shutdown pin also has an internal pull up current. Therefore, to turn the part on, the shutdown pin can either be connected to AVIN or left open.

**Current Limit Protection**

The NCT3107S provides a current limit circuitry for short circuit protection, which monitors the output current and controls internal power MOSFET gate voltage to limit the output current. This reduction is a non latch protection.

**Thermal Shutdown**

The NCT3107S has a thermal shutdown circuitry to limit the junction temperature. When the junction temperature exceeds 150°C, the thermal shutdown circuitry let the output into tri-state, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 30°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal protection is designed to protect the IC in the event of over temperature conditions. For reliabile operation, the junction temperature cannot exceed 125°C.

**Input Decoupling**

To achieve the best results when using the NCT3107S, decouple the power supply for AVIN with a 0.1uF to 4.7uF capacitor. For PVIN pin, use a 10uF (or greater) capacitor to improve performance during large load transients to prevent the input rail from dropping. Provide more input capacitance as more output capacitance is used at VTT. In general, use one-half of the COUT value for input. Use a high quality ceramic surface mount capacitor if possible. Surface mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high frequency response for decoupling applications.

### Output Stability

To maintain circuit stability and improve transient response over temperature and current, the NCT3107S needs a suitable output capacitor. In order to insure the circuit stability, the suitable output capacitor should be larger than 10uF. For worse case test condition (from maximum sinking current to maximum sourcing current), the capacitance has to be large than 100uF. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of VTT. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop.

### Thermal Design

Because the NCT3107S is a linear regulator, the VTT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between PVIN and VTT times IOUT current becomes the power dissipation as shown in below equation.

$$P_{DISS\_SRC} = (PVIN - VTT) \times IOUT_{SRC}$$

In this case, if PVIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation, $P_{DISS\_SNK}$ can be calculated by below equation.

$$P_{DISS\_SNK} = VTT \times IOUT_{SNK}$$

Since the device does not sink and source at the same time and IOUT varies rapidly with time, actual power dissipation need to be considered for thermal design is an average of above value over thermal relaxation duration of the system. Another source of power consumption is the current used for internal control circuitry from AVIN supply and PVIN supply. This can be estimated as 5mW or less during normal operating conditions. This power must be effectively dissipated from the package.

Maximum power dissipation allowed by the package is calculated by below equation.

$$P_{PKG} = [T_{J\ (MAX)} - T_{A\ (MAX)}] / \theta_{JA}$$

where

- $T_{J\ (MAX)}$ is +125°C
- $T_{A\ (MAX)}$ Is the maximum ambient temperature in the system
- $\theta_{JA}$ Is the thermal resistance from junction to ambient

$\theta_{JA}$ highly depends on IC package, PCB layout, the aireflow. Thermal resistance $\theta_{JA}$ can be improved by adding copper under the exposed pad of ESOP-8 while the IC package is fixed. The copper under the exposed pad of ESOP-8 is an effective heatsink and is useful for improving thermal conductivity. Figure show the relationship between thermal resistance $\theta_{JA}$ vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at TA = 25°C, PCB copper thickness = 2oz. The 70mm$^2$ copper plane reduce $\theta_{JA}$ from 75°C/W to 45°C/W and increases maximum power disspation from 1.33W to 2.22W.

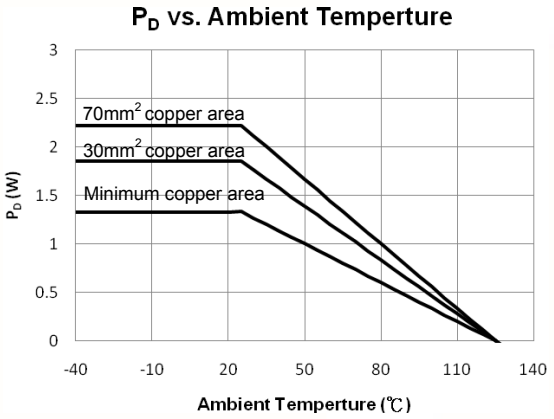



Fig. 6-2 Power Dissipation vs. Ambient Temperature

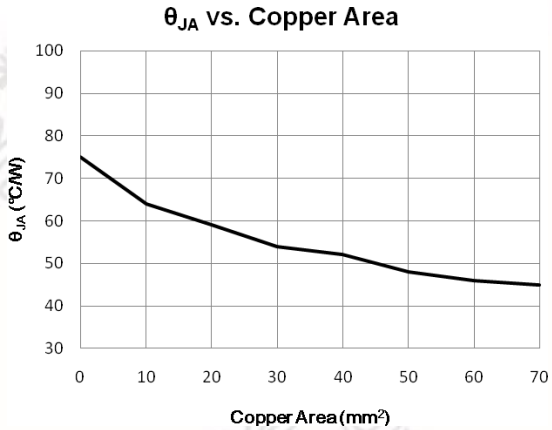



Fig. 6-3 Thermal Resistance $\theta_{JA}$ vs. Copper Area of ESOP Packages

## Layout Consideration

Consider the following points before starting the NCT3107S layout design.

- The input bypass capacitors for AVIN, PVIN and VSEN should be placed as close as possible to the pin with short and wide connections.
- The output capacitors for VTT and VREF should be placed close to the pin with short and wide connection in order to avoid ESR and/or ESL trace inductance.
- VSEN should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line. The configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimized any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor(s).
- VDDQ can be connected separately from PVIN. Remember that this sensing potential is the reference voltage of VREF. Avoid any noise generative lines.
- The negative nose of the VTT output capacitor(s) and the VREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current. Also, place bulk caps close to the DIMM load point, route the VSEN to the DIMM load sense point.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. The wide traces of component and the side copper connected to the thermal land pad help to dissipate heat. The thermal land connected to the ground plane could also be used to help dissipation. Numerous vias connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation.

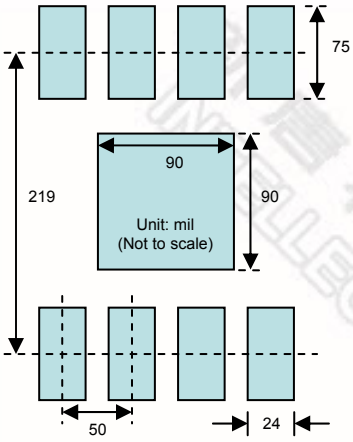



Fig. 6-4 Recommended Land Pattern

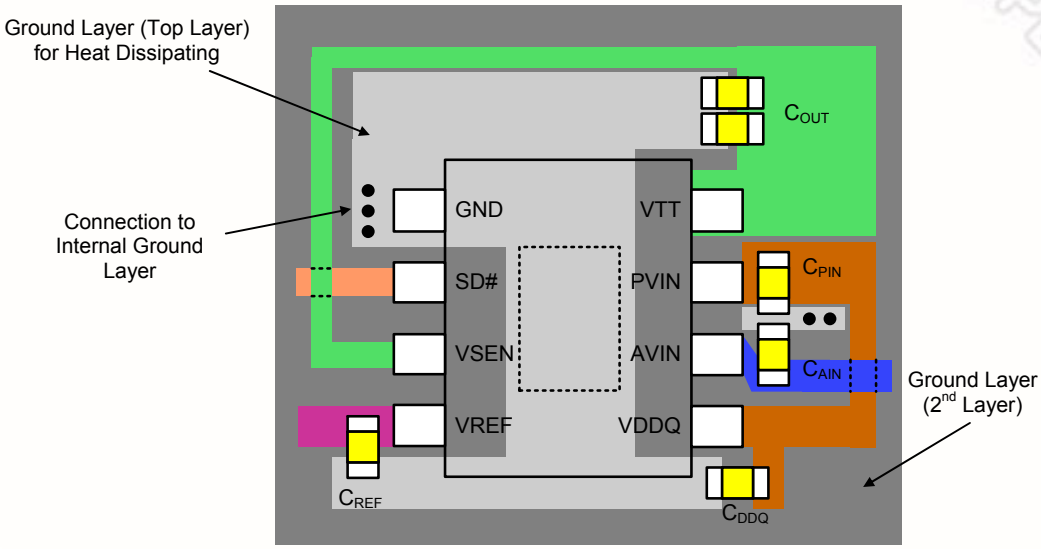



Fig. 6-5 PCB Layout Guideline

# 7. ELECTRICAL CHARACTERISTIC

## Absolute Maximum Ratings

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| Power Pins AVIN, PVIN, VDDQ | | -0.3 to 6V | V |
| Voltage on Other Pins | | -0.3 to 6V | V |
| Junction Temperature | | 150 | °C |
| Storage Temperature | | -50 to 150 | °C |
| Soldering Temperature | | Refer to IPC/JEDEC J-STD-020 Specification | |
| ESD Protection | Human Body Mode | 2 | kV |
| | Machine Mode | 200 | V |
| | Latch-up | 100 | mA |

Note1. No pin should exceed AVIN.

Note2. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note3. Devices are ESD sensitive. Handling precaution recommended.

## Thermal Information

| ITEM | RATING | UNIT |
|---|---|---|
| Power Dissipation, $P_D$ @ $T_A$=25℃ | 1.33 | W |
| Package Thermal Resistance, ESOP8, $\theta_{JA}$ | 75 | ℃/W |

Note1. At elevated temperatures, devices must be de-rated based on thermal resistance. The device in the ESOP-8 package must be de-rated at $\theta_{JA}$=75˚C/W junction to ambient with minimum PCB footprint.

## Recommended Operating Conditions

| PARAMETER | RATING | UNIT |
|---|---|---|
| Operating Temperature | -40 to 85 | °C |
| Junction Temperature | -40 to 125 | °C |
| Supply Voltage, AVIN | 2.2 to 5.5 | V |
| Capacitance of AVIN Decoupling Capacitor | 0.1 to 4.7 | uF |
| Capacitance of PVIN Decoupling Capacitor | 10 to 270 | uF |
| Capacitance of VDDQ Decoupling Capacitor | 0.1 to 270 | uF |
| Capacitance of VREF Regulation Capacitor | 0.01 to 0.1 | uF |
| Capacitance of VTT Regulation Capacitor | 10 to 470 | uF |

## Electrical Characteristics

AVIN=2.5V, PVIN=VDDQ=1.8V, COUT=10uF and all outputs are unload (unless otherwise noted). Typical value are at Ta=25°C and limits apply over the full operating temperature, Ta= -40~85°C.

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **Reference Voltage** | | | | | | |
| VREF | | 0.49×VDDQ | 0.5×VDDQ | 0.51×VDDQ | V | $I_{REF}$=0mA |
| Source Current | $I_{REF+}$ | 10 | | | mA | |
| Sink Current | $I_{REF-}$ | | | -10 | mA | |
| VREF Voltage Tolerance | | -15 | | +15 | mV | $I_{REF}$=±10mA |
| VDDQ Input Impedance | $Z_{VDDQ}$ | | 100 | | kΩ | |
| **Input / Output Current** | | | | | | |
| Quiescent Current(1) | $I_Q$ | | 320 | 500 | uA | $I_{OUT}$=0A |
| Shutdown Quiescent Current(1) | $I_{SD}$ | | 115 | 150 | uA | SD#=0V |
| Shutdown Leakage Current | $I_{Q\_SD}$ | | 2 | 5 | uA | SD#=0V |
| VSEN Input Current | $I_{VSEN}$ | -1 | | 1 | uA | |
| VTT Discharge Current in Shutdown | $I_{VTT\_Dis}$ | | 20 | | mA | SD#=0V, VTT=0.4V |
| **Output Voltage Offset (VREF-VTT)** | | | | | | |
| DDR2, PVIN=VDDQ=1.8V | $V_{OS}$ | -20 | | 20 | mV | $I_{OUT}$=0A |
| DDR3, PVIN=VDDQ=1.5V | | -20 | | 20 | mV | $I_{OUT}$=0A |
| DDR2, PVIN=VDDQ=1.8V | | -30 | | 30 | mV | $I_{OUT}$ =±1.5A(2) |
| DDR3, PVIN=VDDQ=1.5V | | -30 | | 30 | mV | $I_{OUT}$ =±1.2A(2) |
| **Logic Input Level** | | | | | | |
| Minimum Shutdown High Level | $V_{IH}$ | 1.9 | | | V | AVIN=2.2V~5.5V |
| Maximum Shutdwon Low Level | $V_{IL}$ | | | 0.8 | V | |
| **Current Limit Protection** | | | | | | |
| Output Current Limit | $I_{LIM}$ | 2.5 | | | A | PVIN=VDDQ=1.8V |
| | | 1.5 | | | A | PVIN=VDDQ=1.5V |
| **Over Temperature Protection** | | | | | | |
| Thermal Shutdown Temperature(3) | | 145 | 150 | 160 | °C | |
| Thermal Shutdown Hysteresis | | 20 | 30 | 40 | °C | |

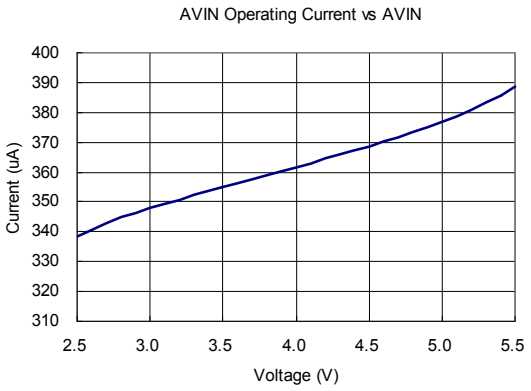
Note1. Quiescent is defined as the current flow into AVIN.

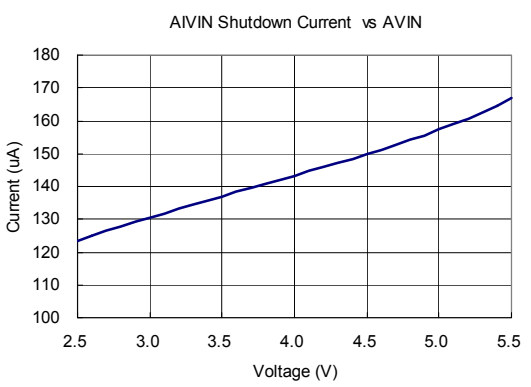
Note2. VTT load regulation is tested by using a 10ms current pulse and measuring VTT.

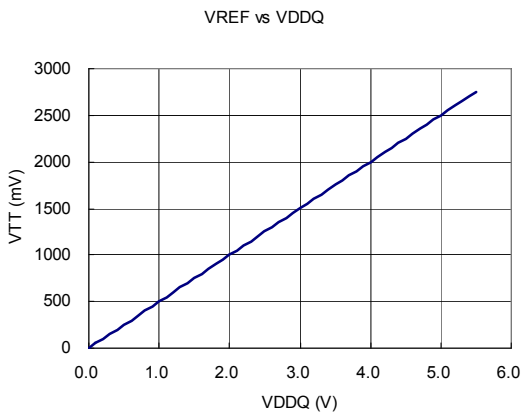
Note3. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J\ (MAX)}$, the junction to ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$ exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown. Ensured by design, no production tested.

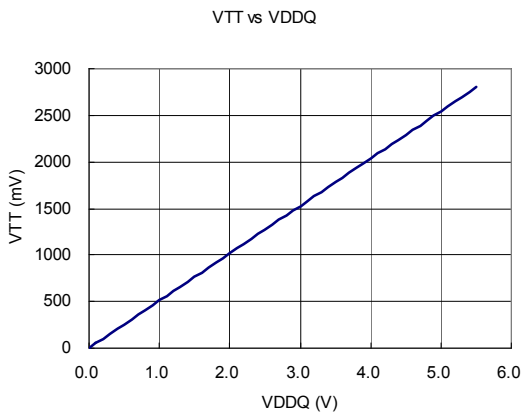
Note4. Limits are 100% production tested at 25˚C. Limits over operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate average outgoing quality level.

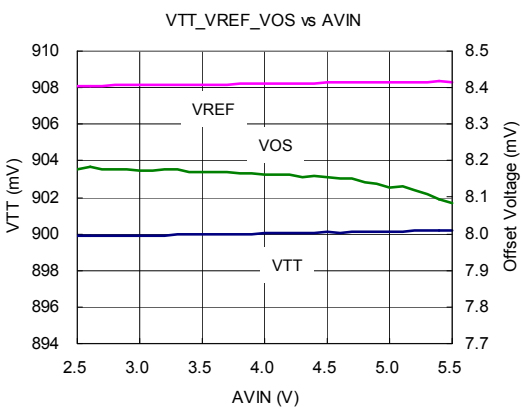
## 8. TYPICAL OPERATING CHARACTERISTICS AND WAFEFORMS

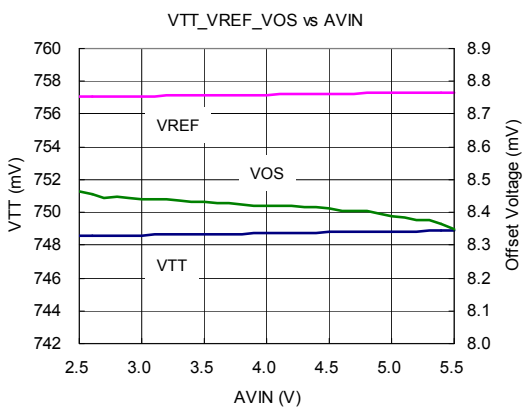


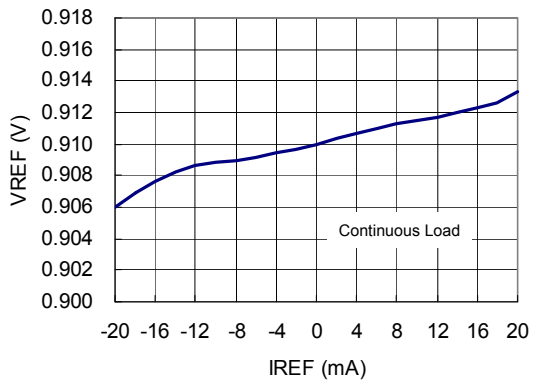



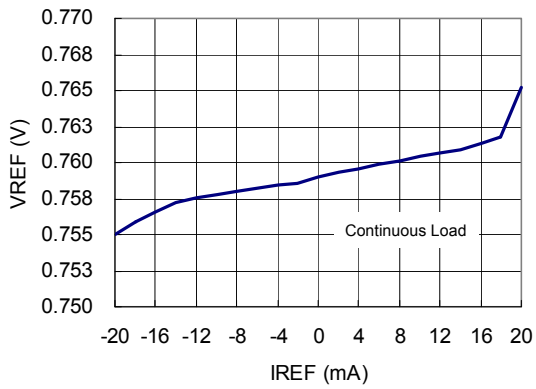



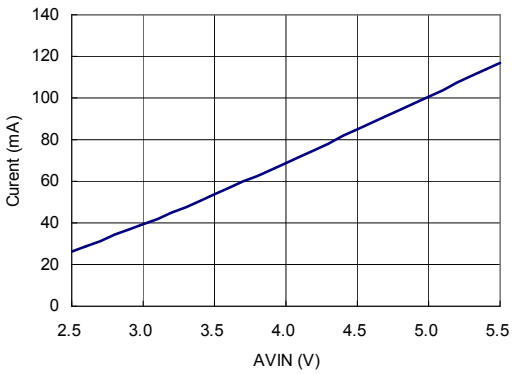
VREF vs IREF



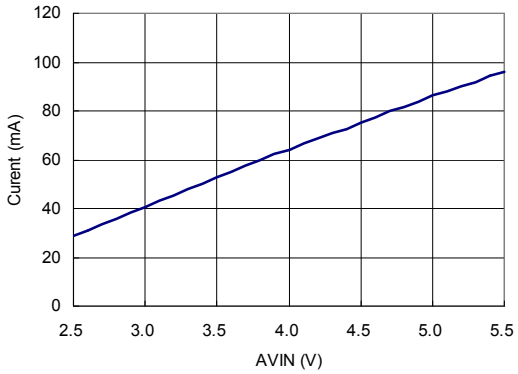

VREF vs IREF



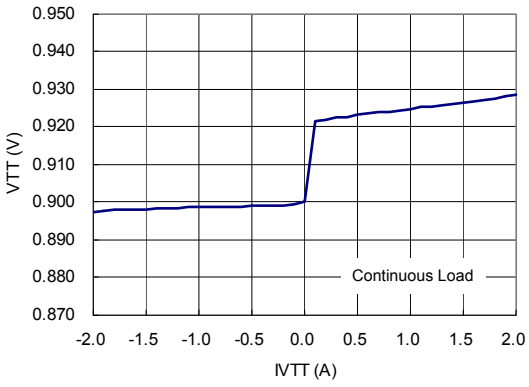

VREF Sourcing Current Limit vs AVIN



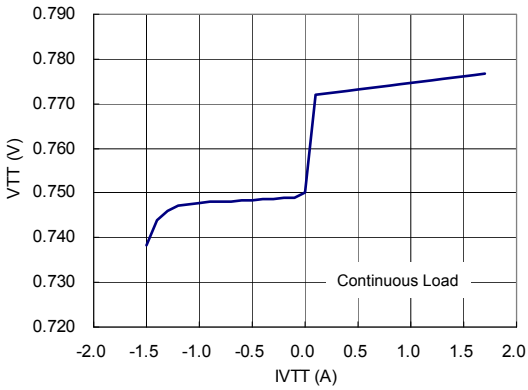

VREF Sinking Current Limit vs AVIN

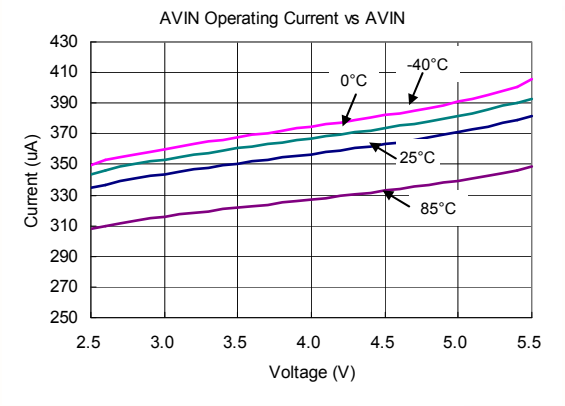


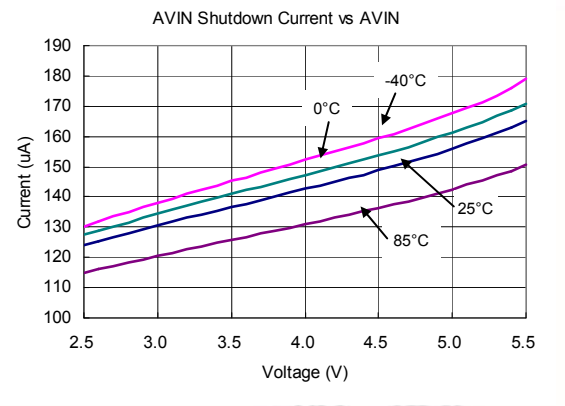

VTT vs IVTT

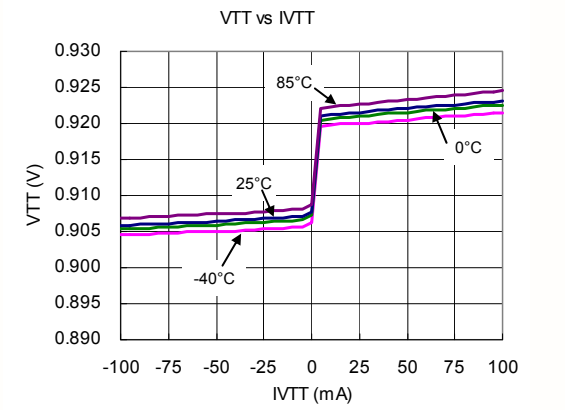


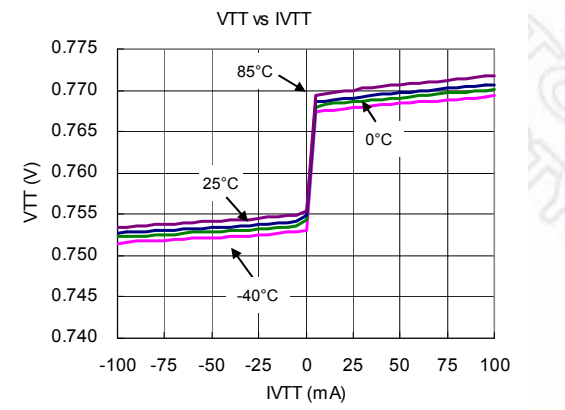

VTT vs IVTT

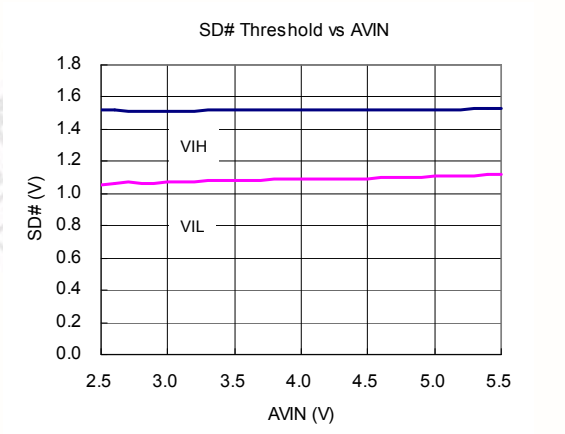



AVIN Operating Current vs AVIN
Current (uA)
Voltage (V)
-40°C
0°C
25°C
85°C


AVIN Shutdown Current vs AVIN
Current (uA)
Voltage (V)
-40°C
0°C
25°C
85°C

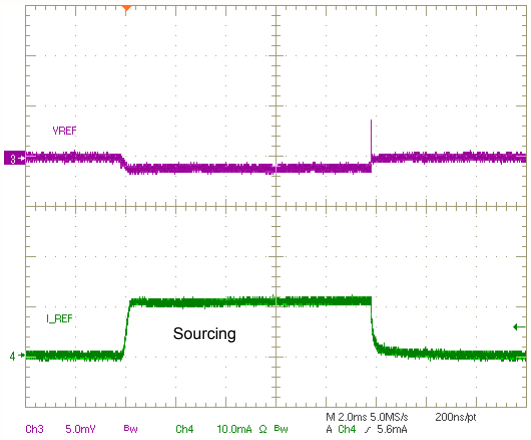

VTT vs IVTT
VTT (V)
IVTT (mA)
85°C
0°C
25°C
-40°C

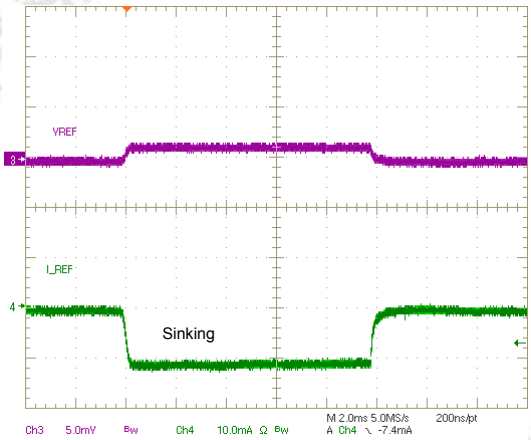

VTT vs IVTT
VTT (V)
IVTT (mA)
85°C
0°C
25°C
-40°C

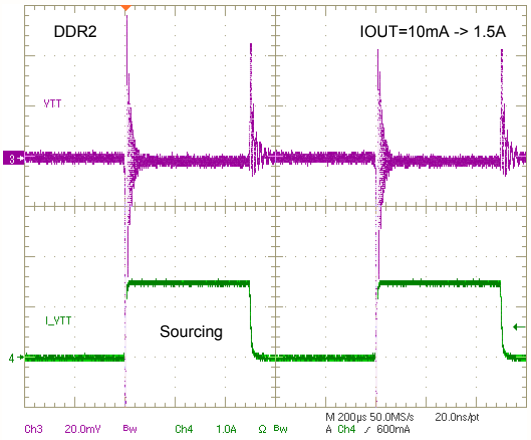

SD# Threshold vs AVIN
SD# (V)
AVIN (V)
VIH
VIL

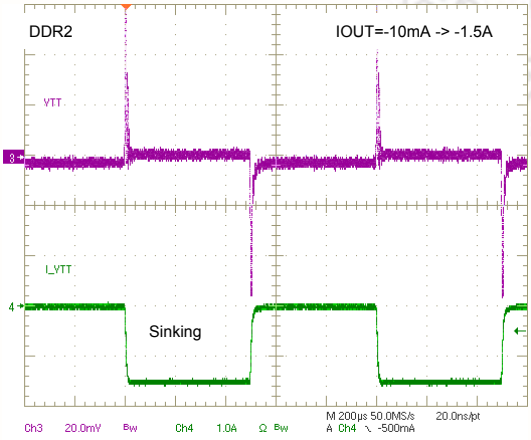
## Operating Waveforms

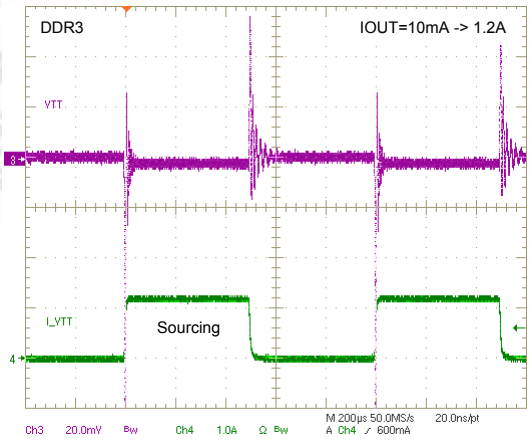
AVIN=2.5V, PVIN=VDDQ=1.8V, COUT=10uF MLCC

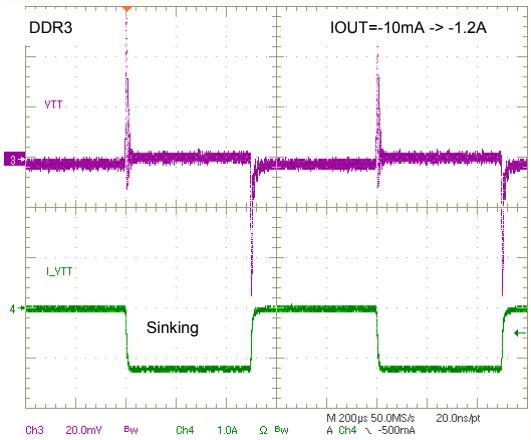


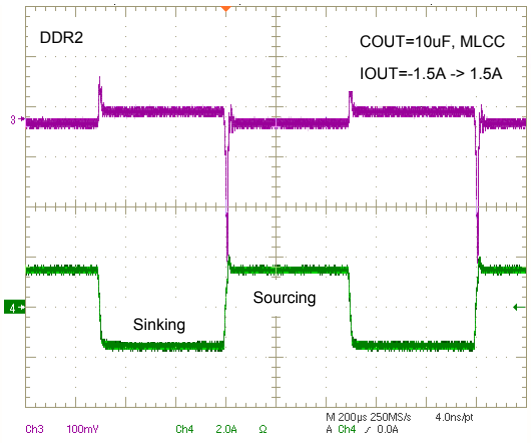



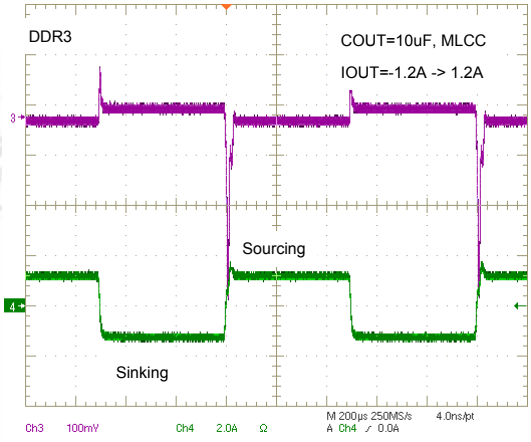



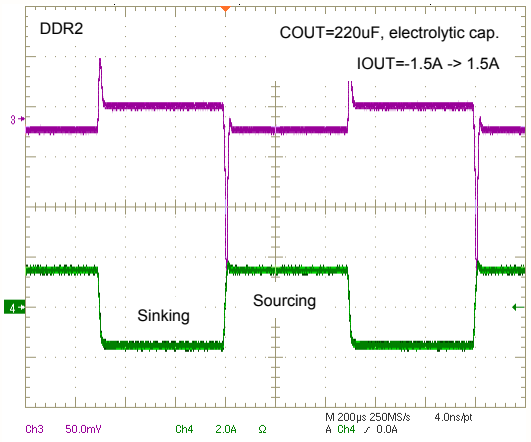



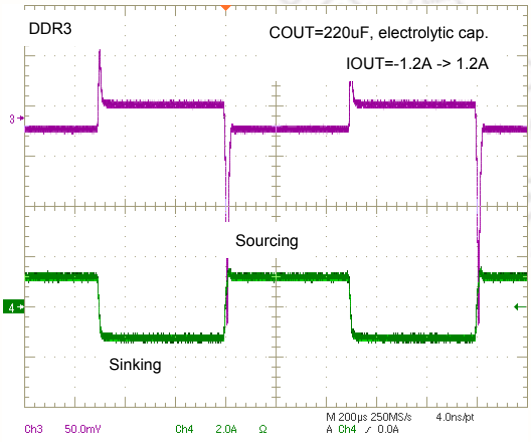



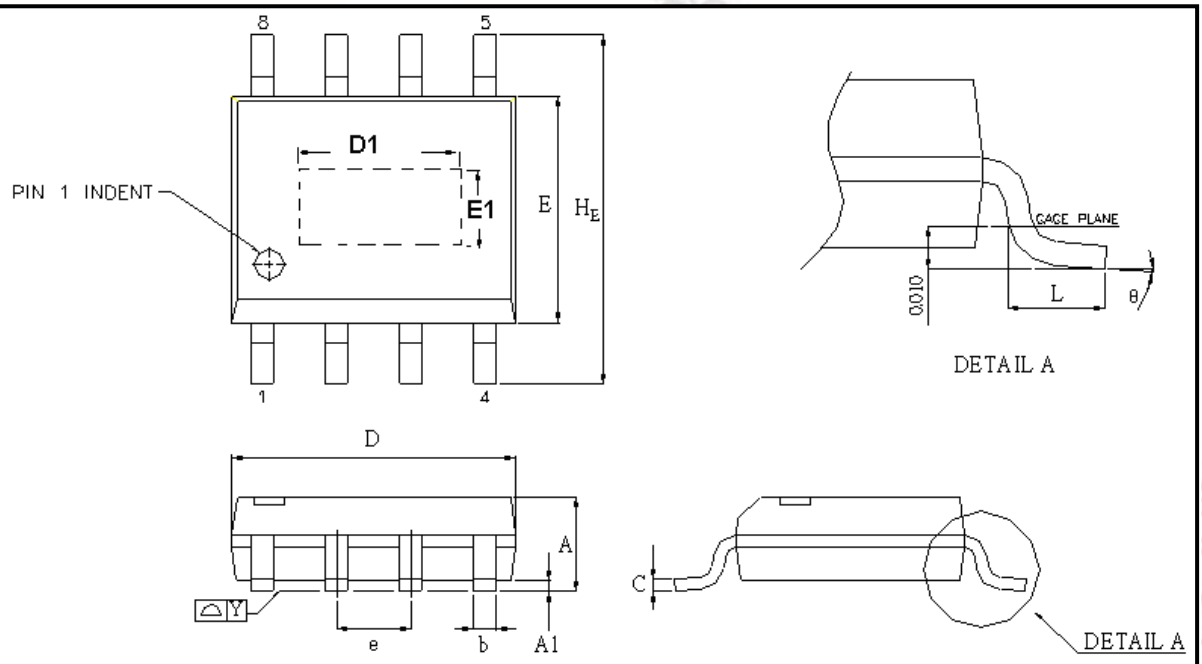


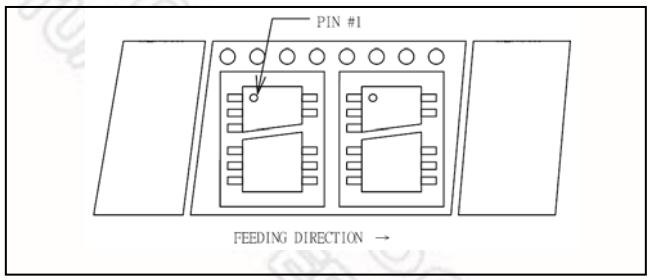



## 9. PACKAGE DIMENSION




| SYMBOLS | Dimensions In Millimeters | | Dimensions In Inched | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.05 | 0.07 |
| A1 | 0.05 | 0.25 | 0.00 | 0.01 |
| b | 0.31 | 0.51 | 0.01 | 0.02 |
| c | 0.10 | 0.25 | 0.00 | 0.01 |
| D | 4.70 | 5.10 | 0.19 | 0.20 |
| E | 3.80 | 4.00 | 0.15 | 0.16 |
| e | 1.27 BASIC | | 0.05 BASIC | |
| $H_E$ | 5.80 | 6.20 | 0.23 | 0.24 |
| Y | -- | 0.10 | -- | 0.00 |
| L | 0.40 | 1.27 | 0.02 | 0.05 |
| $\theta$ | 0° | 10° | 0° | 10° |
| D1 | 1.94 | 3.50 | 0.08 | 0.14 |
| E1 | 1.94 | 2.60 | 0.08 | 0.10 |

### Taping Specification



## 10. ORDERING INFORMATION

NCT3107S Package

| Part Number | Package Type | Supplied as | Production Flow |
|---|---|---|---|
| NCT3107S | 8PIN ESOP (Green Package) | T Shape: 2,500 units/T&R | Commercial, -40°C to + 85°C |

## 11. TOP MARKING SPECIFICATION


1st Line: Nuvoton logo

2nd Line: 3107S (NCT3107S)

3rd line: Tracking code

- 046: packages assembled in Year 2010, week 46
- A: assembly house ID.
- X: IC version. (A means A; B means B and C means C…etc.

## 12. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A0 | 2010/12/17 | All | First Published |
| A1 | 2011/1/17 | 8 | Add PCB Layout Guideline |
| A2 | 2011/11/10 | 8, 16, 17 & 19 | 1. Modified Recommended Land Pattern<br>2. Modified Thermal Pad Dimension<br>3. Modified Ordering Information<br>4. Modified Importance Notice |

## Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**