NCT5104D

Nuvoton 4 COM IC

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1. GENERAL DESCRIPTION

The NCT5104D is a LPC to UART IC, which supports 4 high-speed serial communication port (UART). Each UART includes a 128-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

In addition to UART, the NCT5104D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions. The NCT5104D supports port 80 decode on the LPC bus and could output the signal via SOUTC. It also supports LED control.

The configuration registers inside the NCT5104D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Spec. 1.1
Support SERIRQ (Serialized IRQ)
Support DPM (Device Power Management)
Programmable configuration settings
Single 24-MHz or 48-MHz clock input
Support selective pins of 5 V tolerance

UART

Support 4 high-speed, 16550-compatible UART with 128-byte send / receive FIFO
Support RS485 auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

General Purpose I/O Ports

GPIO0 ~ GPIO1 programmable general purpose I/O ports
Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

Watch Dog Timer Function

LED Function

This is multi-function with some GPIO pins

Operation voltage

3.3 voltage

Package

48-pin LQFP
Green

3. BLOCK DIAGRAM

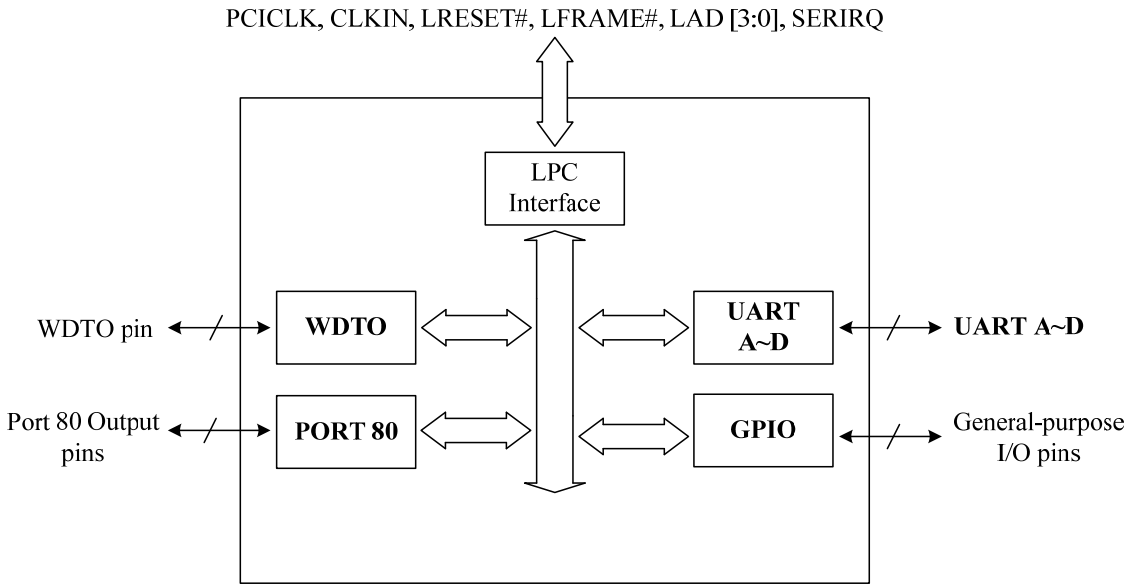


Figure 3-1 NCT5104D Block Diagram

4. PIN LAYOUT

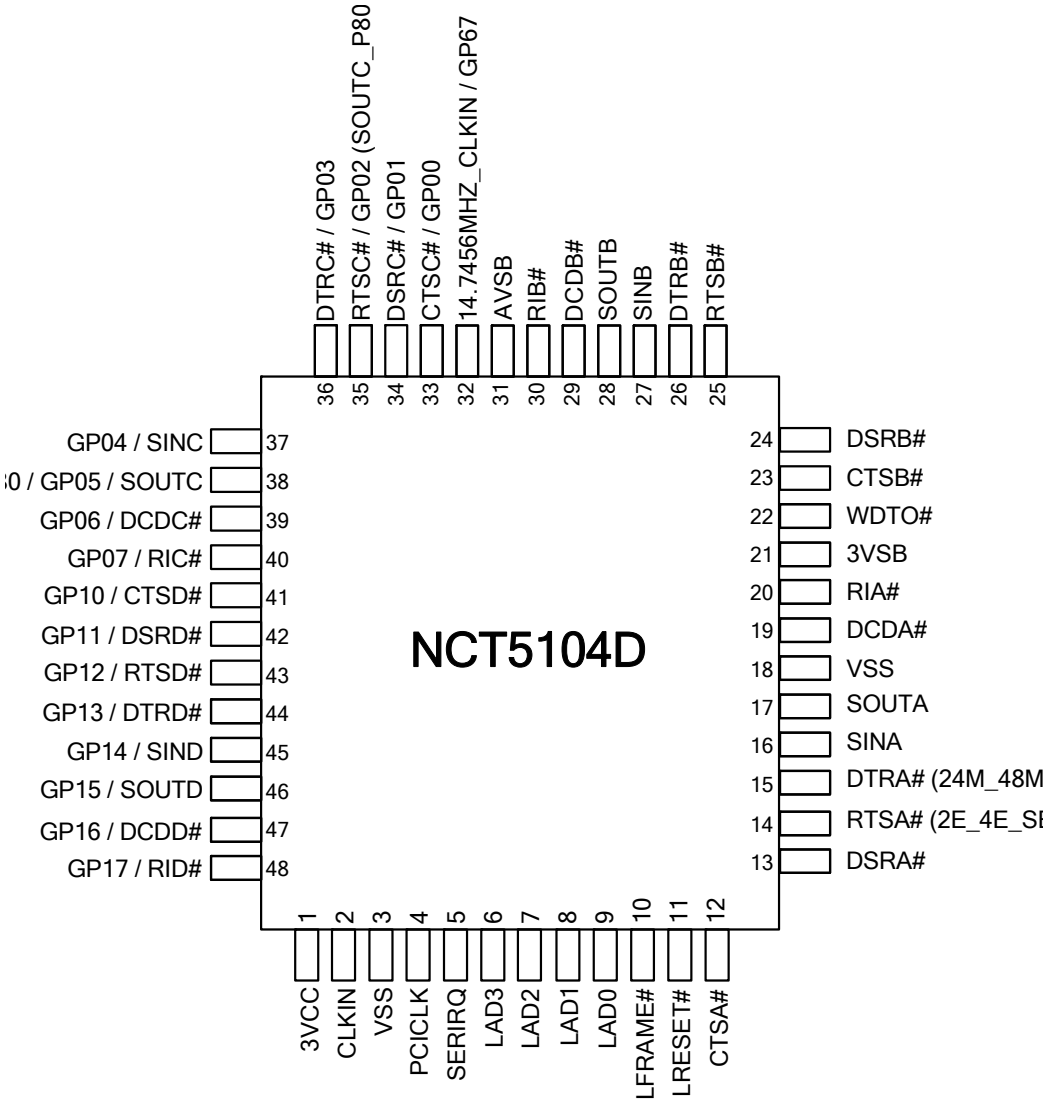


Figure 4-1 NCT5104D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 13.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{tsp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5} - 5V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
IN_{tup5} - 5V TTL-level input pin with internal pull-up resistor
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
2	CLKIN	I	IN_{tp5}	VCC	System clock input, either 24MHz or 48MHz. The actual frequency must be specified by 24M_48M_SEL strapping.
4	PCICLK	I	IN_{tp3}	VCC	PCI-clock 33-MHz input.
5	SERIRQ	I/O	IN_{tp3} O_{12} OD_{12}	VCC	Serialized IRQ input / output.
6-9	LAD[3:0]	I/O	IN_{tp3} OD_{12}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
10	LFRAME#	I	IN_{tp3}	VCC	Indicates the start of a new cycle or the termination of a broken cycle.
11	LRESET#	I	IN_{tp3}	VCC	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
20	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
19	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
17	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
16	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
15	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
14	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
13	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
12	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
30	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
29	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
28	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
27	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
26	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
25	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
24	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
23	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
40	RIC#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
39	DCDC#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
38	SOUTC	O	O_{12}	VSB	UART C Serial Output. This pin is used to transmit serial data out to the communication link.
38	SOUTC_P80	O	O_{12}	VSB	PORT80 to UART Serial Output. This pin is used to transmit serial data out to the communication link.
37	SINC	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
36	DTRC#	O	O_{12}	VSB	UART C Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
35	RTSC#	O	O_{12}	VSB	UART C Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
34	DSRC#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
33	CTSC#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
48	RID#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
47	DCDD#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
46	SOUTD	O	O_{12}	VSB	UART D Serial Output. This pin is used to transmit serial data out to the communication link.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
45	SIND	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
44	DTRD#	O	O_{12}	VSB	UART D Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
43	RTSD#	O	O_{12}	VSB	UART D Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
42	DSRD#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
41	CTSD#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
32	14.7456MHZ _CLKIN	I	IN_{tp5}	VSB	UART-clock 14.7456-MHz input

5.3 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
21	3VSB	I		3VSB	+3.3 V stand-by power supply for the digital circuits.
1	3VCC	I		3VCC	+3.3 V power supply for driving 3 V on host interface.
31	AVSB	I		AVSB	Analog +3.3 V power input. Internally supply power to all analog circuits.
3, 18	VSS	I		VSS	Ground.

5.4 WatchDog

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
22	WDTO#	O		VSB	Watchdog Timer output signal.

5.5 General Purpose I/O Port

5.5.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
33	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 0.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
34	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 1.
35	GP02	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 2.
36	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 3.
37	GP04	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 4.
38	GP05	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 5.
39	GP06	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 6.
40	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 7.

5.5.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
41	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
42	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
43	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.
44	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
45	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
46	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.
47	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
48	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.5.3 GPIO-6 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
32	GP67	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 7.

5.6 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	2E_4E_SEL	I	IN_{tdp5}	VSB	NCT5104D I/O address selection. (Strapped by LRESET#) Strapped to high: NCT5104D I/O address is 4Eh/4Fh. Strapped to low: NCT5104D I/O address is 2Eh/2Fh.
15	24M_48M_SEL	I	IN_{tdp5}	VSB	Input clock rate selection (Strapped by VCC [internal Power OK signal without any delay]) Strapped to high: The clock input on pin 2 is 48MHz. Strapped to low: The clock input on pin 2 is 24MHz.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
35	SOUTC_P80_SEL	I	IN_{tdp5}	VSB	Pin38 function selection. (Strapped by VCC [internal Power OK signal without any delay]) See configuration register.

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# Strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.7 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	14	VSB	Pull-down	47.4K	1
24M_48M_SEL	15	VSB	Pull-down	47.4K	1
SOUTC_P80_SEL	35	VSB	Pull-down	47.4K	1

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

6. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT5104D uses a special protocol to access configuration registers to set up different types of configurations. The NCT5104D has the following Logical Devices: UARTA (Logical Device 2), UARTB (Logical Device 3), GPIO (Logical Device 7), GPIO & WDT1 (Logical Device 8), GPIO (Logical Device F), UARTC (Logical Device 10), UARTD (Logical Device 11), and PORT80 (Logical Device 14).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT5104D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the NCT5104D. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the NCT5104D is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the NCT5104D configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

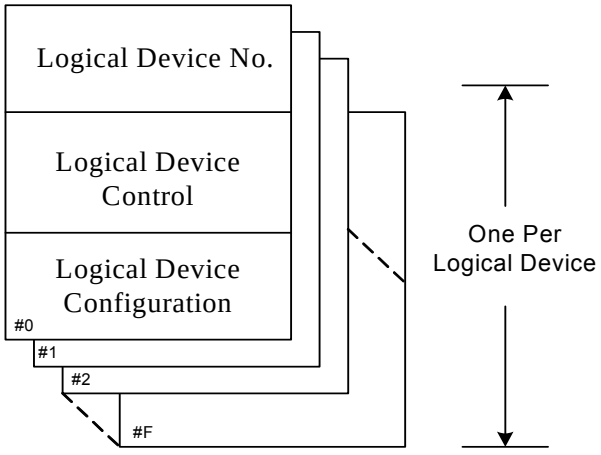


Figure 6-1 Structure of the Configuration Register

Table 6-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	Reserved	
1	Reserved	
2	UARTA	100h ~ FF8h
3	UARTB	100h ~ FF8h
4	Reserved	
5	Reserved	
6	Reserved	
7	GPIO	Reserved
8	GPIO, WDT1	Reserved
9	Reserved	
A	Reserved	
B	Reserved	
C	Reserved	
D	Reserved	
E	Reserved	
F	GPIO	Reserved
10	UARTC	100h ~ FF8h
11	UARTD	100h ~ FF8h
12	Reserved	
13	Reserved	
14	PORT80	100h ~ FF8h
15	Reserved	
16	Reserved	

6.1 Configuration Sequence

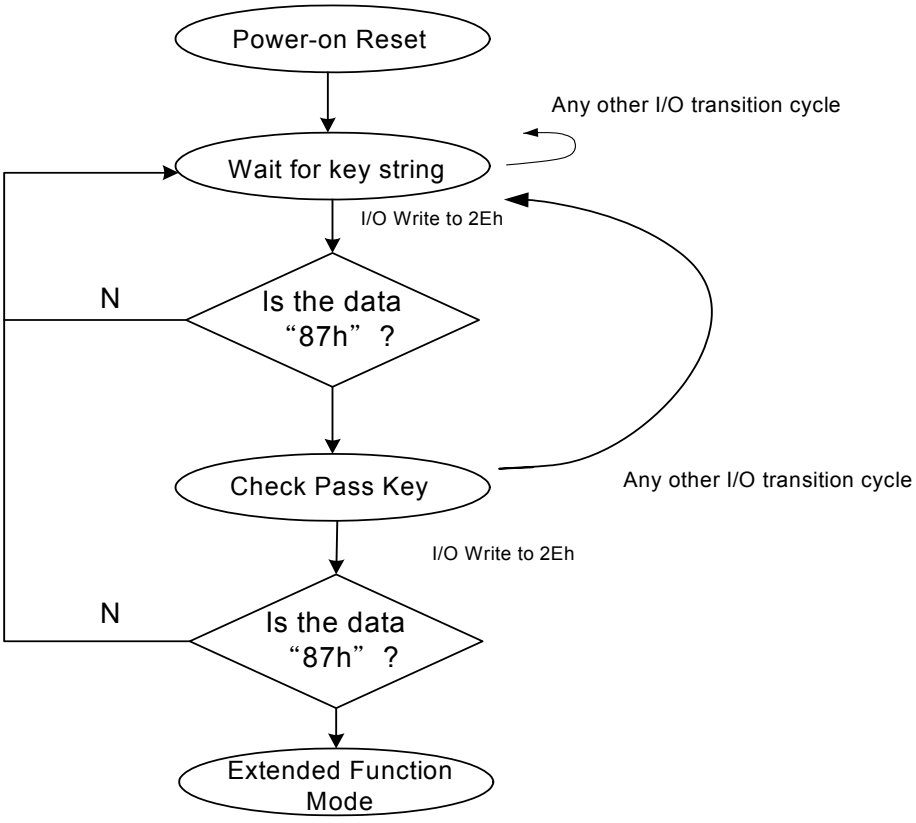


Figure 6-2 Configuration Register

To program the NCT5104D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

6.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

6.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Second, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

6.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

6.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR [26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;-------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
MOV    DX, 2FH
MOV    AL, 3CH
OUT    DX, AL          ; update CRF0 with value 3CH
;-----------------------------------------------
; Exit the Extended Function Mode
;-----------------------------------------------
MOV    DX, 2EH
MOV    AL, AAH
OUT    DX, AL
```

7. UART PORT

NCT5104D supports 4 UART – UART A, UART B, UART C, and UART D.

7.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits

DLS1	DLS0	DATA LENGTH
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 7-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

7.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

7.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

7.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

7.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

7.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.

5-4	**RESERVED.**	
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

7.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	**RESERVED.**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the

BIT	DESCRIPTION
	handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

7.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER			
Pre-Div: 13 1.8461M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage
50	650	**2304**	**
75	975	**1536**	**
110	1430	**1047**	0.18%
134.5	1478.5	**857**	0.099%
150	1950	**768**	**
300	3900	**384**	**
600	7800	**192**	**
1200	15600	**96**	**
1800	23400	**64**	**
2000	26000	**58**	0.53%
2400	31200	**48**	**
3600	46800	**32**	**
4800	62400	**24**	**
7200	93600	**16**	**
9600	124800	**12**	**
19200	249600	**6**	**
38400	499200	**3**	**
57600	748800	**2**	**
115200	1497600	**1**	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A.

7.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

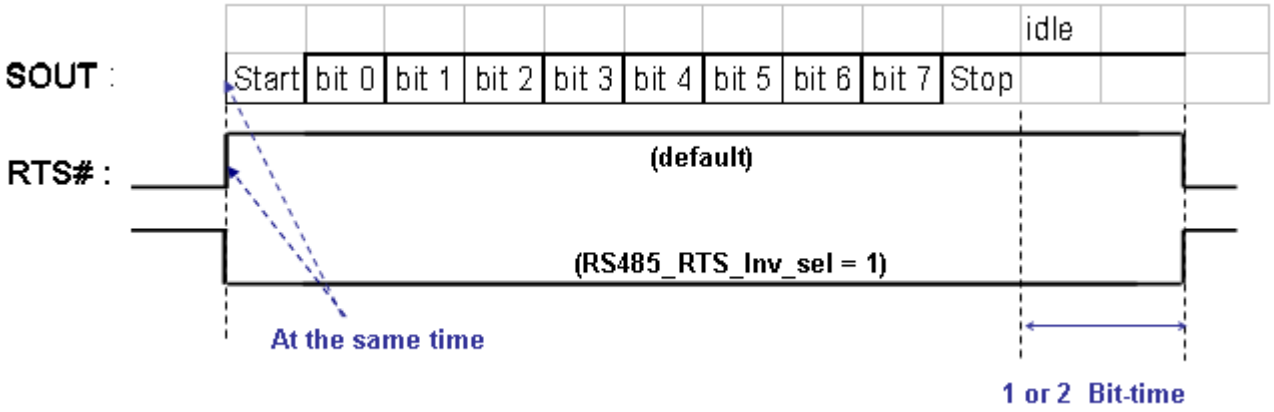
7.10 Extendding FIFO

We support FIFO size extending to 32bytes for RX and TX block. (Enable bit: CRF8, Bit0)

7.11 UART RS485 Auto Flow Control

NCT5104D supports RS485 auto flow control function for UARTA ~ UARTF. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA ~ UARTF when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA ~ UARTF.



The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1 or 2 Bit-Time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA ~ UARTF.

	UARTA	UARTB	UARTC	UARTD	UARTE	UARTF
RTS485_enable	Logic Device 2, CRF2_Bit1	Logic Device 3, CRF2_Bit1	Logic Device 10, CRF2_Bit1	Logic Device 11, CRF2_Bit1	Logic Device 12, CRF2_Bit1	Logic Device 13, CRF2_Bit1
RTS485_inv_sel	Logic Device 2, CRF2_Bit4	Logic Device 3, CRF2_Bit4	Logic Device 10, CRF2_Bit4	Logic Device 11, CRF2_Bit4	Logic Device 12, CRF2_Bit4	Logic Device 13, CRF2_Bit4
RST_low_time_sel	Logic Device 2, CRF2_Bit5	Logic Device 3, CRF2_Bit5	Logic Device 10, CRF2_Bit5	Logic Device 11, CRF2_Bit5	Logic Device 12, CRF2_Bit5	Logic Device 13, CRF2_Bit5

7.12 UART 9BIT-MODE

7.12.1 Function Dscription

► **Tx function block:**

1. 9bit-TX block supports 9bit-mode or original RS232 mode TX signal output.
2. 9bit-TX block supports sending address byte
   (Setting **En_9bit_mode =1** and **En_address_byte =1** will force parity bit turned to high bit)
3. 9bit-TX block supports 9bit-mode RS485 RTS or original RS232 mode RTS signal output.
4. 9bit-TX block supports 9bit-mode inverted and time selected for the RS485 RTS signal.
   (RS485 RTS time selected: one or two TXC period)
5. 9bit-TX block supports clear "en_address_byte" bit automatic.

	Register location (UART A) Logic Device 2	Register location (UART B) Logic Device 3	Register location (UART C) Logic Device 10	Register location (UART D) Logic Device 11	Register location (UART E) Logic Device 12	Register location (UART F) Logic Device 13
En_address_byte	03f9, Bit7 (default)	02f9, Bit7 (default)	03f9, Bit7 (default)	03f9, Bit7 (default)	03f9, Bit7 (default)	03f9, Bit7 (default)

► **Rx function block:**

1. 9bit-RX block supports 9bit-mode or original RS232 mode RX signal output.
2. 9bit-RX block supports comparison between with the slave address and broadcast address byte determined by the two registers. (see blow: slave_address and slave_address_mask registers)

3. 9bit-RX block supports received address byte pass into RX block FIFO.
4. 9bit-RX block supports UART 9bit-mode IRQ output and could select to be issued only when receiving any address bytes or only received address matched.
5. 9bit-RX block will automatic modify parity bit of address/data byte to meet parity check from UART receiver block when using 9bit-bit mode.
6. 9bit-RX block supports different mode that have different functions by setting RX_ctrl_set[2:0].
   (default: RX_ctrl_set[2:0] = 000)

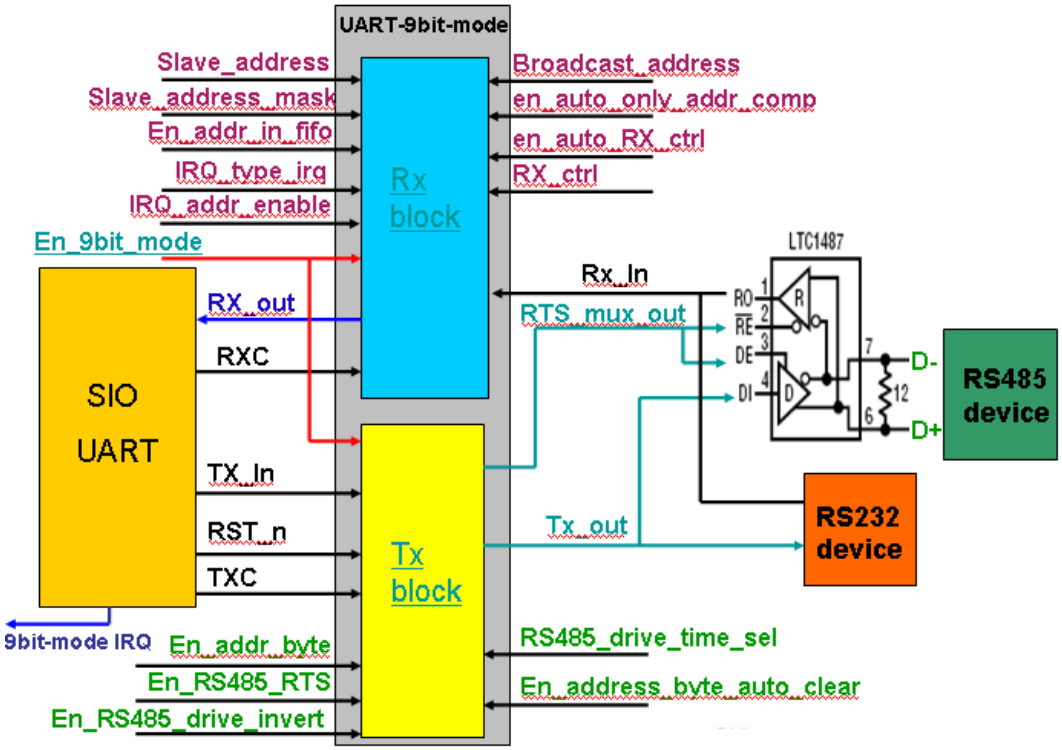
	Register location (UART A) Logic Device 2	Register location (UART B) Logic Device 3	Register location (UART C) Logic Device 10	Register location (UART D) Logic Device 11	Register location (UART E) Logic Device 12	Register location (UART F) Logic Device 13
RX_ctrl_set[2]: **(**en_auto_only_addr_comp**)**	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6
RX_ctrl_set[1]:	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7

(en_auto_RX_ctrl)						
RX_ctrl_set[0]: (RX_ctrl)	03f9, Bit6 (default)	02f9, Bit6 (default)	03f9, Bit6 (default)	03f9, Bit6 (default)	03f9, Bit6 (default)	03f9, Bit6 (default)

RX_ctrl_set[2:0]	Function Description
000	1. 9bitmode RX block function will pass all data or address bytes to UART receiver block directly. 2. 9bitmode RX block function will not compare any address byte. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
001	1. 9bitmode RX block function will only pass address bytes to UART receiver block. 2. 9bitmode RX block function will not compare any address byte. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
010	1. 9bitmode RX block function will update RX_ctrl Bit automatically. When RX_ctrl = 0: If receive address byte, 9bitmode RX block function will update RX_ctrl=1 automatically. In order to receive address byte at next byte cycle. (RX block function will ignore the current address byte. Then the transmitter needs to resend this address byte again.) 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
011	1. 9bitmode RX block function will update RX_ctrl Bit automatically. When RX_ctrl = 1: If address byte matched, 9bitmode RX block function will update RX_ctrl=0 automatically. In order to receive data byte at next byte cycle. 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
100 (The same as 000)	1 9bitmode RX block function will pass all data or address bytes to UART receiver block directly. 2 9bitmode RX block function will not compare any address byte. 3 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)

101 (The same as 001)	1. 9bitmode RX block function will only pass address bytes to UART receiver block. 2. 9bitmode RX block function will not compare any address byte. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
110	1. 9bitmode RX block function will not update RX_ctrl Bit automatically. When RX_ctrl = 0: If receive address byte, in order to receive the address byte, we need set RX_ctrl = 1 manually. 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)
111	1. 9bitmode RX block function will not update RX_ctrl Bit automatically. When RX_ctrl = 1: If address byte matched, in order to receive the proceeding data bytes, we need set RX_ctrl = 0 manually. 2. 9bitmode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bitmode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bitmode RX block function will generate IRQ. (Refer to CRF6 description.)

7.12.2 Function Block



11.13 UART switch

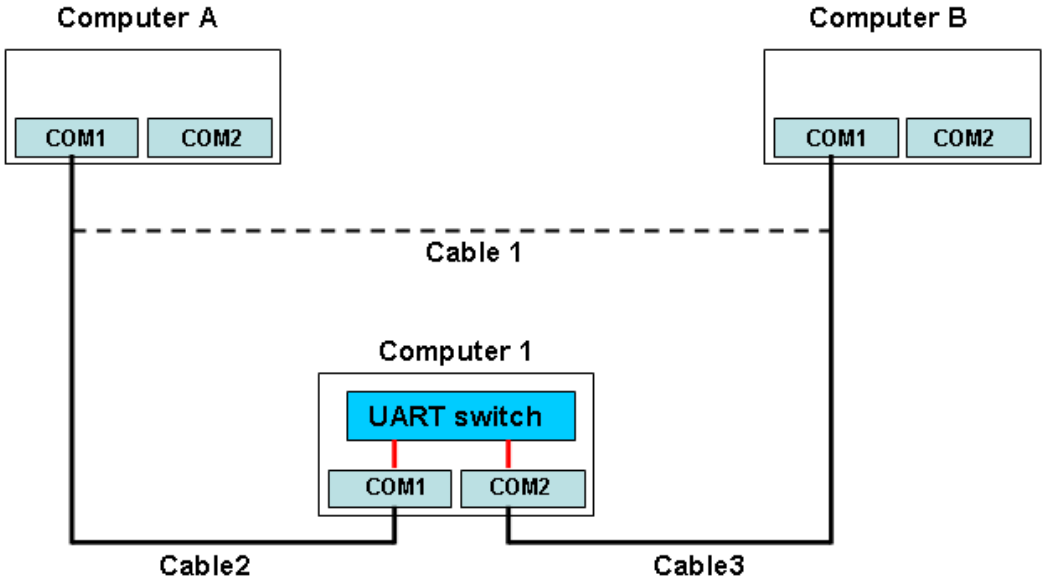
Due to the limitation length of the cable for the communication of UART,

We support 2 sets of switches to fix this limitation. They are UARTAB and UARTCD switches.

Switch Name	Switch Enable Bit	Description
UARTAB switch	Logic Device 02, IndexF8_Bit4	Conection with UARTA and UARTB
UARTCD switch	Logic Device 10, IndexF8_Bit4	Conection with UARTC and UARTD

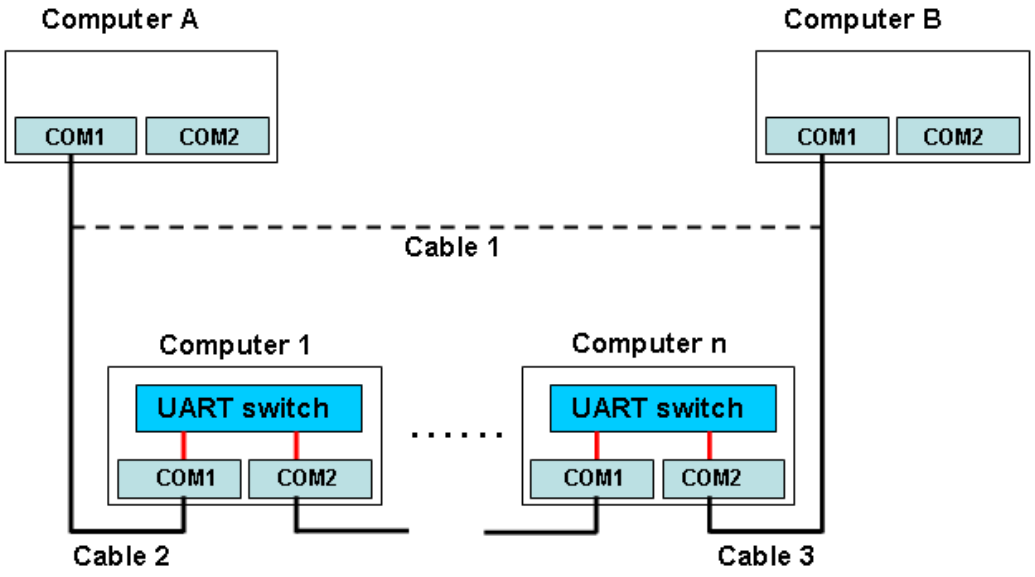
For example, if computer A and computer B will transfer data to each other with UART, but the distance between computer A and B is over the limitation length of the cable. See the figure shown below, and the cable 1 is over the limitation.

And we could use uart switch to fix this limitation. If the switch of computer1 is enabled, computer A could transfer data to computer 1 and computer 1 would bypass the data to computer B. In the same method, computer B also could achieve the goal to transfer data to computer A.



The connection of UART switch with single computer

We also could connect mult-switch to fix the limitataion length of the cable, if the distance between computer A and computer B is too far. The figure below shows the connection method of multi-switch.



The connection of UART switch with multi-computer

8. SERIALIZED IRQ

The NCT5104D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

8.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT5104D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT5104D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

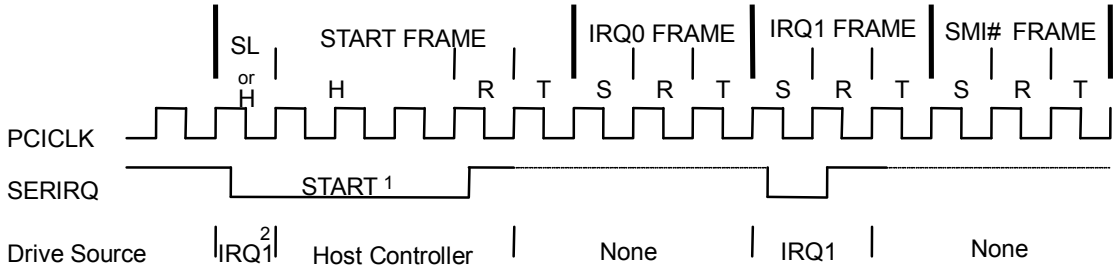


Figure 8-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT5104D because IRQ1 of the NCT5104D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

8.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT5104D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT5104D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT5104D device drives the SERIRQ high. During the Turn-around phase, the NCT5104D device leaves the SERIRQ tri-stated. The NCT5104D starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 8-1.

Table 8-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Reserved
3	SMI#	8	Reserved
4	IRQ3	11	Reserved
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	Reserved
8	IRQ7	23	Reserved
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Reserved
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

8.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

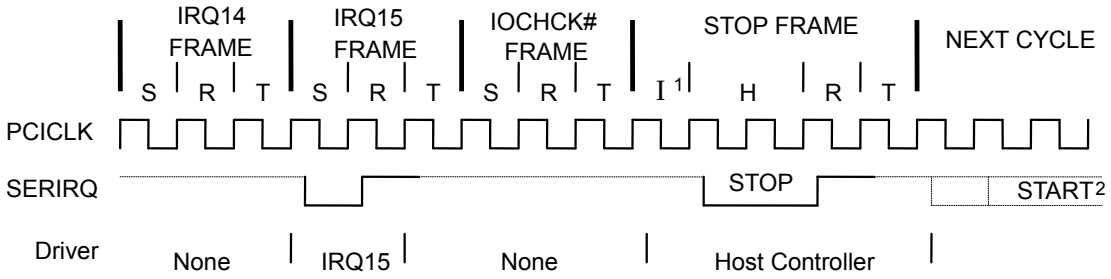


Figure 8-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

9. WATCHDOG TIMER

The Watchdog Timer of the NCT5104D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0 and GPIO6 provide an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F0h], bit[3]. The time-out value is set at Logical Device 8, CR[F1h], default is 4. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0 bit[1], [5], GPIO6 bit[7] will trigger a low pluse apporx 100mS. Also the event could go to pin22 WDTO#. In other words, when the value is counted down to zero, the timer stops, and the NCT5104D sets the WDT1 status bit in Logical Device 8, CR[F2h], bit[4]. Writing a zero will clear the status bit. This bit will also be cleared if LRESET# signal is asserted.

10. GENERAL PURPOSE I/O

10.1 GPIO ARCHITECTURE

The NCT5104D provides 17 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. GPIO ports are configured through control registers in logical device 7. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inverse). Port value is read/written through data register.

Table 10-1 GPIO Group Programming Table

Equips maximum 17-pin GPIOs.					
GPIO0 Group Enable: Logic Device 7, CR30[0] Data: Logic Device 7, E0~E3 Multi-function: YLW, GRN, WDTO#, SUSLED (Logic Device 8, CRE0[7-0]) Reset: Logic Device 9, CRE2[0] OD/PP: Logic Device F, CRE0					
Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP00	33	GP00	input	3VSB	
GP01	34	GP01	input	3VSB	
GP02	35	GP02	input	3VSB	
GP03	36	GP03	input	3VSB	
GP04	37	GP04	input	3VSB	
GP05	38	GP05	input	3VSB	
GP06	39	GP06	input	3VSB	
GP07	40	GP07	input	3VSB	
GPIO1 Group Enable: Logic Device 7, CR30[1] Data: Logic Device 7, E4~E7 Multi-function: YLW, GRN, BEEP, SMI (Logic Device 8, CRE1[7-0]) Reset: Logic Device 9, CRE2[1] OD/PP: Logic Device F, CRE1					
Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP10	41	GP10	input	3VSB	
GP11	42	GP11	input	3VSB	
GP12	43	GP12	input	3VSB	
GP13	44	GP13	input	3VSB	
GP14	45	GP14	input	3VSB	
GP15	46	GP15	input	3VSB	
GP16	47	GP16	input	3VSB	

GP17	48	GP17	input	3VSB	
GPIO6 Group Enable: Logic Device 7, CR30[6] Data: Logic Device 7, F8~FB Multi-function: YLW, GRN, BEEP, SMI, WDTO#, SUSLED, PLED (Logic Device 8, CRE6[7-0]) Reset: Logic Device 9, CRE2[6] OD/PP: Logic Device F, CRE6					
Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP67	32	GP67	input	3VSB	

Table 10-2 GPIO Multi-Function Routing Table

Bit	GPIO0	GPIO1
7	0: GPIO07 1: YLW	0: GPIO17 1: YLW
6	0: GPIO06 1: GRN	0: GPIO16 1: GRN
5	0: GPIO05 1: WDTO#	0: GPIO15 1: BEEP
4	0: GPIO04 1: SUSLED	0: GPIO14 1: SMI
3	0: GPIO03 1: YLW	0: GPIO13 1: YLW
2	0: GPIO02 1: GRN	0: GPIO12 1: GRN
1	0: GPIO01 1: WDTO#	0: GPIO11 1: BEEP
0	0: GPIO00 1: SUSLED	0: GPIO10 1: SMI

Bit	GPIO6
7	000: GPIO67 001: YLW 001: GRN 001: BEEP 001: SMI 001: WDTO# 001: SUSLED 001: PLED

10.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 11-3. Base address plus 0 to 4 are GPIO registers, base address plus 5 and 6 are watchdog registers.Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#1 for GPIO0 ~ GPIO1 respectively). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time.

Table 10-3 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved				INDEX			
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							
Base + 5	Wdtmod	Watchdog Timer I (WDT1) Control Mode Register							
Base + 6	Wdttim	Watchdog Timer I (WDT1) Control Register							

11. PORT80 TO UART

The NCT5104D provides UART interface to transfer PORT80 information to other peripheral devices. Default baud rate is 115200Hz for universal UART protocol and it could be change by LD14 CRE2 and LD14 CRE3. When BIOS program PORT80 LED, in proportion to UART baud rate, it changes very frequently. Thus, some information might be lose. But we make sure the last one would be send.

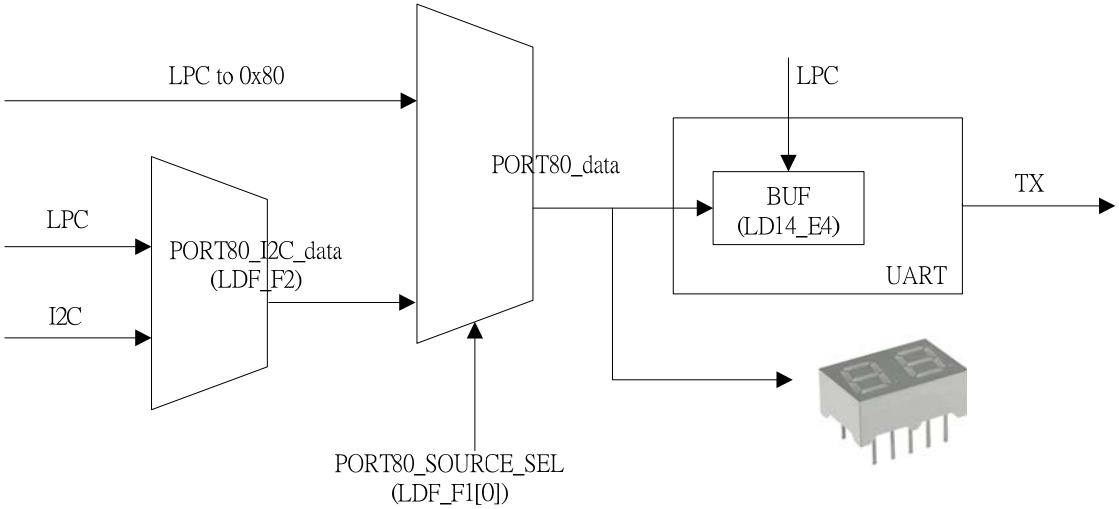


Figure 11-1 PORT80 to UART Block Diagram

After enter OS, we support other root to control PORT80 LED by write LDF CRF2 and LDF CRF1 to change other path. The UART could be control by other root, too. It is set by LD14 CRE4.

12. CONFIGURATION REGISTER

12.1 Chip (Global) Control Register

CR 02h. Software Reset Register

Location: Address 02h
Attribute: Write Only
Power Well: VCC
Reset by: LRESET#
Default :
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. Logical Device Selection

Location: Address 07h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Location: Address 10h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3-0	Reserved	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Location: Address 11h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	WDTO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTD IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3-2	Reserved	
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Location: Address 13h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Location: Address 14h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ch. Multi Function Selection

Location: Address 1Ch
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	Pin32 function selection CR27 [Bit2] / CR1C [Bit4] / Pin32 0 / 0 / 14.7456MHZ_CLKIN 0 / 1 / GP67 1 / x / Reserved
3	R / W	Pin33-40 function selection SOUTC_P80_SEL / CR1C [Bit3] / Pin33-40 1 / x / GP0x, SOUTC_P80 0 / 0 / GP0x 0 / 1 / UARTC
2	R / W	Pin41-48 function selection CR1C [Bit2] / Pin41-48 0 / GP1x 1 / UARTD
1-0	Reserved.	

CR 20h. Chip ID (High Byte)

Location: Address 20h
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 10h (high byte).

CR 21h. Chip ID (Low Byte)
Location: Address 21h
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 61h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 61h (low byte)

CR 22h. Device Power Down
Location: Address 22h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 7Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3-2	Reserved	
1	R / W	IPD (Immediate Power Down). When set to 0, the whole chip is put into power-down mode immediately.
0	Reserved	

CR 24h. Multi Function Selection & Global Option
Location: Address 24h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

7-1	Reserved	
0	R / W	PNPCVS => = 0 The compatible PNP address-select registers have default values. = 1 The compatible PNP address-select registers have no default values.

CR 25h. Interface Tri-state Enable
Location: Address 25h
Attribute: Read/Write

Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	UARTDTRI
4	R / W	UARTCTRI
3	R / W	UARTBTRI
2	R / W	UARTATRI
1-0	Reserved	

CR 26h. Global Option s: value by strapping
Location: Address 26h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 0s000000b
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin14).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4-2	Reserved.	
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable URAT B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. Global Option
Location: Address 27h
Attribute: Read/Write
Power Well: VSB

Reset by: RSMRST#
Default : 00h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R / W</td><td>Pin32 function selection
<table>
<tr><th>CR27 [Bit2]</th><th>CR1C [Bit4]</th><th>Pin32</th></tr>
<tr><td>0</td><td>0</td><td>14.7456MHZ_CLKIN</td></tr>
<tr><td>0</td><td>1</td><td>GP67</td></tr>
<tr><td>1</td><td>x</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>1-0</td><td colspan="2">Reserved</td></tr>
</table>

CR 29h. Global Option
Location: Address 29h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : F0h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	UARTD Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTC Power Down. 0: Powered down. 1: Not powered down.
3-2	Reserved	
1	R / W	DSUDLGRQ => = 0 Enable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUCLGRQ => = 0 Enable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 2Fh. Strapping Function Result
Location: Address 2Fh
Attribute: Read/Write
Power Well: VSB
Reset by: PWROK#, RSMRST# (Bit2)
Default : by 000s_ssss
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	SOUTC_P80_SEL Strapping result reading, it can output the port80 data to UARTE interface.
2-1	Reserved	
0	R / W	24M_48M_SEL Strapping result reading

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

3) VSB Strapping result can be programming by LPC, and reset by RSMRST#
4) VCC Strapping result can be programming by LPC, and reset by PWROK

LRESET Strapping (2E_4E_SEL) : No change

12.2 Logical Device 2 (UARTA)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: UART A clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTA 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTA 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTA 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTA 9bit-mode Broadcase Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTA 9bit-mode Interrupt Control Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTA 9bit-mode IRQ output. 1: Enalbe UARTA 9bit-mode IRQ output.

CR F7h. UARTA 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTA 9bit-mode Status Bit** 0: UARTA 9bit-mode IRQ have not been triggered. 1: UARTA 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTA Control Register
Location: Address F8h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartAB_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**fifo_level_mode:** **(Also check UFR register B7-6 definition)**

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

5	**Reserved.**
4	**uartAB_switch_enable (Bypass mode)** **0: switch disable** **1: switch enable**
3-1	**Reserved. (All should be set to 0)**
0	**Extending fifo enable bit:** **0:** Disable128bytes TX and RX FIFO. **1:** Enable128bytes TX and RX FIFO.

12.3 Logical Device 3 (UARTB)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, F8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 2.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART B clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART B clock source is 2 MHz (24 MHz / 12). 0 0: UART B clock source is 24 MHz (24 MHz / 1). 0 0: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTB 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTB 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTB 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTB 9bit-mode Broadcase Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTB 9bit-mode Interrupt Control Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTB 9bit-mode IRQ output. 1: Enalbe UARTB 9bit-mode IRQ output.

CR F7h. UARTB 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTB 9bit-mode Status Bit** 0: UARTB 9bit-mode IRQ have not been triggered. 1: UARTB 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTB Control Register
Location: Address F8h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**fifo_level_mode:** **(Also check UFR register B7-6 definition)**
5-4	**Reserved.**
3-1	**Reserved.** **(All should be set to 0)**
0	**Extending fifo enable bit:** **0:** Disable128bytes TX and RX FIFO. **1:** Enable128bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

12.4 Logical Device 7 (GPIO)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, LRESET# (Bit2)
Default : DFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: GPIO6 is inactive. 1: GPIO6 is active.
5-2	Reserved	
1	R / W	0: GPIO1 is inactive. 1: GPIO1 is active.
0	R / W	0: GPIO0 is inactive. 1: GPIO0 is active.

CR E0h. GPIO0 I/O Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Location: Address E3h
Attribute: Read Only
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP07-GP00, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO1 I/O Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

CR E5h. GPIO1 Data Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST

Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO1 Inversion Register
Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO1 Status Register
Location: Address E7h
Attribute: Read Only
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F8h. GPIO6 I/O Register
Location: Address F8h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F9h. GPIO6 Data Register

Location: Address F9h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR FAh. GPIO6 Inversion Register

Location: Address FAh
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR FBh. GPIO6 Status Register

Location: Address FBh
Attribute: Read Only
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

12.5 Logical Device 8 (GPIO, WDT1)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR E0h. GPIO0 Multi-function Select Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO07 1: GPIO07 → YLW
6	R / W	0: GPIO06 1: GPIO06 → GRN
5	R / W	0: GPIO05 1: GPIO05 → WDTO#
4	R / W	0: GPIO04 1: GPIO04 → SUSLED

BIT	READ / WRITE	DESCRIPTION
3	R / W	0: GPIO03 1: GPIO03 → YLW
2	R / W	0: GPIO02 1: GPIO02 → GRN
1	R / W	0: GPIO01 1: GPIO01 → WDTO#
0	R / W	0: GPIO00 1: GPIO00 → SUSLED

CR E1h. GPIO1 Multi-function Select Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → YLW
6	R / W	0: GPIO16 1: GPIO16 → GRN
5	R / W	0: GPIO15 1: GPIO15 → BEEP
4	R / W	0: GPIO14 1: GPIO14 → SMI
3	R / W	0: GPIO13 1: GPIO13 → YLW
2	R / W	0: GPIO12 1: GPIO12 → GRN
1	R / W	0: GPIO11 1: GPIO11 → BEEP
0	R / W	0: GPIO10 1: GPIO10 → SMI

CR E7h. GPIO6 Multi-function Select Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST (Bit7-5)
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	000: GPIO67 001: GPIO67 → YLW 010: GPIO67 → GRN 011: GPIO67 → BEEP 100: GPIO67 → SMI 101: GPIO67 → WDTO# 110: GPIO67 → SUSLED 111: GPIO67 → PLED
4-0	Reserved.	

CR F0h. Watchdog Timer I (WDT1) Control Mode Register

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Watchdog Timer I count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode.
2-0	Reversed	

CR F1h. Watchdog Timer I(WDT1) Counter Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F2h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after $5.03x10^7$ CLKIN cycle time, by analogy. ($5.03x10^7$x (1/48MHz) = 1.046s)

CR F2h. Watchdog Timer I (WDT1) Control & Status Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	Write “1” Only	Trigger Watchdog Timer I event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer I status bit 0: Watchdog Timer I is running. 1: Watchdog Timer I issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer I

12.6 Logical Device F (GPIO)

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E1h.

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP1 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E6h.

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP6 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR F1h. I2C to 80PORT Control Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#

Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	80PORT Display 0: Enable 1: Disable
0	R / W	LPC or I2C to 80PORT switch 0: LPC 1: I2C

CR F2h. I2C to 80PORT Data Register
Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

12.7 Logical Device 10 (UARTC)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, E0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 3.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART C clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART C clock source is 2 MHz (24 MHz / 12). 0 0: UART C clock source is 24 MHz (24 MHz / 1). 0 0: UART C clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTC 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTC 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTC 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTC 9bit-mode Broadcase Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTC 9bit-mode Interrupt Control Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTC 9bit-mode IRQ output. 1: Enalbe UARTC 9bit-mode IRQ output.

CR F7h. UARTC 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTC 9bit-mode Status Bit** 0: UARTC 9bit-mode IRQ have not been triggered. 1: UARTC 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTC Control Register
Location: Address F8h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartCD_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**fifo_level_mode:** **(Also check UFR register B7-6 definition)**

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

5	**Reserved.**
4	**uartCD_switch_enable (Bypass mode)** **0: switch disable** **1: switch enable**
3-1	**Reserved. (All should be set to 0)**
0	**Extending fifo enable bit:** **0:** Disable128bytes TX and RX FIFO. **1:** Enable128bytes TX and RX FIFO.

12.8 Logical Device 11 (UARTD)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, E0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 4.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART D clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART D clock source is 2 MHz (24 MHz / 12). 0 0: UART D clock source is 24 MHz (24 MHz / 1). 0 0: UART D clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTD 9bit-mode Config Register

Location: Address F1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bitmode RX block function will pass all data or address byte and not compare any address byte. 1: 9bitmode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bitmode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bitmode RX block function.
5	R / W	**RST_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX blockwill keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data. 1: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data.

BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ingored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bitmode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTD 9bit-mode Slave Address Register

Location: Address F2h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTD 9bit-mode Slave Mask Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTD 9bit-mode Broadcase Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcase Address**

CR F6h. UARTD 9bit-mode Interrupt Control Register
Location: Address F5h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTD 9bit-mode IRQ output. 1: Enalbe UARTD 9bit-mode IRQ output.

CR F7h. UARTD 9bit-mode IRQ Status Register
Location: Address F6h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	**UARTD 9bit-mode Status Bit** 0: UARTD 9bit-mode IRQ have not been triggered. 1: UARTD 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTD Control Register
Location: Address F7h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**fifo_level_mode:** **(Also check UFR register B7-6 definition)**
5-4	**Reserved.**
3-1	**Reserved.** **(All should be set to 0)**
0	**Extending fifo enable bit:** **0:** Disable128bytes TX and RX FIFO. **1:** Enable128bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

12.9 Logical Device 14 (PORT80)

CR E0h. PORT80 UART Control Register

Location: Address E0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved.	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length selecion) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved.	

CR E1h. PORT80 UART Status Register

Location: Address E1h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Location: Address E2h
Attribute: Read/Write

Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte
Location: Address E3h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer
Location: Address E4h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

CR F0h.
Location: Address F0h
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	

BIT	READ / WRITE	DESCRIPTION
1~0	R / W	**Bits** **1 0** 0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: IR clock source is 2 MHz (24 MHz / 12). 0 0: IR clock source is 24 MHz (24 MHz / 1). 0 0: IR clock source is 14.769 MHz (24 MHz / 1.625).

13. SPECIFICATIONS

13.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	-40 to +85	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

13.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	μA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	IVCC			25	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
Vtt Quiescent Current	IVTT			1	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V VTT = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
AIN – Analog input						

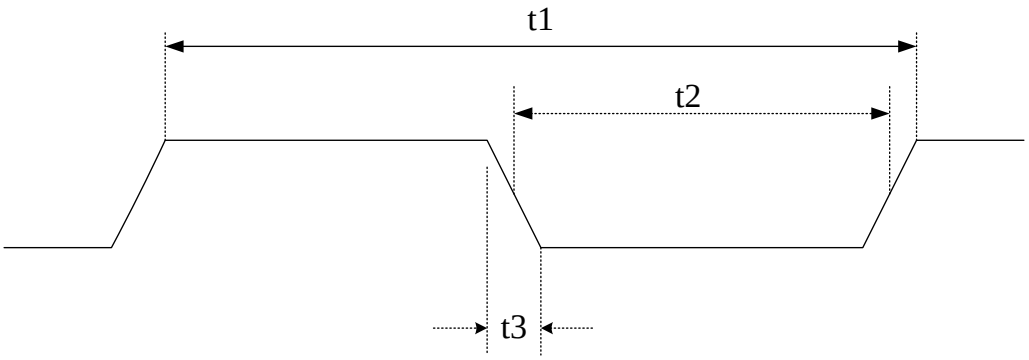
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
AOUT – Analog output						
IN_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{gp5} – 5V GTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
IN_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OD8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
O12 – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD12 – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O24 – Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD24 – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
O48 – Output pin with 48mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -48 mA
OD48 – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
O12cu – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD12cu – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

14. AC CHARACTERISTICS

14.1 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



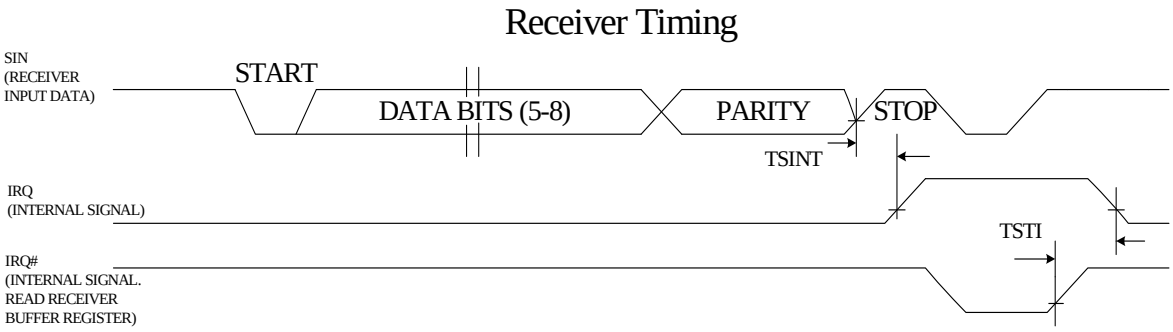
PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

14.2 UART

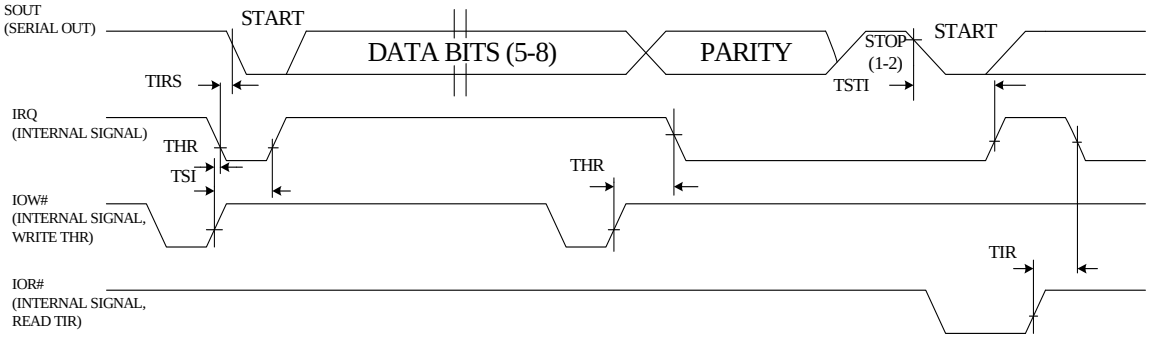
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate

Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

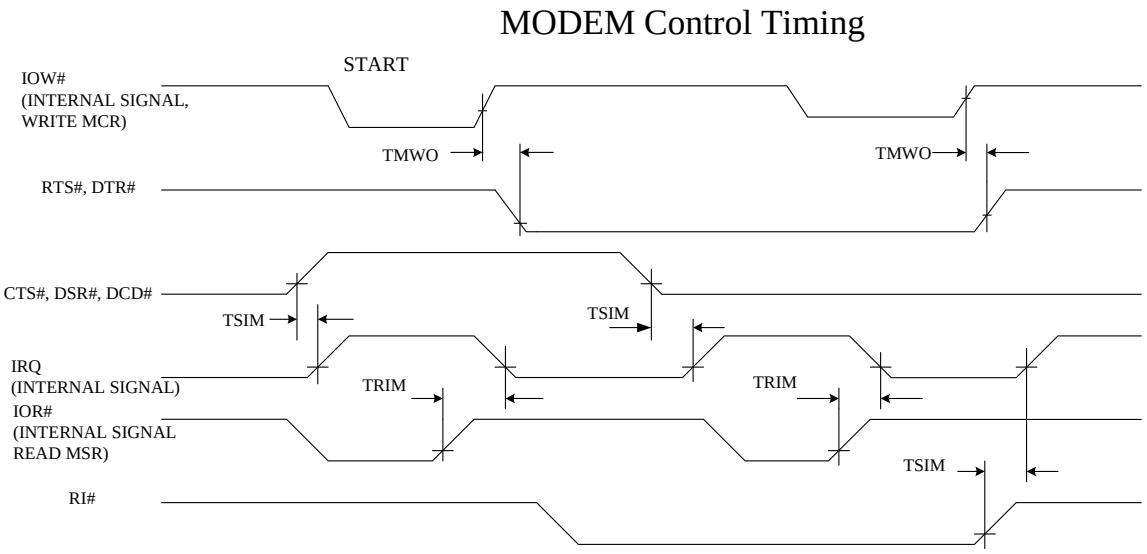


UART Transmitter Timing



14.3 Modem Control Timing

Modem Control Timing



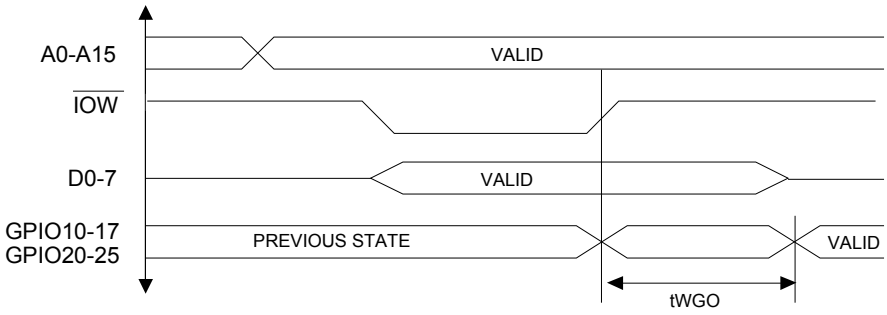
14.4 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec

Note: Refer to Microprocessor Interface Timing for Read Timing.

14.4.1 GPIO Write Timing

GPIO Write Timing diagram



15. TOP MARKING SPECIFICATIONS

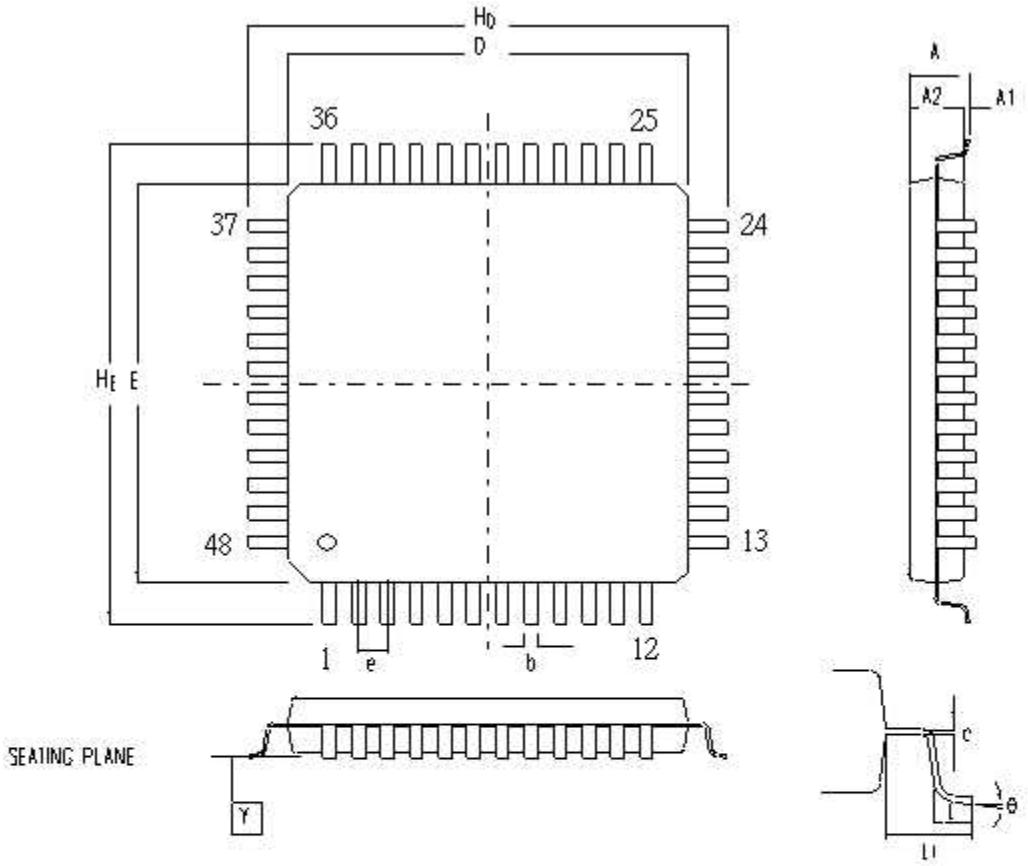
1st line: Nuvoton logo
2nd line: part number NCT5104D
3rd line: wafer production series lot number 2211B234
4th line: tracking code 206G9BFA

206: packages made in 2012, week 06
G: assembly house ID; G means GR, A means ASE, etc
9: code version; 9 means code 009
B: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use

16. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT5104D	48Pin LQFP (Green package)	**-40℃~+85℃**

17. PACKAGE SPECIFICATION



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

48-pin LQFP (7mm x 7mm)

18. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.0	02/03/2012	N.A.	First release to public

Important Notice

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