Precision Operational Amplifier, 25 μV Offset, Zero-Drift, 36 V Supply, 2 MHz

NCS21911, NCV21911, NCS21912, NCV21912, NCS21914, NCV21914

The NCS2191x family of high precision op amps feature low input offset voltage and near−zero drift over time and temperature. These op amps operate over a wide supply range from 4 V to 36 V with low quiescent current. The rail−to−rail output swings within 10 mV of the rails. The family includes the single channel NCS(V)21911, the dual channel NCS(V)21912, and the quad channel NCS(V)21914 in a variety of packages. All versions are specified for operation from −40°C to +125°C. Automotive qualified options are available under the NCV prefix.

Features

- Input Offset Voltage: ±25 μV max
- Zero−Drift Offset Voltage: ±0.085 μV/°C max
- Voltage Noise Density: 22 nV/√Hz typical
- Unity Gain Bandwidth: 2 MHz typical
- Supply Voltage: 4 V to 36 V
- Quiescent Current: 570 μA max
- Rail−to−Rail Output
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−free, Halogen free/BFR free and are RoHS compliant

Typical Applications

- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Current Sensing
- Automotive

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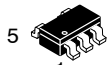
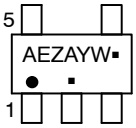
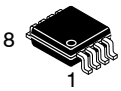
MARKING DIAGRAMS

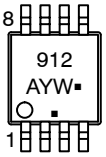


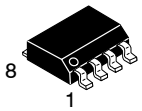
TSOP−5
CASE 483



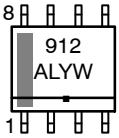


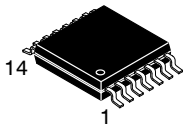
Micro8
CASE 846A−02



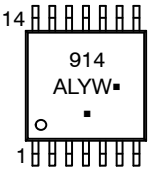


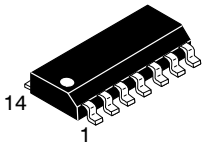
SOIC−8 NB
CASE 751−07



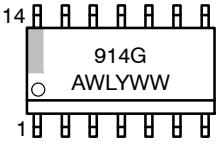


TSSOP−14 WB
CASE 948G





SOIC−14 NB
CASE 751A−03



XXXXX = Specific Device Code
A = Assembly Location
L or WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

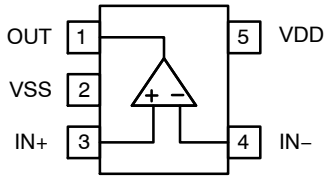
(Note: Microdot may be in either location)

ORDERING INFORMATION

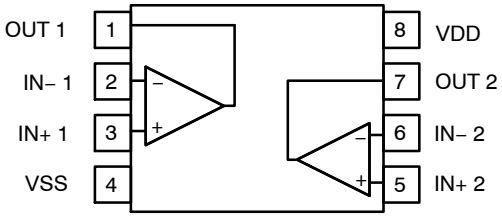
See detailed ordering and shipping information on page 2 of this data sheet.

PIN CONNECTIONS

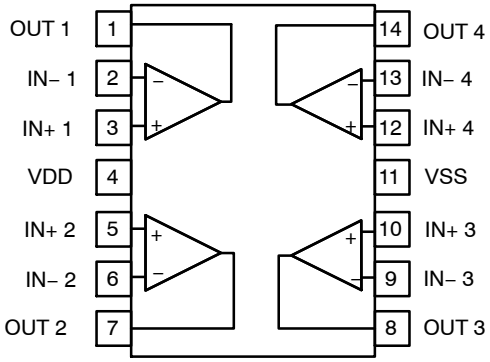
Single Channel Configuration
NCS21911



Dual Channel Configuration
NCS21912



Quad Channel Configuration
NCS21914



ORDERING INFORMATION

Channels	Device	Package	Shipping †
Single	NCS21911SN2T1G	SOT23–5 / TSOP–5	3000 / Tape & Reel
Dual	NCS21912DR2G	SOIC–8	2500 / Tape & Reel
	NCS21912DMR2G	MICRO–8	4000 / Tape & Reel
Quad	NCS21914DR2G	SOIC–14	2500 / Tape & Reel
	NCS21914DTBR2G	TSSOP–14	2500 / Tape & Reel
Automotive Qualified			
Channels	**Device**	**Package**	**Shipping †**
Single	NCV21911SN2T1G	SOT23–5 / TSOP–5	3000 / Tape & Reel
Dual	NCV21912DR2G	SOIC–8	2500 / Tape & Reel
	NCV21912DMR2G	MICRO–8	4000 / Tape & Reel
Quad	NCV21914DR2G	SOIC–14	2500 / Tape & Reel
	NCV21914DTBR2G	TSSOP–14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Supply Voltage (VDD− VSS)	40	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	VSS − 0.3 to VDD + 0.3	V
Differential Input Voltage (Note 2)	±17	V
Input Current (Notes 1 and 2)	±10	mA
Output Short Circuit Current (Note 3)	Continuous	mA
TEMPERATURE		
Operating Temperature	−40 to +125	°C
Storage Temperature	−65 to +150	°C
Junction Temperature	+150	°C
ESD RATINGS (Note 4)		
Human Body Model (HBM)	3000	V
Charged Device Model (CDM)	2000	V
OTHER RATINGS		
Latch−up Current (Note 5)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input terminals are diode−clamped to the power−supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
2. The inputs are diode connected with a total input protection of 1.65 kΩ, increasing the absolute maximum differential voltage to ±17 V_{DC}. If the applied differential voltage is expected to exceed this rating, external resistors should be added in series with the inputs to limit the input current to ±10 mA.
3. Short−circuit to V_{DD} or V_{SS}. Short circuits to either rail can cause an increase in the junction temperature. The total power dissipation must be limited to prevent the junction temperature from exceeding the 150°C limit.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017 (AEC−Q100−002)
   ESD Charged Device Model tested per JEDEC standard JS−002−2014 (AEC−Q100−011)
5. Latch−up Current tested per JEDEC standard JESD78E (AEC−Q100−004).

THERMAL INFORMATION (Note 6)

Rating	Symbol	Package	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	TSOP−5 / SOT23−5	170	°C/W
		Micro8/MSOP8	116	
		SOIC−8	87	
		SOIC−14	59	
		TSSOP−14	78	

6. As mounted on an 80x80x1.5 mm FR4 PCB with 2S2P, 2 oz copper, and a 200 mm^2 heat spreader area. Following JEDEC JESD51−7 guidelines.

OPERATING CONDITIONS

Parameter	Symbol	Range	Unit
Supply Voltage (V_{DD} − V_{SS})	V_S	4 to 36	V
Specified Operating Temperature Range	T_A	−40 to 125	°C
Input Common Mode Voltage Range	V_{CM}	V_{SS} to V_{DD}−1.5	V
Differential Voltage (Note 7)	V_{DIFF}	±17	V

7. The inputs are diode connected with a total input protection of 1.65 kΩ, increasing the absolute maximum differential voltage to ±17 V_{DC}. If the applied differential voltage is expected to exceed this rating, external resistors should be added in series with the inputs to limit the input current to ±10 mA.

ELECTRICAL CHARACTERISTICS V_S = 4 V to 36 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}				±1	±25	μV
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$				**±0.02**	**±0.085**	μV/°C
Input Bias Current (Note 8)	I_{IB}				±100	±500	pA
						±3500	pA
Input Offset Current (Note 8)	I_{OS}				±200	±500	pA
						±3500	pA
Common Mode Rejection Ratio	CMRR	$V_{SS} \le V_{CM} \le V_{DD}-1.5$ V	V_S = 36 V	140	150		dB
				130			
			V_S = 12 V (Note 8)	130	150		
				120			
			V_S = 8 V (Note 8)	130	140		
				120			
			V_S = 4 V	120	130		
				110			
Input Capacitance	C_{IN}	Common Mode			3		pF
EMI Rejection Ratio	EMIRR	f = 5 GHz			100		dB
		f = 400 MHz			80		
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	A_{VOL}	V_{SS} + 0.5 V < V_O < V_{DD} – 0.5 V		130	150		dB
				125	**135**		
Open Loop Output Impedance	Z_{OUT_OL}	No Load			See Figure 23		Ω
Output Voltage High, Referenced to Rail	V_{OH}	No Load			5	10	mV
		R_L = 10 kΩ			100	210	
					140	**250**	
Output Voltage Low, Referenced to Rail	V_{OL}	No Load			5	10	mV
		R_L = 10 kΩ			100	210	
					140	**250**	
Short Circuit Current	I_{SC}	Sinking Current			18		mA
		Sourcing Current			16		
Capacitive Load Drive	C_L				1		nF
DYNAMIC PERFORMANCE							
Gain Bandwidth Product	GBW	C_L = 100 pF			2		MHz
Gain Margin	A_M	C_L = 100 pF			13		dB
Phase Margin	φ_M	C_L = 100 pF			55		°
Slew Rate	SR	G = +1			1.6		V/μs
Settling Time	t_S	V_S = 36 V	0.1%		20		μs
			0.01%		45		μs
Overload Recovery Time	t_{OR}	V_S = ±18 V, A_V = –10, V_{IN} = ±2.5 V			1		μs

8. Guaranteed by characterization and/or design.

ELECTRICAL CHARACTERISTICS V_S = 4 V to 36 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1 kHz, A_V = 1, V_{OUT} = 1 Vrms		0.0003		%
Voltage Noise Density	e_N	f = 1 kHz		22		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		100		fA/√Hz
Voltage Noise, Peak−to−Peak	e_{PP}	f = 0.1 Hz to 10 Hz		400		nV_{PP}
Voltage Noise, RMS	e_{rms}	f = 0.1 Hz to 10 Hz		70		nV_{rms}
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 36 V		**0.02**	**0.3**	μV/V
			130	**154**		dB
Quiescent Current	I_Q	Per channel		475	570	μA
					570	

GRAPHS

Typical performance at T_A = 25°C, unless otherwise noted.

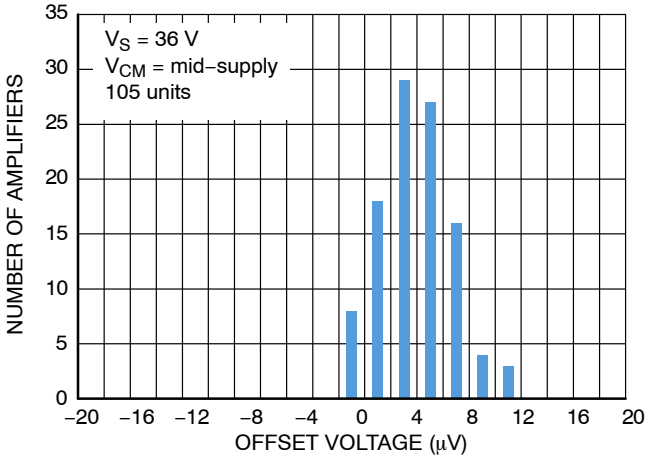


Figure 1. Offset Voltage Distribution

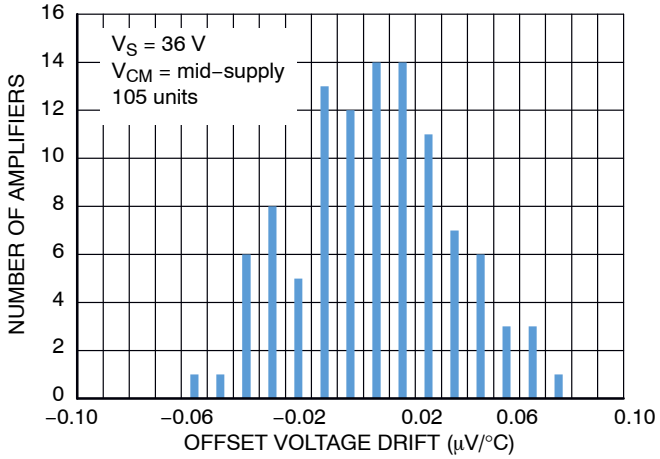


Figure 2. Offset Voltage Drift Distribution

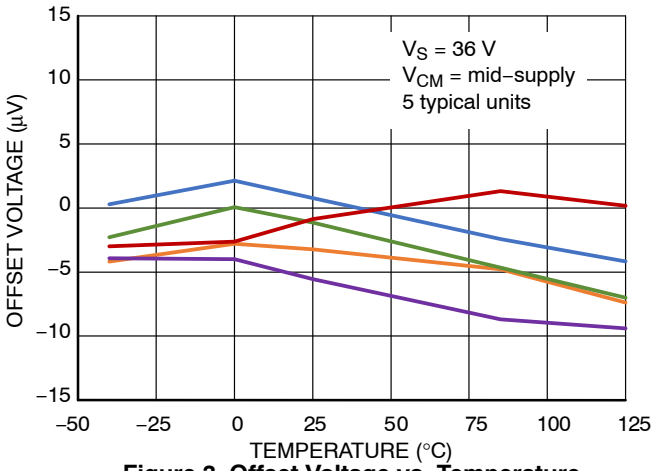


Figure 3. Offset Voltage vs. Temperature

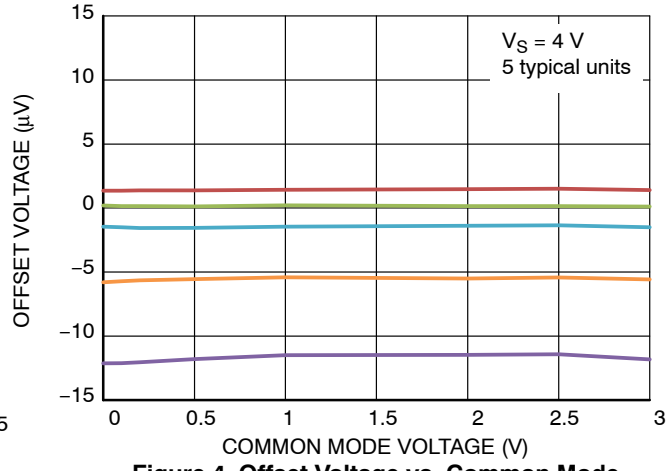


Figure 4. Offset Voltage vs. Common Mode Voltage

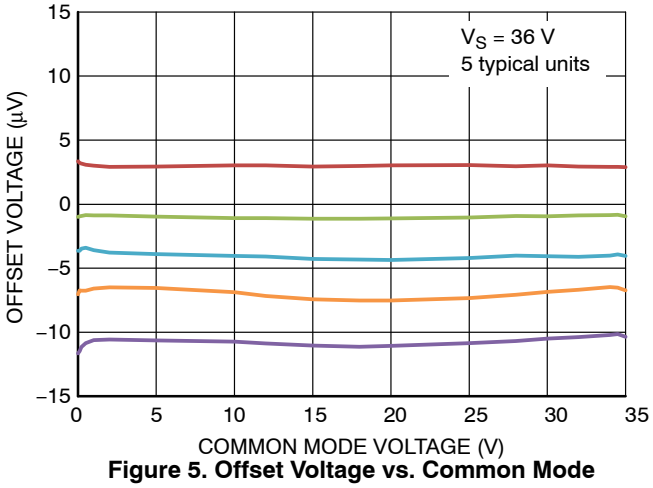


Figure 5. Offset Voltage vs. Common Mode Voltage

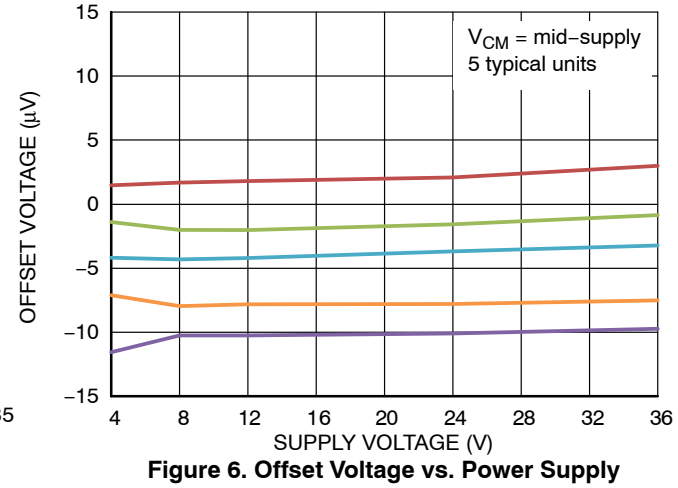


Figure 6. Offset Voltage vs. Power Supply

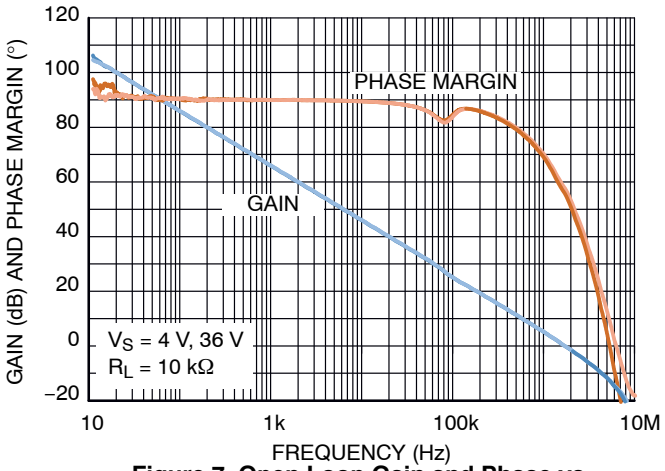


Figure 7. Open Loop Gain and Phase vs. Frequency

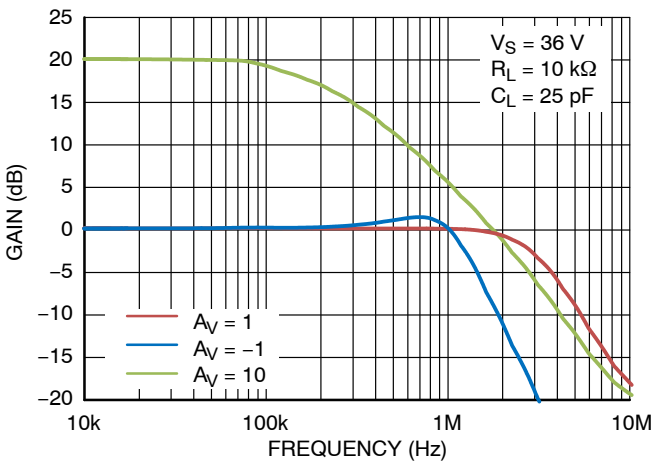


Figure 8. Closed Loop Gain vs. Frequency

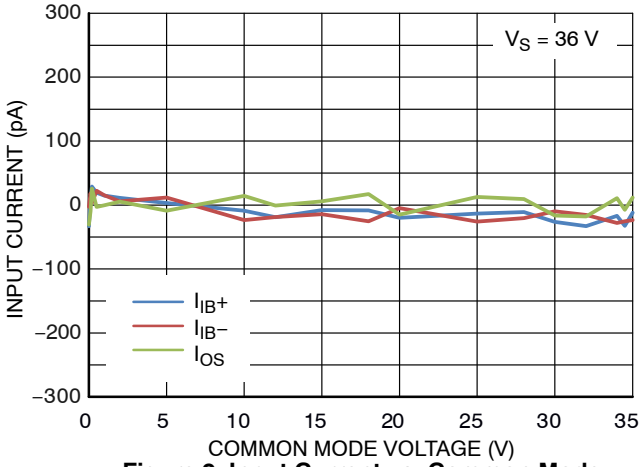


Figure 9. Input Current vs. Common Mode Voltage

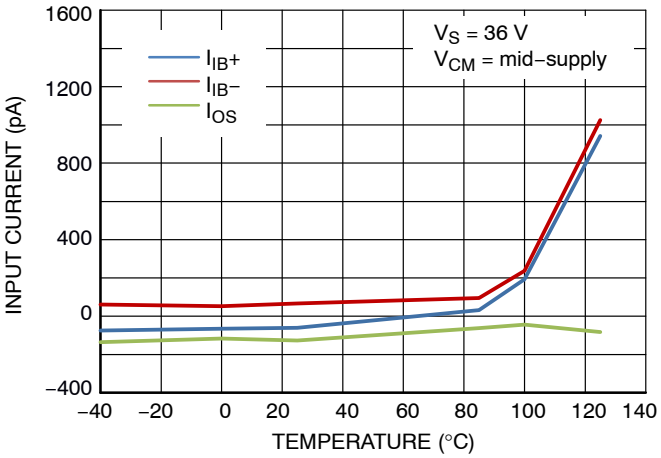


Figure 10. Input Current vs. Temperature

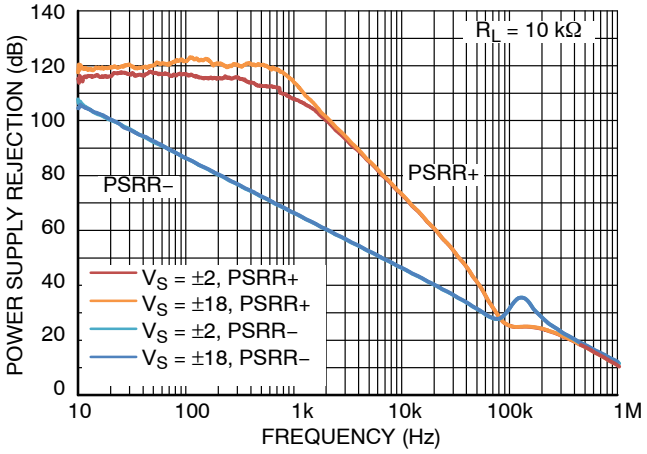


Figure 11. PSRR vs. Frequency

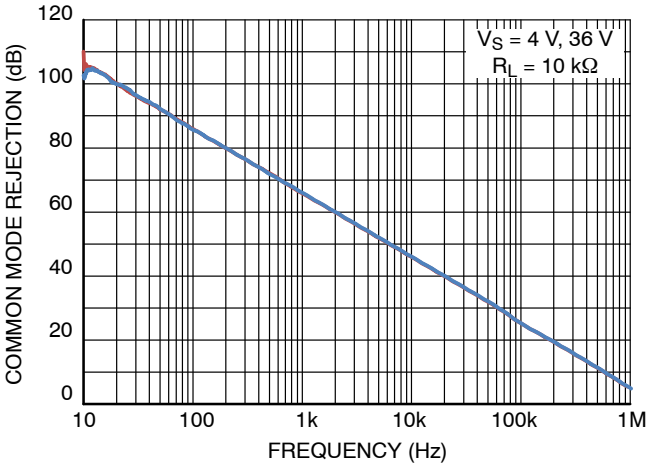


Figure 12. CMRR vs. Frequency

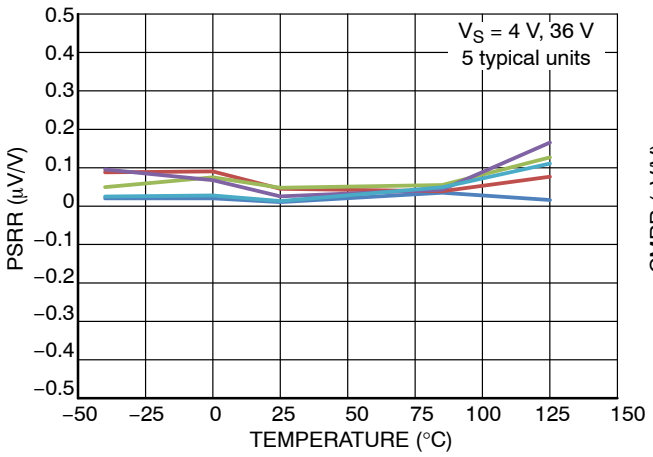


Figure 13. PSRR vs. Temperature

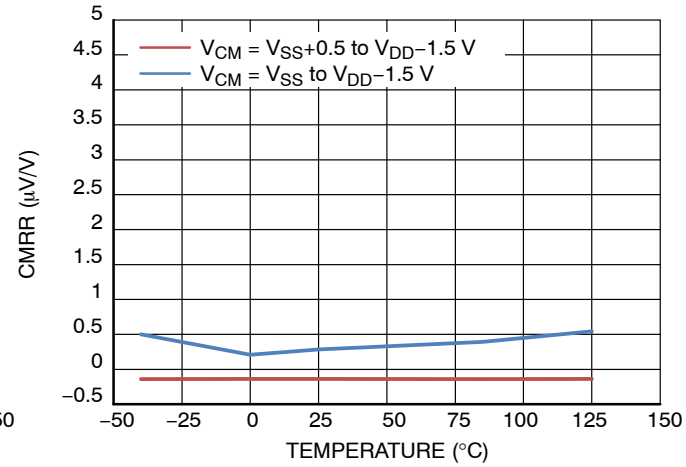


Figure 14. CMRR vs. Temperature at V_S = 4 V

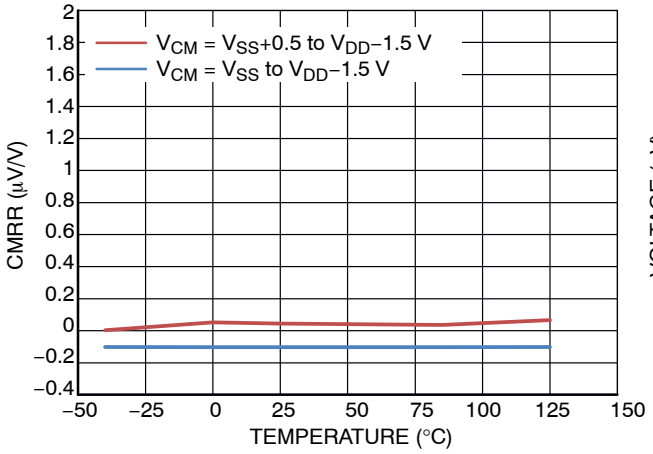


Figure 15. CMRR vs. Temperature at V_S = 36 V

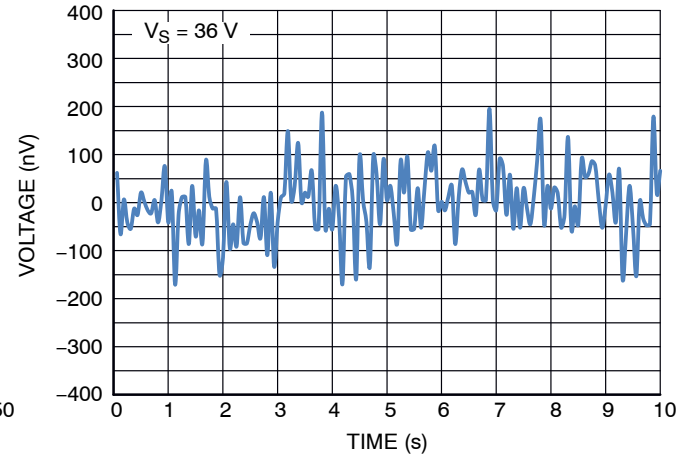


Figure 16. 0.1 Hz to 10 Hz Noise

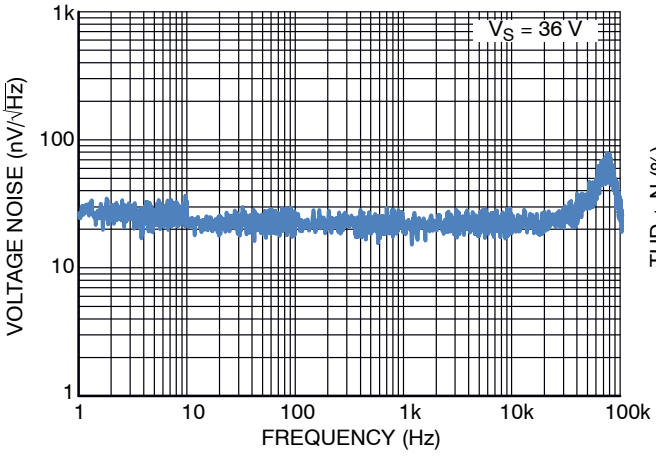


Figure 17. Voltage Noise Density vs. Frequency

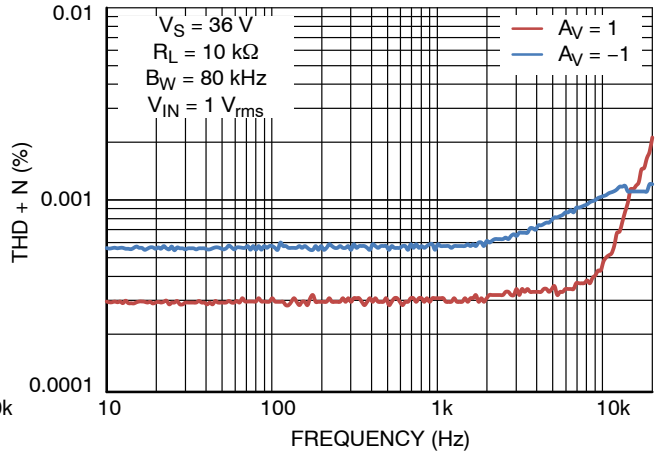


Figure 18. THD+N vs. Frequency

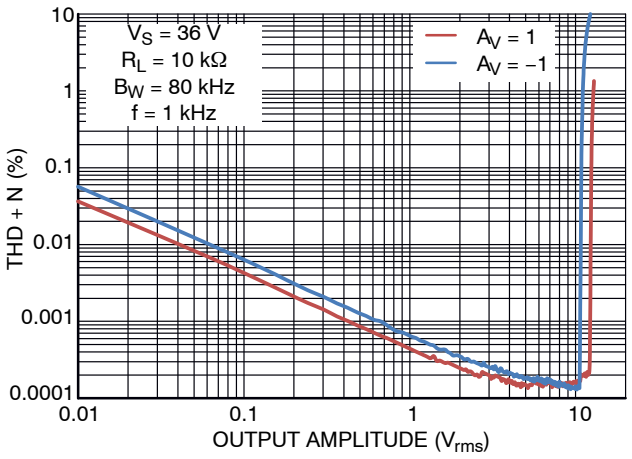


Figure 19. THD+N vs. Output Amplitude

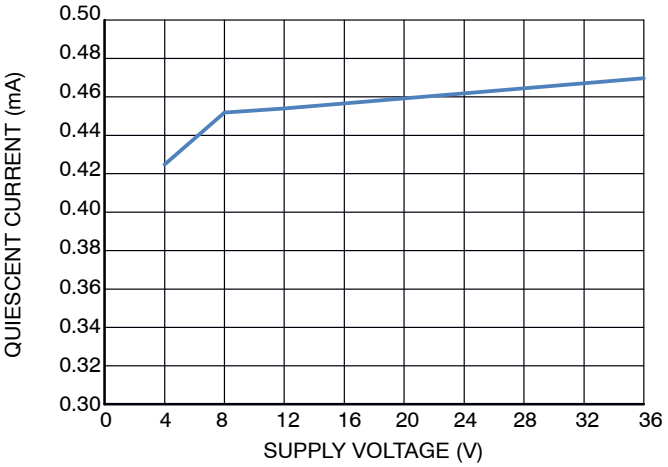


Figure 20. Quiescent Current vs. Supply Voltage

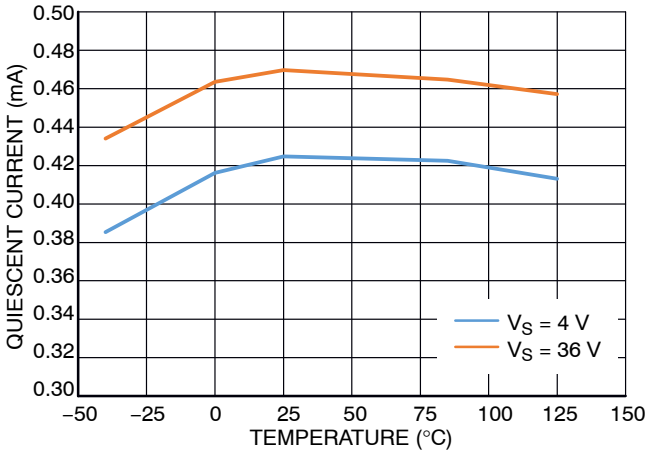


Figure 21. Quiescent Current vs. Temperature

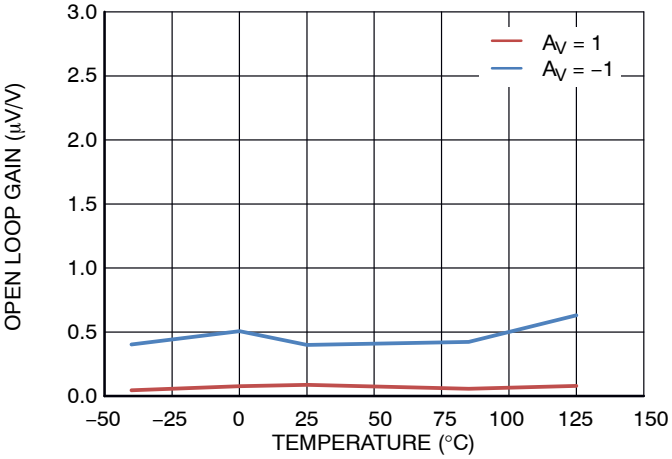


Figure 22. Open Loop Gain vs. Temperature

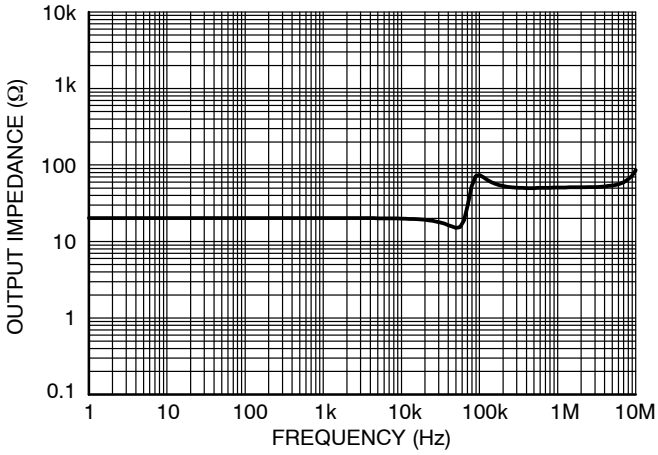


Figure 23. Open Loop Output Impedance vs. Frequency

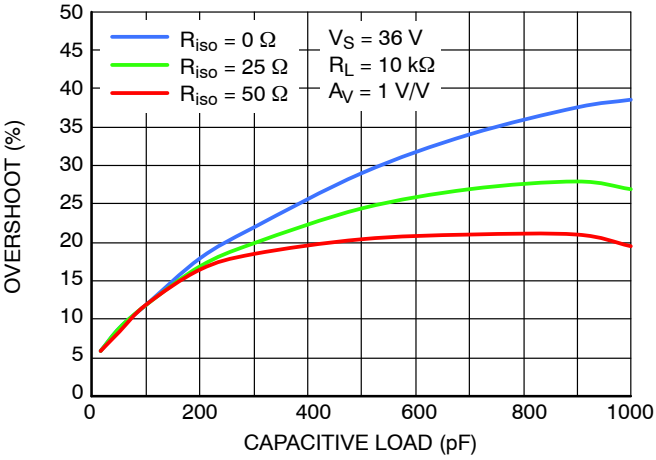


Figure 24. Small Signal Overshoot vs. Capacitive Load (100 mV Output Step)

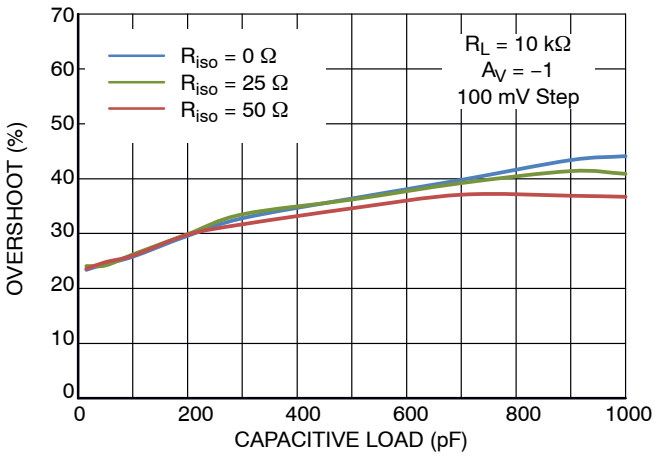


Figure 25. Small Signal Overshoot vs. Capacitive Load (100 mV Output Step)

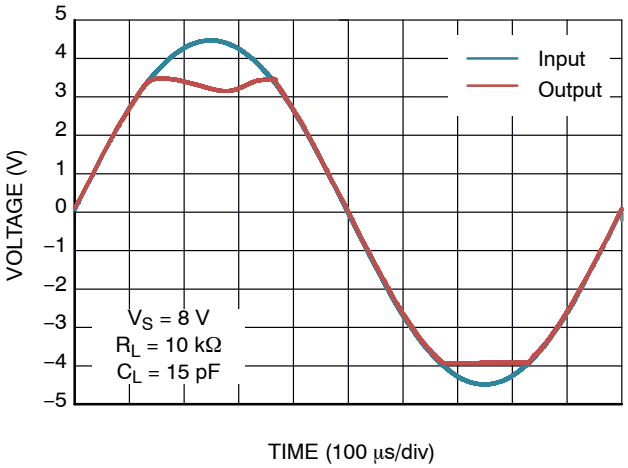


Figure 26. No Phase Reversal

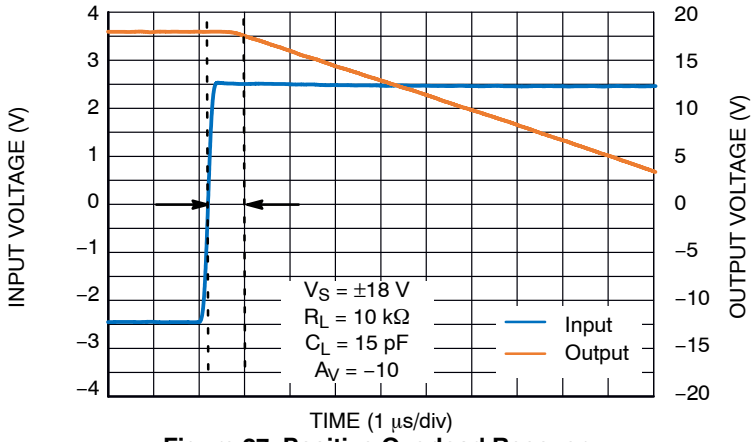


Figure 27. Positive Overload Recovery

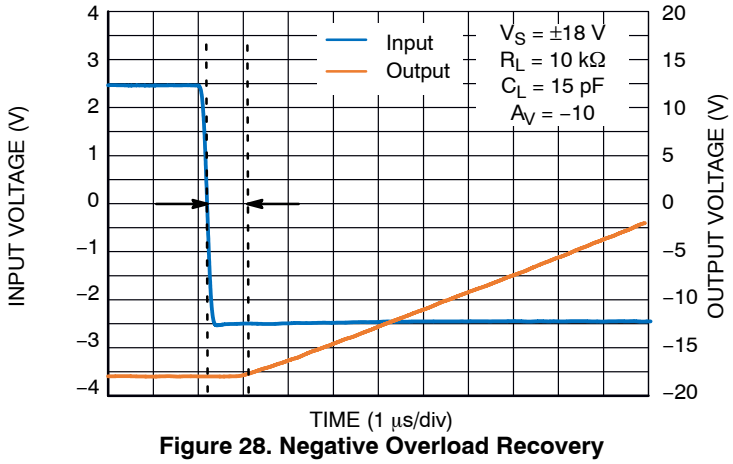


Figure 28. Negative Overload Recovery

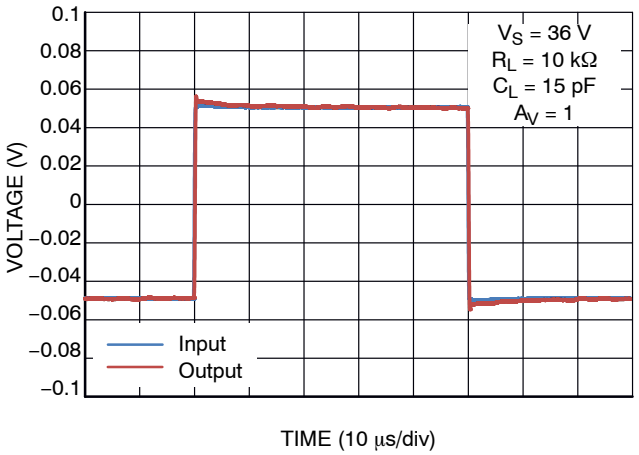


Figure 29. Non−Inverting Small Signal Step Response

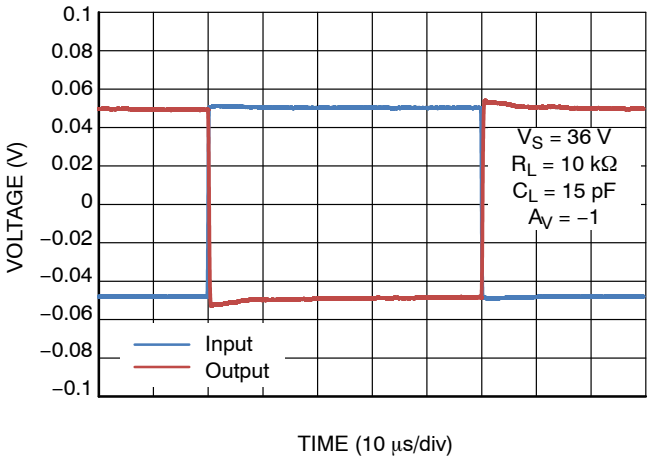


Figure 30. Inverting Small Signal Step Response

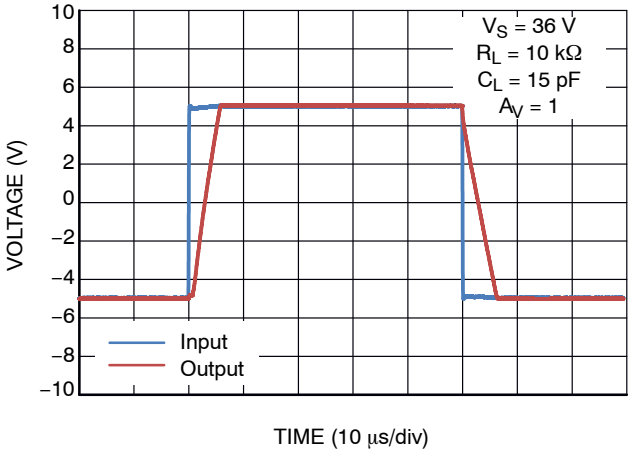


Figure 31. Non−Inverting Large Signal Step Response

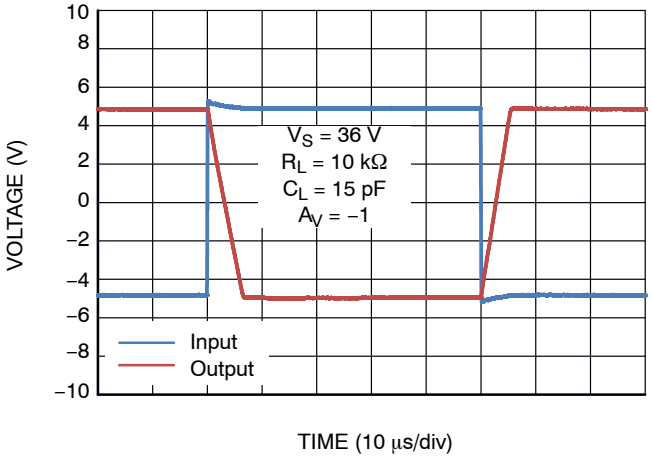


Figure 32. Inverting Large Signal Step Response

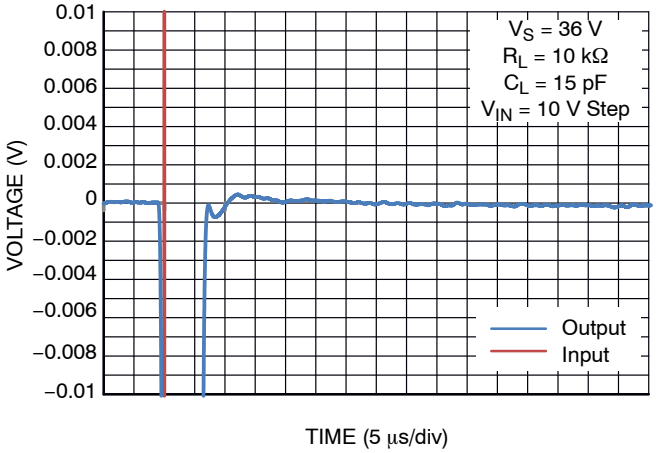


Figure 33. Large Signal Settling Time, Low−to−High

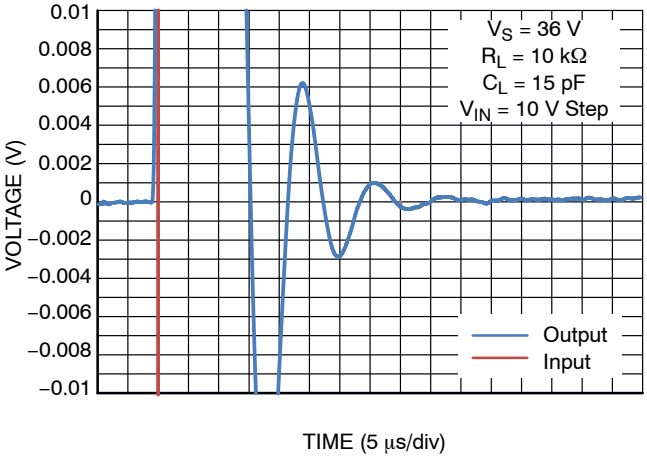


Figure 34. Large Signal Settling Time, High−to−Low

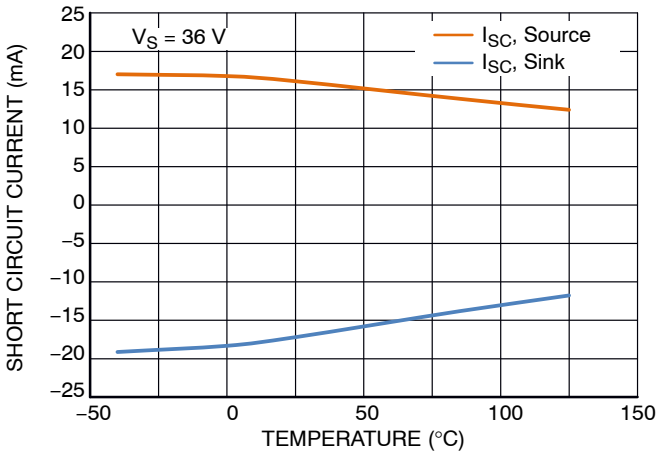


Figure 35. Short Circuit Current vs. Temperature

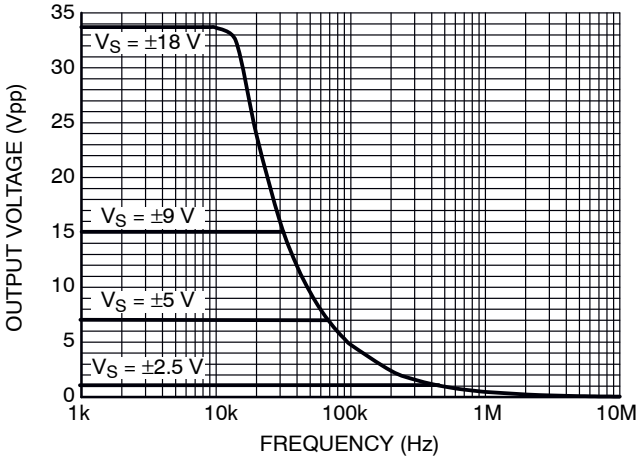


Figure 36. Maximum Output Voltage vs. Frequency (A_V = 1 for V_S = ±2.5 V, ±5 V, ±9 V; A_V = 2 for V_S = ±18 V)

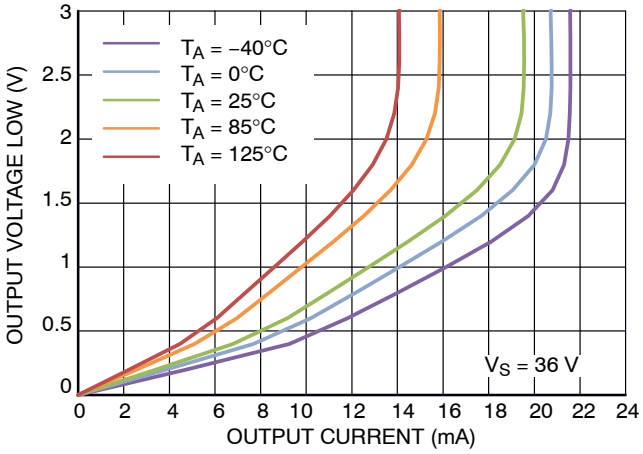


Figure 37. Output Voltage Low vs. Output Current

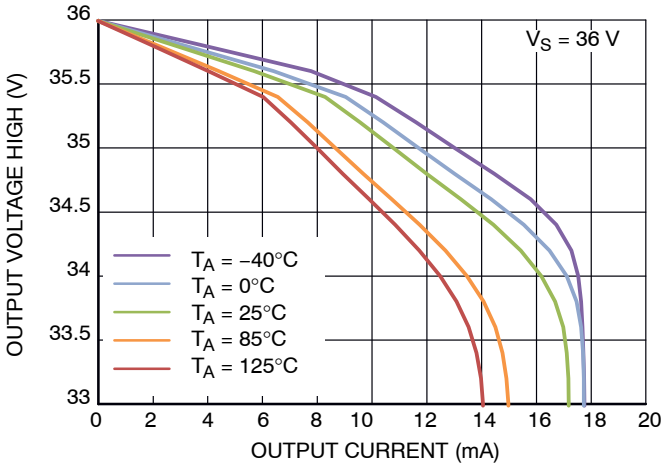


Figure 38. Output Voltage High vs. Output Current

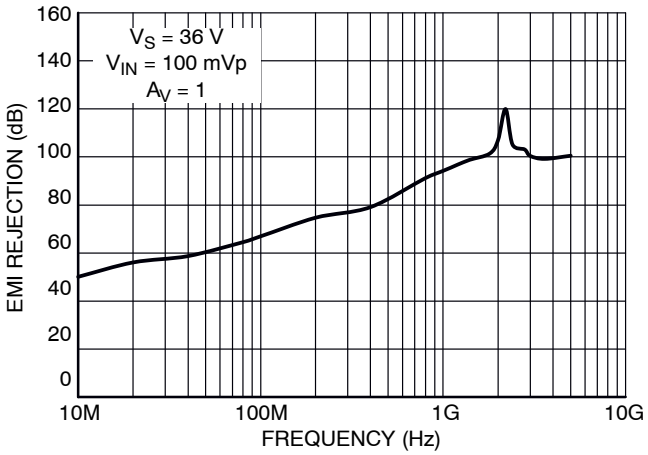


Figure 39. EMIRR IN+ vs. Frequency

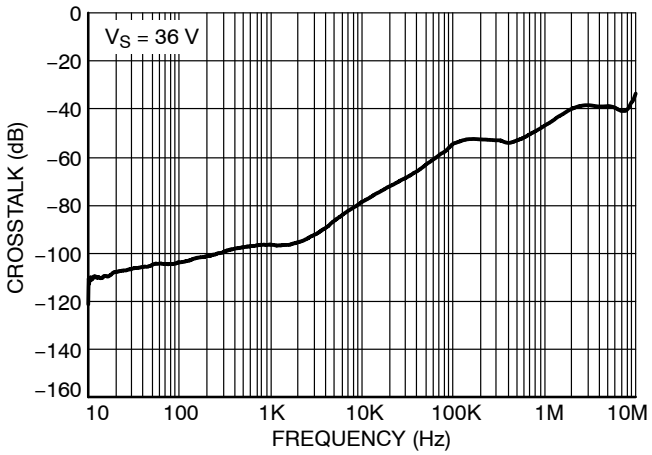


Figure 40. Channel−to−Channel Crosstalk

APPLICATION INFORMATION

Overview

The NCS21911, NCS21912, and NCS21914 precision op amps provide low offset voltage and zero drift over temperature. With a maximum offset voltage of 25 μV and input common mode voltage range that includes ground, the NCS21911 series is well−suited for applications where precision is required, such as low side current sensing and interfacing with sensors.

The NCS21911 series of amplifiers uses a chopper−stabilized architecture, which provides the advantage of minimizing offset voltage drift over temperature and time. The simplified block diagram is shown in Figure 41. Unlike the classical chopper architecture, the chopper stabilized architecture has two signal paths.

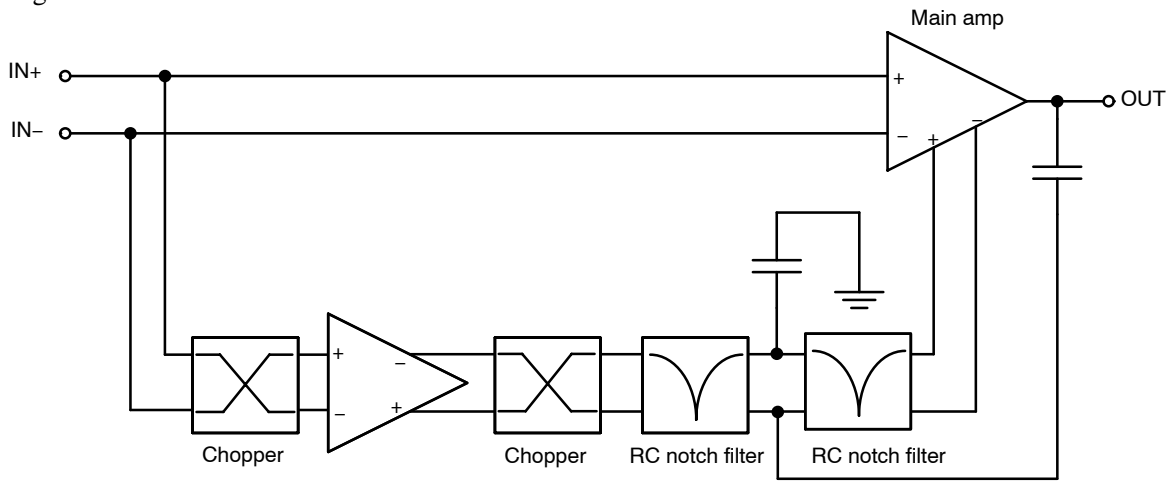


Figure 41. Simplified NCS21911 Block Diagram

In Figure 41, the lower signal path is where the chopper samples the input offset voltage, which is then used to correct the offset at the output. The offset correction occurs at a frequency of 250 kHz. The chopper−stabilized architecture is optimized for best performance at frequencies up to the related Nyquist frequency (1/2 of the offset correction frequency). As the signal frequency exceeds the Nyquist frequency, 125 kHz, aliasing may occur at the output. This is an inherent limitation of all chopper and chopper−stabilized architectures. Nevertheless, the NCS21911 series op amps have minimal aliasing up to 200 kHz and are less susceptible to aliasing effects when compared to competitor parts from other manufacturers. ON Semiconductor's patented approach utilizes two cascaded, symmetrical, RC notch filters tuned to the chopper frequency and its fifth harmonic to reduce aliasing effects.

The chopper−stabilized architecture also benefits from the feed−forward path, which is shown as the upper signal path of the block diagram in Figure 41. This is the high speed signal path that extends the gain bandwidth up to 2 MHz. Not only does this help retain high frequency components of the input signal, but it also improves the loop gain at low frequencies. This is especially useful for low−side current sensing and sensor interface applications where the signal is low frequency and the differential voltage is relatively small.

Application Circuits

Low−Side Current Sensing

Low−side current sensing is used to monitor the current through a load. This method can be used to detect over−current conditions and is often used in feedback control, as shown in Figure 42. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

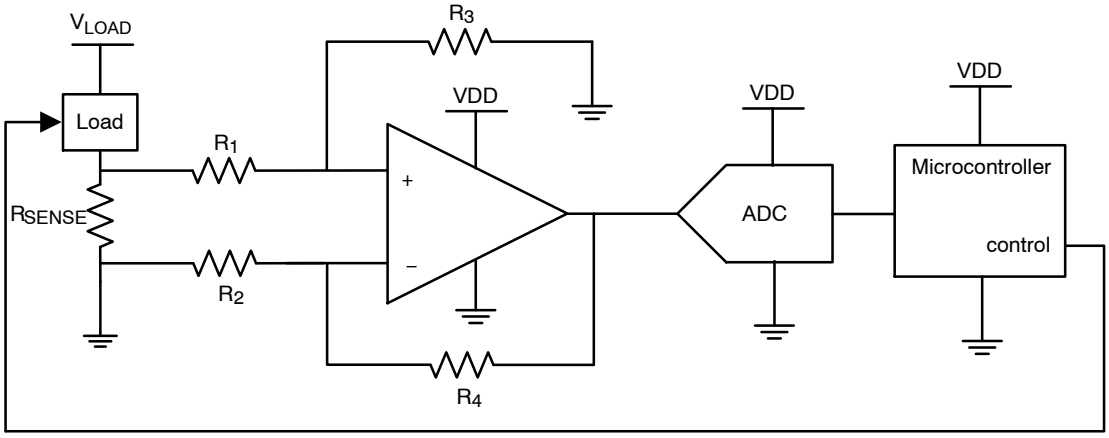


Figure 42. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 43. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

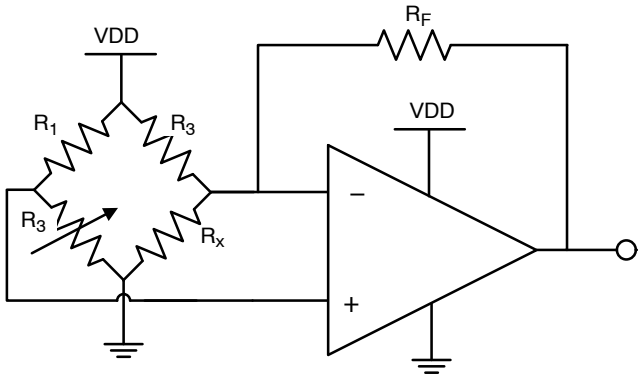


Figure 43. Wheatstone Bridge Circuit Amplification

EMI Susceptibility and Input Filtering

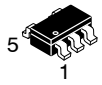
Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI−induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS2191x integrates low−pass filters to decrease its sensitivity to EMI. Figure 39 shows the EMIRR performance.

General Layout Guidelines

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric coefficients and prevent temperature gradients from heat sources or cooling fans.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

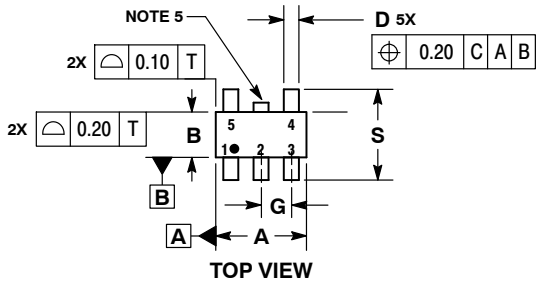
ON Semiconductor®



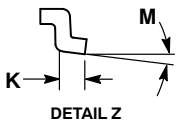
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

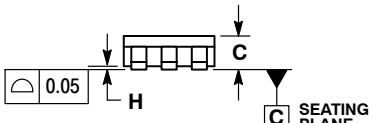
DATE 12 AUG 2020



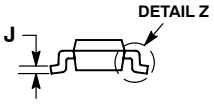
TOP VIEW



DETAIL Z



SIDE VIEW

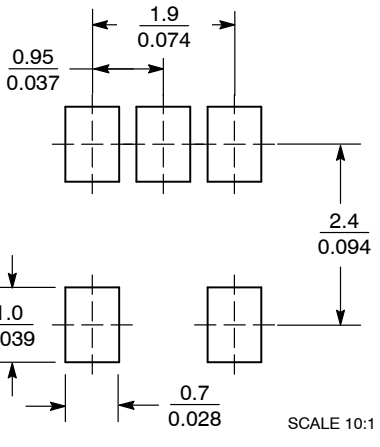


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

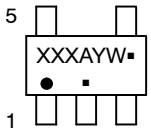
SOLDERING FOOTPRINT*



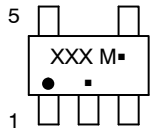
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

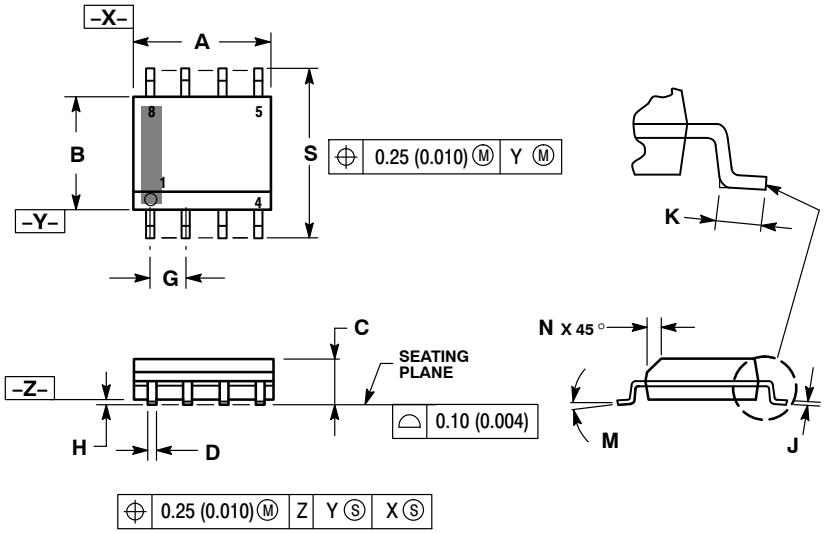
DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−5	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

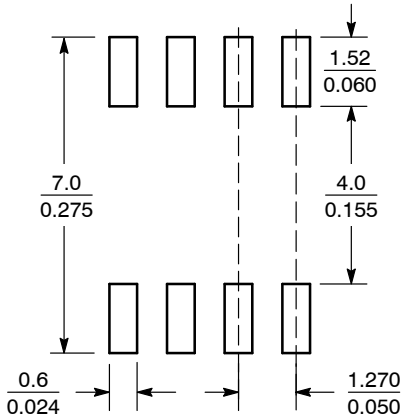
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

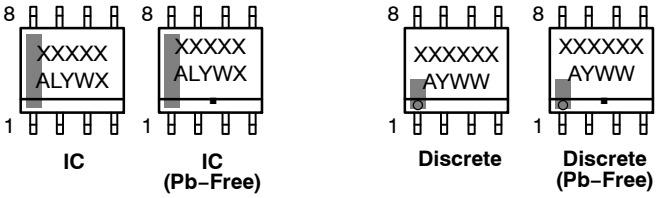
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

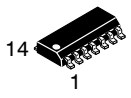
STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

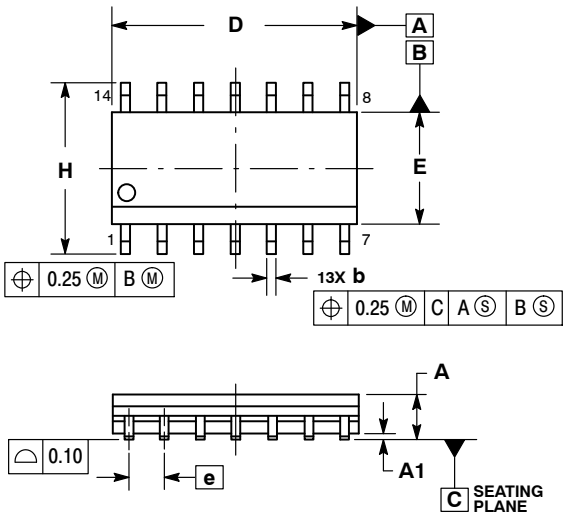
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

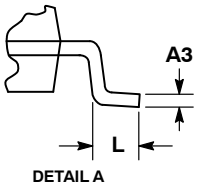


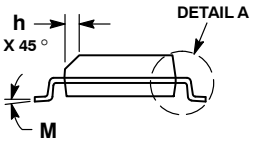
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



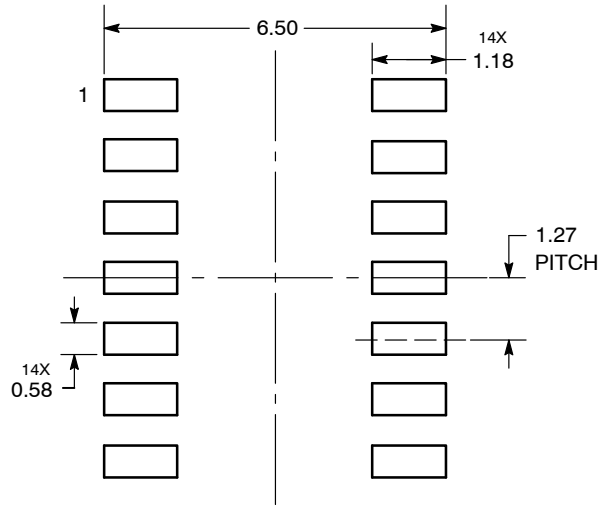




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

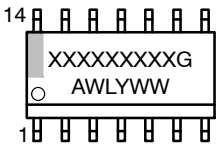
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

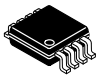
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

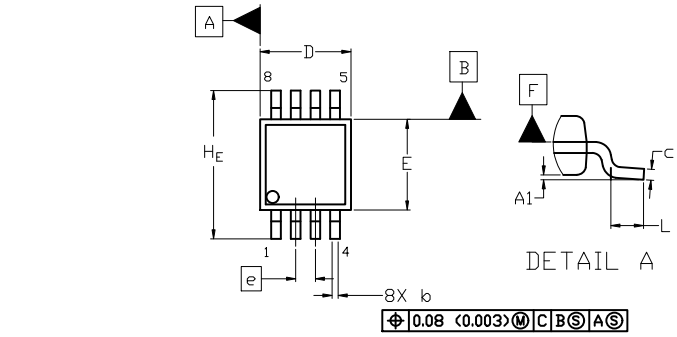
ON Semiconductor®

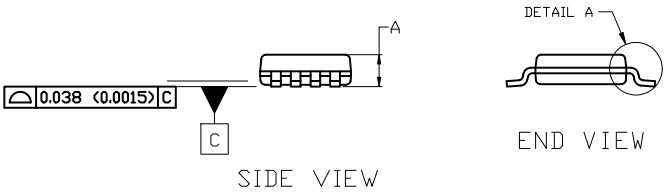


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

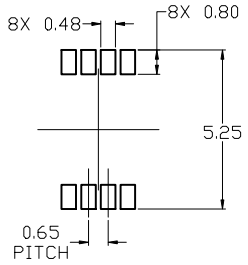
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

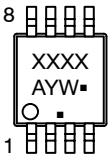


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

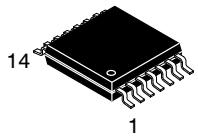
STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

DOCUMENT NUMBER:	**98ASB14087C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

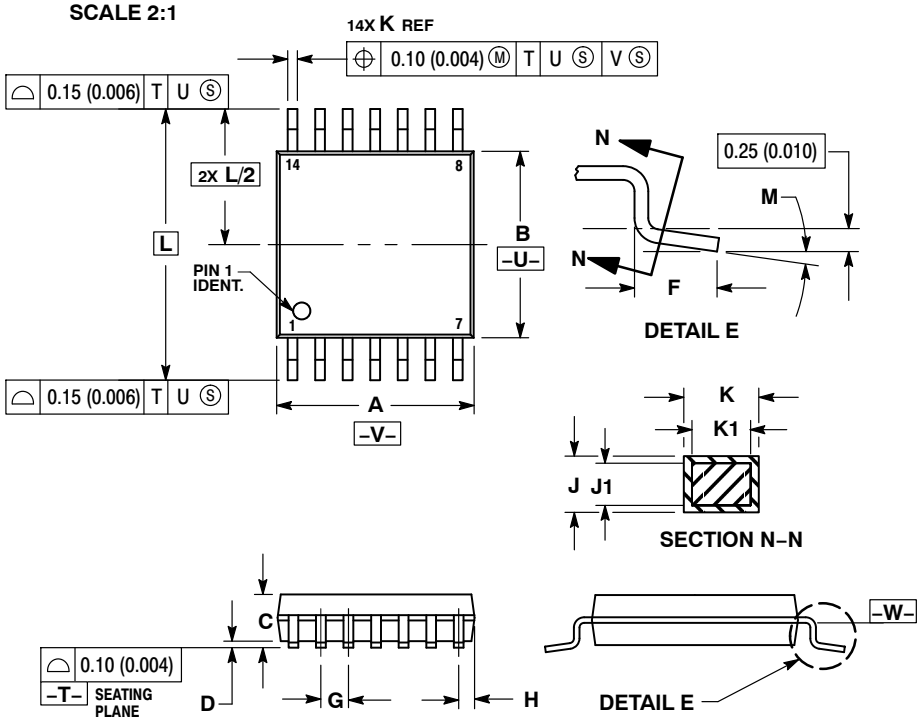
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



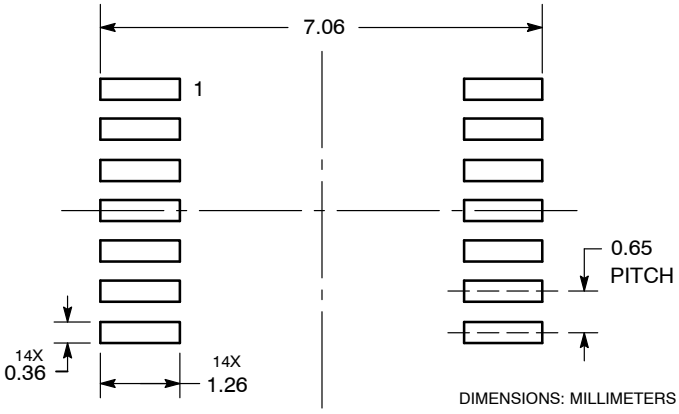
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

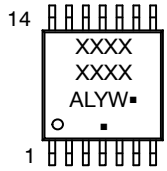
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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