NCP6992A, NCV6992A

Wireless Power Transmitter ASIC

The NCP6992A is a Wireless Power Transmitter ASIC that provides power, measurement and supporting functions required for AIRFUEL™-MR-compliant Power Transmitting Unit (PTU). Using an I^2C series link, the NCP6992A interfaces a control processor with a boost converter, a power amplifier, its matching circuit and power transmitting resonator. Coupled to the Bluetooth® Low Energy (BLE) signaling protocol embedded in the control processor, the NCP6992A adjusts and optimizes the power applied to the transmitter coil by managing power transfer including efficiency as well as monitoring fault conditions. The NCP6992 has been designed for scalable power covering Class 2 (10 W) up to Class 5 (50 W) types of transmitters. The NCV6992A is the automotive release of this Wireless Power Transmitter ASIC.

Features

- Input Voltage Range from 4.5 V to 22 V (AV_{IN} & PV_{IN})
  - Direct Supply from Wall Adapter or USB-Type Port
- 50-W PA Boost Controller Featuring Converter Programmable from 9 V to 55.2 V in 200 mV Steps with Over-Voltage Protection and Automatic Control Input Option Featuring Continuous and Window Control Modes.
- Fixed-5 V & 500 mA Output, Fully Integrated System Buck Converter
- System LDO, Programmable from 1.2 V to 3.6 V in 100 mV steps with Dynamic Voltage Scaling (DVS)
- Four Phase Selectable 6.78 MHz PA Drivers with Over-Current Protection
- 10-Bit ADC for PA Supply Voltage, Current & Temperature Measurements
- Differential AC Power Measurement Circuit with ADC Reading
- 3 Full-Bridge Peak Detectors with 6-Bit Programmable Thresholds and Fault Handling
- 3 Impedance Control Drivers and One Impedance Control Detector
- PWM Controlled Relay Driver for Antenna Switching
- 2 Programmable LED Drivers w/ Blinking and Protection
- Frontend for USB BC 1.2 Detection and QC 2.0/QC 3.0 Control Capability
- Integrated 27.12 MHz Crystal Oscillator Driver
- 2 Versatile GPIO Usable for Logic I/O, ADC Input or Clock Output.
- Configurable Sleep Mode and Fast Wakeup Cycling with Direct Input Control
- Widely programmable through 3.4-MHz I^2C Interface
- Available in a Small 7 × 7 mm^2 Wettable Flank Plated QFN−56 at Pitch 0.4 mm
- AEC−Q100 Qualified (Grade 3) and PPAP Capable

Typical Applications

- AIRFUEL-MR (Magnetic Resonance) Compliant (A4WP/Rezence™) for Wireless Charging Pad or Charging Station

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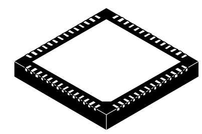
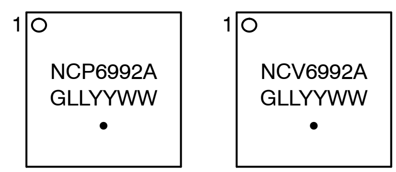


QFN56 7×7, 0.4P
CASE 485BT

MARKING DIAGRAM



G	= Assembly Location
LL	= Lot Trace Code
YY	= Year
WW	= Work Week

Pb-Free indicator, microdot (•), may or may not be present

ORDERING INFORMATION

See detailed ordering and shipping information on page 85 of this data sheet.

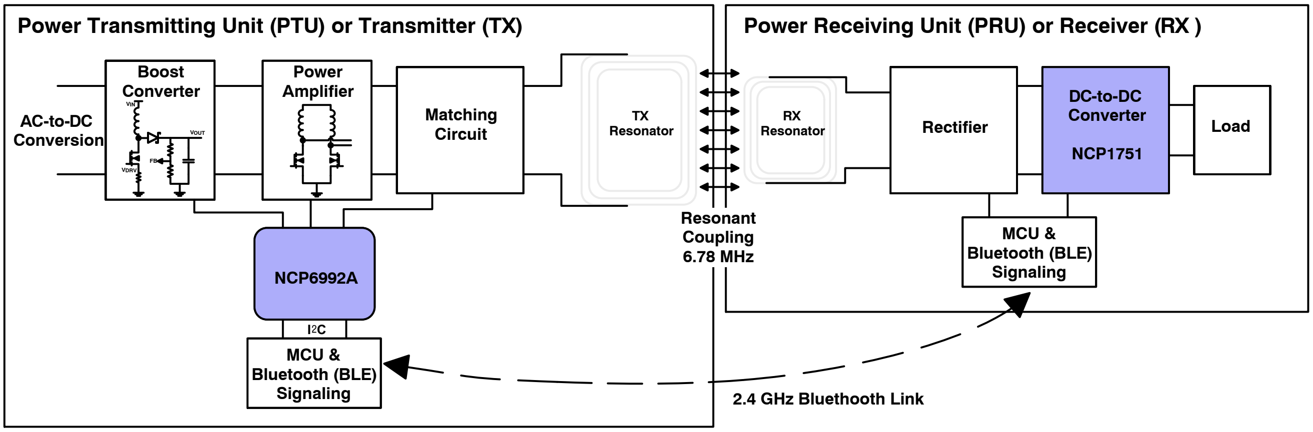


Figure 1. Typical Application

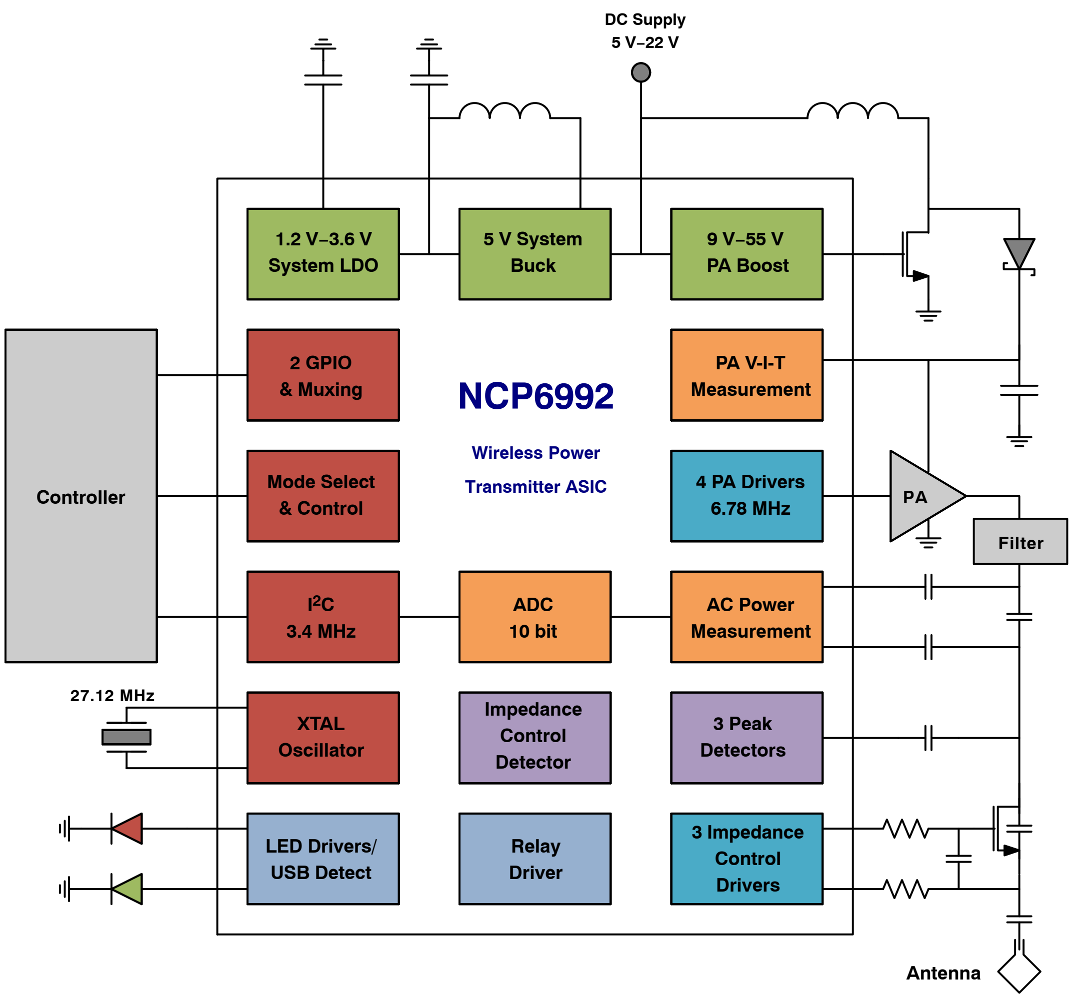


Figure 2. Block Diagram

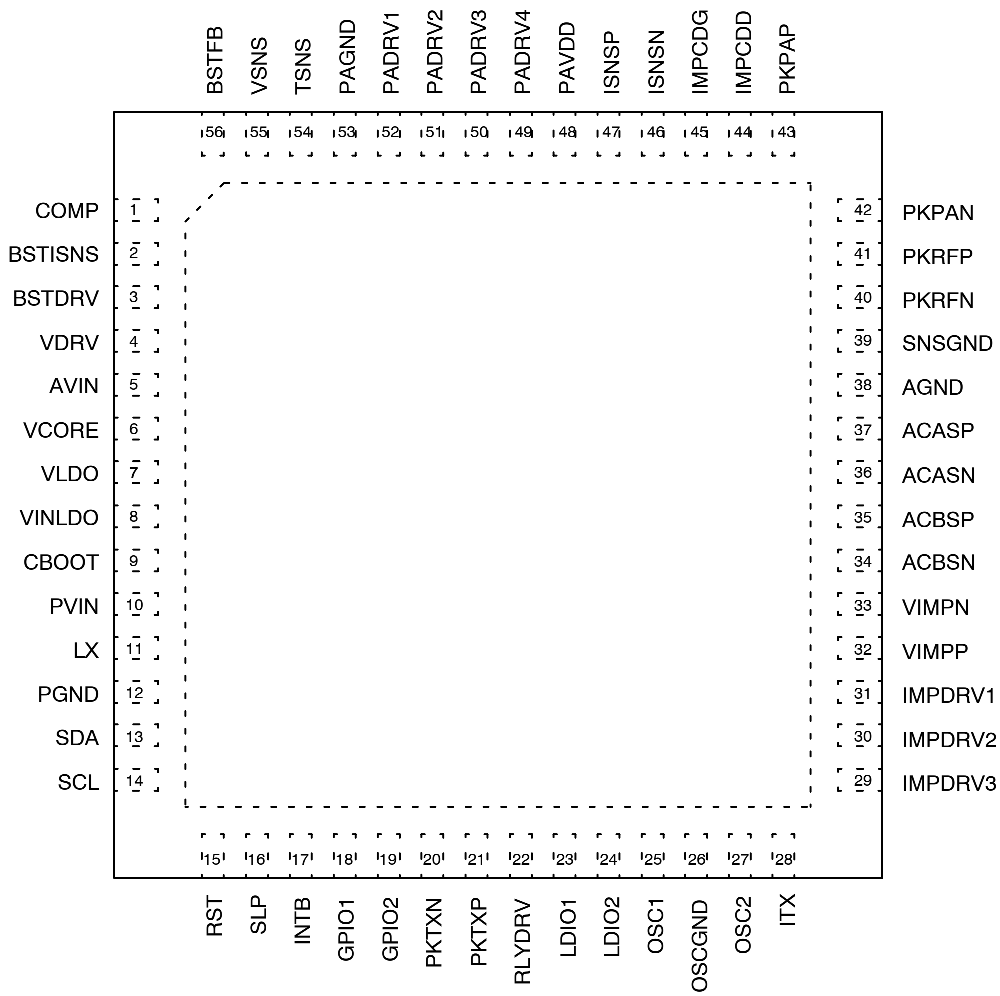


Figure 3. Package Pinout – QFN−56

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
CORE SUPPLY			
4	VDRV	Power	Supply for Drivers
5	AVIN	Power	IC Core Input Supply
6	VCORE	Power	IC Core Supply
38	AGND	Ground	Small Signal Ground
CRYSTAL OSCILLATOR			
25	OSC1	–	1. Crystal Oscillator Connection 1 2. Or External Clock Input
26	OSCGND	Ground	Crystal Oscillator Ground
27	OSC2	Input	1. Crystal Oscillator Connection 2 2. Or Connected to OSCGND if External Clock Input
CONTROL			
13	SDA	Input/Output	I^2C Data Line
14	SCL	Input	I^2C Clock Line
15	RST	Input	Reset Input
16	SLP	Input	Sleep Mode Select Input
17	INTB	Output	Interrupt Output

Table 1. PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Type	Description
GPIOS			
18	GPIO1	Input/Output	General Purpose Input/Output 1
19	GPIO2	Input/Output	General Purpose Input/Output 2
SYSTEM SUPPLIES			
7	VLDO	Power	Linear Regulator Output
8	VINLDO	Power	1. Linear Regulator Supply Input 2. Buck Converter Output/Feedback
9	CBOOT	–	Bootstrap Capacitor Connection
10	PVIN	Power	Power Supply Input
11	LX	–	Buck Converter Switching Node
12	PGND	Ground	Power Ground
PA BOOST CONVERTER			
1	COMP	Input	Boost Converter Compensation Network
2	BSTISNS	Input	Boost Converter Current Sense
3	BSTDRV	Output	Boost Converter Low Side Driver Output
28	ITX	Input	Transmit Current Discriminator Input
56	BSTFB	Power	Boost Converter Feedback
PA DRIVERS			
48	PAVDD	Power	PA Driver Supply Input
49	PADRV4	Output	PA Driver Output 4
50	PADRV3	Output	PA Driver Output 3
51	PADRV2	Output	PA Driver Output 2
52	PADRV1	Output	PA Driver Output 1
53	PAGND	Ground	PA Driver Ground and Boost Controller Ground
IMPEDANCE CONTROL DRIVERS			
29	IMPDRV3	Output	Impedance Control Driver 3
30	IMPDRV2	Output	Impedance Control Driver 2
31	IMPDRV1	Output	Impedance Control Driver 1
32	VIMPP	–	Charge Pump Positive Voltage Rail
33	VIMPN	–	Charge Pump Negative Voltage Rail
IMPEDANCE CONTROL DETECT			
44	IMPCDD	Input	Impedance Control Detect PA FET Drain Input
45	IMPCDG	Input	Impedance Control Detect PA FET Gate Input
ADC			
39	SNSGND	Ground	ADC Ground
46	ISNSN	Input	PA Current Sense Negative Input
47	ISNSP	Input	PA Current Sense Positive Input
54	TSNS	Input	PA Temperature Sense Input
55	VSNS	Input	PA Voltage Sense Input
AC POWER MEASUREMENT			
34	ACBSN	Input	AC Power B Measurement Positive Input
35	ACBSP	Input	AC Power B Measurement Negative Input
36	ACASN	Input	AC Power A Measurement Positive Input
37	ACASP	Input	AC Power A Measurement Negative Input

Table 1. PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Type	Description
PEAK DETECTOR			
20	PKTXN	Input	TX Peak Detector Negative Input
21	PKTXP	Input	TX Peak Detector Positive Input
40	PKRFN	Input	RF Peak Detector Negative Input
41	PKRFP	Input	RF Peak Detector Positive Input
42	PKPAN	Input	PA Peak Detector Negative Input
43	PKPAP	Input	PA Peak Detector Positive Input
RELAY DRIVER			
22	RLYDRV	Output	Relay Driver Output
LED DRIVERS			
23	LDIO1	Input/Output	LED Driver 1 or USB Detect
24	LDIO2	Input/Output	LED Driver 2 or USB Detect
FLAG			
–	–	–	Thermal Ground

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog Power Input Pins: AV_{IN}, PV_{IN} (Non Operating (e.g.: Hot-Plug))	V_{HP}	−0.3 to +30.0	V
Analog Power Input Pins: AV_{IN}, PV_{IN}, LX (Operating)	V_P	−0.3 to +26.0	V
Analog Power Input Pins: PAVDD	V_A	−0.3 to +6.0	V
Analog Power Output Pins: V_{DRV}, VIMPP, BSTDRV	V_{PO}	−0.3 to V_P + 0.3 V ≤ 16.0	V
Analog Power Output Pins: VIMPN	V_{NO}	−6 ≤ −V_P − 0.3 to +0.3	V
Analog Outputs: IMPDRV1, IMPDRV2, IMPDRV3	V_{AP}	−6 ≤ −V_{PO} − 0.3 to V_{PO} + 0.3 ≤ 16	V
Analog Power Output Pins V_{CORE}, VLDO, VINLDO	V_O	−0.3 to V_A + 0.3 ≤ 6.0	V
CBOOT with respect to LX	V_{CBOOT_LX}	−0.3 to V_A + 0.3 ≤ 6.0	V
Digital Input Pins : SCL, SDA, SLP, RST, GPIO1, GPIO2 Input Voltage Input Current	V_{IDG} I_{IDG}	−0.3 to V_A + 0.3 ≤ 6.0 10	V mA
Digital Output Pins: SDA, GPIO1, GPIO2, INTB Output Voltage	V_{ODG}	−0.3 to 6.0	V
Analog Inputs: ISNSN, ISNSP, TSNS, VSNS, ACBSN, ACBSP, ACASN, ACASP, PKPAP, PKPAN, PKRFP, PKRFN, PKTXP, PK-TXN, IMPCDD, IMPCDG, BSTFB, COMP, ITX, BSTISNS	V_{AN} I_{AN}	−0.3 to V_A + 0.3 ≤ 6.0 10	V mA
Crystal Pins: OSC1, OSC2	V_{OSC}	−0.3 to V_A + 0.3 ≤ 6.0 10	V mA
Analog Outputs: PADRV1, PADRV2, PADRV3, PADRV4, RLYDRV, LDIO1, LDIO2	V_{AO}	−0.3 to V_A + 0.3 ≤ 6.0	V
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range (Note 1)	T_J	−40 to +125	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to + TSD (150)	°C
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\Theta JA}$	30	°C/W
Moisture Sensitivity (Note 3)	MSL	MSL1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
2. The Junction-to-Ambient thermal resistance is a function of Printed Circuit Board (PCB) layout and application. These data are measured using 4-layer PCBs (2s2p). For a given ambient temperature T_A it has to be pay attention to not exceed the max junction temperature T_{JMAX}.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. GLOBAL OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN}	IC Core Supply Input (Note 4)		4.5		22	V
PV_{IN}	Power Supply Input (Note 4)		4.5		22	V
F_{CLK}	Valid Clock Range	At OSC1	27.06	27.12	27.18	MHz
V_{CLKpp}	External Clock Level	Peak-to-Peak	0.5	–	V_{LDO}	V
DC_{CLK}	External Clock Duty Cycle		49	–	51	%
Cout	Charge Pump Converters Min Recommended Output Capacitors on VIMPN and VIMPP (Notes 5 & 6)	Capacitor Bias Voltage ≥ 16 V	–	10	–	nF
Cout	V_{CORE} and V_{LDO} Min Recommended Output Capacitors (Note 5)	Capacitor Bias Voltage ≥ 10 V	–	2.2	–	μF
Cout	VDRV Min Recommended Output Capacitor (Notes 5 & 6)	Capacitor Bias Voltage ≥ 16 V	–	2.2	–	μF
Cout	Buck Converter Min Recommended Output Capacitor (Notes 5 & 6)	Capacitor Bias Voltage ≥ 16 V	–	10	–	μF
Cout	Boost Converter Min Recommended Output Capacitor (Notes 5 & 6)	Capacitor Bias Voltage ≥ 100 V	–	5	–	μF
$L_{\_Boost}$	Boost Converter Recommended Inductor (Note 6)		–	33	–	μH
$L_{\_Buck}$	Buck Converter Recommended Inductor (Note 6)		–	10	–	μH

4. Operation above 22 V input voltage may affect device reliability.
5. CMS capacitor values vary with voltage applied across their terminals. Capacitance de-rating with bias across has to be taken into account when selecting decoupling capacitors.
6. See corresponding applications details for external component selection, implementation and converter set-up conditions.

Table 4. ELECTRICAL CHARACTERISTICS: SUPPLY INPUTS AVIN & PVIN AND CORE SUPPLIES
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NCP6992A SUPPLY INPUTS AVIN & PVIN						
I_Q	Operating Quiescent Current with AV_{IN} = PV_{IN} = 12 V	**Standby** = Core + VDRV Clamp (Note 7). Standby ON, all other blocks OFF.	–	25	100	μA
		Deep Power Save (DPS) Conditions DPS = Standby + On-Chip Clock Core + Buck (PFM) + LDO, no load, no switching DPS ON, all the other blocks OFF	–	100	–	μA
		Power Save (PS) Conditions PS = DPS + Crystal Oscillator (crystal included), no load, no switching PS ON, all the other blocks OFF	–	2.0	–	mA
		Full Chip Enabled with ADC input stages activated, Impedance Control Detectors and ADC are not enabled (Note 8), no load, no switching	–	4.0	–	mA
CORE SUPPLIES (Note 9)						
UVLO	Under-Voltage Lockout	Rising Edge of AV_{IN}	3.8	–	4	V
		Hysteresis	–	200	–	mV
V_{CORE}	Core Supply voltage	AV_{IN} > 6 V	–	5	–	V
T_{SSCORE}	Core Supply Soft-Start (Note 11)	From AV_{IN} = 0.9 × 12 V to 0.9 × V_{CORE} nominal (AV_{IN} from 0 to 12 V with rise time > 0.6 V/μs)	0.1	–	1	ms
V_{DRV}	Driver Supply Clamp Voltage	Low Voltage Value (default)	–	10.5	–	V
		High Voltage Value	–	12.5	–	
T_{SSDRV}	Driver Supply Soft-Start (Note 11)	From AV_{IN} = 0.9 × 12 V to V_{DRV} = 0.9 × V_{DRV} (AV_{IN} from 0 to 12 V with rise time > 0.6 V/μs)	0.1	–	1.5	ms
T_{WRN}	Thermal Warning		–	135	–	°C
T_{SD}	Thermal Shutdown		–	150	–	°C
T_{ReA}	Thermal Re-Arming		–	120	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. Core Includes V_{CORE}, bandgap, references, logic and detectors.
8. ADC enabled only during conversion.
9. External Components: C_{VCORE} = 2.2 μF, C_{VDRV} = 2.2 μF.

Table 5. ELECTRICAL CHARACTERISTICS: BUCK CONVERTER & REGULATOR
(Min & Max Limits apply for T_A from −40°C to +85°C; $AV_{IN} = PV_{IN}$ = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SYSTEM BUCK CONVERTER (Note 10)						
PV_{IN}	Operating Input Voltage Range (Note 11)		6	–	22	V
V_{DCDC}	Output Voltage	AV_{IN} = 12 V, I_{OUT} = 250 mA, Forced PWM	4.75	–	5.25	V
I_{O_DCDC}	Output Current Capability (Note 11)		500	–	–	mA
I_{Peak}	Current Limit		0.9	–	2.0	A
F_{SW_BUCK}	Buck Switching Frequency (Note 12)	$F_{CLK\_INT}/2$	–	1700	–	kHz
η	Efficiency (Note 11)	I_{Load} = 50 mA, PFM, Xtal Off	–	81	–	%
		I_{Load} = 250 mA, PWM	–	90	–	%
T_{SSDCDC}	Soft-Start	From Buck Enable to 0.9 × V_{DCDC}, No Load	0.2	–	0.8	ms
$R_{BUCKDIS}$	Output Discharge Path	At V_{DCDC} = 5 V	–	65	–	Ω
V_{PG}	Power Good Threshold	Low (PV_{IN} Falling)	–	4.25	–	V
		High (PV_{IN} Rising)	–	4.50	–	V
V_{PG_acc}	Power Good Threshold Accuracy		−5	–	5	%
ΔT_{PG}	Power Good Detection Debounce Period (Notes 11 & 12)		–	30	–	μs
SYSTEM REGULATOR (Note 13), V_{LDO} = 3.3 V						
V_{INLDO}	Operating Input Voltage Range (Note 11)	at VINLDO	V_{PG}	–	5.5	V
V_{LDO}	Output Voltage Range	VSET, VSLP (Note 14)	1.20	–	3.60	V
V_{STEP}	Output Voltage Ramp Step		–	100	–	mV
T_{SPEED}	Output Voltage Ramp Speed		–	10	–	μs
V_{LDO_Acc}	Regulator Output Voltage Accuracy	VINLDO = 5 V	−2	–	2	%
I_{LDO}	Output Current Capability		100	–	–	mA
I_{LDOMAX}	Current Limit		180	–	350	mA
I_{FB}	Fold Back current			100		mA
T_{SS_LDO}	Soft Start	VDCDC Power Good to 2.5 V	–	280	–	μs
R_{LDODIS}	Output Discharge Path	At VLDO = 3.3 V		65	–	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Buck DC-DC External Components: L = 10 μH, C = 10 μF.
11. Characterized and guaranteed by design.
12. Tested by scan.
13. LDO External Components: C = 2.2 μF.
14. Represents Programmable Range (bits VLDOSET[4:0] & VLDOSLP[4:0]), the Default VSET level is selectable through factory fuse and VSLP = VSET.

Table 6. ELECTRICAL CHARACTERISTICS: BOOST CONTROLLER
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PA BOOST CONVERTER (Notes 15 & 16)						
PV_{IN}	Operating Input Voltage Range (Note 11)	At PV_{IN}	8	–	22	V
P_{OUT}	Output Power Capability (Notes 11 & 17)	Standard Range (Default) (BSTPWR = 0)	0	–	25	W
		High Power Range (BSTPWR = 1)	10	–	50	W
V_{BSTFB}	Boost Feedback Voltage (Note 15)	VPA = 28.4 V	–	1	–	V
V_{OUT}	Output Voltage Range	PV_{IN} < VPA	9	–	55.2	V
ΔV_{OUT_STEP}	Ramp Step		–	200	–	mV
T_{BST}	Ramp Speed Range (Notes 12 & 18)		9.4375	–	1208	µs
T_{BSTDIS}	Disable Ramp Speed	Per Ramp Step	–	18.88	–	µs
I_{PKlim}	Peak Current Limit (Note 19)	Power Standard Range (BSTPWR = 0)	–	1.75	–	A
			–	2.25	–	
			3	3.5	4	
			4	4.5	5	
		High Power Range (BSTPWR = 1)	–	3.5	–	A
			–	4.5	–	
			–	7	–	
			–	9	–	
T_{deb_ILIM}	Peak Current Limit Debounce Time (Number of Boost Clock Cycle F_{SW_BST})	(Note 12)	–	64	–	Cycles
F_{SW_BST}	Boost Switching Frequency (Note 12)	27.12 MHz / 32	–	847.5	–	kHz
	Output Ripple (Note 11)	PV_{IN} = 12 V, VPA = 50 V, I_{LOAD} = 400 mA, P_{OUT} = 20 W, C_{OUT} = 5 µF	–	–	200	mVpp
$LOAD_{TR}$	Load Transient Response (Note 11)	PV_{IN} = 12 V, VPA = 50 V, I_{LOAD} = 0 to 500 mA, T_R = T_F = 20 µs	−3	–	3	V
		PV_{IN} = 12 V, VPA = 36 V, I_{LOAD} = 0 to 360 mA, T_R = T_F = 20 µs	−2	–	2	V
V_{GBST}	Gate Drive Voltage (Note 11)		0	–	VDRV	V
T_R	Rise Time	1 nF, 10% − 90%	–	10	–	ns
T_F	Fall Time	1 nF, 10% − 90%	–	10	–	ns
ΔV_{PG}	Power Good Detection Window	At BSTFB Compared to DAC Setting	–	−7	–	mV
		At VPA	–	−200	–	mV
ΔT_{DEB_PG}	Power Good Debounce		–	20	–	µs
T_{EN}	Enable Time	PV_{IN} = 12 V, from BSTEN to Boost Ramping Start	–	–	1	ms

Table 6. ELECTRICAL CHARACTERISTICS: BOOST CONTROLLER (continued)
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DISCRIMINATOR						
Dhi	Discriminator High Threshold Range		0	–	3.5915	V
Dlo	Discriminator Low Threshold Range		0	–	3.5915	V
ΔV_{TH}	Thresholds Granularity	8 bits	–	14.084	–	mV
TH_{ACC}	Thresholds Accuracy			±0.5		LSB
T_{ITX}	Sampling Speed Range (Note 12)		18.88	–	1208	µs
T_{ITXG}	Sampling Speed Granularity (Note 12)	8 bits	–	18.88	–	µs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

15. External Feedback Network Using 10 kΩ and 274 kΩ for a 1/28.4 divider.
16. External Components: L = 33 µH, C = 5 µF, R_{ISNS} = 50 mΩ, NMOS = BSZ440N10N, Rectifier = D = SS2H10.
17. The appropriate transistor and rectifier have to be selected for satisfying the power dissipation requirements in regards to the Boost output power.
18. Eg: Enable to 36 V, 200 mV/604 µs, ramp starts at 0.1479 V × 28.4 = 4.2 V, ramp duration is 96.4 ms.
19. Peak current limit is tested in Open Loop.

Table 7. ELECTRICAL CHARACTERISTICS: CORE CONTROL

(Min & Max Limits apply for T_A from −40°C to +85°C; $AV_{IN} = PV_{IN}$ = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CONTROL: SCL, SDA, RST, SLP, GPIO1, GPIO2, INTB						
F_{I2C}	I^2C Operating Frequency (Notes 11 & 20)		–	–	3.4	MHz
V_{IH}	High Input Voltage SCL SDA		 1.6 1.2	 – –	 – –	V
V_{IL}	SCL, SDA, Low Input Voltage		–	–	0.4	V
V_{OL}	SDA, Low Output Voltage	Sink 3 mA	–	–	0.4	V
V_{IH}	RST, SLP Logic High Input Voltage		1.1	–	5.5	V
V_{IL}	RST, SLP Logic Low Input Voltage		–	–	0.4	V
V_{OH}	INTB Logic High Output Voltage (Note 11)	Open Drain	–	–	V_{INLDO}	V
V_{OL}	INTB Logic Low Output Voltage	1 mA	–	–	0.2	V
T_{DEB}	RST, SLP Debounce Period (Note 12)		–	20	–	μs
V_{IH}	GPIO1, GPIO2 Logic High Input Voltage		$0.7 \times V_{LDO}$	–	V_{LDO}	V
V_{IL}	GPIO1, GPIO2 Logic Low Input Voltage		0	–	$0.3 \times V_{LDO}$	V
V_{OH}	GPIO1, GPIO2 Logic High Output Voltage	1 mA	$V_{LDO} - 0.2$	–	V_{LDO}	V
V_{OL}	GPIO1, GPIO2 Logic Low Output Voltage	1 mA	0	–	0.2	V
T_R	GPIO1 & GPIO2 Rise Times	V_{LDO} > 1.7 V, $C_{LOAD} \le 20$ pF (Note 11)	–	–	5	ns
T_F	GPIO1 & GPIO2 Fall Times		–	–	5	ns
V_{I_Range}	GPIO1 & GPIO2 Analog Input Voltage Range	To ADC	0	–	2.4	V
R_{O_IO2}	GPIO2 Output Impedance (Note 22)	Drain Detect Out	–	33	–	kΩ
CLOCKING: CRYSTAL OSCILLATOR (Note 23)						
T_{SU_XTAL}	Crystal Oscillator Start-Up Time (Note 11)	From Clock Enable to Clock Valid and Stable	–	0.9	1	ms
T_{CLKTO}	Oscillator Clock Validation Timeout (Note 12)		–	10	–	ms
F_{CLK_INT}	Internal Clock Frequency		3.0	–	3.75	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

20. The 4 available I^2C addresses are 0010000, 0010100, 0011000, 0011100 with A7 MSB bit programmable (see Table 17). Through I^2C the MSB can be programmed to a 1 for a software initiated address change.
21. If the SCL and SDA pull-ups are not connected to VLDO, the I^2C bus cannot be operated for the lower voltage settings of VLDO.
22. See § "GPIOs" and Figure 83 for Drain Detect ADC reading.
23. Crystal Used: 7B−27.120MEEQ−T.
24. Quiescent current depends on the amplitude of the clock signal. Higher is the amplitude lower is I_Q.

Table 8. ELECTRICAL CHARACTERISTICS: DRIVERS
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER AMPLIFIER DRIVERS (Note 25)						
PAV_{DD}	Operating Input Voltage Range (Note 11)	At PAV_{DD}	V_{PG}	–	5.5	V
F_S	Signal Frequency (Note 12)	27.12 MHz Divided by 4	–	6.78	–	MHz
V_{PADRV}	Gate Drive Voltage		0	–	PAV_{DD}	V
GD_{Delay}	Relative Gate Drive Delay (Notes 26 & 11)	Between Rising Edges	–	±1	–	ns
		Between Falling Edges	–	±1	–	ns
		Rising versus Falling Edges	–	±1	–	ns
T_R & T_F	Rise & Fall Times (Notes 27 & 11)	Fast (Default)	–	6	10	ns
		Mid	–	–	20	ns
		Slow	–	–	40	ns
T_{EN}	Enable Time (Note 11)		–	–	10	μs
TO_{PA}	PA Time Out (Note 12)	Short	–	0.3	–	s
		Medium	–	1.2	–	s
		Long	–	9.8	–	s
IMPEDANCE CONTROL DRIVERS (Note 28)						
VINLDO	Operating Input Voltage Range (Note 11)		V_{PG}	–	5.5	V
F_{SW_CP}	Charge Pump Switching Frequency (Note 12)	27.12 MHz / 6	–	4.52	–	MHz
VIMPN	Charge Pump Negative Voltage (Note 29)	$-V_{INLDO}$	–	−5	–	V
VIMPP	Charge Pump Positive Voltage (Note 29)	$3 \times V_{INLDO}$	–	14	–	V
VIMPxHI	Driver Output High Voltage Programmability Range		0	–	12.7	V
ΔVIMPxHI	Driver Output High Voltage Granularity		–	100	–	mV
R_{OUT_OFF}	Output Impedance in OFF Mode (Master Enable Disabled)		–	0.5	–	kΩ
V_{IMPDOH_ACC}	Driver Output High Voltage Accuracy (Note 30)	$V_{IMPP} = 3 \times V_{INLDO}$ or V_{DRV}, $V_{IMPxHI} \le 3.0$ V, $I_{OH} = +3 \times 10$ μA	−100	–	+100	mV
		$V_{IMPP} = 3 \times V_{INLDO}$ or V_{DRV}, $V_{IMPxHI} \ge 3.0$ V, $I_{OH} = +3 \times 10$ μA	−3	–	+3	%
I_{OUT_MAX}	Maximum Source Capability (Note 31)	$V_{IMPP} = V_{DRV}$, 150 mV Drop VIMPxHI ≤ 9.0 V for V_{DRV} = 10.5 V VIMPxHI ≤ 9.5 V for V_{DRV} = 12.5 V	100	–	–	μA
		$V_{IMPP} = V_{DRV}$, 100 mV Drop VIMPxHI ≤ 10 V for V_{DRV} = 10.5 V VIMPxHI ≤ 11.5 V for V_{DRV} = 12.5 V	10	–	–	μA
$V_{IMPDROL}$	Driver Output Low Voltage (Note 31)	VIMPDRVx = VIMPN, IOL = −50 μA	–	−5	−4.8	V
		VIMPDRVx = GND, IOL = −100 μA	–	0	+0.1	V
T_{ZC_SU}	Start-Up Time (Note 11)	Charge Pump, No Load From IMPMEN to VIMPDRVx = 0.9 × VIMPLO or to VIMPDRVx = 0.9 × VIMPxHI	–	–	1	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
25. External Components: NMOS = BSZ22DN20N.
26. Valid For Fastest Rise/Fall Time Setting.
27. C_{LOAD} = 1 nF, Rise and Fall Times Considered between 10% and 90% of PAVDD.
28. External Components: NMOS = BSZ440N10N, VIMPN and VIMPP C_{LOAD} = 10 nF.
29. Charge Pump & All Drivers at no load.
30. Load equally distributed over the 3 impedance control drivers.
31. Current values are indicated for one single driver

Table 9. ELECTRICAL CHARACTERISTICS: MISCELLANEOUS DRIVERS
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RELAY DRIVER						
VINLDO	Operating Input Voltage Range (Note 11)		V_{PG}	–	5.5	V
T_{ON}/T_{OFF}	Turn On/Off Delay	From RLYEN to Relay Driver Low Side MOSFET On or Off (100% Duty Cycle)	–	–	50	μs
R_{RLY}	Relay Driver Impedance		–	–	15	Ω
I_{RLY}	Relay Driver Current Handling		50	–	–	mA
V_{Detect_Open}	Relay Open Detection	At RLYDRV	–	30	–	mV
TO_{RLY_Open}	Relay Open Timeout (Note 12)		–	80	–	ms
V_{OH_RLY}	Output Voltage High		–	–	5.5	V
F_{PWM}	PWM Frequency (Note 12)	27.12 MHz / 512	–	53	–	kHz
DC_{PWM}	PWM Duty Cycle Range (Note 12)		50	–	100	%
ΔDC_{PWM}	PWM Duty Cycle Granularity (Note 12)		–	12.5	–	%
LED DRIVER (LDIO1, LDIO2)						
VINLDO	Operating Input Voltage Range (Note 11)		V_{PG}		5.5	V
I_{LED}	LED Current Range Programming	3 bits	2.5	–	20	mA
ΔI_{LED}	LED Current Granularity		–	2.5	–	mA
ACC_{ILED}	LED Current Accuracy	VLED = 1.8 V	−10	–	+10	%
M_{ILED}	LED Current Matching	VLED = 1.8 V	–	±5	–	%
SR_{ILED}	LED Current Slew Rate (Note: Tested w/ a LED)	2.5 mA (10% – 90%)	–	5	–	μs
		20 mA (10% – 90%)	–	20	–	μs
V_{OH_LDR}	LED Driver Output Voltage High Level (Note 11)	20 mA	1.2	–	V_{INLDO} – 1.0	V
V_{OPEN}	LED Open Detect		V_{INLDO} – 0.6	–	–	V
V_{SC}	LED Short Detect		–	–	1.0	V
T_{ON_BLINK}	Blinking Pattern on Period (Note 12)	No Blinking (Note 32)	–	0	–	ms
		Very Short	–	250	–	ms
		Short	–	500	–	ms
		Long	–	1,000	–	ms
T_{REP_BLINK}	Blinking Pattern Repetition Rate (Note 12)	Very Fast	–	500	–	ms
		Fast	–	1,000	–	ms
		Slow	–	2,000	–	ms
		Very Slow	–	4,000	–	ms
$\Delta T_{ON/OFF}$	Turn On/Off Delay (Note 11)	From LED Driver EN (Through I^2C bit LDIOxCTRL)	–	–	100	μs

Table 9. ELECTRICAL CHARACTERISTICS: MISCELLANEOUS DRIVERS (continued)
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USB BC 1.2 DETECT & QC 3.0 CONTROL (LDIO1, LDIO2)						
VD_{SRC}	USB Source Voltage Low	I_{LOAD} < 250 μA	0.5	–	0.7	V
ID_{SINK}	USB Sink Current	(Note 33)	50	–	150	μA
V_{DATREF}	USB Detect Voltage		0.25	–	0.35	V
VD_{UP}	USB Source Voltage High	From V_{LDO} (Note 34)	3.0	3.3	3.6	V
RD_{UP}	USB Source Voltage High Serial Resistance	From VD_{UP} to LDIO	0.90	1.24	1.57	kΩ
RD_{SRC}	USB Source Voltage Low Serial Resistance	From VD_{SRC} to LDIO	–	150	–	Ω
T_{DEB_USB}	USB Debounce Time (Note 12)		–	2	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
32. The fourth setting of the blinking pattern will maintain the LED driver on (no Blinking).
33. Limits are applicable for the combined V_{DATREF} and VD_{SRC} ranges.
34. VD_{UP} is based on the regulator output VLDO which has to be set equal to 3.3 V typically.

Table 10. ELECTRICAL CHARACTERISTICS: ANALOG-TO-DIGITAL CONVERTER
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER						
VINLDO	Operating Input Voltage Range (Note 11)		V_{PG}	–	5.25	V
V_{ADC}	Reference Voltage		–	2.4	–	V
F_{CLK_REF}	Reference Clock Frequency (Note 12)	27.12 MHz / 14	–	1.937	–	MHz
V_{IN_adc}	Input Range	From Zero to Full Scale	0	–	2.4 – LSB	V
LSB	Resolution	10 bits	–	2.344	–	mV
T_{CONV}	Conversion Time (Note 12)	Per Channel	–	–	20	μs
		AC Power per Configuration	–	–	40	μs
T_{WAIT}	Conversion Request Wait Timer (Note 12)	Very Short	–	0.5	–	ms
		Short	–	1	–	ms
		Medium	–	2	–	ms
		Long	–	10	–	ms
T_{RATE}	Conversion Repetition Rate (Note 12)	Very Fast	–	0.5	–	ms
		Fast	–	1	–	ms
		Medium	–	2	–	ms
		Slow	–	10	–	ms
ERR_{Offset}	Offset Error (Note 11)		–	–	1	LSB
ERR_{Gain}	Gain Error (Note 11)		–	–	1.5	LSB
INL	Integral Non-linearity (Note 11)		−1.5	–	1.5	LSB
DNL	Differential Non-linearity (Note 11)		−1	–	1	LSB
TUE	Total Unadjusted Error $TUE = \sqrt{(ERR_{Offset}^2 + ERR_{Gain}^2 + INL^2 + DNL^2)}$ (Note 35)		–	–	+0.5	%
$RangeD_{IG}C$	Digital Comparator Range		0	–	255	
LSBC	Digital Comparator Resolution	8 bits	–	9.375	–	mV
CNT	Digital Comparator Counter	7 bits	0	–	127	

Table 10. ELECTRICAL CHARACTERISTICS: ANALOG-TO-DIGITAL CONVERTER (continued)
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER INPUT STAGES						
V_{BST_OV}	Boost Overvoltage Detect (Note 38)		2.00	2.042	2.08	V
T_{deb_BSTOV}	Boost Overvoltage Debounce Time		–	500	–	μs
V_{TH_PATemp}	PA Temperature Protection Threshold (Note 39)		–	VADC/2	–	V
ACC_{PATemp}	PA Temperature Protection Accuracy		−2	–	+2	%
R_{SCE}	Max Source Resistance (Note 11)	ISNSP, ISNSN (Note 36)	–	1	–	kΩ
		Other Inputs (Note 37)	–	–	10	kΩ
R_{PUP}	NTC Pull-Up Resistor		9.8	10.0	10.2	kΩ
$Scale_{\_AVIN}$	Input Voltage Measurement Scaling	From AVIN		0.1		X
V_{Die_Temp}	Die Temperature Measurement	T_j = 25°C	–	2.2	–	V
	Die Temperature Measurement Coefficient		–	−5.2	–	mV/K
G_{ISNS}	Current Sense Amplifier Voltage Gain (Note 11)	Low	19.0	20.0	21.0	
		High	39.0	40.0	41.0	
ATT_{ISNS}	Current Sense Low Pass Filter Rejection (Note 11)	Freq = 13.56 MHz	−50	–	–	dB
		Freq = 847.5 kHz	−30	–	–	dB
V_{OC_PA}	PA Over-Current Detect (Note 40)	Bypass	–	2.335	–	V
		Gain = 20	–	123	–	mV
		Gain = 40	–	61.5	–	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
35. Same unit has to be used in the equation for the different parameters. The TUE is an indication of the absolute rms error.
36. A higher source impedance will introduce offset and gain errors in the current sense preamplifier.
37. Higher source impedance will slow down the time response of the ADC input thus creating readout errors.
38. Equivalent to 57 V_{min} and 59 V_{max} in case of a 1/28.4 divider at the VSNS input.
39. For an NTC = 100 kΩ with B = 4,000, the equivalent trip temperature is 87°C, with 4.87 kΩ in series 110°C, with 6.04 kΩ in series 120°.
40. Measured after current sense amplifier, equivalent to 1164 mA for gain x20 and 100 mΩ sense resistor.

Table 11. ELECTRICAL CHARACTERISTICS: AC POWER MEASUREMENTS & DETECTORS
(Min & Max Limits apply for T_A from −40°C to +85°C; AV_{IN} = PV_{IN} = 12 V. Typical values are given for T_A = +25°C and default configuration. These conditions are true unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AC POWER MEASUREMENTS						
V_{CORE}	Operating Input Voltage Range (Note 11)	At VINLDO	V_{PG}	–	5.5	V
T_{EN_ACP}	Enable Time	Bias Only, 1.5 nF to Ground	–	5	–	ms
V_{IS}	Input Voltage Range (Note 11)		0	–	2.4	V
V_{REF}	Amplifier Reference Voltage		–	1.6	–	V
G_V	Amplifier Voltage Gain (Notes 41 & 42)	DC Gain	–	±0.1	–	dB
			–	3	–	dB
			–	6	–	dB
			–	9	–	dB
ATT	Total Harmonic Rejection (Note 11)	Freq = 13.56 MHz	−50	–	–	dB
T_{SET_OUT}	Amplifier Output Settle Time (Notes 43 & 11)		–	–	10	μs
PEAK DETECTORS						
V_{CORE}	Operating Input Voltage Range (Note 11)	At VINLDO	V_{PG}	–	5.5	V
T_{ENPK_DET}	Enable Time (Note 11)	External $C_{IN} \leq$ 680 pF	–	–	100	μs
V_{IS}	Input Voltage Range (Note 11)		0	–	4.8	V
R_{IN_BIAS}	Input Bias Resistance		–	6	–	kΩ
V_{IREF}	Input Reference Voltage		–	2.4	–	V
V_{DAC}	DAC Range	6 bits (Note 45)	2.406	–	3.969	V
ΔV_{DAC}	DAC Granularity		–	31.25	–	mV
ACC_{PK_DET}	Peak Detector Accuracy	Half Range (Note 46)		±1	–	LSB
ΔT_{PK}	Peak Detector Response Time (Note 11)	Overdrive 30 mV	–	20	30	μs
IMPEDANCE CONTROL DETECTORS						
V_{CORE}	Operating Input Voltage Range	At VINLDO	V_{PG}	–	5.5	V
T_{ENIC_DET}	Enable Time (Note 12)		–	–	250	μs
C_{IN}	Input Load Capacitance	IMPCDG	–	–	1	nF
V_{IS}	Input Voltage Range (Note 11)	IMPCDD	0	–	2.4	V
		IMPCDG	0	–	PAVDD	V
R_{IN_BIAS}	Input Bias Resistance	IMPCDG	–	90	–	kΩ
DIVG	Reference Divider Range		0.2	–	0.8	x
$STEP_{DIV}$	Reference Divider Step		–	0.2	–	x
VI_{OF_COMP}	Comparator Input Offset (Note 11)		–	–	10	mV
ΔT_{ZDET}	Impedance Control Detector Delay (Note 11)	Overdrive 30 mV	–	3	15	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
41. Gain is specified as the DC value at ACSNSP−ACSNSP divided by the peak voltage of a sinusoidal input signal between respectively ACASP−ACASN and ACBSP−ACBSN at 0° if phase shift.
42. All tested units are in the limits.
43. Accounted for in the ADC conversion timings.
44. The integrated output noise is specified from shorted inputs to ADC input during AC power measurements.
45. High end of 6-bit range clamped at 3.969 V, non-addressable full range would go as high as 3.969 V.
46. The accuracy refers to the final error in peak detection at the comparator, offset included, of the peak-to-peak of the input differential signal.

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN}$ = 12 V, T_A = 25°C (Unless Otherwise Noted))

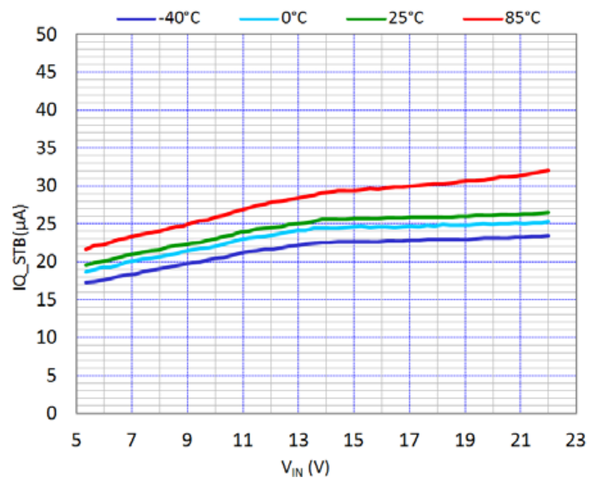


Figure 4. Standby Current vs. V_{IN} (V)

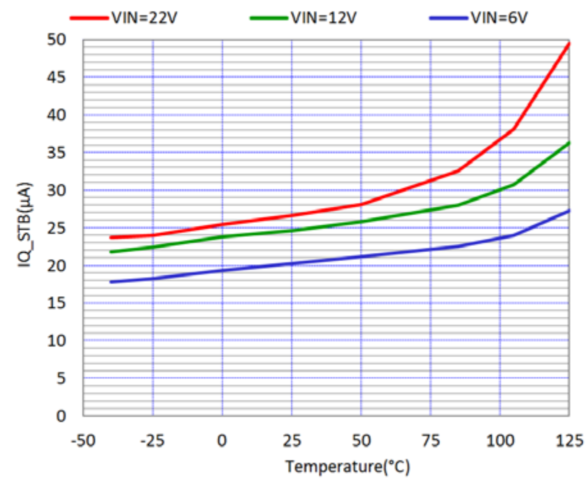


Figure 5. Standby Current vs. Temperature (T_A)

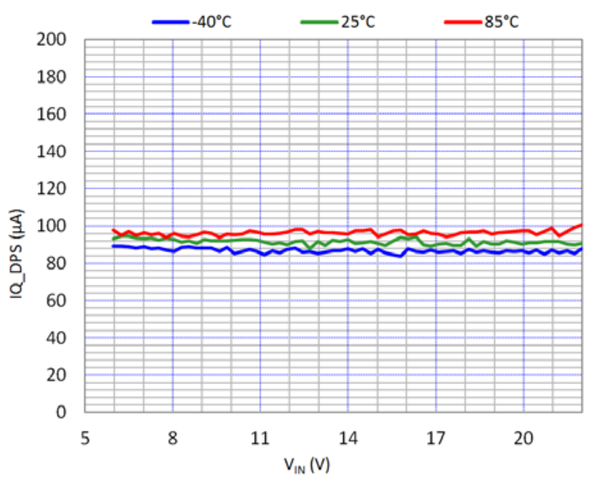


Figure 6. Deep Power Save Current vs. V_{IN} (V)

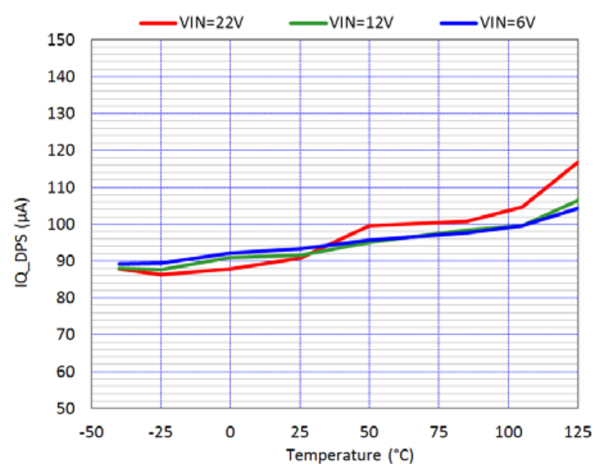


Figure 7. Deep Power Save Current vs. Temperature (T_A)

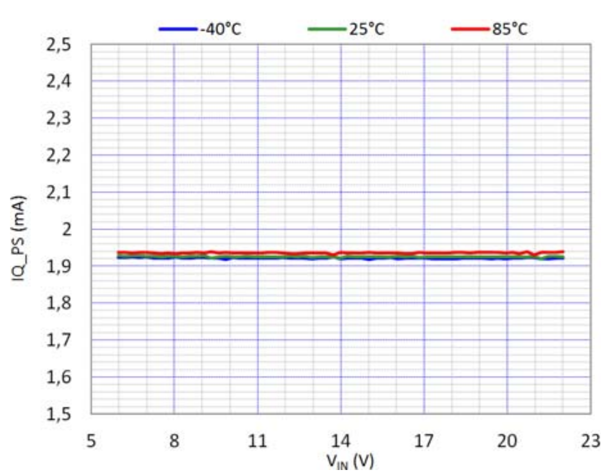


Figure 8. Power Save Current vs. V_{IN} (V)

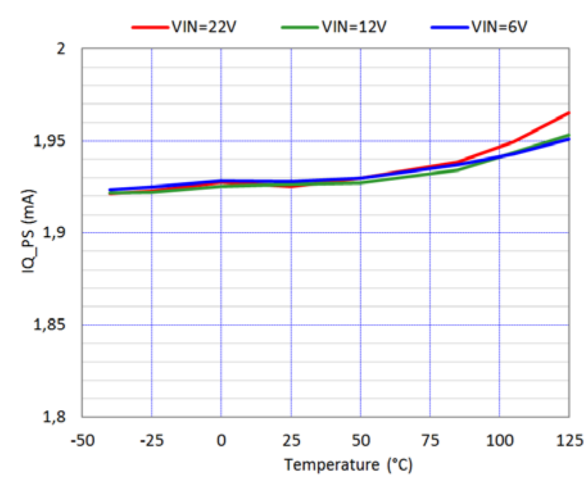


Figure 9. Power Save Current vs. Temperature (T_A)

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN}$ = 12 V, T_A = 25°C (Unless Otherwise Noted))

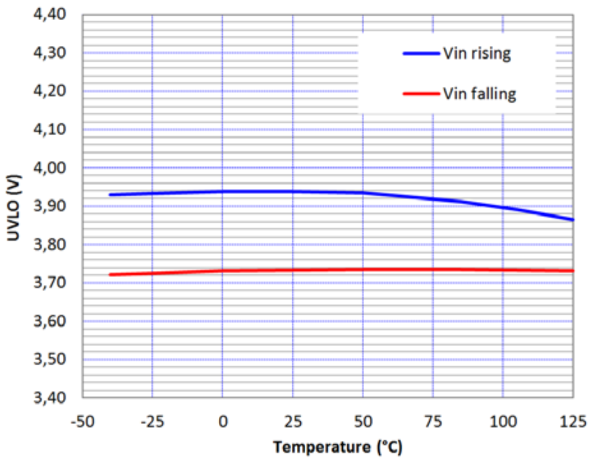


Figure 10. UVLO vs. Temperature (T_A)

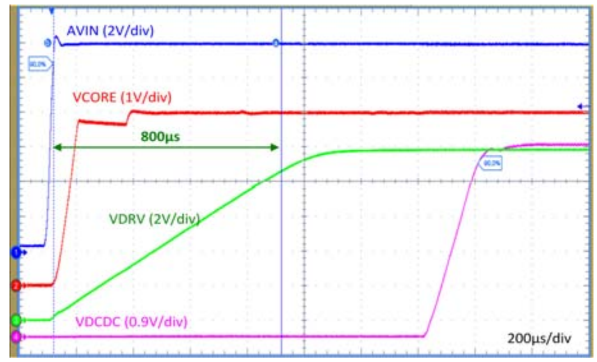


Figure 11. Core System Power-up (AV_{IN} from 0 to 12 V, Rise Time 3 V/5 µs)

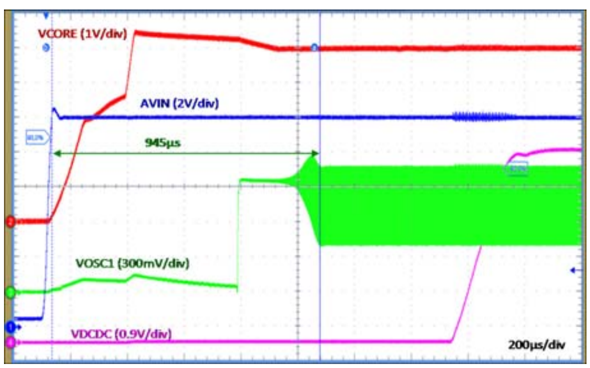


Figure 12. Crystal Oscillator Start-up Time (AV_{IN} from 0 to 12 V, Rise Time 3 V/5 µs)

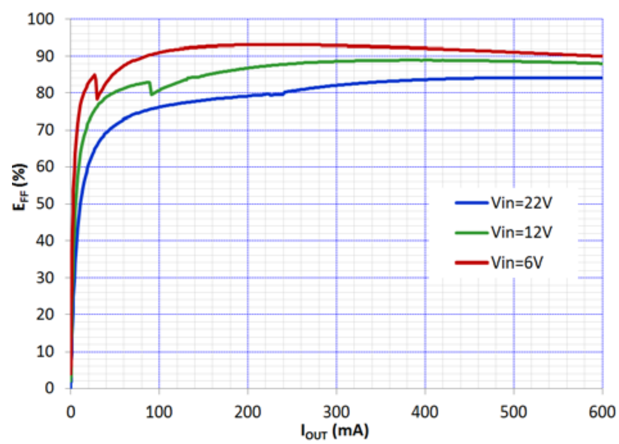


Figure 13. Buck Converter Efficiency

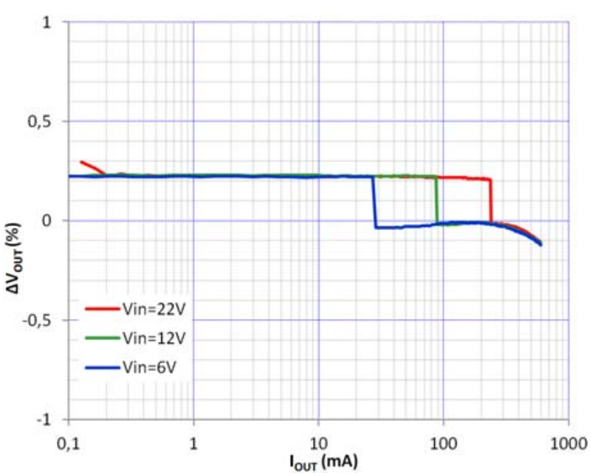


Figure 14. Buck Converter Output Voltage Accuracy vs. Output Current

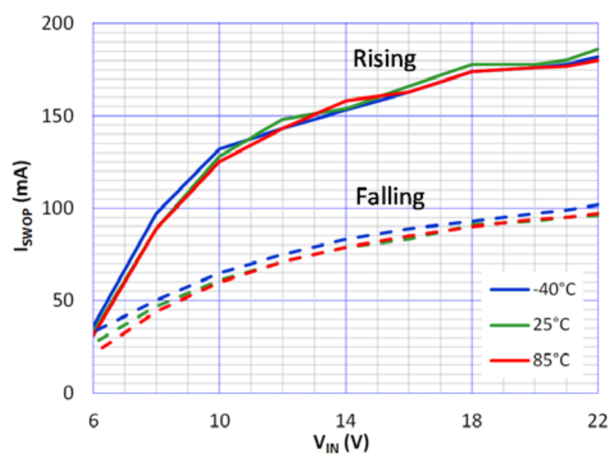


Figure 15. Buck Converter Switchover Point vs. V_{IN}

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN}$ = 12 V, T_A = 25°C (Unless Otherwise Noted))

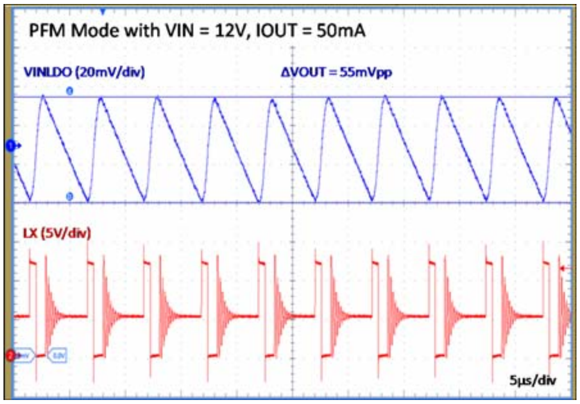


Figure 16. Buck Converter Ripple in PFM Mode

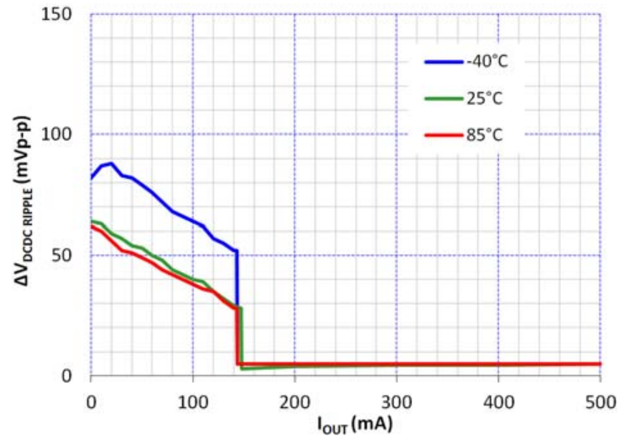


Figure 17. Buck Converter Output Ripple vs. I_{OUT}

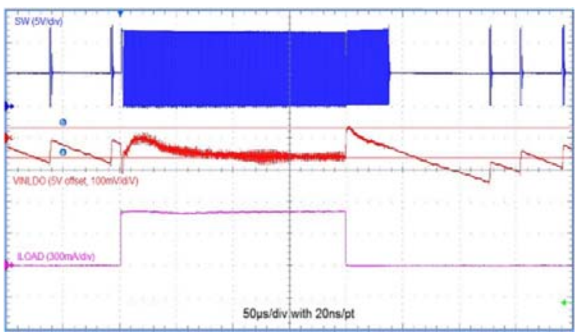


Figure 18. Buck Converter Load Transient Response (5–500 mA, $T_R = T_F$ = 250 ns)

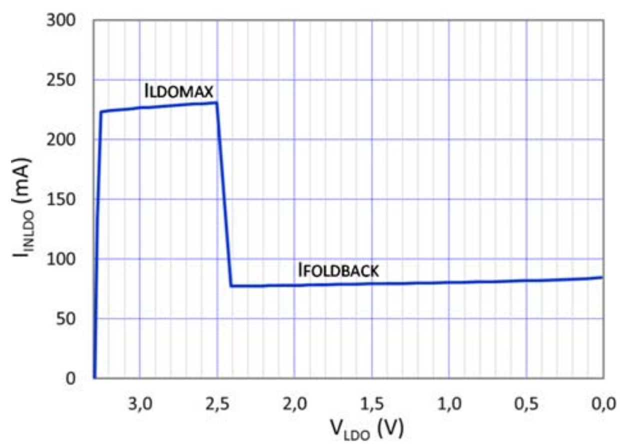


Figure 19. LDO Short Circuit Protection (V_{IN} = 12 V, VLDOSET[4:0] = 3.3 V, VINLDO = 5 V)

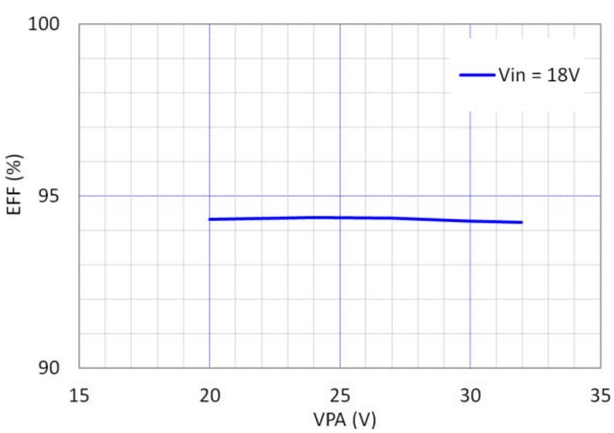


Figure 20. Boost Converter Efficiency vs. V_{PA}

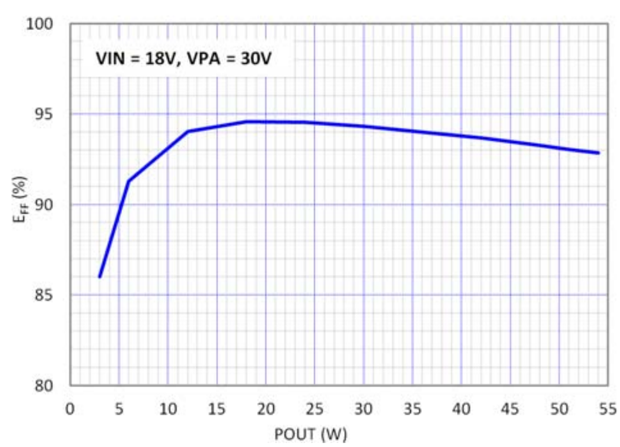


Figure 21. Boost Converter Efficiency vs. P_{OUT}

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN}$ = 12 V, T_A = 25°C (Unless Otherwise Noted))

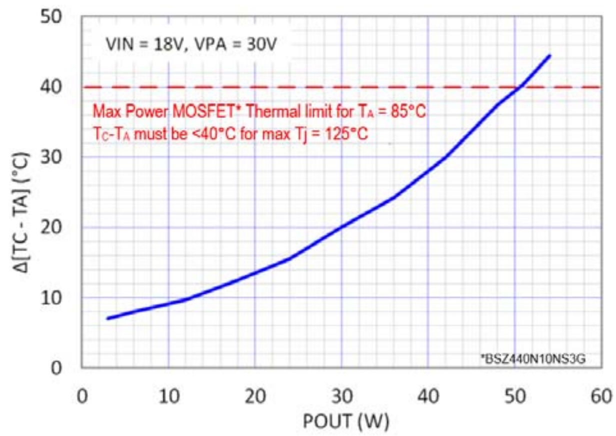


Figure 22. Boost LS Power MOSFET Heating vs. P_{OUT}

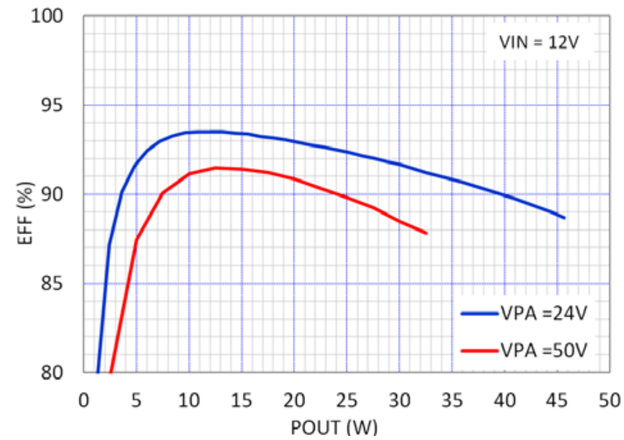


Figure 23. Boost Converter Efficiency vs. P_{OUT}

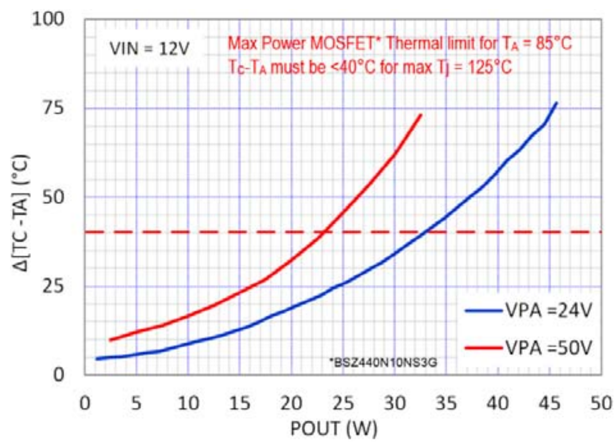


Figure 24. Boost LS Power MOSFET Heating vs. P_{OUT}

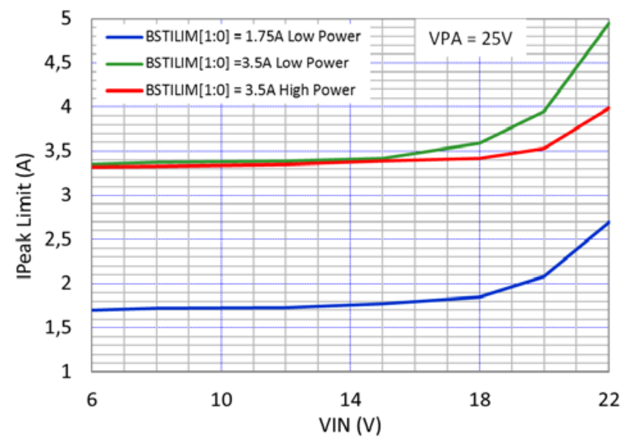


Figure 25. Boost Converter I_{peak} Limit vs. V_{IN} (V)

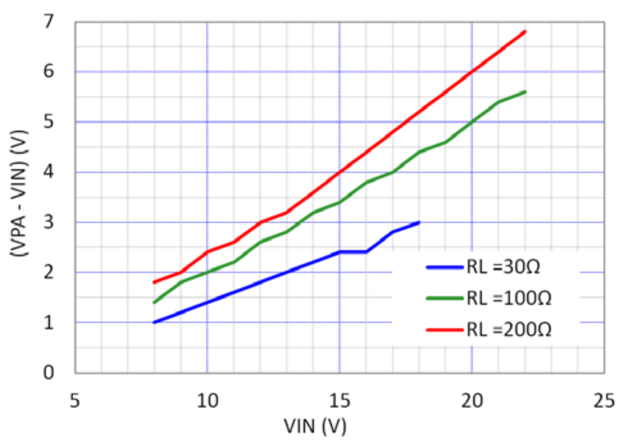


Figure 26. Boost (V_{PA} – V_{IN}) Threshold Voltage Transition from Continuous Mode to Pulse Skipping Mode vs. V_{IN}

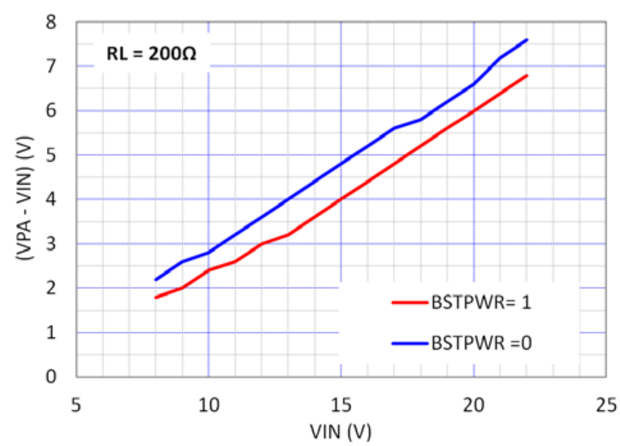


Figure 27. Boost (V_{PA} – V_{IN}) Threshold Voltage Transition from Continuous Mode to Pulse Skipping Mode vs. V_{IN}

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN}$ = 12 V, T_A = 25°C (Unless Otherwise Noted))

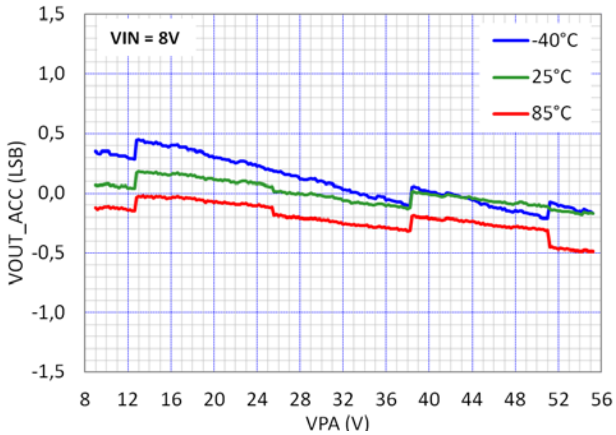


Figure 28. Programming Table Accuracy of the Boost Output Voltage V_{PA}

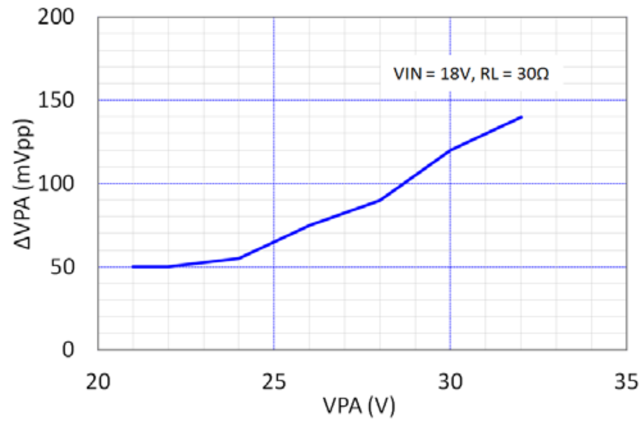


Figure 29. Boost Converter Output Voltage Ripple vs. V_{PA}

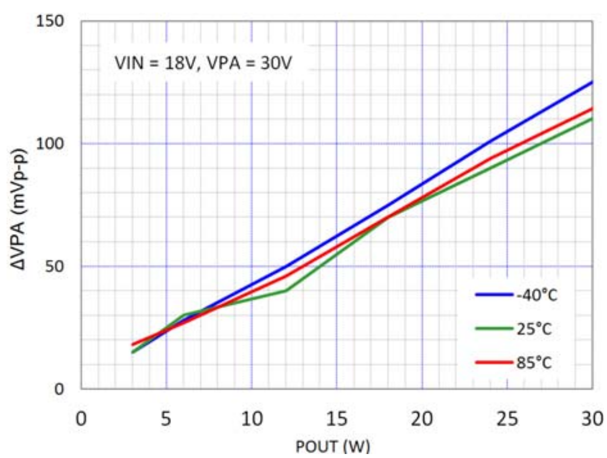


Figure 30. Boost Converter Output Voltage Ripple vs. P_{OUT}

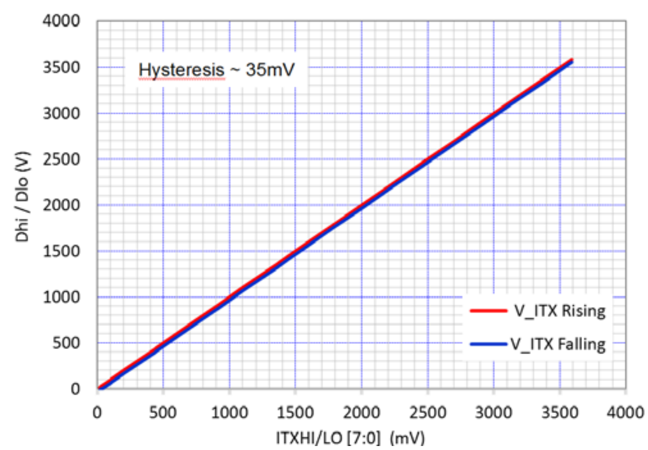


Figure 31. Discriminator Threshold Voltage Programming Table

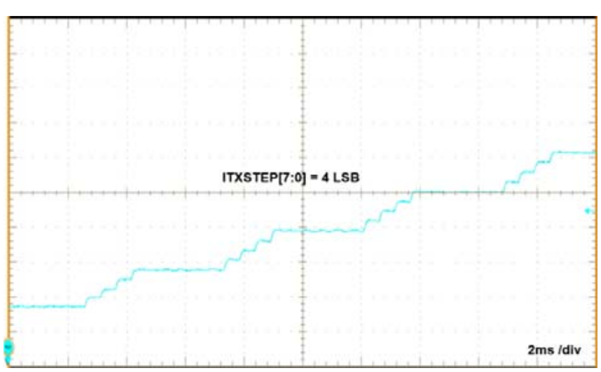


Figure 32. Discriminator Continuous Mode w/ N_{ITX} = 4 LSB

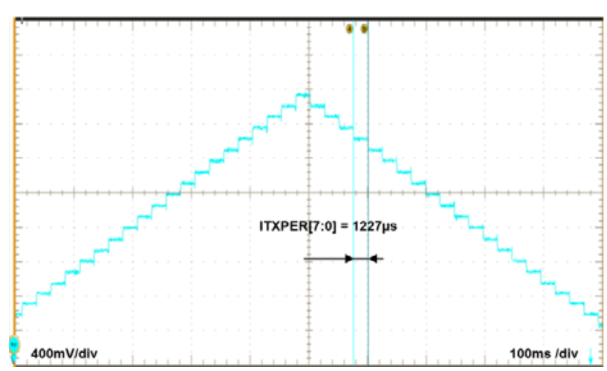


Figure 33. Discriminator Continuous Mode w/ N_{ITX} = 1,227 μs

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN}$ = 12 V, T_A = 25°C (Unless Otherwise Noted))

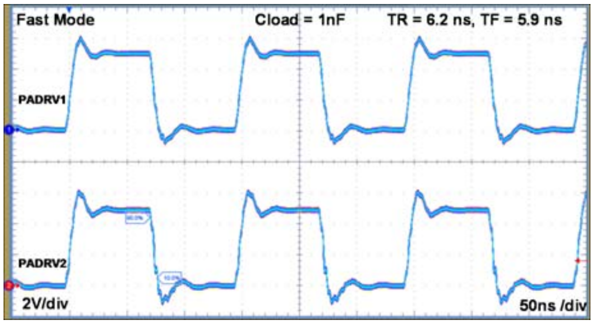


Figure 34. PA Drivers' Waveforms in Fast Mode with C_{load} = 1 nF

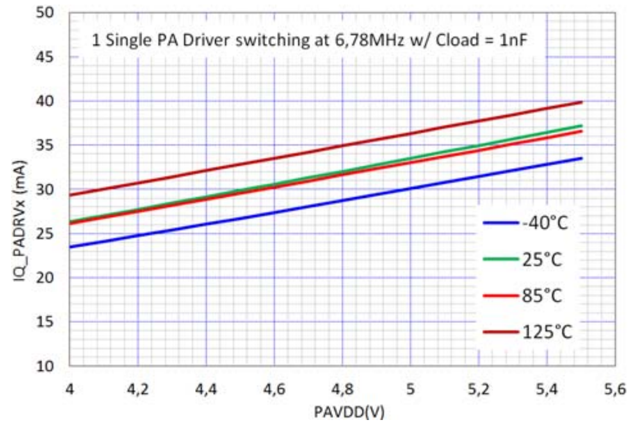


Figure 35. Current Consumption vs. PAVDD per PA Driver w/ C_{load} = 1 nF and Fast Mode

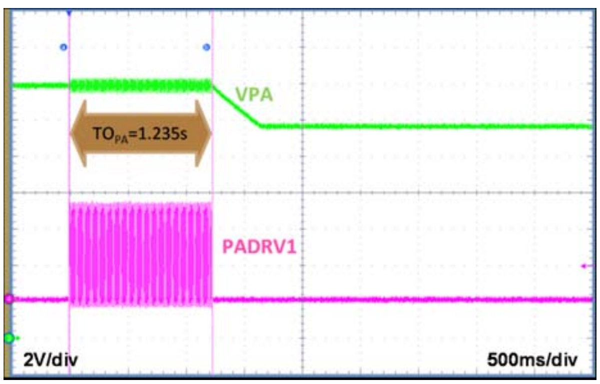


Figure 36. PA Driver Time Out Medium Time

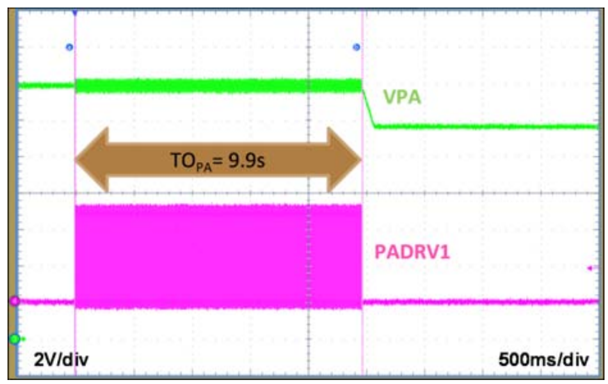


Figure 37. PA Driver Time Out Long Time

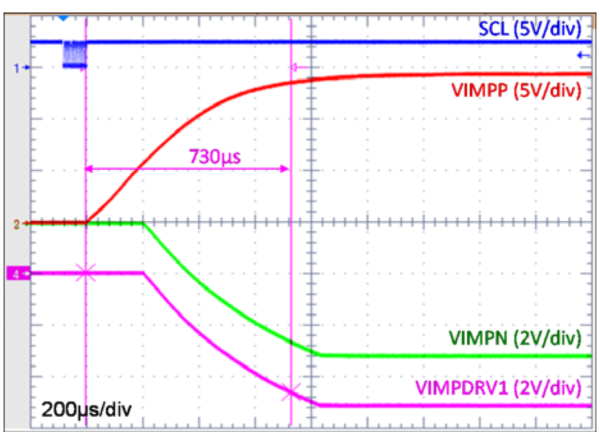


Figure 38. Impedance Control Driver Turn-on (IMPMEN) with VIMPP = 3xVINLDO & Negative Rail = VIMPN Mode (IMPxEN = 0)

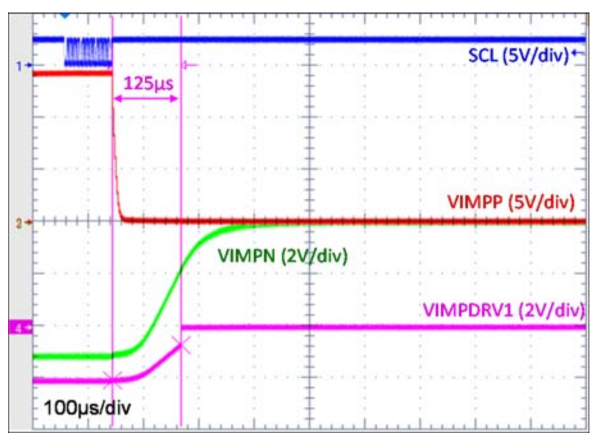


Figure 39. Impedance Control Driver Turn-off (IMPMEN) with VIMPP = 3xVINLDO & Negative Rail = VIMPN Mode (IMPxEN = 0)

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN} = 12$ V, $T_A = 25°C$ (Unless Otherwise Noted))

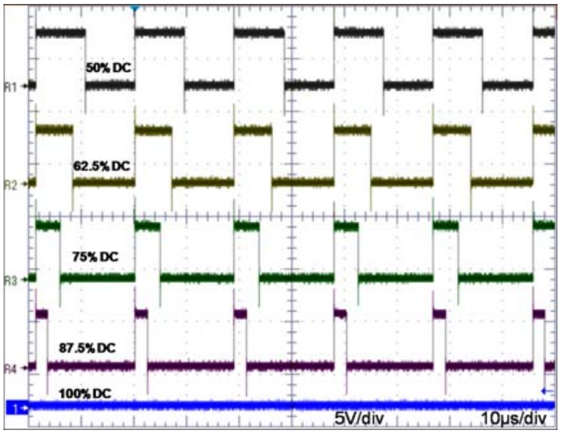


Figure 40. Relay Driver PWM Control

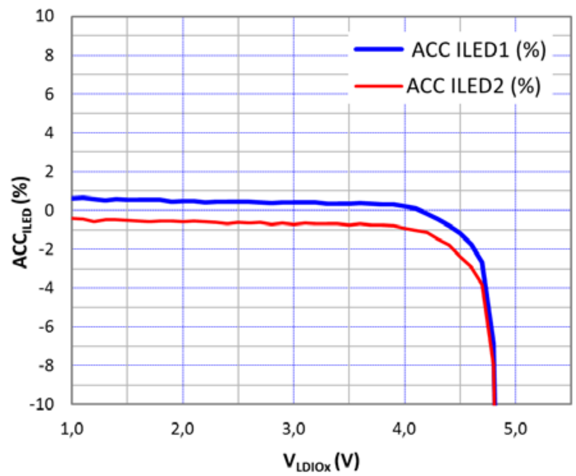


Figure 41. LED Drivers Current Accuracy (I_{LED} = 2.5 mA)

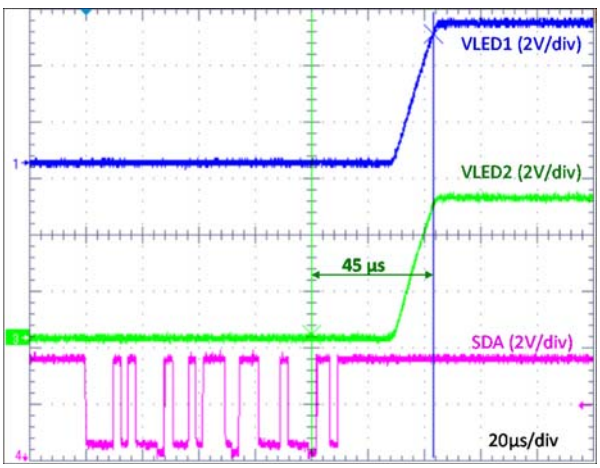


Figure 42. LED Driver Start-up Time

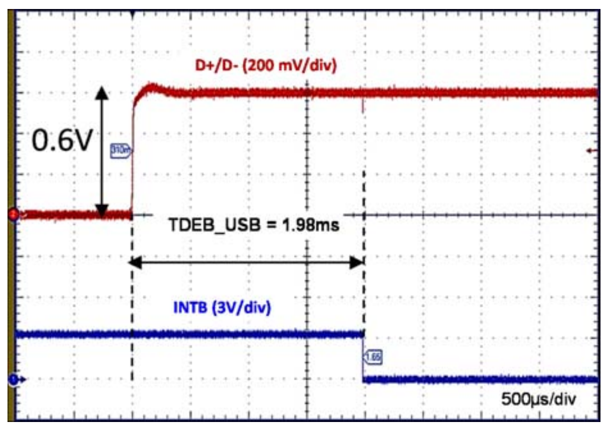


Figure 43. USB Debounce Time

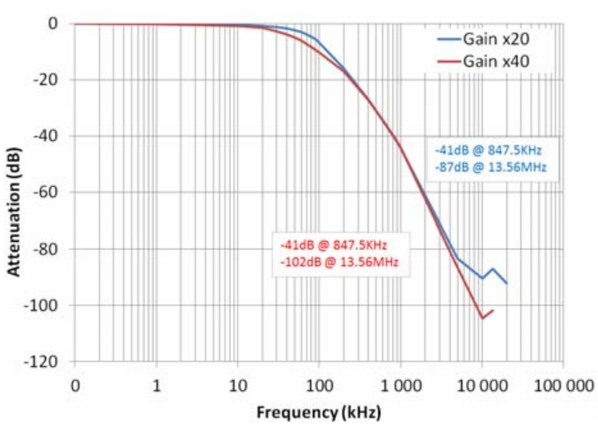


Figure 44. ADC Current Sense (ISNS) Amplifier and Filter Frequency Response

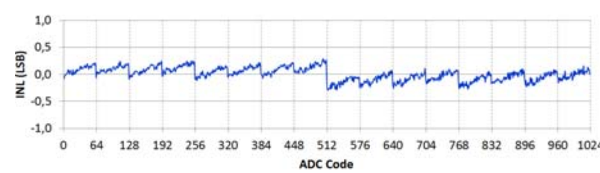


Figure 45. 10-bit ADC Integral Non-linearity (INL), V_{IN} = 12 V

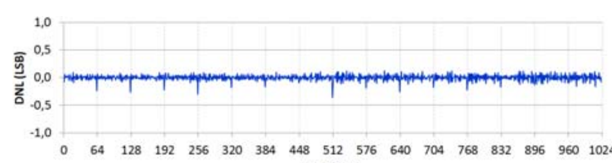


Figure 46. 10-bit ADC Differential Non-linearity (DNL), V_{IN} = 12 V

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN} = 12$ V, $T_A = 25°C$ (Unless Otherwise Noted))

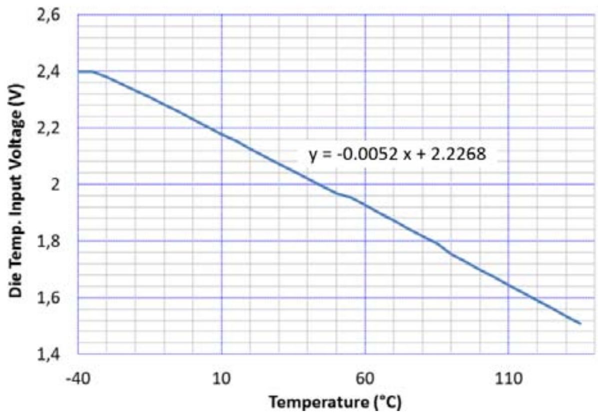


Figure 47. Die Temperature from ADC Channel 5

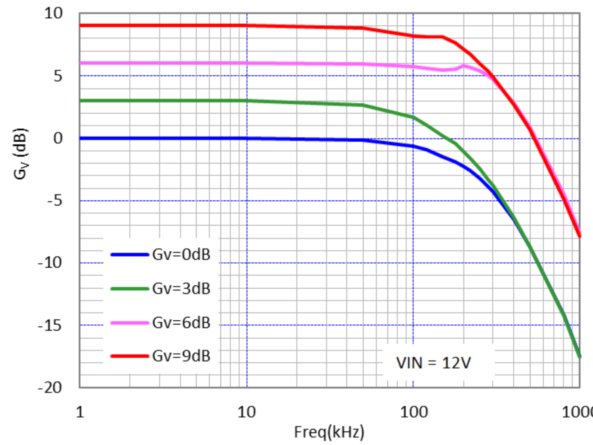


Figure 48. ACPM Frequency Response and Gains w/ V_{IN} = 12 V

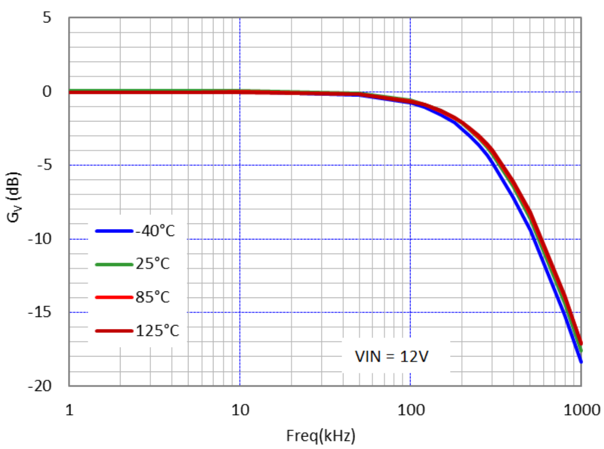


Figure 49. ACPM Frequency Response vs. Temperature w/ V_{IN} = 12 V and Gain 0 dB

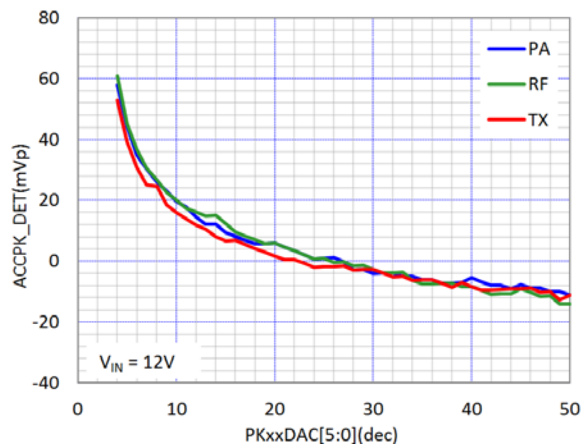


Figure 50. Peak Detector Error vs. Code

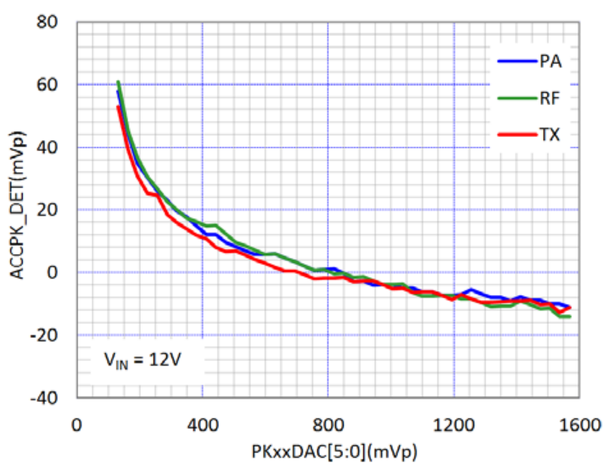


Figure 51. Peak Detection Error vs. Rectified Input Voltage (mVp)

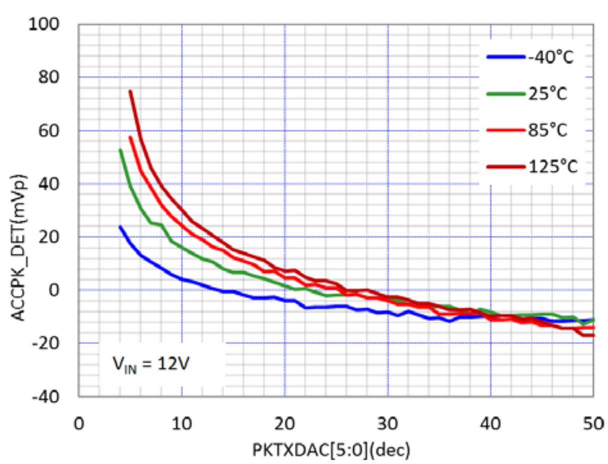


Figure 52. TX Peak Detector Detection Error vs. Code vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN} = 12$ V, $T_A = 25°C$ (Unless Otherwise Noted))

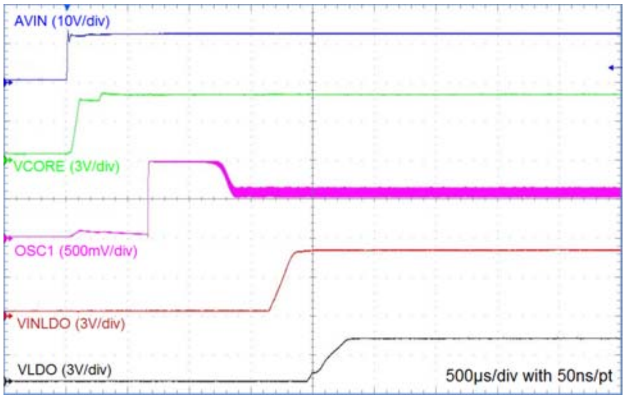


Figure 53. Initial Power-up Timings

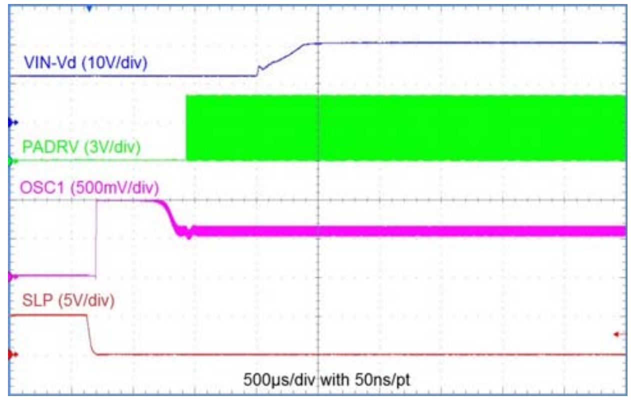


Figure 54. Oscillator, PA Boost and PA Driver Enabling Timing Out fo Sleep Mode

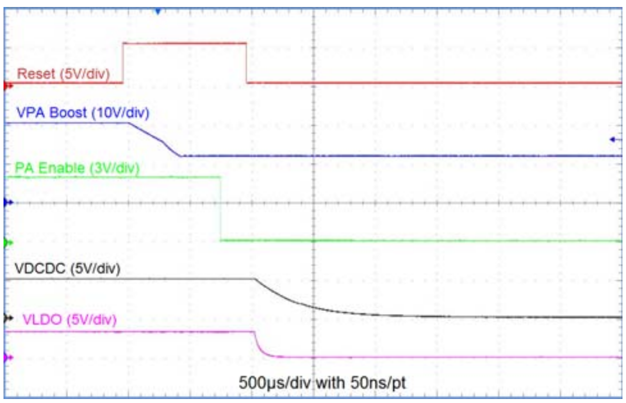


Figure 55. Power-down upon Hard Reset

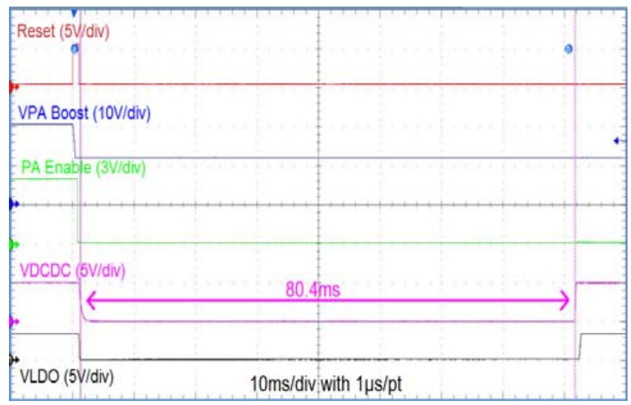


Figure 56. Buck and LDO Power-up after Hard Reset

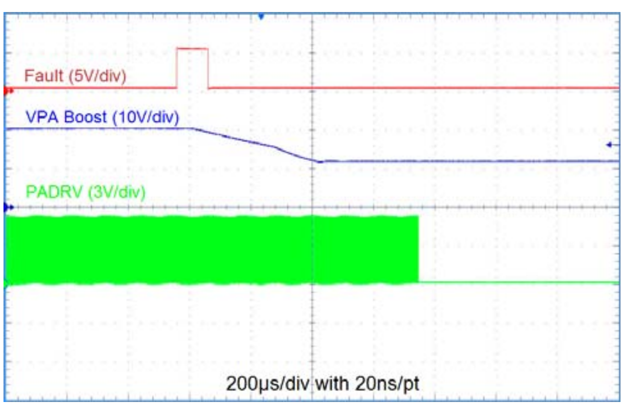


Figure 57. PA or Boost Fault Mode Shutdown Cycle

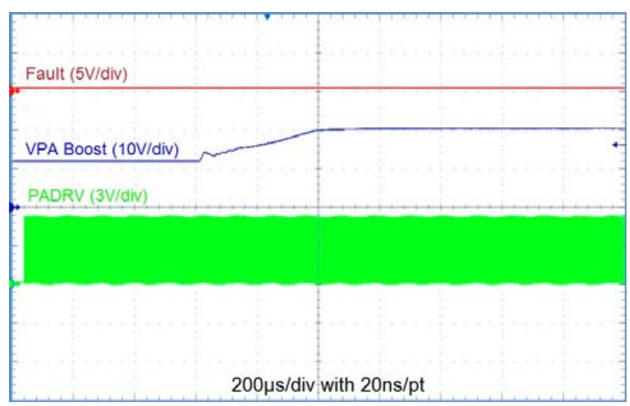


Figure 58. PA or Boost Fault Mode Restart Cycle

TYPICAL OPERATING CHARACTERISTICS

($AV_{IN} = PV_{IN} = 12$ V, $T_A = 25°C$ (Unless Otherwise Noted))

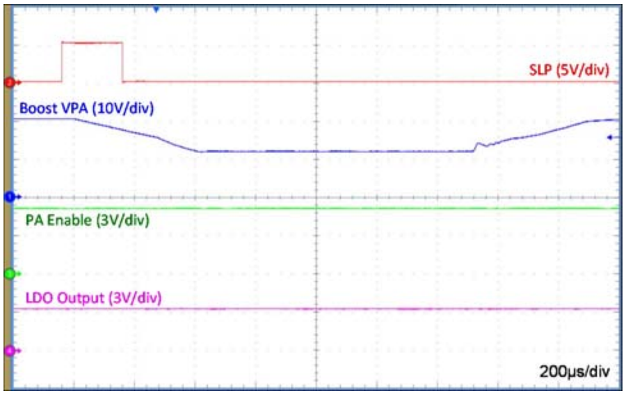


Figure 59. Sleep Shutdown and Restart Cycle during Boost Ramp-down

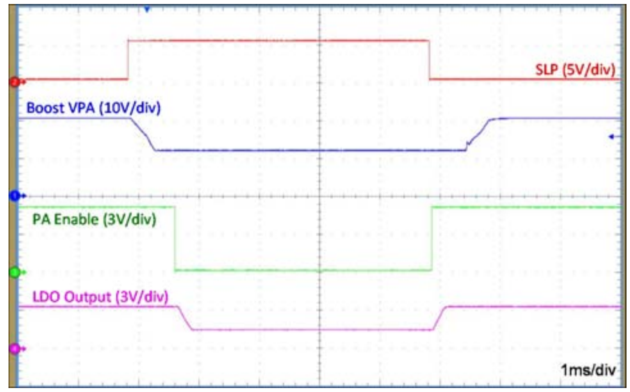


Figure 60. Sleep Shutdown and Restart Cycle

OPERATING DESCRIPTION

Transmitter System

The wireless charger base, also referred to as transmitter or PTU, converts its input supply to transmitted power according to the figure below.

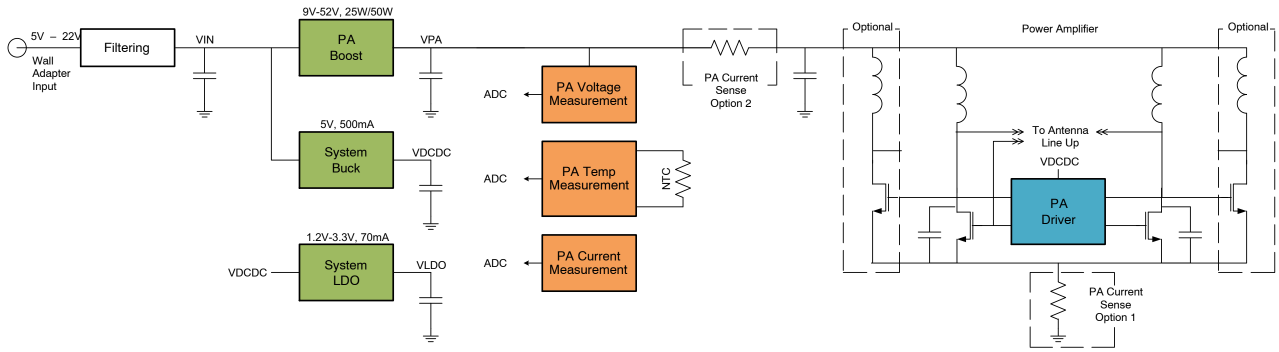


Figure 61. Transmitter Supply Tree and PA

The input supply is filtered before being applied to the System Buck, the System LDO and the PA Boost. The System Buck and the system LDO provide regulated supplies to the Microcontroller, Bluetooth interface and other miscellaneous peripherals. The PA Boost provides the supply for the PA amplifier. Its output voltage determines the maximum power the PA can transmit. For optimum efficiency the PA Boost voltage is to be kept as low as possible and is therefore frequently reprogrammed. An external feedback network, low side FET and flying diode are used to keep the high voltages off-chip.

The voltage applied to the PA as well as the current drawn are scaled and converted by the on-chip 10 bit ADC. In addition, the temperature of the PA transistors is monitored.

The PA consists of up to 4 FETs that are driven by the PA Drivers. Those are always running at 6.78 MHz. The two FETs of each PA pair run in opposite phase.

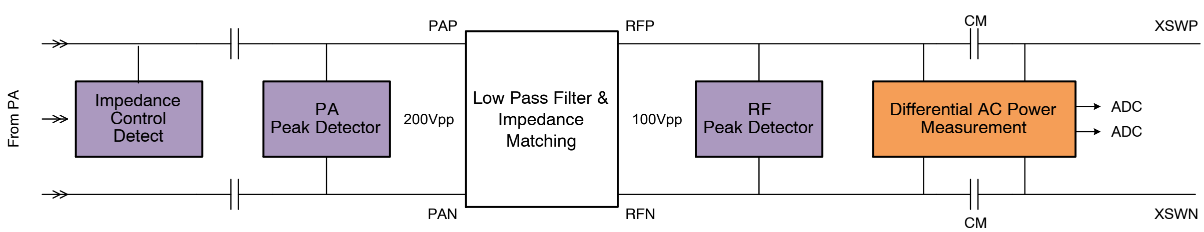


Figure 62. Transmitter Antenna Line-Up Part 1

The switching signals of the output stage of the PA are monitored by the impedance control detector, and it is verified if the resonance of the antenna line up is perfectly tuned to 6.78 MHz. The differential output of the PA is low pass filtered and at the same time the impedance between PA and antenna is matched. The signal level is monitored by a set of peak detectors before and after the low pass filter.

The amount of transmitted power and the impedance of the antenna (real and imaginary) are calculated by the microcontroller based on the ADC readings of the differential AC power measurement block. The coupling capacitors CM serve as the sense elements.

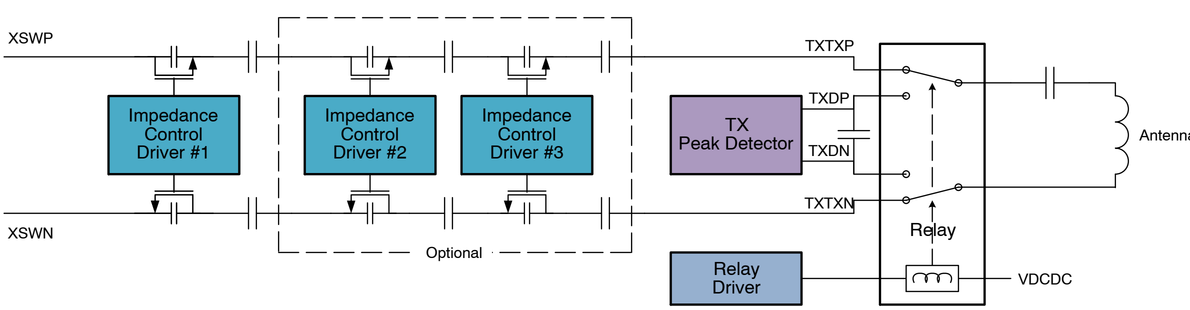


Figure 63. Transmitter Antenna Line-Up Part 2

Based on the impedance measurements it may be needed to adapt the impedance of the antenna line up. The antenna looks like a capacitor in series with an inductor and for efficient power transfer is operated at or close to resonance. To achieve such over varying loads, the LC is tuned by switching in/out series capacitors or driving other controlling elements such as integrated filters.

When not transmitting, the antenna is connected to a set of transmit peak detectors through a relay switch while maintaining the possibility for the antenna to get into resonance. This allows for detecting neighboring chargers or foreign objects.

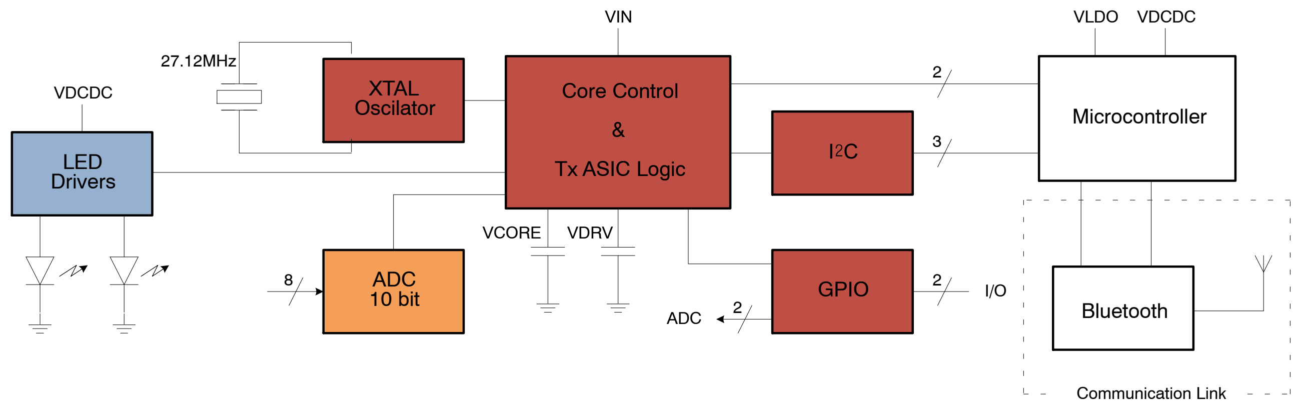


Figure 64. Transmitter Antenna Line-Up Part 2

The transmitter is controlled by a microcontroller and communicates by means of a low power Bluetooth (BLE). A 27.12 MHz crystal oscillator serves as the master clock for the system and allows deriving the 6.78 MHz transmission frequency. Two signal LED drivers provide indication to the user on the state of operation. Additional GPIO functions allow amongst others routing out the system clock to peripherals or routing in on board signals to the ADC. I^2C is used as the control bus.

Core Supplies

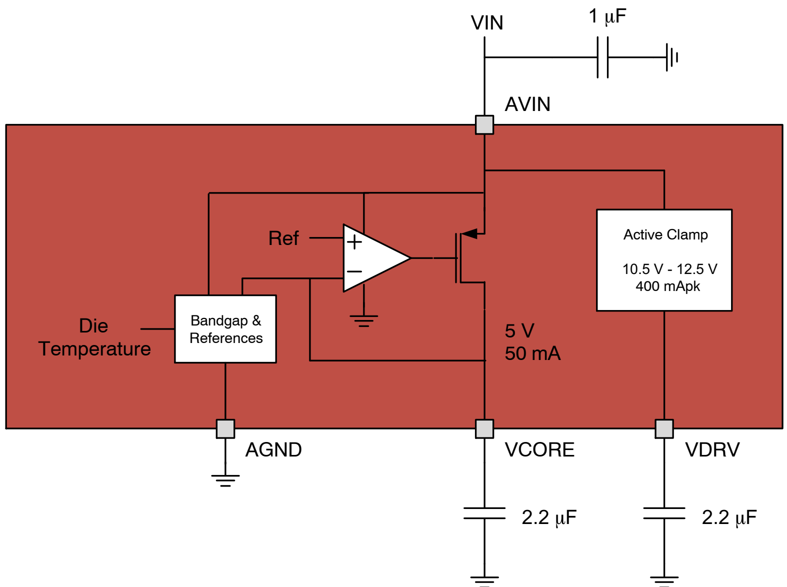


Figure 65. Core Supplies

The IC core is supplied from the AVIN pin and a locally generated supply rail VCORE that supplies all low voltage analog circuitry including the band-gap and other references, as well as the logic. In addition, a VDRV is generated from the AVIN pin and is used to supply the medium voltage drivers. The VDRV output voltage is a clamped version of AVIN and its clamp voltage is selectable by I^2C. Depending on the input voltage conditions, VCORE and VDRV will follow the input voltage. Both supplies must be bypassed with a capacitor to AGND. AGND is considered as the system ground. AVIN must be connected to PVIN in the application.

The core only operates for voltages that are above the under-voltage lockout threshold UVLO.

The die temperature is monitored by the core. When crossing the thermal warning threshold an interrupt is generated so that the controller can take appropriate action. When the die temperature increases further and crosses the thermal shutdown threshold, all functions will be disabled and the register contents reset. The IC will automatically power up after it is cooled down and an interrupt is generated to signal the thermal shutdown event.

Clocking

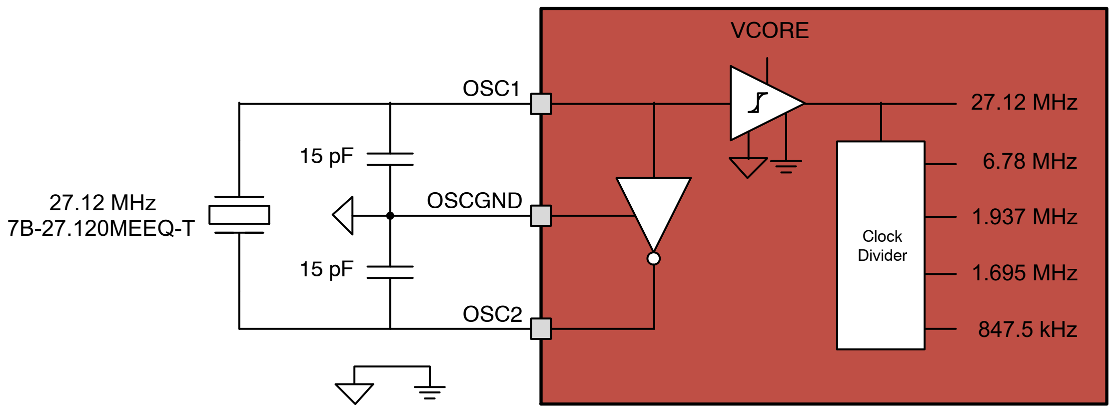


Figure 66. Crystal Oscillator and Clock Generation

The IC runs on a crystal oscillator generated high frequency clock. The crystal has to be connected between the OSC1 and OSC2 terminals and loaded as required with small capacitors to OSCGND. The OSCGND can be connected to the system ground.

The crystal clock is divided down to provide lower frequencies as used by the different circuitry on chip. The divider ratios are fixed and are not programmable.

The oscillator will automatically start running when the input voltage at AVIN is above the UVLO threshold. The generated clock is continuously compared with a loose on-chip oscillator before being used by the rest of the IC. This way, any clock variations are avoided during startup, invalid clocks are rejected, and sudden loss of the crystal clock is detected. The status of the clock selection can be read out through I^2C.

The oscillator can be disabled through I^2C or by SLP. Without the oscillator clock, all blocks related to the transmitter line-up will no longer be functional but the I^2C, the GPIO routing, the relay and LED drivers as well as the system supplies will continue to operate with the LDO active and the DCDC in Auto Mode.

The OSC1 pin accepts a DC coupled external sinusoidal or squared clock source. When an external clock source is applied the OSC2 pin must be grounded.

System Buck Converter

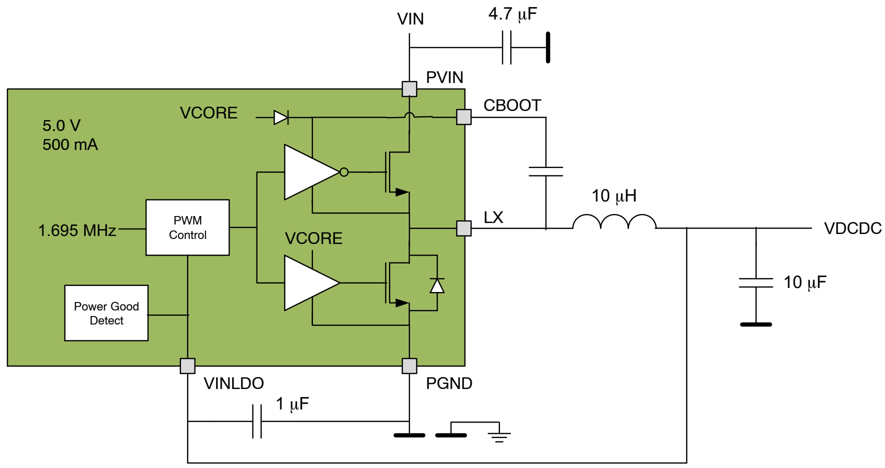


Figure 67. System Buck Converter Topology

The System Buck converter supplies a number of peripherals in the application as well as on-chip circuitry. The output voltage is set to a fixed level and is thus neither programmable nor adjustable.

The Buck converter has a fully integrated NMOS output stage driving the LX pin. The high side NMOS is driven from the bootstrap capacitor connected to CBOOT. The Buck converter is supplied from PVIN and referenced to PGND. PVIN has to be bypassed with a capacitor placed close to the pin to reduce switching noise and improve performance. PGND can be connected to the system ground. The output voltage VDCDC of the Buck converter is directly fed back into the VINLDO pin that serves as the converter feedback pin and LDO input supply pin. For the latter purpose, the signal trace needs to be low impedance and a bypass capacitor has to be placed close to the pin. An external compensation network is not required.

The Buck converter runs on the divided by oscillator clock at the OSC1 pin. At low loading the Buck converter will automatically transition from PWM to PFM mode of operation. When the load increases, the PWM mode is again engaged. In addition to this auto-mode, the PWM mode of operation can be forced through I^2C if desired. In absence of an oscillator clock, the Buck will operate in auto mode based on the loose on-chip clock.

The Buck converter is by default enabled so that the system gets supplied upon application of power. Although not advised, the Buck converter can be disabled through I^2C. When the Sleep mode is engaged through pin SLP, the Buck converter can be left enabled in auto-mode or can be disabled. When disabling the Buck through I^2C, in sleep mode, or as a result of events such as hard system reset or thermal shutdown, a discharge path may optionally be activated on VINLDO to discharge the VDCDC rail.

The output voltage of the Buck is monitored by a power good detection circuit. At startup it serves to signal the output voltage has become in range, while during operation it serves as a brown out detection. In the latter case, when the output of the Buck sags to the power good detection threshold an interrupt is generated and all functional blocks of the IC, except the system Buck converter, the system regulator and the oscillator, will be disabled and their corresponding registers cleared.

In case of the use of an external 5 V supply, the system buck converter may be bypassed. The external 5 V is directly connected to VINLDO and the PVIN and LX pins are left floating with no inductor populated. The buck converter can remain disabled while its discharge path should not be activated in order to avoid unnecessary current drain.

Table 12. RECOMMENDED INDUCTORS

Supplier	Part #	Value (μH)	Size (L × l × T) (mm)	DC Rated Current* (A)	DCR Max @ 25°C (mΩ)
Murata	FDSD0420−H−100M = P3	10	4.2 × 4.2 × 2	3.3	200
Coilcraft	XAL4040−103MEB	10	4.0 × 4.0 × 4.1	3	92.4
Würth Elektronik	74437324100	10	4.45 × 4.06 × 1.8	2.4	243
Taiyo Yuden	MDWK4040T100MM	10	4.0 × 4.0 × 2.0	3.1	194
TDK	SPM4020T−100M−LR	10	4.4 × 4.1 × 2.0	2.3	284

*Based on the inductance change rate (30% below the nominal value).

Regulator

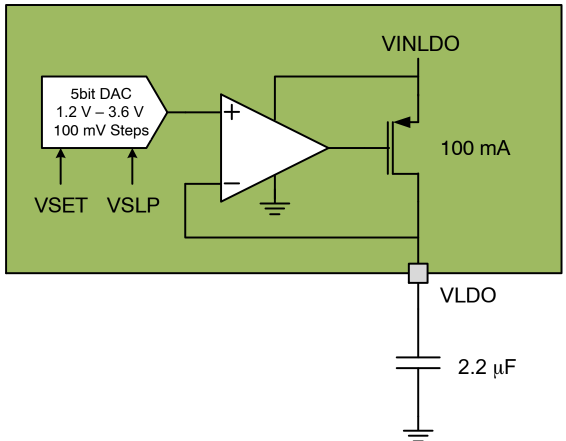


Figure 68. System Regulator Topology

The system Low Drop-Out (LDO) regulator supplies the controller and a number of other peripherals in the application as well as on-chip circuitry. The output voltage is programmable through I^2C and supports Dynamic Voltage Scaling (DVS).

The LDO is supplied from the VINLDO pin and referenced to AGND. VINLDO is shared with the Buck converter feedback line so it cannot be supplied from another supply rail other than the system Buck converter. The output has to be bypassed with a capacitor. No external feedback or compensation networks are required.

The LDO is by default enabled to VSET so that the system is supplied upon application of power. During the power-up sequence, the LDO enabling is gated by the power good detector of the buck converter. When in Sleep mode, the LDO can automatically be set to a preprogrammed lower voltage setting VSLP. This provides the possibility for power reduction by controllers supporting voltage scaling. VSLP can be set equal to VSET if this feature is not desired. Although not advised, the LDO can be disabled through I^2C and automatically disabled when the Sleep mode is engaged. When disabling the LDO through I^2C, in sleep mode, or as a result of events such as hard system reset or thermal shut down, a discharge path may optionally be activated on VLDO.

Current Mode Boost Controller and PA Boost Converter

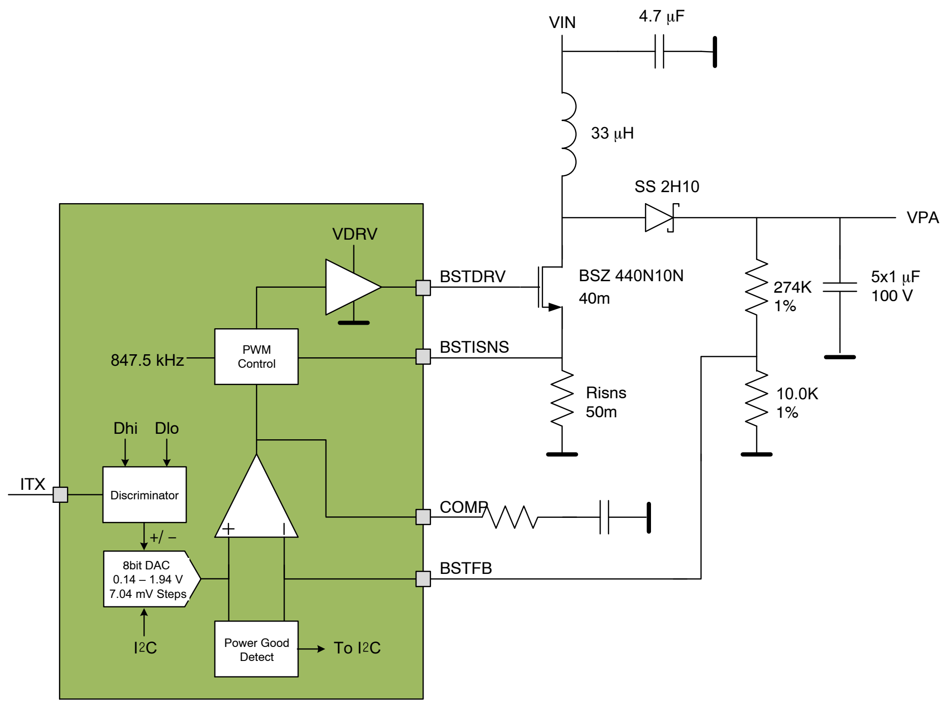


Figure 69. PA Current Mode Boost Converter Topology

Boost Functionality

The PA is supplied from a Boost converter of which the output voltage determines the maximum amount of power transmitted by the PA. The output voltage VPA is set directly by I^2C programming or set indirectly based on a load current discriminator; see end of this section. In both cases, it can be set to the optimum voltage depending on the use case. When changing the output voltage, and as well as during startup and shutdown, the ramp of the output voltage is controlled to eliminate any overshoot or undershoot and it also ensures a soft start that limits the resonator inrush currents. The ramp speed T_{BST} is programmable. In case of voluntary shutdown or in case of fault modes, the output is ramped down at a fast rate T_{BSTDIS} and not at the programmed speed T_{BST}.

The output voltage of the boost converter is monitored through a power good comparator. It will generate an interrupt and indicate through I^2C that the output voltage has reached the programmed value. When the boost is disabled the output is considered as not good. When enabled, the power good signal will only go high once the output has reached the desired output voltage. In other words, during soft start or when a higher output voltage is programmed, the power good signal will temporarily go low. When programming a lower voltage, the power good signal will remain high. In steady state operation the power good detector is insensitive to output voltage variations due to load transients.

Given the output voltage range and the overall power levels involved, the boost is implemented as a controller, driving the gate of a discrete high voltage NMOS connected to the BSTDRV pin, complemented by a discrete Schottky rectifying diode. To keep the high voltages off-chip, the output voltage at VPA is divided down by an external resistor divider before being connected to the feedback pin BSTFB. The Boost converter is based on a fixed frequency PWM with a low side current sensing architecture using a low impedance sense resistor in series with the NMOS and connected to the BSTISNS pin. An adjustable compensation network connected to COMP is required for stability. The ground for the Boost converter is PAGND. The Boost converter can operate in a standard power range or in high power range with the very same set of discrete components. For proper operation, the power range needs to be indicated through I^2C; if not indicated the default range will apply.

The Boost converter is by default disabled which will make its output voltage VPA equal to the input voltage VIN minus the Schottky diode voltage drop. When enabled, the output will start ramping from this output voltage and not from the lowest output voltage setting. The Boost converter can be enabled through I^2C and automatically disabled when the Sleep mode is engaged through the SLP pin. The Boost converter only runs on the divided by oscillator clock at OSC1. In absence of the oscillator clock, the Boost converter is not enabled.

The output current of the Boost converter is limited by means of a current limiter. The current through the low impedance sense resistor R_{ISNS} is measured at the current sense terminal BSTISNS and therefore only limits the peak current into the inductor when actually switching. When a current limit is detected, the boost converter will continue to operate but at minimum duty cycle. Optionally if the current limiting situation persists after 64 cycles the boost converter reference automatically ramps down at its fastest ramp down speed and both boost converter and PA drivers are disabled. In both cases an interrupt is generated. By limiting the output current both the inductor and the PA are protected from overstress. The current limit is programmable through I^2C to adapt to the different end applications. The current limit can be fine-tuned by adjusting the R_{ISNS} resistor.

Table 13. RECOMMENDED R_{ISINS} RESISTOR VALUES

R_{ISINS}	Sense Resistor	Up to 50 W Applications	40	50	60	mΩ
		Up to 12.5 W Applications	–	100	–	mΩ

As an additional safety for the application, a boost output voltage limiter (activated by BSTOVEN = 1) will temporarily halt the boost converter (pulse skipping mode) if the overvoltage detector at the VSNS input of the ADC is tripped, this until the overvoltage condition disappears. Optionally with BSTOVEN = 1 and BSTOVAP = 1, it can also automatically ramp down the boost converter and disable the PA drivers after a debounce period (T_{deb_BSTOV}). In both cases an interrupt is generated. The output voltage limiter uses the ADC input pin and resistor divider network to allow for separate adjustments and to cover for any boost converter resistor divider issues. This safety feature can be enabled and disabled through I^2C. For more details on this protection feature, see the “A-to-D Conversion” section.

For current and voltage protections the sense bits are reflecting the debounced version of the overvoltage and current limit detection. The BSTOVS is set high only after a T_{deb_BSTOV} debounce period. The BSTLIMS is set high only after 64 consecutive cycles of current limiting. Based on the BSTOVAP setting that is known by the software, the interrupt generation BSTOVI and BSTLIMI can be properly interpreted as being an overvoltage and current limit detection only or as a detection followed by a ramp down of the boost and disabling of the PA drivers.

Generally speaking, in case of shut-down due to a fault (Boost Over-Voltage (OV), Boost Over-Current (OC), PA OC, PA Over-Temperature (OT), Peak Detection) or normal shut-down request (Disable, Reset), a fast ramp down (T_{BSTDIS}) of the boost converter is engaged. In normal operation, reprogramming the boost converter for a lower voltage will follow the programmed slow ramp. The use of the different ramp speeds is shown in the diagram below.

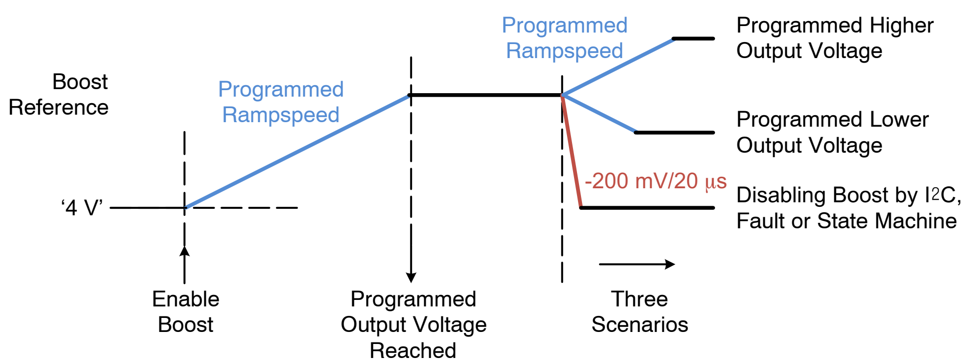


Figure 70. Boost Converter Ramp-Up and -Down Management

Once the boost is ramped down, the PA can be disabled, and if applicable the relay can be put in its default position. Also, in case of a hard system reset, the Buck converter and the LDO can now be disabled followed by the crystal oscillator. Before doing so, it is recommended to disable all other blocks first.

The auto clearing of the I^2C bits takes place at the detection of the event. These bits can be reprogrammed before the boost is totally ramped down. The new I^2C enabling programming will be taken into account at that point so blocks may stay enabled. Boost converter and PA shutdown modes are depicted in detail in the “Power-Up and Power-Down Sequences” section – considering Reset, Fault and Sleep Shutdown cases.

Discriminator Option

The boost converter topology regulates the output voltage based on an amplified reference voltage applied by the 8-bit DAC. This option is provided to control the DAC by an analog voltage at the ITX pin that represents the peak of the transmit current in the resonator. The analog voltage is run through a widely programmable discriminator in order to provide low frequency information to the DAC and the boost controller, thus avoiding instability issues. The discriminator can be operated in window mode, continuous mode and test mode.

The discriminator compares the voltage at the ITX pin with a high threshold Dhi and a low threshold Dlo that are both independently programmable. The comparator samples the input at a programmable interval Titx.

In window mode the boost DAC setting will be incremented at each interval Titx when the voltage is below Dlo or decremented when the voltage is above Dhi. The induced DAC step change Nitx is programmable. When in between both thresholds the DAC setting is left unchanged. In continuous mode, the boost DAC settings are continuously incremented and decremented at the Titx rate such that ITX stays between the Dhi and Dlo thresholds.

The I²C register that normally is used for programming the DAC value is re-used in the discriminator operating modes for clamping the boost voltage to a maximum. The purpose is to avoid the boost converter to rise to its maximum if the ITX signal is not present. The actual DAC setting cannot be read out through I²C, instead the ADC reading of the VSNS channel should be used. The power good comparator will always indicate that the output of the boost converter is in range.

The ramp speed of the boost Tbst is respected during the change, so for Titx to be the dominant factor in the response of the boost converter, the Titx should be set longer than Nitx times Tbst.

In all operating modes, the outputs of the discriminator can be routed to the GPIO1 and GPIO2 pins for verification purposes. In addition, in test mode the discriminator result is not taken into account by the boost DAC. The test mode therefore allows reprogramming of the DAC through I²C as result of the discriminator outputs.

The below diagram shows the overall behavior for the window mode and the continuous mode of operation.

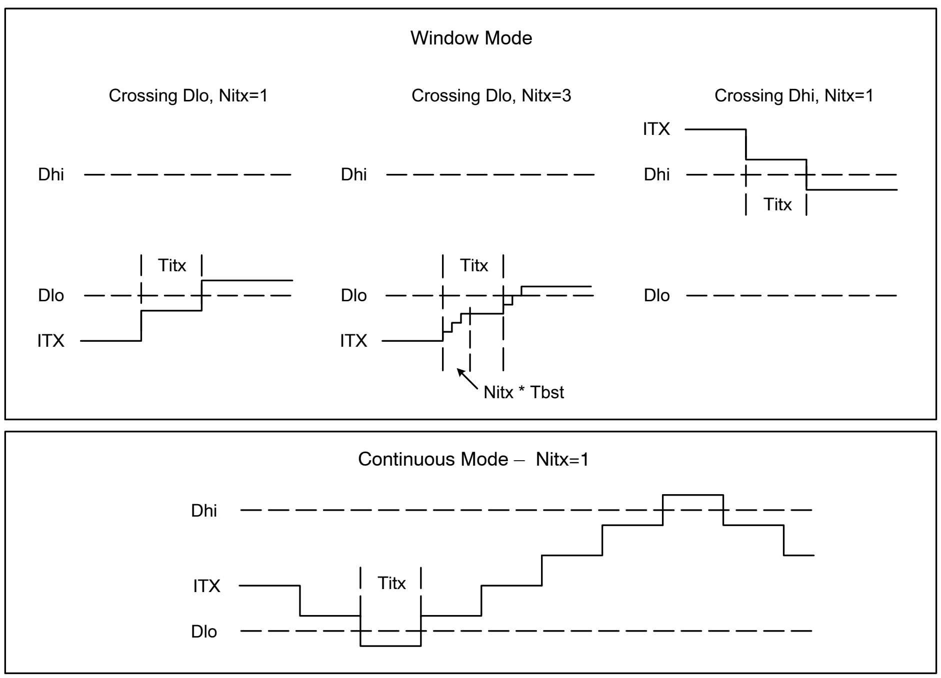


Figure 71. Discriminator Functionality

Power Amplifier Drivers

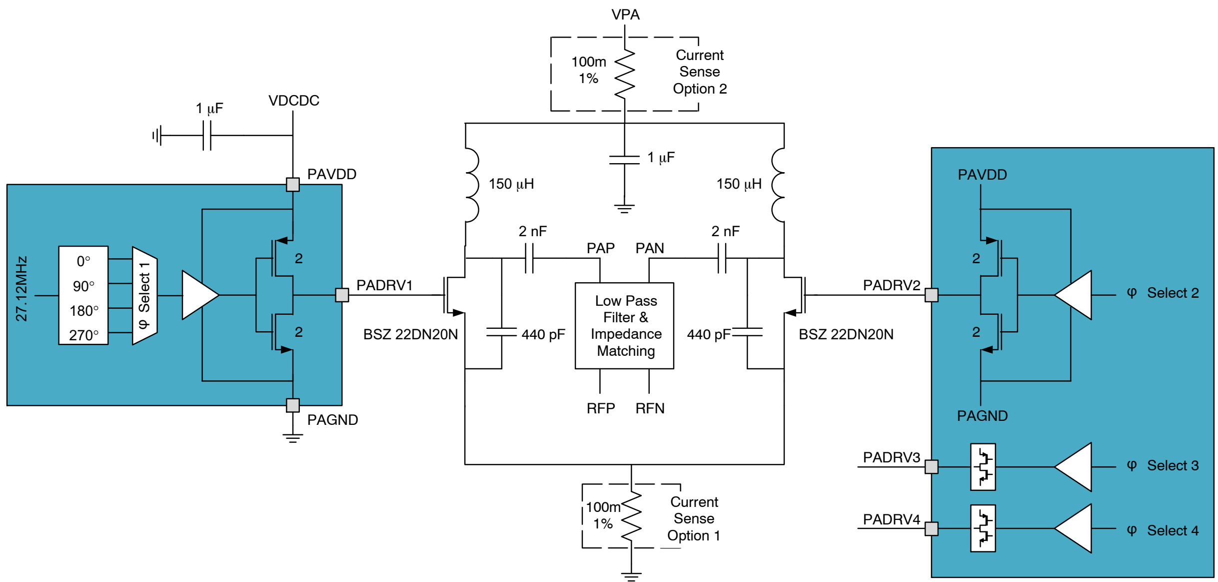


Figure 72. Power Amplifier Driver

The Power Amplifier (PA) is based on a discrete implementation composed of one or two NMOS pairs that convert the VPA supply into a transmit signal. An impedance matching and low pass filtering network is placed between the antenna driver and the antenna itself.

Each driver at the PADRVx pins is connected to the gate of a discrete high voltage NMOS. The outputs are driven high to the PAVDD level and low to PAGND. The PAVDD is connected to VDCDC and bypassed with a capacitor placed close to the pin. The PAGND can be connected to the system ground. In case of low side current sensing a sense resistor has to be placed between PAGND and the system ground.

The PA drivers run at 1/4th of the clock frequency as present at OSC1. To allow for different PA implementations, the phase of each output with respect to the others can be independently selected. Also, each PA driver can be enabled individually. The drive strength of the drivers is programmable while care is taken to match the individual strengths to keep the phase error to a minimum.

The PA driver is by default disabled tying the PADRVx pins to ground, and can be enabled through I^2C. In absence of a valid clock at OSC1 the outputs will be maintained low. In Sleep mode, the PA driver can be disabled.

The PA drivers and the PA Boost will in most cases be enabled together. To allow doing this in a single I^2C access, a PA Driver master enable bit is located with the PA Boost enable bit in addition to the individual enable bits. In cases where the PA Boost needs to be present before PA enabling, the PA enabling can be gated by the power good of the Boost converter (PAMPG). Once established, the power good of the boost converter will have no more influence on the PA enabling. This feature avoids I^2C access in−between the enabling of both blocks.

The current consumed by the PA line-up is an indication of the overall efficiency and the amount of power provided by the Boost converter. This current can be measured for the entire line-up at the output VPA. Given the high voltage levels and the accuracy in play, this requires a 60 V robust current sense solution (option 2 in the above diagrams). As an alternative a low side current sense at the PA ground can be used (option 1 in the above diagrams).

The current sense is also used to protect the PA from over-current situations. When detected an interrupt is generated. Optionally, the Boost converter can be ramped down and the PA drivers disabled. This safety feature can be enabled and disabled through I^2C. For more details on the current sense circuitry and the protection feature, see the “A-to-D Conversion” section.

An additional protection for the PA is provided by means of a time out feature. When the PA and the Boost converter are both enabled a timer is started. The timer is reset upon I^2C access to the boost and upon access to the PA registers. In absence of an I^2C access, the timer will time out and a hard reset cycle is engaged including the ramp down of the boost converter and disabling of all supplies. By default this protection mechanism is disabled.

Impedance Control Drivers

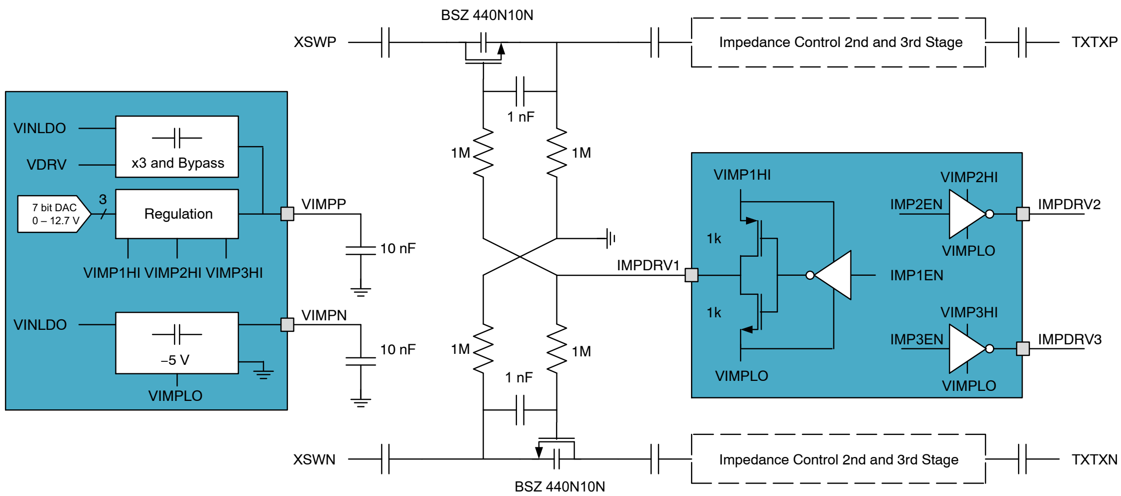


Figure 73. Impedance Control Driver

The impedance of the antenna line-up can be changed by turning on/off the impedance control NMOS transistor pairs. The NMOS pairs are made conducting or non-conducting through the impedance control drivers. By the cross–coupled arrangement of the NMOS pair, only a single differential driver is required per pair. Up to 3 NMOS pairs are supported, each can be controlled independently.

Starting from the VINLDO node, an embedded charge pump generates a negative voltage on VIMPN and a boosted voltage at VIMPP. Both supplies are bypassed with a capacitor on board. From VIMPP three independent regulated drive supply rails VIMP1HI, VIMP2HI and VIMP3HI are created, one for each of the impedance drivers. The VIMPxHI rails are programmable and referenced with respect to ground, not to VIMPN. This allows an alternate drive scheme for ground referenced tunable filter arrays.

The impedance control driver output IMPDRVx is a push-pull architecture that can swing between VIMPxHI and VIMPLO. A selector allows VIMPLO to be routed to the negative charge pump VIMPN or to ground. When using discrete NMOS pairs to control the impedance, VIMPN is selected. This forces the NMOS pair off even with the presence of large signals in the circuitry. When using tunable filters, the ground is selected for VIMPLO. For both configurations, a bypass mode is available that allows connecting VIMPP directly to VDRV. Changing the modes on the fly is not allowed.

Since the voltage swing in the antenna line-up can be as high as 100 Vpp, the impedance control driver signals are connected to the NMOS pair through an RC network to keep the higher voltages off-chip. The source of the NMOS pairs is connected through the same RC network to ground.

The impedance control drivers and the charge pump are by default disabled tying IMPDRVx to ground with an output impedance seen from the pin IMPDRVx of about 1 kΩ. Of course this applies also when the impedance control drivers are turned off through the master enable bit, IMPMEN.

When the charge pump is enabled, the drivers will make the output Low or High based on the I^2C controlled IMPxEN signal. In Sleep mode, the impedance control drivers and the charge pump can be disabled.

Relay Driver

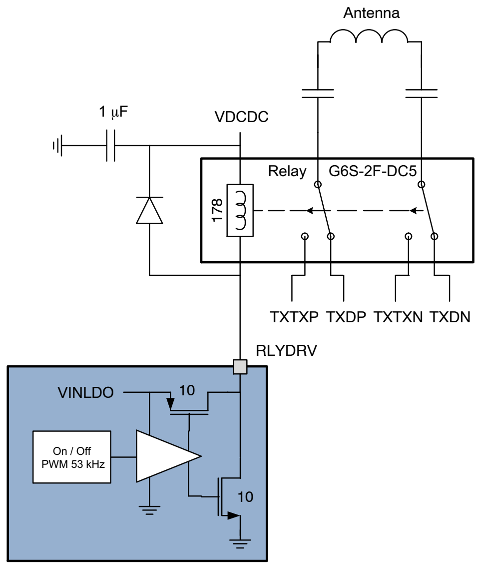


Figure 74. Relay Driver

The antenna can be either connected to the PA line-up or to the peak detectors. In the first case the application is transmitting power, in the second case it is measuring the presence of any incoming power. The selection between both routings is done through a relay as shown in above diagram.

The relay is driven from the RLYDRV pin where the relay-coil is supplied from VDCDC. When asserting the relay, a current will be established through the relay-coil that exceeds the pick-up current and as a result the relay switches over. When de-asserting the relay, this current is absorbed by a freewheeling diode. The freewheeling diode can be embedded in the relay or otherwise added to the application.

Once the relay is switched the current through the coil can be reduced to save on power while maintaining the relay state. To this end, the output driver will, after an initial delay Tpu, apply a PWM signal at its output at a programmable duty cycle. The PWM duty cycle directly reduces the average coil current. During the off periods of the PWM signal the coil current circulates through the on-chip FET connected between RLYDRV and VINLDO, and thus VDCDC. This circulation phase further reduces the power as taken from VDCDC. By setting the PWM duty cycle to 100% the full relay current will continue to flow. The PWM clock is derived from the crystal clock or from the loose on−chip clock if the crystal clock is not present.

In case the relay is broken, no current will flow through the relay driver when activated. When this condition is detected an interrupt is generated.

The relay driver is by default disabled and can be enabled through I^2C. In Sleep mode the relay driver can be maintained even in absence of the XTAL based clock. It can also be disabled in which case the relay takes its default position. The relay driver is supplied from VINLDO, so from VDCDC, and referenced to AGND.

LED Drivers

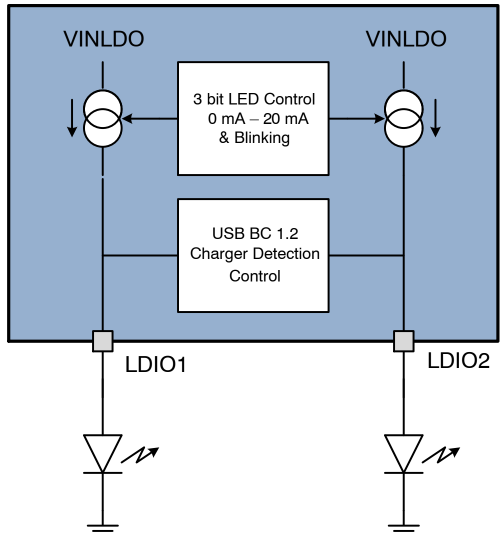


Figure 75. LED Drivers or USB BC 1.2

Two general purpose signaling LED drivers provide the possibility to indicate the state of operation of the unit. Typically a red and a green LED are connected although the available voltage headroom also allows for the connection of blue, white or bright green LEDs.

The LED drivers at LDIO1 and LDIO2 are composed of high side current sources supplied from VINLDO, which allows the cathode of the LEDs to be connected to the system ground. The current sources are programmable independently in order to adapt the LED current to the type of LED connected.

An interrupt is generated when an open or a short is detected at one of the LED driver outputs. The driver itself is not automatically disabled.

With the LED drivers, basic low frequency blinking patterns are provided. Though independently programmable, the blinking patterns of both LEDs are maintained synchronous. Typical patterns would be an alarm indication with a very short on period and very fast repetition rate, an in progress indication with a short on period and fast repetition rate, or a standby indication with a very short on period and very slow repetition rate. The blinking patterns are based on the loose on-chip clock. The current source enabling and disabling is slewed in order to avoid perturbations on the neighboring crystal oscillator block.

By default the LED drivers are disabled and LDIO1 and LDIO2 pins are high impedance. The LED’s can be enabled through I^2C at the desired current level and desired pattern. In Sleep mode the drivers can be disabled but also maintained active with the same settings as in normal operating.

USB BC 1.2 Detection

In addition to LED drivers functions, the LDIO1 and LDIO2 pins can also be configured for USB BC 1.2 charger detection and signaling.

To detect the type of charger a primary and secondary detection on the D+ and D− lines is necessary. During primary detection a voltage VD_{SRC} is applied to D+ (for instance LDIO1) while a current sink IDSINK is activated at D− (for instance LDIO2). The voltage at D− is compared versus V_{DATREF} and a logic low or high is reflected by the same sense and interrupt bit as used for the LED fault detection. During secondary detection the roles of D+ and D− are reversed. A single set of source, sink and comparator is embedded while their activation and assignment to pin LDIO1 and/or LDIO2 is fully under I^2C control; no timers or state machines are included. The below table summarizes above detection mechanism, for more details, see the USB BC 1.2 charger specification.

Table 14. USB BC 1.2 DETECTION

Detection Phase	D+	D−	Detection	USB Port Type
Primary	VD_{SRC}	IDSINK	D− < V_{DATREF}	SDP or standard USB port. End of detection.
			D− > V_{DATREF}	Go to secondary detection phase.
Secondary	IDSINK	VD_{SRC}	D+ < V_{DATREF}	CDP or high power USB port.
			D+ > V_{DATREF}	DCP or high power wall charger.

A-to-D Conversion

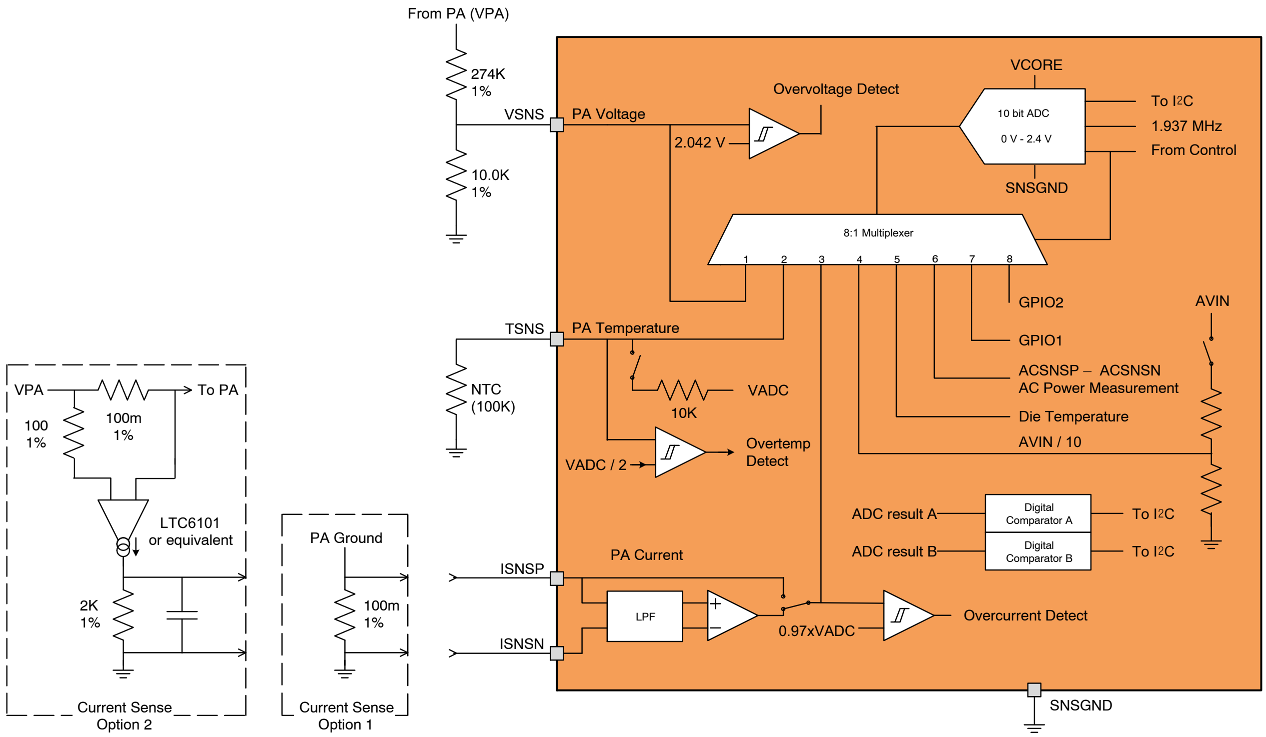


Figure 76. A-to-D Converter

Introduction

Different voltage and current levels in the application can be measured with the 10-bit A-to-D converter (ADC). The conversion results are stored in I^2C registers as 10-bit values. Conversions can be executed upon demand or in an automated fashion. Digital comparators are provided on some channels.

The ADC is supplied from a local supply voltage derived from the core voltage V_{CORE}. This allows stable operation even in critical V_{CORE} supply conditions. The ADC is referenced to SNSGND. The ADC requires the presence of a valid clock at the OSC1 input. The ADC is entirely controlled through I^2C. The ADC can automatically be disabled in sleep mode or continue operating as configured for normal mode.

Input Channels

A divided by version of VPA is measured at VSNS. It can be used to verify the actual VPA voltage level. This is in addition to the power good detection of the PA Boost converter. The VSNS channel is also used as the boost overvoltage detection input. The detector level is fixed, but the ratio of the scaling network at VSNS can be different from that of the boost converter and therefore determines the effective overvoltage detection level.

The PA Current is measured as an amplified voltage drop over a sense resistor. Three options are available in the application: Low Side sense, High Side sense and ByPass sense.

The Low Side sense uses a sense resistor placed between the PA ground and the system ground. The High Side sense uses a sense resistor placed in the PA Boost converter supply line. In this case, a discrete current sense circuit will have to be used to convert the High Side differential voltage into a Low Side referred differential voltage. In both the Low and High Side sense cases, the differential voltage between ISNSP and ISNSN is amplified and Low Pass filtered to filter out any switching noise from the Boost converter and the PA before being converter by the ADC.

The ByPass sense option bypasses the differential amplifier and connects the input ISNSP directly to the ADC without amplification and filtering. The externally amplified signal is to be referenced to the SNSGND.

The ISNSP-ISNSN channel is also used as the PA over-current detection input. The detection level is fixed, but the amplifier gain and the value of the external sense resistor determine the effective detection level.

The PA temperature is measured by means of an NTC (negative temperature coefficient) sense resistor connected to TSNS. The NTC is biased through an internal pull-up resistor to the VADC level. To avoid the NTC being biased in low power modes, the pull-up can automatically be disconnected based on the SLP signal. It is possible to leave the internal pull up unconnected to allow for an external pull up arrangement.

Based on the ADC readings, the PA temperature is monitored by software and corrective actions can be taken if necessary. As an additional safety, the voltage at TSNS is monitored by a comparator that trips in case of a too low voltage at the TSNS pin. The low voltage can be caused by a very high PA temperature or by a missing NTC. When detected, an interrupt is generated and optionally the boost converter can be ramped down automatically and the PA disabled. The detection level is fixed but by proper selection of the NTC and by adding a series resistor the effective trip temperature can be adjusted. This safety feature can be enabled and disabled through the I^2C.

A scaled version of the supply input voltage at AVIN can be measured at channel 4. The voltage is scaled with a resistive network. To avoid unnecessary current consumption through the network, it is only enabled upon I^2C command and only during conversions.

The die temperature can optionally be measured at channel 5 as a voltage over a series of diodes. The diodes are biased such that the resulting voltage exhibits a near constant negative temperature coefficient over the temperature range of interest.

The AC Power is measured differentially at the output of the AC Power measurement solution. The converted result is available as a signed 10-bit value. See the “AC Power” section for more details.

The inputs GPIO1 and GPIO2 are converted without any scaling or filtering.

The boost overvoltage, PA over-temperature and PA over-current detection circuits as well as the necessary pre-amplifiers can be maintained enabled independently from the ADC activity.

Operating Modes

The ADC can be operated in two different modes: trigger mode and auto mode.

In trigger mode the ADC conversion is started after an I^2C initiated request or based on the SLP pin activity. In both cases a programmable delay T_{WAIT} is applied before starting the conversions that allows the local supply, its references and the input stage to stabilize first. The delay also allows aligning the conversion to specific events. In trigger mode a selected channel can be converter once or 8 times, all 8 channels can be converted in sequential order or all 8 AC power measurement combinations. When the conversion is finished, a conversion done interrupt is generated and the ADC core and its references are disabled.

In auto mode ADC conversions take place at a programmable repetition rate T_{ADRATE}. This ensures the latest ADC results are always available through I^2C. In the auto mode one can convert all 8 channels in sequential order, or all 8 AC power measurement combinations. At the end of each conversion cycle a conversion done interrupt can be generated and the ADC core is disabled.

The different timings and sequencing of the A-to-D converter are shown in the diagram below:

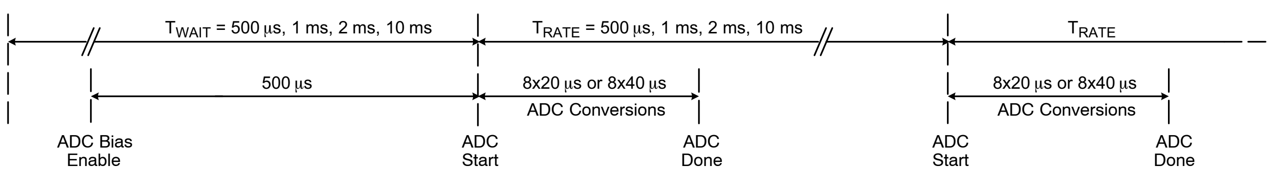


Figure 77. A-to-D Converter Timings

The ADC result registers of the I^2C are used to store the results of each channel or the result of the 8 single channel measurements or 8 AC power measurements. In the first case every channel result is stored in the related register, for example PA voltage is stored in result register 1, PA temperature in register 2, etc. In the second case the 8 results will be stored in a sequential fashion in result register 1 to 8. Storing 8 results for a single channel allows software to average the result or to eliminate noise and other variations.

The conversion results in the I^2C registers get updated when the ADC conversion is finished. In case of for instance 8 AC power measurements, the I^2C contents are updated only after the 8 combinations have been converted. The contents will not be updated while an I^2C read of the ADC results is ongoing in which case the update takes place once an I^2C stop bit has been detected. Therefore, to guarantee that all 8 results are originating from the same set of conversions, the ADC results should be consulted by using the I^2C consecutive read option. All results will be cleared to zero when entering sleep mode in case the ADC was configured for being disabled in sleep mode.

In addition to the conversions themselves, the result can also be compared to an 8-bit reference value pre-programmed through the I^2C. This is also referred to as digital comparator. Two digital comparators A and B are available that can be assigned to the PA voltage, PA temperature, PA current, GPIO1 (A) or GPIO2 (B).

The digital comparator output is by default reflected through an I^2C sense bit. When the sense bit value changes from either low to high or from high to low, an interrupt is generated. The sense bit can be debounced by a 7-bit programmable debounce counter CNT. The CNT can be started on the rising or the falling edge of the comparator output transition. The sense bit will now only change value after the ADC yields a stable result during CNT conversions. The digital comparators are therefore particularly useful in auto conversion mode where the T_{RATE} serves as the time tick for the CNT.

The below diagram show an example where the two digital comparators are assigned to a single channel (the PA Current Sense) and where they are configured for detecting a pulse of PA Current of a given duration.

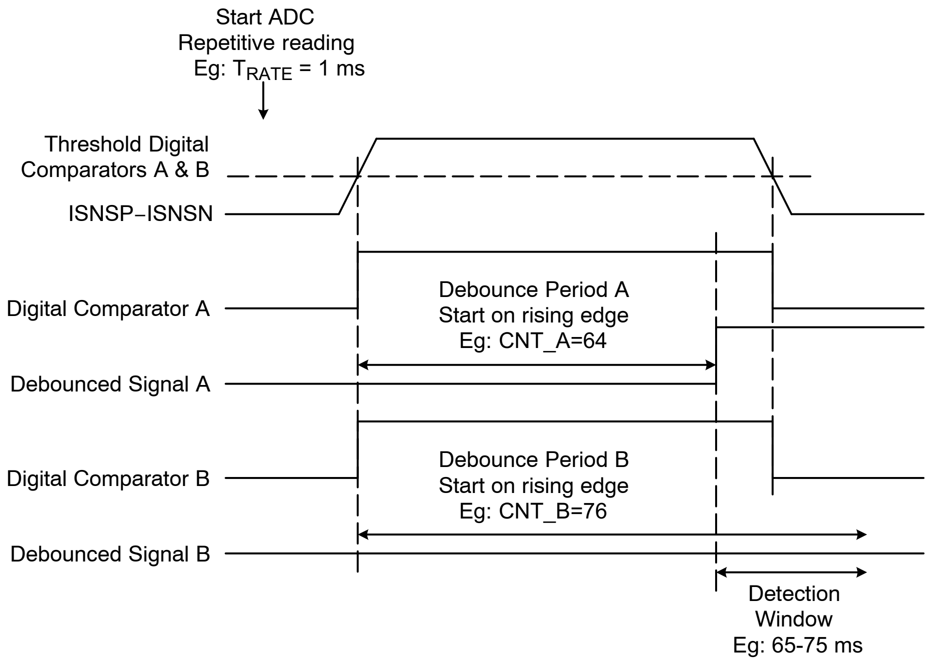


Figure 78. Diagram Comparator Use Case Example

AC Power Measurement

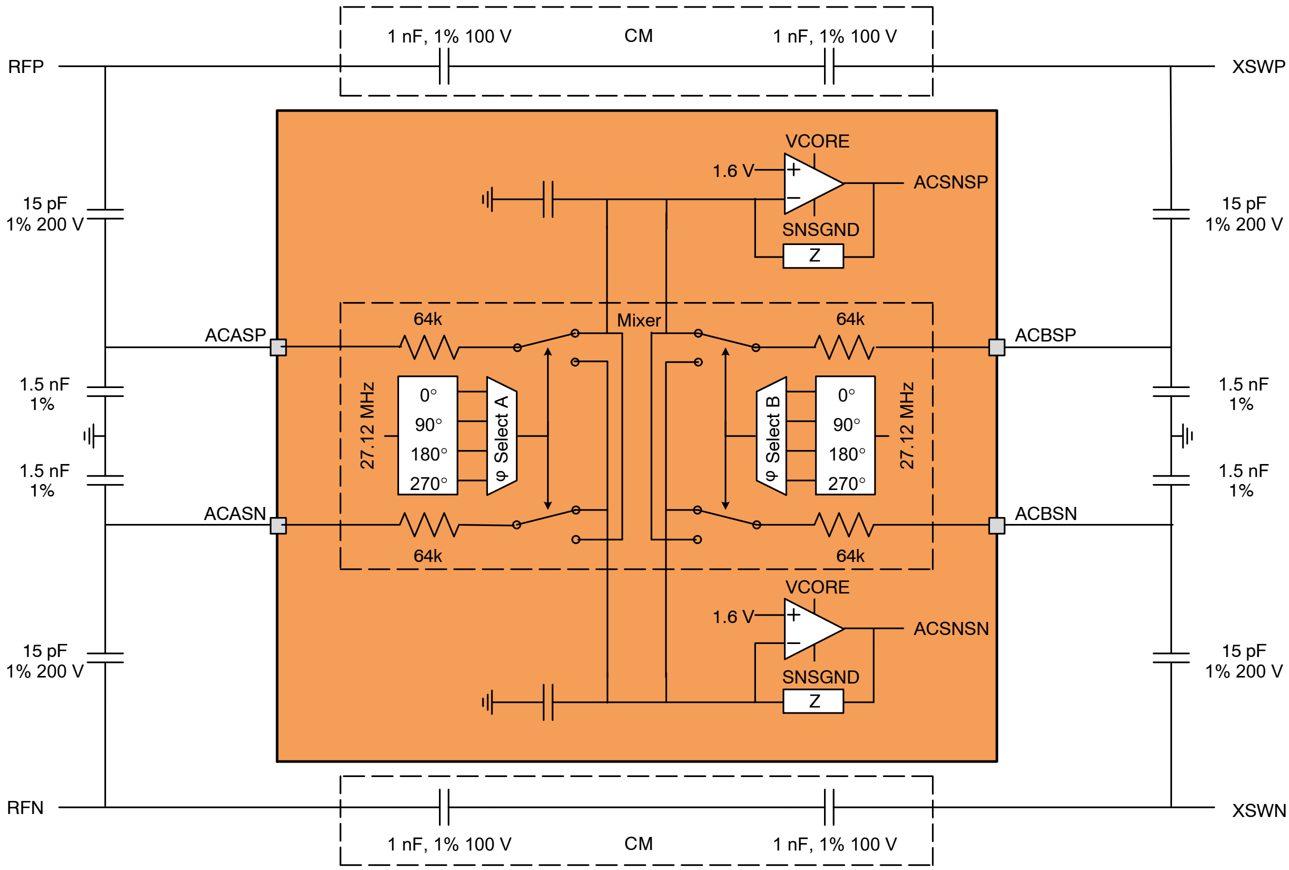


Figure 79. AC Power Measurement

The AC Power that is transmitted to the antenna is measured by means of the CM capacitance (also called Series Measurement Capacitor) that is inserted in the antenna line-up. The power is calculated by multiplying the AC voltage on the line-up by the current through CM. Using a capacitive element instead of a resistive element provides a lossless method to derive both the real and imaginary parts of the power. The measurements are done differentially on the positive rail (P measurement) and the negative rail (N measurement) in order to compensate for any imbalance in the line-up.

The voltage levels at RFP, RFN (the A measurement) as well as XSWP, XSWN (the B measurement) can be as high as 100 Vpp. The voltage is therefore first divided by precise capacitors with a ratio in the order of 1:100. The divided by signal is then connected to the respective input pins ACASP, ACASN, ASBSP and ACBSN. These input signals are switched and summed by a quadrature mixer to a set of programmable inverting voltage amplifiers with outputs ACSNSP and ACSNSN. The signal from the quadrature mixers is second order low pass filtered to remove the high frequency by-products of the mixer.

The quadrature mixer consists of 4 clocked switches. Each switch routes an input to one of the two inverting voltage amplifiers. The switches for the P and the N measurement always run in opposite phase. The switches for the A and B measurement can be phase shifted by 0°, 90°, 180° or 270°. The four phase shifted clocks are derived from the oscillator clock resulting in a switch clock that is identical to the PA transmission frequency plus a constant phase shift. Not all combinations of the A and B phase shifted clocks can be selected but only those that relate to the measurement of the actual I and Q signals, respectively the four 0° and 180° and the four 90°C and 270°C combinations.

The quadrature mixer and the amplifiers are supplied from V_{CORE} and referenced to SNSGND. By default the block is disabled. Its biasing, which preloads its inputs ACASP, ACASN, ACBSP, ACBSN to the internal common mode, must be enabled through the I^2C at least T_{EN_ACM} (see Electrical Characteristics table) before running a first AC power conversion. In Sleep mode the block can be disabled.

Peak Detectors

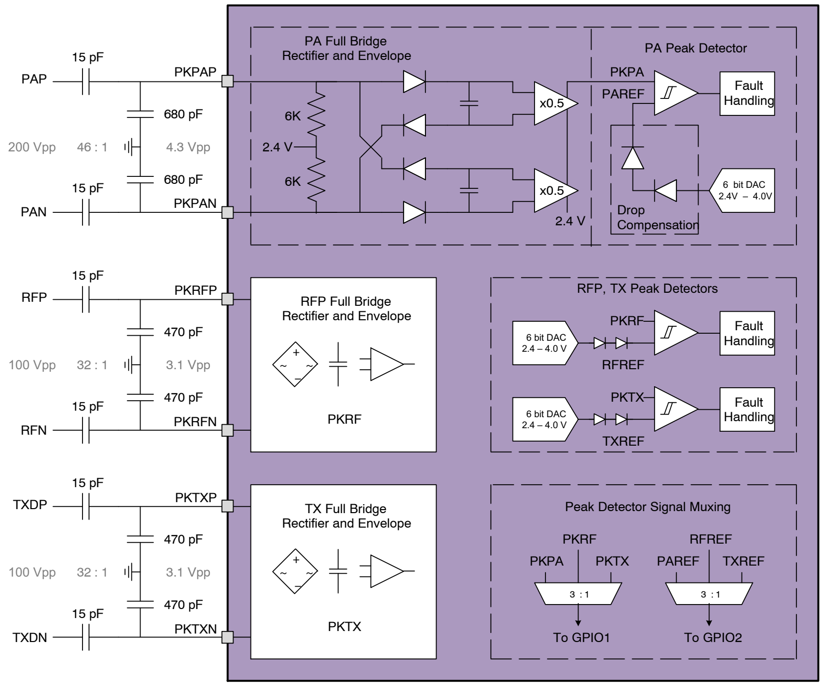


Figure 80. Peak Detectors

The signal voltage on the transmitter line-up is permanently monitored by a set of programmable peak detectors. This allows for detection of signals received by the antenna in case of the PA is not transmitting (TXDP, TXDN) and for detecting any unexpected overvoltage while transmitting (PAP, PAN at the PA outputs and RFP, RFN after the impedance matching filter). The measurements are done differentially and full bridge in order to compensate for any asymmetry in the line-up.

The voltage levels at RFP, RFN and TXDP, TXDN can be as high as 100 Vpp while PAP, PAN can even reach 200 Vpp. The voltage is therefore first divided by precise capacitors with a ratio in the order of 50:1. The divided by signal is then connected to the respective input pins PKRFP, PKRFN, PKTXP, PKTXN and PKPAP, PKPAN. Given the high frequency nature of the signals, the input voltage itself cannot be directly fed into the comparators of the peak detectors. First a lower frequency full bridge rectified peak-to-peak envelope signal is created. The full bridge signal is composed of the sum of the positive excursions and the negative excursions divided by two. The peak-to-peak envelope is compared to a programmable reference. The rectifier introduces diode drops on the envelope signal which is compensated at the reference side. Each of the 3 inputs has its own independently programmable reference DAC, diode drop compensation and comparator. For test purposes, the envelope of each peak detector as well as the reference can be routed to respectively the GPIO1 and GPIO2 outputs.

The peak detectors are supplied from V_{CORE} and referenced to SNSGND. By default the block is disabled and must be enabled through the I^{2}C. In Sleep mode the block can be disabled. When disabled the inputs are internally connected to ground.

Table 15. PEAK DETECTORS AUTO PROTECTION BEHAVIOR

State		**Peak Detect** (Note 47)		**Action**	
VPA & PA	**Relay**	**PAP−PAN/RFP−RFN**	**TXP−TXN**	**VPA & PA**	**Relay**
ON	ON	Hi	–	Power Down Cycle (Note 48)	Stays ON
ON	OFF	Hi	Hi	Power Down Cycle (Note 48)	Stays OFF
OFF	ON	Hi	–	Block Enabling (Note 49)	Turn OFF
OFF	OFF	–	Hi	Block Enabling (Note 49)	Stays OFF

47. PAP−PAN/RFP−RFN stands for a logic OR of the output signals of the related detector outputs.
48. Clears PA Driver and Boost converter enable bits, ramps down the PA Boost converter entirely followed by a disabling of the PA drivers. The enable bits can be set through I^{2}C during the ramp down cycle but will only be taken into account after the ramp down cycle has finished.
49. The enable bits can be set through I^{2}C but will only be taken into account when the fault condition is no longer present.

Impedance Control Detectors

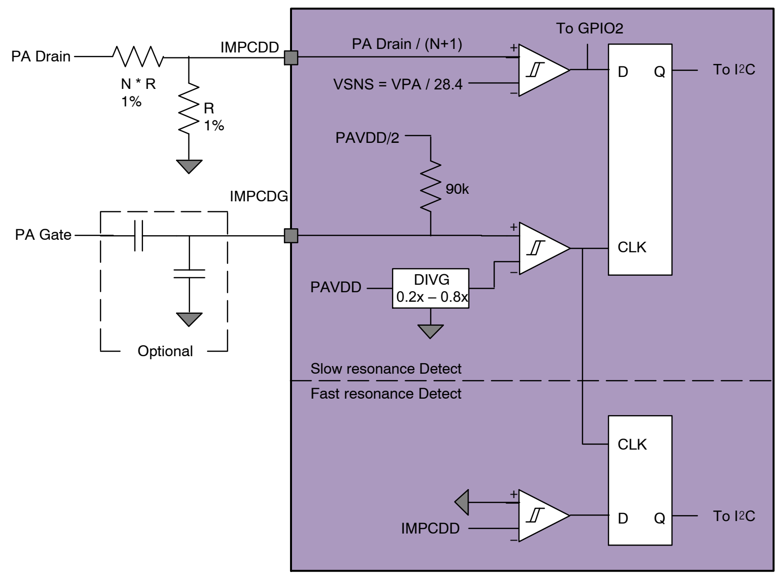


Figure 81. Impedance Control Detect

The Class E Power Amplifier operation relies on proper resonance of its output resonance network while the resonance frequency is affected by the load presented to the antenna loop. When the natural resonance frequency is not exactly 6.78 MHz then the FETs of the PA may be turned on while the drain is already below zero (clamped by the body diode) or still at a high voltage level. In particular in the latter case the efficiency of the PA is degraded by the forced discharge of the drain to source resonance capacitor. Therefore, in addition to the PA drivers and the impedance control drivers, an impedance control detector is provided. The purpose of this detector is to verify that the natural resonance frequency of the network does stay near the 6.78 MHz. When a deviation is detected, an interrupt is generated and action can be taken by the system software such as readjusting the impedance of the PA line-up.

In addition, when an object is placed in the reach of the antenna, its impedance strongly changes the resonance frequency which is easily detected by the impedance control detection circuit as well. A capacitive load will increase the resonance frequency and an inductive load will decrease it.

The impedance control detection circuit is divided in a slow resonance detection block and a fast resonance detection block.

The slow resonance detect consists of two high speed comparators and a D flip-flop. One comparator takes a divided by version of the PA FET drain signal at input IMPCDD and compares it to a divided by version of the PA Boost output voltage as measured at VSNS. Its output is connected to the D input of the flip-flop and is routed to the GPIO2 output. A second comparator takes the PA FET gate signal at input IMPCDG and compares it to a ratio of the gate drive voltage PAVDD. The input IMPCDG is biased at PAVDD/2 to allow capacitive coupling of the PA FET gate signal. Its output is connected to the CLK input of the flip-flop. As a result, when the drain signal is too high at the moment of the rising edge of CLK, the Q output of the flip-flop will go high.

The fast resonance detect consists of one high speed comparator and a D flip-flop that uses the same clock signal as the slow resonance detector. The comparator takes the signal at IMPCDD and compares it to ground. When the drain signal is below zero at the rising edge of CLK, the output of the flip-flop will go high.

An interrupt is generated when the out-of-resonance event has been detected. The type of resonance shift is determined by combining the reading of the interrupt bit (read then cleared) with the reading of the corresponding sense bit according to the below table (see also I^2C Register Map description). If needed two additional sense bits (IMPCDFS & IMPCDSS) are available in the Impedance Control Register map section (*Impedance5* Register) to sense real time the type of resonance shift.

Table 16. OUT-OF-RESONANCE DETECTION PROCESS (SEE I²C REGISTER MAP)

Condition	IMPCDS	IMPCDI	IMPCDFS	IMPCDSS
No Detect	Keep previous fault event	No Change to Interrupt Bit	0	0
Slow Detect	1	Set 1, can be Cleared by Software	0	1
Fast Detect	0	Set 1, can be Cleared by Software	1	0

As soon as the interrupt is generated and the type of shift identified, the impedance of the PA line-up can be readjusted by the system.

The impedance control detection circuit is supplied from V_{CORE} and referenced to AGND.

When disabled the bias circuitry at IMPCDG is also disabled. When enabling the detection circuit a power up sequence is applied to avoid the generation of any false interrupts.

By default the impedance control detection block is disabled and must be enabled through the I^2C. Fast and slow resonance detection functions can be disabled independently. In Sleep mode the block can be disabled and the IMPCDSLP corresponding bit applies on both functions. When disabled the bias circuitry at IMPCDG is also disabled. When enabling the detection circuit a power-up sequence is applied to avoid the generation of any false interrupts.

GPIOs

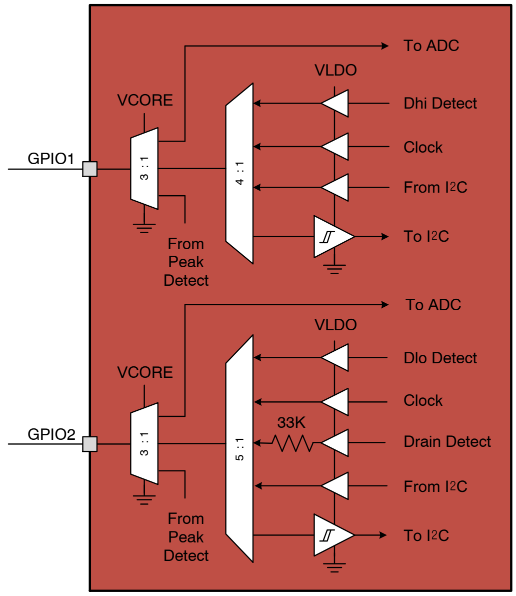


Figure 82. GPIOs Routing and Multiplexing

Two general purpose IO's are provided as GPIO1 and GPIO2. These pins can be independently configured as an input or as an output.

When configured as an input, the signal can be either routed to the ADC for conversion or detected as being a logic low or logic high. The logic input detection is signaled through dedicated I^2C sense and interrupt bits.

When configured as an output, the signal can be forced Low or High through I^2C programming. It can also route out the clock as present at OSC1 or the divided by 4 version. In addition the output of the drain signal comparator can be routed to GPIO2 and optionally to the ADC input at the same time. A small external bypass capacitor filters the high frequency components such that the DC value representing the duty cycle of the comparator output can be read by the on-chip ADC.

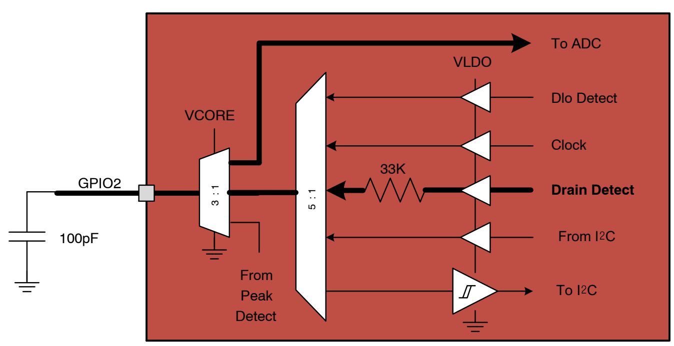


Figure 83. Fast Resonance Detection Implementation Scheme using GPIO2 and Internal ADC

For testing purposes, the boost converter discriminator signals and the peak detector envelopes can be routed out as well; Dhi and peak detector envelopes to GPIO1 and Dlo and peak detector reference to GPIO2.

The GPIO1 and GPIO2 pins and their interface can be disabled when entering sleep mode through the SLP pin. When not disabled it allows maintaining the routing as configured for normal operation, for instance maintaining a logic high on one of the outputs.

Control & I^{2}C Interface

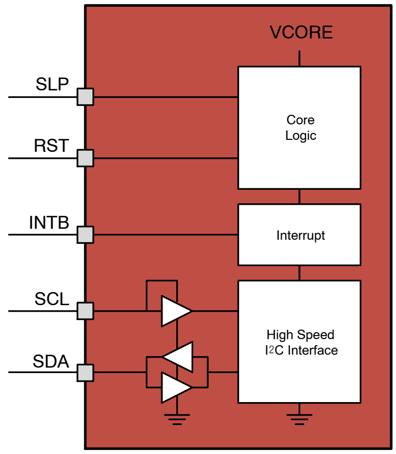


Figure 84. Control and I^{2}C Interface

The device is programmable through the I^{2}C interface. The interface follows the I^{2}C standard for high speed devices thus supporting 400 kHz and 3.4 MHz operation and supports consecutive read and write access for reduced traffic overhead. The interface at SDA and SCL is referenced with respect to a locally generated supply as a function of the peak voltage of the SCL and SDA lines. The internal logic of the IC is supplied by the core circuitry and as a result will be held in reset for an input voltage below the UVLO threshold.

The I^{2}C bus is an addressable interface. To avoid bus conflicts with other devices, four addresses are available through factory fuse. In addition, the MSB of the I^{2}C address can be changed in application by software. The device only supports 7-bit addressing.

The IC can be operated in sleep mode by making the SLP pin high (default polarity). As a result a low power mode is entered in which each individual block is disabled, put in a low power state or left enabled. The operating mode as a function of the SLP pin is set through the I^{2}C for each block independently. The polarity of the SLP pin can be changed through the I^{2}C.

The IC can be reset by making the RST pin high. The RST pin is debounced to avoid false triggering. Once a valid reset is detected a power down sequence is engaged where all blocks get disabled sequentially and the I^{2}C contents reset (hard reset). Optionally the system buck converter and regulator can be maintained active during the reset (soft reset). During a soft reset the bits related to the DCDC, the LDO and the I^{2}C address are not reset. When the RST pin is low, and after the power down sequence has ended, the part will generate an interrupt, RSTI, which is not reset in order to be acknowledged by the processing unit (CPU) after the CPU has restarted. On the other hand the interrupt mask bit, RSTM, is reset in order to avoid having an interrupt request occurring during CPU start-up. In case of hard reset the part will enable the buck converter and regulator again, see also the “Power Up/Down Sequence” section. The crystal oscillator keeps running during the reset period.

The state of the IC can be read out through a series of sense and latched interrupt bits partitioned over several registers. For a rapid high level identification of the interrupt source, a single status register is provided reflecting the state of each IC function. If desired, each interrupt bit that is set can be reflected on the INTB pin in which case the INTB pin will be made active low (default polarity). In this way, continuous software polling on the I^{2}C bus for important events is avoided. At the opposite masked sources will have no influence on INTB pin. The polarity of the INTB pin can be changed through the I^{2}C. Interrupt registers are automatically cleared to 0 by an I^{2}C read. When the host reads the Interrupt registers and if all fault events are cleared the INTB pin is released to high impedance.

Figure 85 illustrates the general Interrupt process; Figure 86 details the specific interrupt process related to the Analog-to-Digital Converter operating in Auto-Mode.

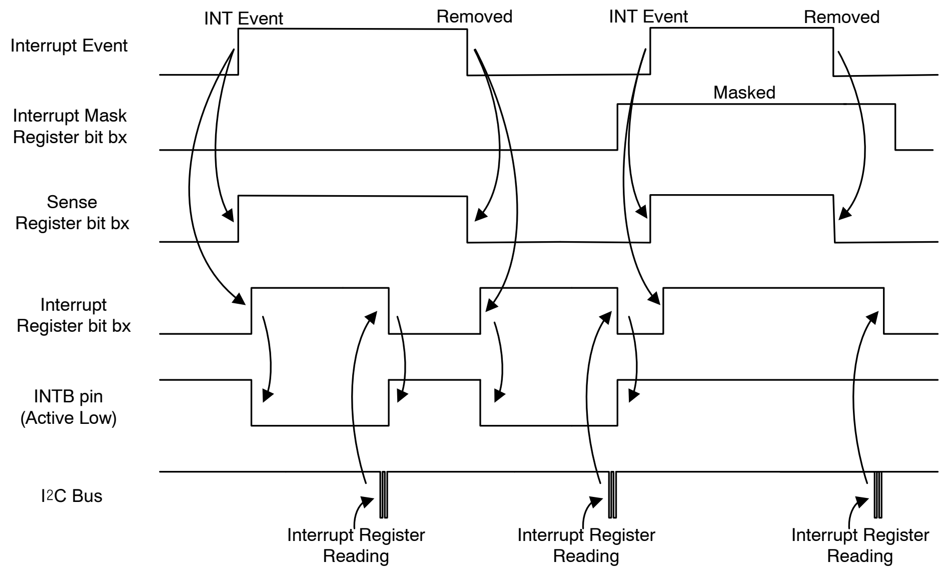


Figure 85. Interrupt Operation Example with INTB Active Low (Default Polarity)

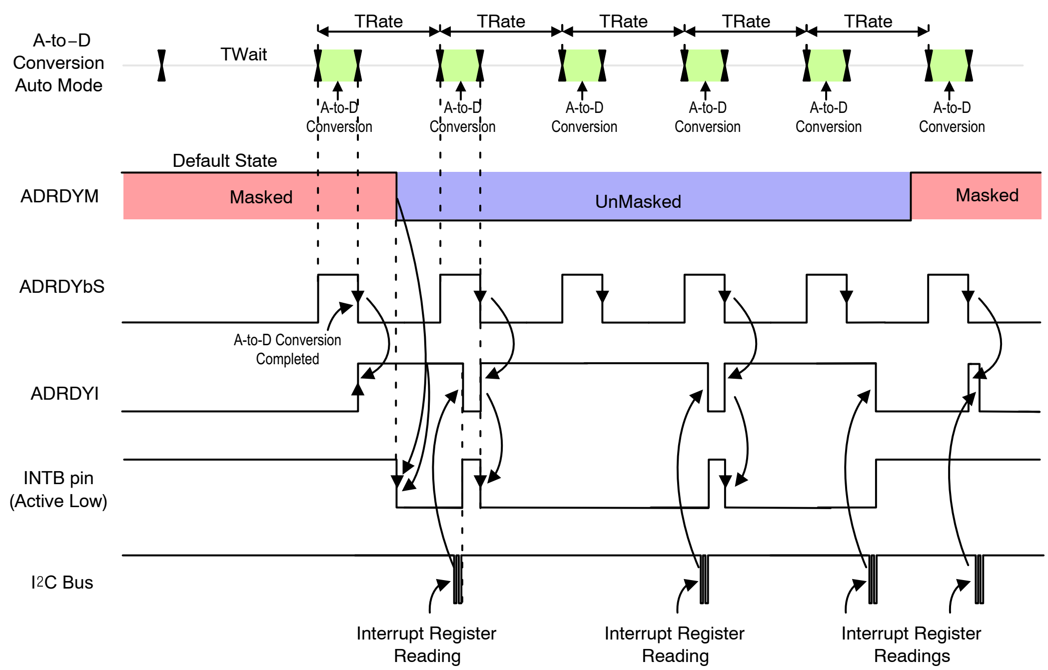


Figure 86. Description of the Interrupt Process of the Bits ADRDYx when the ADC is in Auto-Mode

Power-Up & Power-Down Sequences

The below diagrams depict the different power up and down sequences.

When AVIN is applied a default power-up sequence is started. V_{CORE} will start up after AVIN is above the Under-Voltage Lock-Out (UVLO) threshold. Once V_{CORE} is ok the clock is activated then the buck converter and finally the regulator according to the below Initial Power-Up Timings (Figure 87).

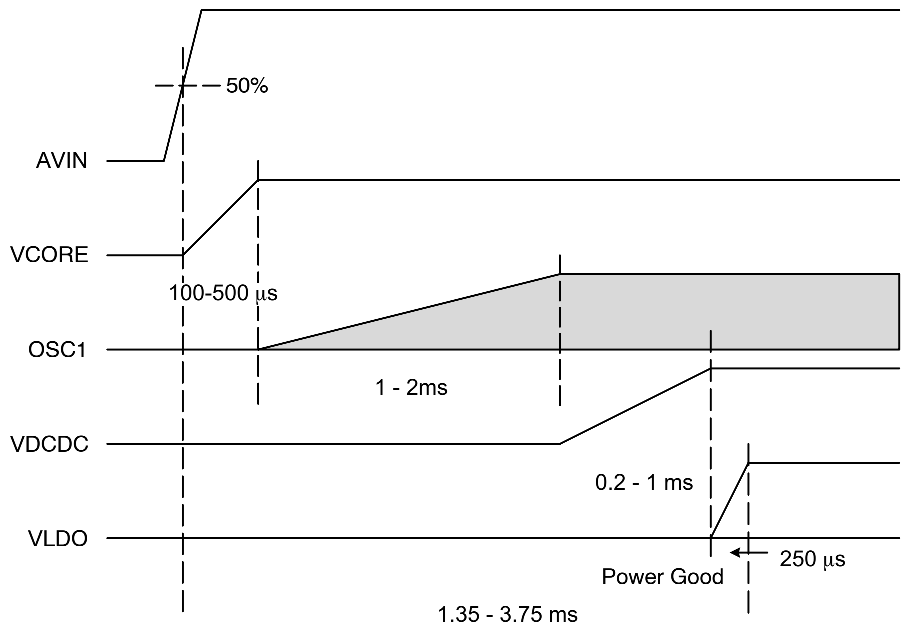


Figure 87. Initial Power-Up Timings

The other circuit blocks including Boost Converter and PA are enabled under the control of the host through dedicated enable bits in normal mode and sleep mode. In normal mode that is out of Sleep mode the Boost Converter and PA can be enabled together according to the below timing diagram after the oscillator is flagged ok that is nominal and stable.

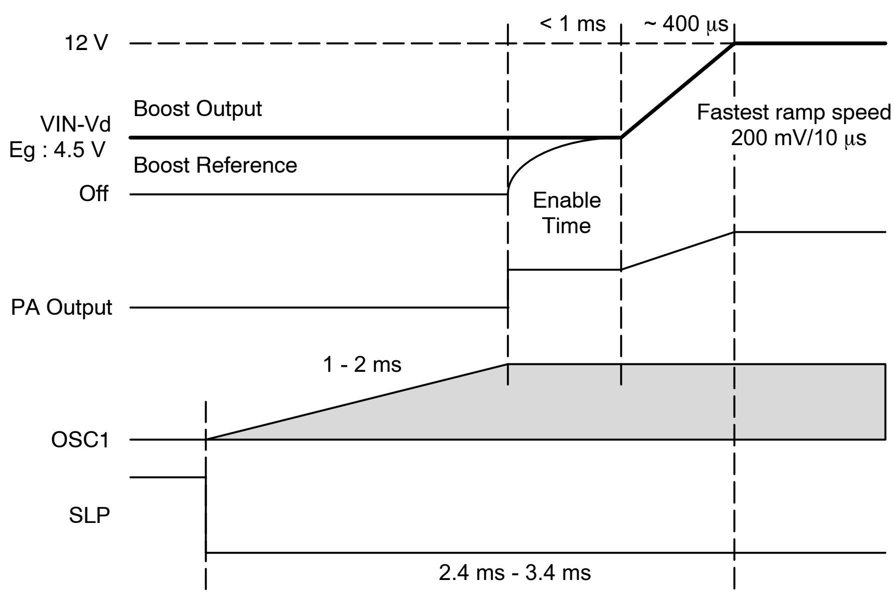


Figure 88. Oscillator, PA Boost and PA Enabling Timing Out of Sleep Mode

If a reset occurs during normal operating mode the boost converter and PA drivers will shutdown first followed by the other blocks. LDO and Buck Converter are only reset upon Hard Reset with crystal oscillator still running. LDO and Buck Converter are not reset in the case of a Soft Reset. Of course this is also true for the corresponding I^2C registers which are cleared upon Hard Reset only. An Interrupt is generated after shutdown sequence is completed (see Figure 89).

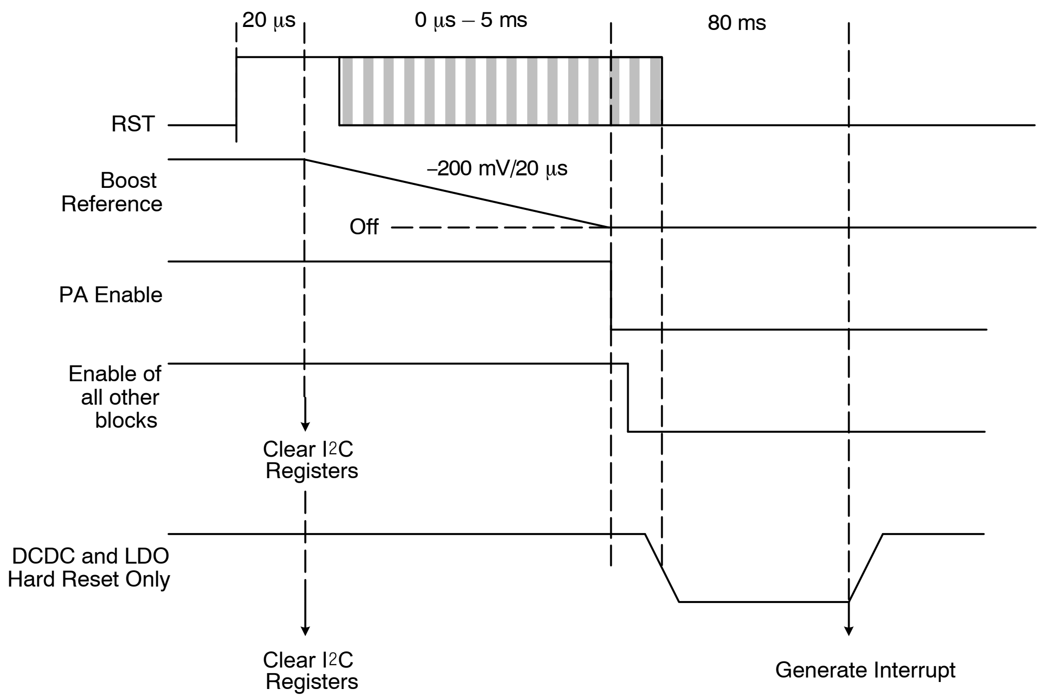


Figure 89. Power Down upon Reset

If a fault is triggered on the PA or Boost Converter (Boost OV, Boost OC (BSTLIM), PA OC, PA OT) or a peak voltage is detected at the Peak Detectors a fast ramp down of 200 mV/20 µs of the boost converter is engaged. The PA is disabled once the boost ramp down sequence is completed (Figure 90). Nevertheless the PA and the boost converter can be re-enabled during the boost ramp-down sequence; in that case the boost restarts on the programmed ramp speed after the boost ramp down sequence is terminated and the PA doesn't disable like illustrated below Figure 91. This applies for other circuit blocks already enabled, they also don't disable.

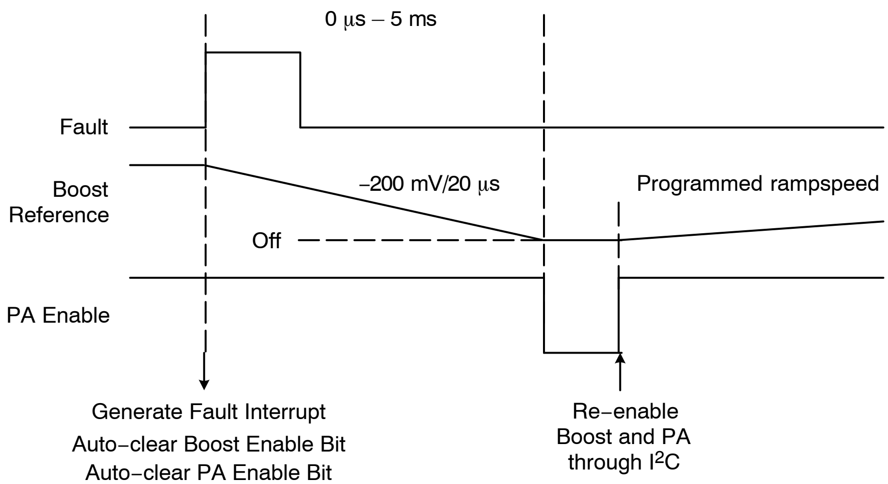


Figure 90. PA or Boost Fault Mode Shutdown and Restart Cycle

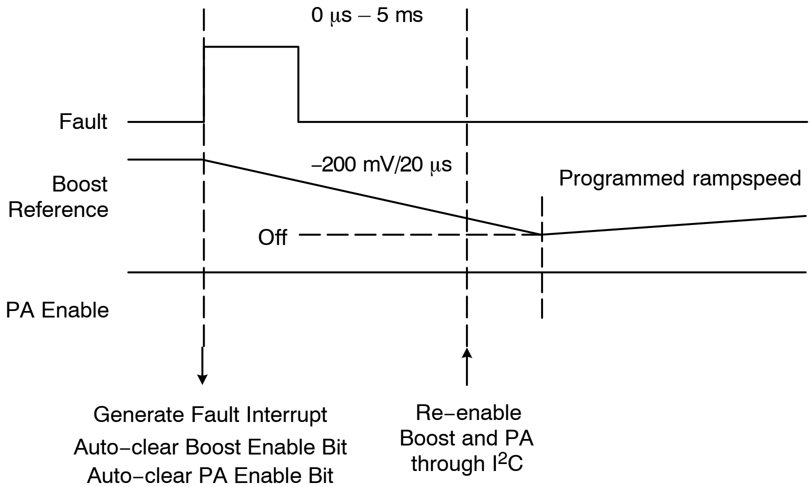


Figure 91. PA or Boost Fault Mode Shutdown and Restart Cycle during Boost Ramp-down

A shutdown request resulting from Sleep mode activation is depicted for two cases Figure 92 and Figure 93.

In the first case (Figure 92) the device sleep mode is disabled during the PA Boost Converter ramping down. The boost converter restarts on the programmed ramp speed after the shutdown ramp down is terminated; the PA and other different blocks if already enabled are not disabled.

In the second case (Figure 93) the device enters a “true” Sleep mode for which the SLP pin is not disabled before boost ramp-down completion − the blocks configured to be disabled are effectively disabled. In this example the PA is disabled, the other blocks configured as disabled in Sleep mode are disabled and the LDO is reprogrammed to its Sleep mode setting value. Note that the Sleep pin level High follows the LDO programmed value and that the buck converter and the crystal oscillator remain enabled. Exiting the Sleep mode restarts sequentially the device to its operating configuration with first the LDO recovering its operating output voltage value, then all together the other blocks affected by the SLP pin, the PA and the Boost Converter ramping up to its nominal value at the programmed ramp speed. The SLP pin features a 20 μs debounce time when enabling and disabling.

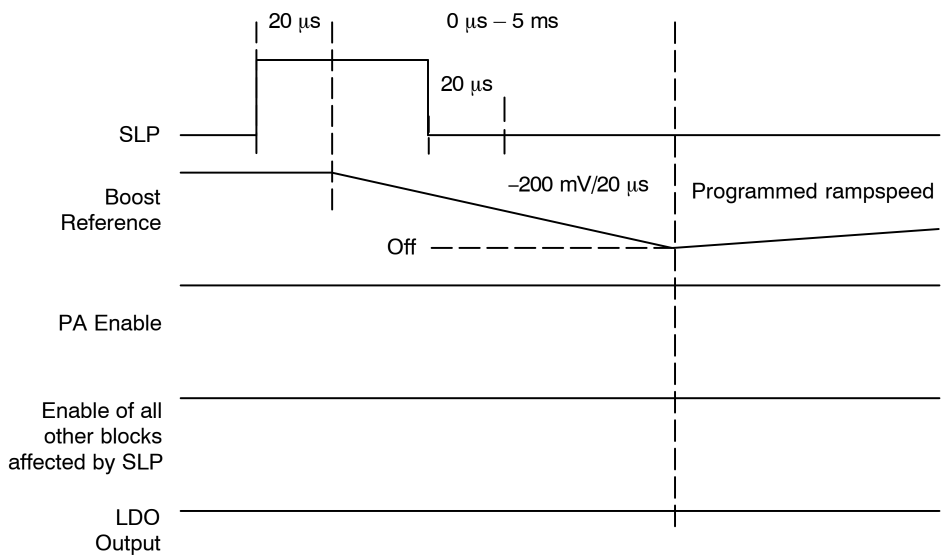


Figure 92. Sleep Shutdown and Restart Cycle during Boost Ramping Down

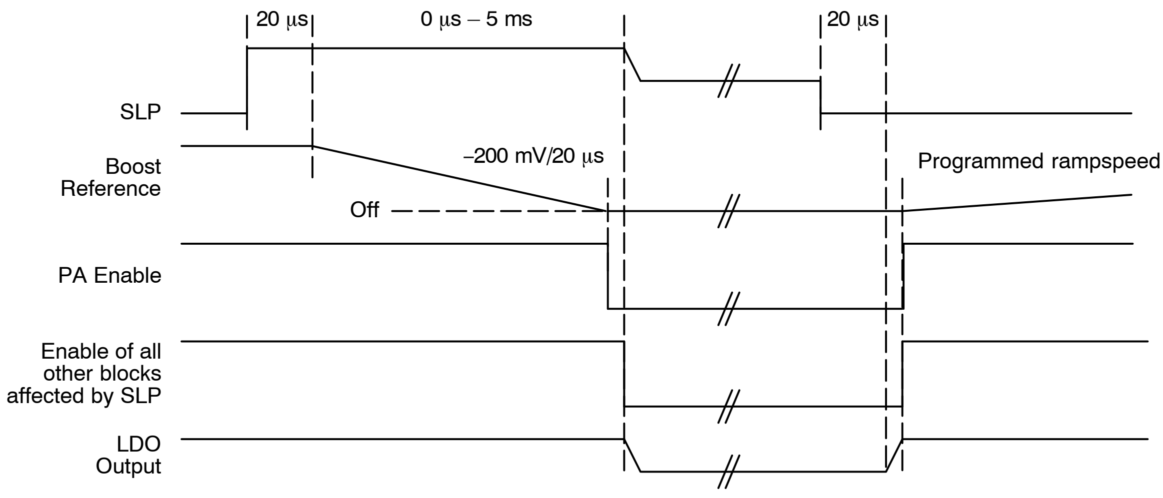


Figure 93. Sleep Shutdown and Restart Cycle

Figure 94 considers the behavior of the Boost Converter and PA when the PA enabling is gated by the Boost Converter's Power Good condition that is when PAMPG = 1. During starting-up if the PA is activated prior to the boost ramp-up completion then the PA enables after Boost Power output is flagged ok. After boost power-up completion the PA enabling occurs immediately without delay. During Boost power-down the PA is disabled after Boost ramp-down is completed otherwise PA disabling occurs immediately.

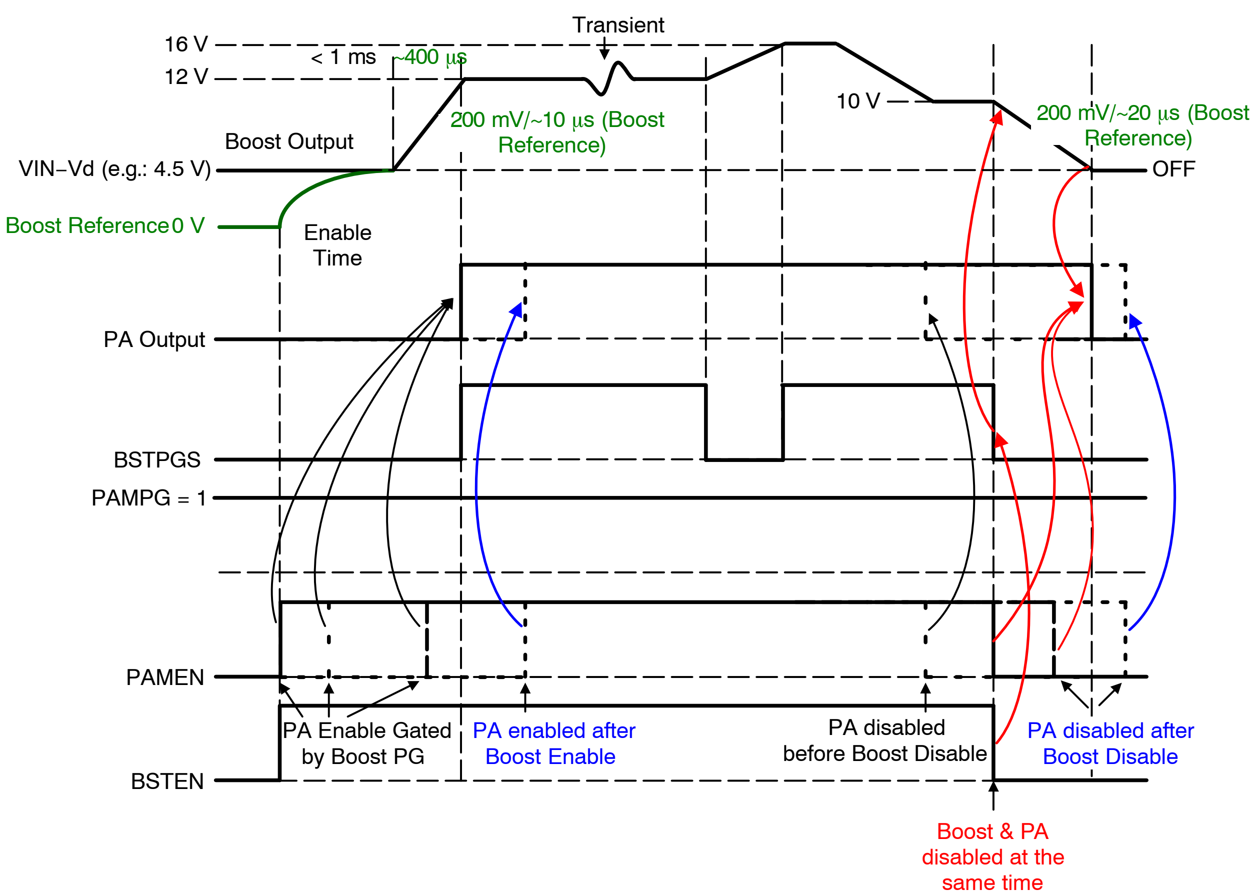


Figure 94. Boost and PA Power-Up and Power-Down when PA Enabling Gated by Boost PG

I²C Interface & Register Map Definition

The NCP6992A communicates with the external processor by means of a serial link using a 400 kHz up to 3.4 MHz I²C two-wire interface protocol. The I²C interface provided is fully compatible with the Standard, Fast and High-Speed I²C modes. The NCP6992A is not intended to operate as a master controller. It is under the control of the main controller (master device), which controls the clock (pin SCL) and the read or write operations through SDA. The I²C bus is an addressable interface (7-bit addressing only) featuring one Read/Write address. The interface at SDA and SCL is referenced with respect to a locally generated supply as a function of the peak voltage of the SCL and SDA lines.

I²C Communication Description

The first byte transmitted is the Chip address (with the LSB bit set to 1 for a read operation, or set to 0 for a Write operation). The following data will be:

- In case of a Write operation, the register address (@REG) pointing to the register we want to write is followed by the data we will write in that location. The writing process is auto-incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1 etc ...
- In case of read operation, the NCP6992A will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto-incremental.

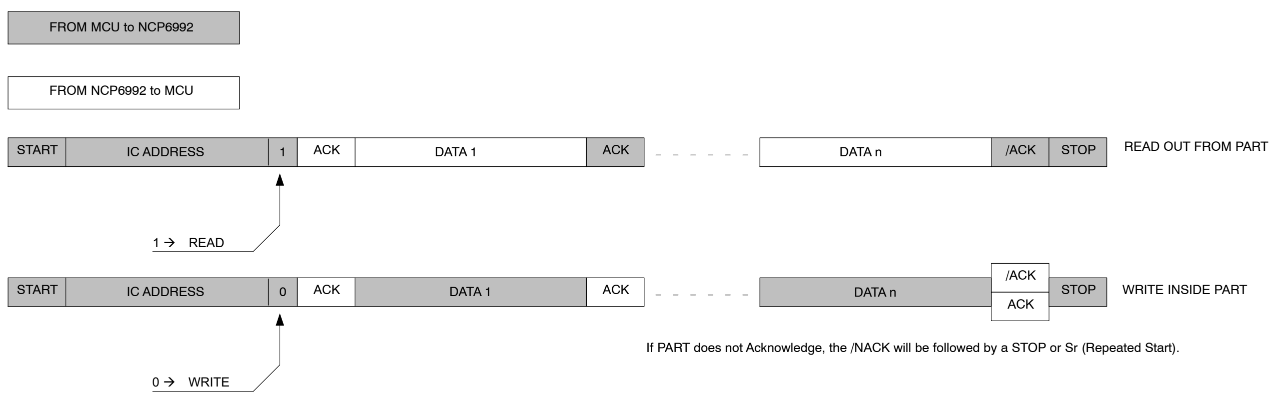


Figure 95. General Protocol Description

Read Out from Part

The Master will first make a "Pseudo Write" transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start (Sr) will initiate the read transaction from the register address the initial write transaction has pointed to:

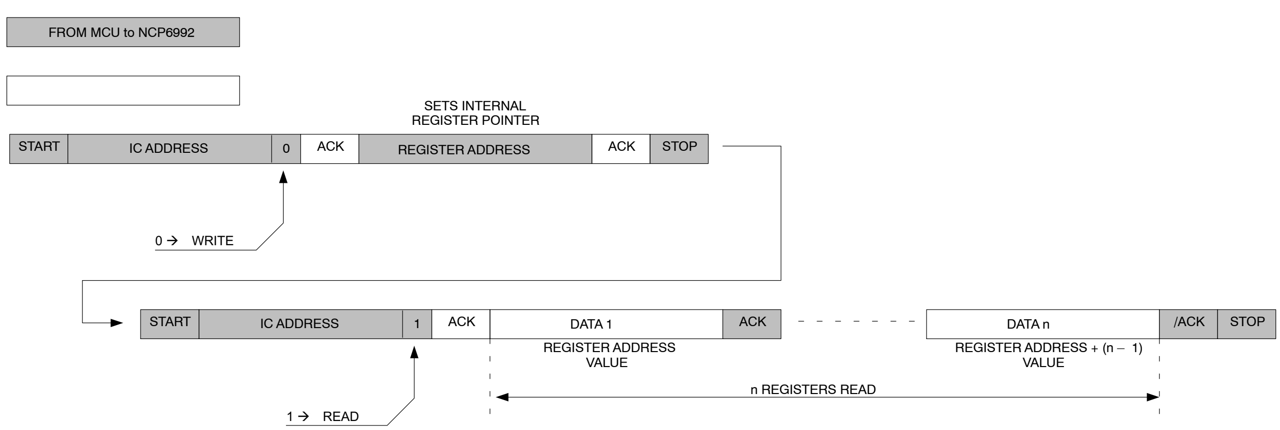


Figure 96. Read Out from Part

The first WRITE sequence will set the internal pointer to the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Read Write then Read

With Stop Then Start:

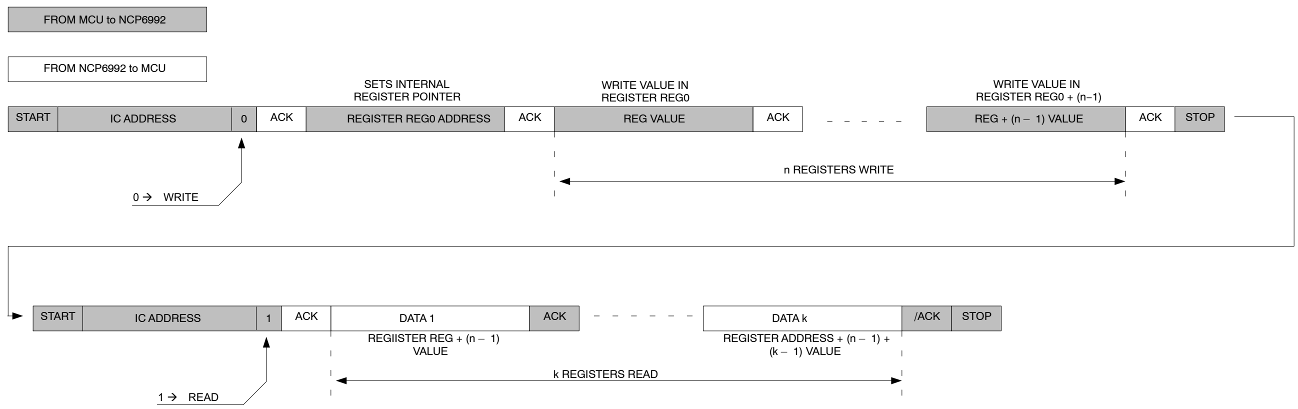


Figure 97. Write Followed by Read Transaction

Write in Part – Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, …, Reg + n.

With *n* Registers:

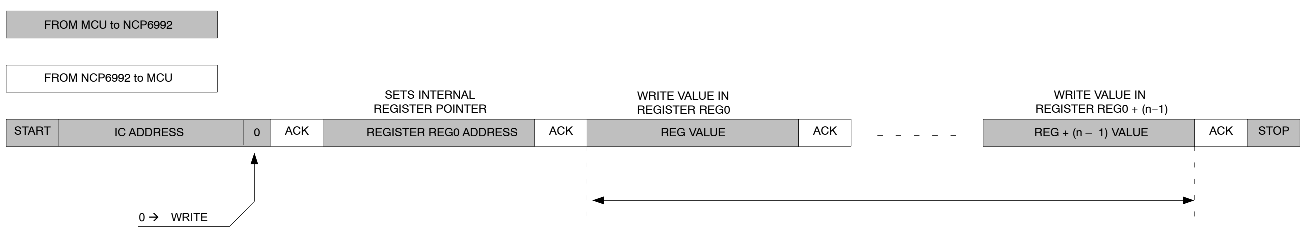


Figure 98. Write in *n* Registers

I^{2}C Address

NCP6992A has four available I^{2}C addresses selectable by factory settings (ADD0 to ADD3). Different address settings can be generated upon request to ON Semiconductor. The default address is set to 28h/29h since the NCP6992A supports 7-bit address and ignores A0.

An additional feature allows configuring the I^{2}C address by software using a specific I2CA7 bit (see Configuration 1 Register). The address bit A7 has the state 0 or 1 programmed in the bit I2CA7.

By default the I^{2}C of the NCP6992A will be addressable at 001xx00 since by default I2CA7=0. By writing a 1 to the I2CA7 bit the I^{2}C address is dynamically changed for 101xx00. Only after a STOP condition and a new START/IC_ADDRESS the new I^{2}C address will have a useful meaning. Meaning, if setting I2CA7 occurs in a consecutive write sequence the I^{2}C address is not repeated in between writes so programming the I2CA7 bit will have no influence at this stage. The I2CA7 bit is only to be reset upon power on reset or upon hard system reset; it is not to be reset during a soft system reset (DCDC & LDO untouched).

Table 17. I2C ADDRESS

I2C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0	W 0x20 R 0x21	I2CA7	0	1	0	0	0	0	R/W
	Add	0x10							–
ADD1 (default)	W 0x28 R 0x29	I2CA7	0	1	0	1	0	0	R/W
	Add	0x14							–
ADD2	W 0x30 R 0x31	I2CA7	0	1	1	0	0	0	R/W
	Add	0x18							–
ADD3	W 0x38 R 0x39	I2CA7	0	1	1	1	0	0	R/W
	Add	0x1C							–

Register Map

Registers can be:

R Read only register
RC Read then Clear (Dual Edge or Rising Edge when indicated)
RW Read and Write register
Reserved Address is reserved and register is not physically designed
Spare Address is reserved and register is physically designed
Fac Factory
Met Metal

Table 18. I2C REGISTER MAP DESCRIPTION

Registers				Data Bit							
Name	Address	Type	Default	7	6	5	4	3	2	1	0
Status	00h	R	00h	THSTAT	GPIOSTAT	DRVSTAT	IMPSTAT	PKSTAT	ADSTAT	PASTAT	PWRSTAT
Interrupt 1	01h	RC	00h	PAOCI	BSTPGI	BSTLIMI	BSTOVI	LDOLIMI	BUCKLIMI	CLKI	RSTI
Interrupt 2	02h	RC	00h	IMPCDI	PKRFI	PKTXI	PKPI	RLYFLTI	ADCMPAI	ADCMPBI	ADRDYI
Interrupt 3	03h	RC	00h	BROI	PAOTI	TSDI	TWARNI	GPIO1I	GPIO2I	LDIOI	TMOI
Sense 1	04h	R	00h	PAOCS	BSTPGS	BSTLIMS	BSTOVS	LDOLIMS	BUCKLIMS	CLKS	–
Sense 2	05h	R	00h	IMPCDS	PKRFS	PKTXS	PKPS	RLYFLTS	ADCMPAS	ADCMPBS	ADRDYbS
Sense 3	06h	R	00h	BROS	PAOTS	TSDS	TWARNS	GPIO1S	GPIO2S	LDIOS	–
Mask 1	07h	RW	FFh	PAOCM	BSTPGM	BSTLIMM	BSTOVM	LDOLIMM	BUCKLIMM	CLKM	RSTM
Mask 2	08h	RW	FFh	IMPCDM	PKRFM	PKTXM	PKPM	RLYFLTM	ADCMPAM	ADCMPBM	ADRDYM
Mask 3	09h	RW	FFh	BROM	PAOTM	TSDM	TWARNM	GPIO1M	GPIO2M	LDIOM	TMOM
Identification 1	0Ah	R	02h	MID[3:0]				PID[3:0]			
Identification 2	0Bh	R	Fac–Met	FID[3:0]				RID[3:0]			
Not Used	0C–0Fh	–	–	–	–	–	–	–	–	–	–
Configuration 1	10h	RW	0Ch	I2CA7	Spare	TMO[1:0]		OSCEN	RSTMOD	SLPPOL	INTPOL
Configuration 2	11h	RW	15h	BUCKDIS	LDODIS	VDRVSET	VLDOSET[4:0]				
Configuration 3	12h	RW	15h	–	–	–	VLDOSLP[4:0]				
Sleep 1	13h	RW	07h	IMPCDSLP	IMPMSLP	PAMSLP	BSTSLP	VDRMSLP	LDOSLP	BUCKSLP	OSCSLP
Sleep 2	14h	RW	00h	–	ADSLP	NTCPUSLP	ACSLP	PKPSLP	PKRFSLP	PKTXSLP	RLYSLP
Sleep 3	15h	RW	00h	–	–	–	–	GPIO1SLP	GPIO2SLP	LED1SLP	LED2SLP
Not Used	16–17h	–	–	–	–	–	–	–	–	–	–
Power Control 1	18h	RW	05h	–	PAMPG	PAMEN	BSTEN	VDRMOD	LDOEN	BUCKMOD	BUCKEN
Power Control 2	19h	RW	01h	–	–	PAOCAP	PAOCEN	PAOTAP	PAOTEN	BSTOVAP	BSTOVEN
Boost 1	1Ah	RW	00h	VBST[7:0]							
Boost 2	1Bh	RW	19h	–	–	BSTSPEED[2:0]			BSTPWR	BSTILIM[1:0]	
Boost 3	1Ch	RW	00h	–	–	–	ITXMOD[1:0]		ITXSTEP[2:0]		

Table 18. I²C REGISTER MAP DESCRIPTION (continued)

Registers				Data Bit							
Name	**Address**	**Type**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Boost 4	1Dh	RW	00h	ITXPER[7:0]							
Boost 5	1Eh	RW	00h	ITXHI[7:0]							
Boost 6	1Fh	RW	00h	ITXLO[7:0]							
PA Drive 1	20h	RW	04h	PADRV12S[1:0]		PADRV1PH[1:0]		PADRV1EN	PADRV2PH[1:0]		PADRV2EN
PA Drive 2	21h	RW	04h	PADRV34S[1:0]		PADRV3PH[1:0]		PADRV3EN	PADRV4PH[1:0]		PADRV4EN
Impedance 1	22h	RW	00h	IMP1EN	VIMP1HI[6:0]						
Impedance 2	23h	RW	00h	IMP2EN	VIMP2HI[6:0]						
Impedance 3	24h	RW	00h	IMP3EN	VIMP3HI[6:0]						
Impedance 4	25h	RW	00h	–	–	–	–	–	IMPCPMOD[1:0)		IMPMEN
Impedance 5	26h	RW	00h	IMPCDFS	IMPCDSS	–	–	IMPCD[1:0]		IMPCDFEN	IMPCDSEN
Peak Detect 1	27h	RW	00h	PKPAP	PKPEN	PKPDAC[5:0]					
Peak Detect 2	28h	RW	00h	PKRFAP	PKRFEN	PKRFDAC[5:0]					
Peak Detect 3	29h	RW	00h	PKTXAP	PKTXEN	PKTXDAC[5:0]					
Relay Control	2Ah	RW	00h	–	–	–	–	RLYPWMEN	RLYPWM[1:0]		RLYEN
GPIO Control 1	2Bh	RW	00h	–	–	–	GPIO1CTRL[2:0]			GPIO1DAT[1:0]	
GPIO Control 2	2Ch	RW	00h	–	–	–	GPIO2CTRL(2:0)			GPIO2DAT[1:0]	
LED/IO Control 1	2Dh	RW	00h	LED1PER[1:0]		LED1RATE[1:0]		LED2PER[1:0]		LED2RATE[1:0]	
LED/IO Control 2	2Eh	RW	00h	LDIO1CTRL	LDIO1DAT[2:0]			LDIO2CTRL	LDIO2DAT[2:0]		
Spare	2Fh	–	–	Spare	Spare	Spare	Spare	Spare	Spare	Spare	Spare
AC Power	30h	RW	00h	–	ACMOD	ACPH[2:0]			ACGAIN[1:0]		ACEN
ADC Control 1	31h	RW	00h	–	TJSNSEN	VINSNSEN	ISNSGAIN[1:0]		ISNSEN	NTCEXT	NTCPUEN
ADC Control 2	32h	RW	00h	–	–	–	–	ADWAIT[1:0]		ADRATE[1:0]	
ADC Control 3	33h	RW	00h	ADCHMD[1:0]		ADCH[2:0]			ADTRMD[1:0]		ADTR
ADC Comparator 1	34h	RW	00h	CMPATR	CMPACNT[6:0]						
ADC Comparator 2	35h	RW	00h	ADCMPA[9:2]							
ADC Comparator 3	36h	RW	00h	CMPBTR	CMPBCNT[6:0]						
ADC Comparator 4	37h	RW	00h	ADCMPB[9:2]							
ADC Comparator 5	38h	RW	00h	–	–	CMPCHA[1:0]		CMPAEN	CMPCHB[1:0]		CMPBEN
Not Used	39–3Fh	–	–	–	–	–	–	–	–	–	–
ADC Result 1 Lo	40h	R	00h	AD1R[7:0]							
ADC Result 1 Hi	41h	R	00h	–	–	–	–	–	AD1POL	AD1R[9:8]	
ADC Result 2 Lo	42h	R	00h	AD2R[7:0]							
ADC Result 2 Hi	43h	R	00h	–	–	–	–	–	AD2POL	AD2R[9:8]	
ADC Result 3 Lo	44h	R	00h	AD3R[7:0]							
ADC Result 3 Hi	45h	R	00h	–	–	–	–	–	AD3POL	AD3R[9:8]	
ADC Result 4 Lo	46h	R	00h	AD4R[7:0]							
ADC Result 4 Hi	47h	R	00h	–	–	–	–	–	AD4POL	AD4R[9:8]	
ADC Result 5 Lo	48h	R	00h	AD5R[7:0]							
ADC Result 5 Hi	49h	R	00h	–	–	–	–	–	AD5POL	AD5R[9:8]	
ADC Result 6 Lo	4Ah	R	00h	AD6R[7:0]							
ADC Result 6 Hi	4Bh	R	00h	–	–	–	–	–	AD6POL	AD6R[9:8]	
ADC Result 7 Lo	4Ch	R	00h	AD7R[7:0]							
ADC Result 7 Hi	4Dh	R	00h	–	–	–	–	–	AD7POL	AD7R[9:8]	
ADC Result 8 Lo	4Eh	R	00h	AD8R[7:0]							
ADC Result 8 Hi	4Fh	R	00h	–	–	–	–	–	AD8POL	AD8R[9:8]	

Registers Description

Table 19. STATUS REGISTER (Default in Bold)

Name: STATUS				**Address: 00h**			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
THSTAT	GPIOSTAT	DRVSTAT	IMPSTAT	PKSTAT	ADSTAT	PASTAT	PWRSTAT
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
PWRSTAT	Power Status, unlatched logic OR of interrupt bits LDOLIMI, BUCKLIMI, CLKI, RSTI, BROI, TMOI **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1
PASTAT	PA Status, unlatched logic OR of interrupt bits PAOCI, BSTPGI, BSTLIMI, BSTOVI **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1
ADSTAT	Analog-to-Digital Converter Status, unlatched logic OR of interrupt bits ADCMPAI, ADCMPBI, ADRDYI **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1
PKSTAT	Peak Detectors Status, unlatched logic OR of interrupt bits PKRFI, PKPI, PKTXI **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1
IMPSTAT	Impedance Control Status, single bit IMPCDI **0: All Related Interrupt Cleared** 1: IMPCDI is 1
DRVSTAT	Driver Status, unlatched logic OR of interrupt bits LDIOI, RLYFLTI **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1
GPIOSTAT	GPIO Status, unlatched logic OR of interrupt bits GPIO1I, GPIO2I when GPIOs configured as logic inputs **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1
THSTAT	Thermal Status, unlatched logic OR of interrupt bits TSDI, TWRNI, PAOTI **0: All Related Interrupt Cleared** 1: One or more of the related Interrupt bits are 1

Table 20. INTERRUPT 1 REGISTER (Each bit at 1, if unmasked, generates an interrupt on INTB pin. Default in Bold)

Name: Interrupt1				Address: 01h			
Type: Read then Clear (RC)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PAOCI	BSTPGI	BSTLIMI	BSTOVI	LDOLIMI	BUCKLIMI	CLKI	RSTI
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
RSTI	Reset Latched Interrupt **0: Cleared** 1: Rising Edge Detection of Reset Process Completion Event
CLKI	Clock Validity Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of CLKS bit
BUCKLIMI	Buck Current Limit Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of BUCKLIMS bit
LDOLIMI	LDO Current Limit Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of LDOLIMS bit
BSTOVI	Boost Over-Voltage Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of BSTOVS bit
BSTLIMI	Boost Peak Current Limit Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of BSTLIMS bit
BSTPGI	Boost Power Good Latched Interrupt **0: Cleared** 1: Rising-Edge Detection of BSTPGS bit
PAOCI	Power Amplifier Over-Current Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of PAOCS

Table 21. INTERRUPT 2 REGISTER (Each bit at 1, if unmasked, generates an interrupt on INTB pin. Default in Bold)

Name: Interrupt2				Address: 02h			
Type: Read then Clear (RC)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMPCDI	PKRFI	PKTXI	PKPI	RLYFLTI	ADCMPAI	ADCMPBI	ADRDYI
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ADRDYI	Analog-to-Digital Conversion Ready Latched Interrupt. Indicates an A-to-D conversion has been completed **0: Cleared** 1: Falling Edge Detection of ADRDYbS bit
ADCMPBI	Digital Comparator B Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of ADCMPBS bit
ADCMPAI	Digital Comparator A Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of ADCMPAS bit
RLYFLTI	Relay Driver Fault Latched Interrupt **0: Cleared** 1: Rising Edge Detection of RLYFLTS bit
PKPI	PA Peak Detector Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of PKPS
PKTXI	TX Peak Detector Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of PKTXS
PKRFI	RF Peak Detector Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of PKRFS
IMPCDI	PA Impedance Control Detector Latched Interrupt **0: Cleared** 1: Rising-edge detection changed by Dual−Edge detection on IMPCDSS or IMPCDFS bits

Table 22. INTERRUPT 3 REGISTER (Each bit at 1, if unmasked, generates an interrupt on INTB pin. Default in Bold)

Name: Interrupt3				Address: 03h			
Type: Read then Clear (RC)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BROI	PAOTI	TSDI	TWARNI	GPIO1I	GPIO2I	LDIOI	TMOI
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
TMOI	Time Out Fault Latched Interrupt **0: Cleared** 1: Rising-Edge Detection of TMOS
LDIOI	LDIO1 and LDIO2 Fault Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of LDIOS
GPIO2I	GPIO2 Pin Latched Interrupt when GPIO2 configured as logic input **0: Cleared** 1: Dual-Edge Detection of GPIO2S
GPIO1I	GPIO1 Pin Latched Interrupt when GPIO1 configured as logic input **0: Cleared** 1: Dual-Edge Detection of GPIO1S
TWARNI	Temperature Warning Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of TWARNS
TSDI	Thermal Shutdown Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of TSDS
PAOTI	Power Amplifier Over-Temperature Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of PAOTS
BROI	Buck DC-DC Brown-Out Event (buck output voltage drop) Latched Interrupt **0: Cleared** 1: Dual-Edge Detection of BROS

Table 23. SENSE 1 REGISTER (Default in Bold)

Name: Sense1				Address: 04h			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PAOCS	BSTGS	BSTLIMS	BSTOVS	LDOLIMS	BUCKLIMS	CLKS	–
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
CLKS	Clock Sense Bit **0: Clock valid** 1: Clock not valid
BUCKLIMS	Buck Current Limit Sense Bit **0: Buck Current Limit is not Reached** 1: Buck Current Limit is Reached
LDOLIMS	LDO Current Limit Sense Bit **0: LDO Current Limit is not Reached** 1: LDO Current Limit is Reached
BSTOVS	Boost Over-Voltage Sense bit (VSNS pin) **0: Boost Voltage Limit is not Reached** 1: Boost Voltage Limit is Reached
BSTLIMS	Boost Current Limit Sense Bit (BSTISNS pin) **0: Boost Inductor Peak Current Limit is not Reached** 1: Boost Inductor Peak Current Limit is Reached
BSTPGS	Boost Power Good Sense Bit **0: Boost Output Voltage VPA Out of Output Voltage Target** 1: Boost Output Voltage VPA on Target
PAOCS	Power Amplifier Over-Current Sense Bit through pins ISNSP and ISNSN **0: PA Output Current Limit is not Reached** 1: PA Output Current Limit is Reached

Table 24. SENSE 2 REGISTER (Default in Bold)

Name: Sense2				**Address: 05h**			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMPCDS	PKRFS	PKTXS	PKPS	RLYFLTS	ADCMPAS	ADCMPBS	ADRDYbS
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ADRDYbS	Analog-to-Digital Converter Busy Sense Bit. Senses the A-to-D converter activity **0: ADC not Busy** 1: ADC Busy (ongoing A to D conversion)
ADCMPBS	Digital Comparator B Trigger Sense Bit: conversion result is compared with an 8-bit reference pre-programmed value, ADCMPB[9:2], through an independent digital comparator B. **0: Below the ADCMPB [9:2] 8-bit pre-programmed value** 1: Above or equal to the ADCMPA [9:2] 8-bit pre-programmed value
ADCMPAS	Digital Comparator A Trigger Sense Bit: conversion result is compared with an 8-bit reference pre-programmed value, ADCMPA[9:2], through an independent digital comparator A. **0: Below the ADCMPA [9:2] 8-bit pre-programmed value** 1: Above or equal to the ADCMPA [9:2] 8-bit pre-programmed value
RLYFLTS	Relay Driver Fault Sense Bit; Open Circuit detected on the relay driver for more than 10 ms typical **0: Normal Operation** 1: Open-Circuit Detected
PKPS	PA Peak Detector Sense Bit **0: Below Pre-programmed Peak Voltage** 1: Pre-programmed Peak Voltage is Reached
PKTXS	TX Peak Detector Sense Acknowledgement **0: Below Pre-programmed Peak Voltage** 1: Pre-programmed Peak Voltage is Reached
PKRFS	RF Peak Detector Sense Acknowledgement **0: Below Pre-programmed Peak Voltage** 1: Pre-programmed Peak Voltage is Reached
IMPCDS	PA Impedance Control Detector Sense Bit **0: Fast resonance Detection or Normal Operation** 1: Slow Resonance Detection

Table 25. SENSE 3 REGISTER (Default in Bold)

Name: Sense3				**Address: 06h**			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BROS	PAOTS	TSDS	TWARNS	GPIO1S	GPIO2S	LDIOS	–
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
LDIOS	LDIO1 and LDIO2 Sense Bit When Configured as LED Drivers **0: Normal Operation** 1: Open or Short Circuit Detected on the LED Drivers When Configured as USB Detection **0: Logic Low Detected** 1: Logic High Detected
GPIO2S	GPIO2 Pin Sense Bit when GPIO2 configured as logic input **0: GPIO2 pin = Low** 1: GPIO2 pin = High
GPIO1S	GPIO1 Pin Sense Bit when GPIO1 configured as logic input **0: GPIO1 pin = Low** 1: GPIO1 pin = High
TWARNS	Temperature Warning Sense Bit **0: Thermal Warning Limit is not Reached** 1: Thermal Warning Limit is Reached
TSDS	Temperature Shutdown Sense Bit **0: Thermal Shutdown Limit is not Reached** 1: Thermal Shutdown Limit is Reached

Table 25. SENSE 3 REGISTER (Default in Bold) (continued)

D7	D6	D5	D4	D3	D2	D1	D0
PAOTS	Power Amplifier Over-Temperature Sense Bit (TSNS pin) **0: Power Amplifier Over-Temperature Limit is not Reached** 1: Power Amplifier Over-Temperature Limit is Reached						
BROS	Buck DC-DC Brown-Out Sense Bit **0: Buck DC-DC Brown-Out Voltage Limit is not Reached** 1: Buck DC-DC Brown-Out Voltage Limit is Reached						

Table 26. INTERRUPT MASK 1 REGISTER (Default in Bold. By default Mask bits are set to 1.)

Name: Mask1				**Address: 07h**			
Type: Read/Write (R/W)				**Default: 11111111b (FFh)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PAOCM	BSTPGM	BSTLIMM	BSTOVM	LDOLIMM	BUCKLIMM	CLKM	RSTM
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Bit	**Bit Description**						
RSTM	RSTI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
CLKM	CLKI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
BUCKLIMM	BUCKLIMI bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
LDOLIMM	LDOLIMI bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
BSTOVM	BSTOVI bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
BSTLIMM	BSTLIMI bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
BSTPGM	BSTPGI bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						
PAOCM	PAOCI bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**						

Table 27. INTERRUPT MASK 2 REGISTER (Default in Bold. By default Mask bits are set to 1.)

Name: Mask2				Address: 08h			
Type: Read/Write (R/W)				Default: 11111111b (FFh)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMPCDM	PKRFM	PKTXM	PKPM	RLYFLTM	ADCMPAM	ADCMPBM	ADRDYM
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bit	Bit Description
ADRDYM	ADRDYI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
ADCMPBM	ADCMPBI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
ADCMPAM	ADCMPAI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
RLYFLTM	RLYFLTI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
PKPM	PKPI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
PKTXM	PKTXI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
PKRFM	PKRFI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
IMPCDM	IMPCDI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**

Table 28. INTERRUPT MASK 3 REGISTER (Default in Bold. By default Mask bits are set to 1.)

Name: Mask3				Address: 09h			
Type: Read/Write (R/W)				Default: 11111111b (FFh)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BROM	PAOTM	TSDM	TWARNM	GPIO1M	GPIO2M	LDIOM	TMOM
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bit	Bit Description
TMOM	TMOI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
LDIOM	LDIOI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
GPIO2M	GPIO2I Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
GPIO1M	GPIO1I Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
TWARNM	TWARNI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
TSDM	TSDI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
PAOTM	PAOTI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**
BROM	BROI Bit Mask 0: Interrupt toggles INTB **1: Interrupt has no influence on INTB**

Table 29. PRODUCT ID AND MANUFACTURING ID REGISTER (Default in Bold)

Name: ID1				**Address: 0Ah**			
Type: Read Only (R)				**Default: 00000010b (02h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MID[3:0]				PID[3:0]			
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Bit	**Bit Description**						
PID[3:0]	Product Identification						
MID[3:0]	Manufacturing Identification						

Table 30. REVISION ID AND FEATURE ID REGISTER (Default in Bold)

Name: ID2				**Address: 0Bh**			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MID[3:0]				PID[3:0]			
FID[3:0]				RID[3:0]			
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
RID[3:0]	Revision Identification 0000: Silicon Revision 1.0 0xxx: Incremental Silicon Revision 1xxx: Production Revision						
FID[3:0]	Feature Identification 0000: Initial OTP configuration						

Table 31. CONFIGURATION 1 REGISTER (Default in Bold)

Name: Configuration1				**Address: 10h**			
Type: Read/Write (R/W)				**Default: 00001100b (0Ch)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
I2CA7	Spare	TMO[1:0]		OSCEN	RSTMOD	SLPPOL	INTPOL
0	**0**	**0**	**0**	**1**	**1**	**0**	**0**
Bit	**Bit Description**						
INTPOL	Interrupt (INTB) Pin Polarity Programming **0: Interrupt Request for INTB pin Low** 1: Interrupt Request for INTB pin High; INTB pin becomes INT						
SLPPOL	SLP Pin Polarity Programming **0: Sleep Mode Enable when SLP pin High** 1: Sleep Mode Enable when SLP pin Low; SLP pin becomes SLPB						
RSTMOD	Reset Mode 0: Soft Reset **1: Hard Reset**						
OSCEN	Crystal Oscillator Enable 0: Disable **1: Enable**						
TMO[1:0]	Time-Out Programming **00: Time-Out Disable** 01: 0.309 s 10: 1.237 s 11: 9.896 s						
I2CA7	Dynamic I^2C Address Change bit **0: Address bit A7 = 0** 1: Address bit A7 = 1						

Table 32. CONFIGURATION 2 REGISTER (Default in Bold)

Name: Configuration2				Address: 11h			
Type: Read/Write (R/W)				Default: 00010101b (15h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BUCKDIS	LDODIS	VDRVSET	VLDOSET[4:0]				
0	**0**	**0**	**1**	**0**	**1**	**0**	**1**
Bit	**Bit Description**						
VLDOSET[4:0]	LDO Output Voltage Setting Programmable from 1.2 V to 3.6 V in step of 100mV in Normal Mode 00000b = 00h = 1.2 V 00001b = 01h = 1.3 V … **10101b = 15h = 3.3 V** … 11000b = 18h = 3.6 V Clamped at 3.6 V above 18h up to 1Fh						
VDRVSET	VDRV Output Voltage Configuration **0: 10.5 V Typical Output Voltage** 1: 12.5 V Typical Output Voltage						
LDODIS	Automatic Discharge of VLDO when the LDO is Disabled **0: Discharge not Allowed** 1: Discharge Allowed						
BUCKDIS	Automatic Discharge of VDCDC when the Buck is Disabled **0: Discharge not Allowed** 1: Discharge Allowed						

Table 33. CONFIGURATION 3 REGISTER (Default in Bold)

Name: Configuration3				Address: 12h			
Type: Read/Write (R/W)				Default: 00010101b (15h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	VLDOSLP[4:0]				
0	**0**	**0**	**1**	**0**	**1**	**0**	**1**
Bit	**Bit Description**						
VLDOSLP[4:0]	Programmable from 1.2 V to 3.6 V in step of 100 mV in Sleep Mode 00000b = 00h = 1.2 V 00001b = 01h = 1.3 V … **10101b = 15h = 3.3 V** … 11000b = 18h = 3.6 V Clamped at 3.6 V above 18h up to 1Fh						

Table 34. SLEEP 1 REGISTER (Default in Bold)

Name: Sleep1				Address: 13h			
Type: Read/Write (R/W)				**Default: 00000111b (07h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMPCDSLP	IMPMSLP	PAMSLP	BSTSLP	VDRMSLP	LDOSLP	BUCKSLP	OSCSLP
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**
Bit	**Bit Description**						
OSCSLP	Crystal Oscillator Enable Bit in Sleep Mode 0: Crystal Oscillator OFF **1: Leaves Operating State Unchanged**						
BUCKSLP	Buck Converter Enable Bit in Sleep Mode 0: Buck Converter OFF **1: Auto Mode PFM−PWM**						
LDOSLP	LDO Enable Bit in Sleep Mode 0: LDO OFF **1: Enabled at programmed VLDOSLP[4:0]**						
VDRMSLP	VDRV Enable Bit in Sleep Mode **0: VDRV Low Current Mode On** 1: Leaves Operating State Unchanged						
BSTSLP	Boost Converter Enable Bit in Sleep Mode **0: Boost Converter OFF** 1: Leaves Operating State Unchanged						
PAMSLP	PA Driver Master Enable Bit in Sleep Mode **0: PA Drivers OFF** 1: Leaves Operating State Unchanged						
IMPMSLP	Impedance Driver Master Enable Bit in Sleep Mode **0: Impedance Drivers OFF** 1: Leaves Operating State Unchanged						
IMCDSLP	Impedance Control Detector Enable Bit in Sleep Mode **0: Disable** 1: Leaves Operating State Unchanged						

Table 35. SLEEP 2 REGISTER (Default in Bold)

Name: Sleep2				Address: 14h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	ADSLP	NTCPUSLP	ACSLP	PKPSLP	PKRFSLP	PKTXSLP	RLYSLP
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
RLYSLP	Relay Driver Enable Bit in Sleep Mode **0: Relay Driver OFF** 1: Leaves Operating State Unchanged						
PKTXSLP	TX Peak Detector Enable Bit in Sleep Mode **0: Peak Detector OFF** 1: Leaves Operating State Unchanged						
PKRFSLP	RF Peak Detector Enable Bit in Sleep Mode **0: Peak Detector OFF** 1: Leaves Operating State Unchanged						
PKPSLP	PA Peak Detector Enable Bit in Sleep Mode **0: Peak Detector OFF** 1: Leaves Operating State Unchanged						
ACSLP	AC Power Measurement Enable Bit in Sleep Mode **0: AC Power Measurement OFF** 1: Leaves Operating State Unchanged						
NTCPUSLP	TSNS Pin Pull-Up Resistor Enable Bit in Sleep Mode **0: Pull-Up Resistor disconnected** 1: Leaves Operating State Unchanged						
ADSLP	Analog-to-Digital Converter Enable Bit in Sleep Mode **0: ADC OFF** 1: Leaves Operating State Unchanged						

Table 36. SLEEP 3 REGISTER (Default in Bold)

Name: Sleep3				Address: 15h			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	GPIO1SLP	GPIO2SLP	LED1SLP	LED2SLP
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
LED2SLP	LED Driver 2 Enable Bit in Sleep Mode **0: LED Driver 2 OFF** 1: Leaves Operating State Unchanged						
LED1SLP	LED Driver 1 Enable Bit in Sleep Mode **0: LED Driver 1 OFF** 1: Leaves Operating State Unchanged						
GPIO2SLP	GPIO2 Enable Bit in Sleep Mode **0: GPIO2 OFF** 1: Leaves Operating State Unchanged						
GPIO1SLP	GPIO1 Enable Bit in Sleep Mode **0: GPIO1 OFF** 1: Leaves Operating State Unchanged						

Table 37. POWER CONTROL 1 REGISTER (Default in Bold)

Name: Power Control 1				Address: 18h			
Type: Read/Write (R/W)				Default: 00000101b (05h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	PAMPG	PAMEN	BSTEN	VDRMOD	LDOEN	BUCKMOD	BUCKEN
0	**0**	**0**	**0**	**0**	**1**	**0**	**1**
Bit	**Bit Description**						
BUCKEN	Buck Converter Enable 0: Disable **1: Enable**						
BUCKMOD	Buck DC-DC Converter Mode of Operating **0: Auto-Mode PFM/PWM** 1: Forced PWM						
LDOEN	LDO Enable 0: Disable **1: Enable**						
VDRMOD	VDRV Modes **0: Low Current Mode** 1: High Current Mode						
BSTEN	Boost Converter Enable **0: Disable** 1: Enable						
PAMEN	Power Amplifier Master Enable **0: Disable** 1: Enable						
PAMPG	Power Amplifier Master Enable under Boost Power Good Condition **0: Disable** 1: Enable						

Table 38. POWER CONTROL 2 REGISTER (Default in Bold)

Name: Power Control 2				Address: 19h			
Type: Read/Write (R/W)				Default: 00000001b (01h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	GPIO1SLP	GPIO2SLP	LED1SLP	LED2SLP
–	–	PAOCAP	PAOCEN	PAOTAP	PAOTEN	BSTOVAP	BSTOVEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Bit	Bit Description
BSTOVEN	Boost Converter Over-Voltage Protection Enable bit. Generates an Interrupt and limits Boost Output Voltage 0: Disable **1: Enable**
BSTOVAP	Boost Converter Over-Voltage Automatic Protection Bit **0: Automatic Protection Not Allowed** 1: Automatic Protection Allowed
PAOTEN	Power Amplifier Over-Temperature Protection Enable bit. Generates an Interrupt only **0: Disable** 1: Enable
PAOTAP	Power Amplifier Over-Temperature Automatic Protection Bit **0: Automatic Protection Not Allowed** 1: Automatic Protection Allowed
PAOCEN	Power Amplifier Over-Current Protection Enable bit. Generates an Interrupt only **0: Disable** 1: Enable
PAOCAP	Power Amplifier Over-Current Automatic Protection Bit **0: Automatic Protection Not Allowed** 1: Automatic Protection Allowed

Table 39. BOOST OVER-VOLTAGE PROTECTION TRUTH TABLE

BSTOVEN	BSTOVAP	Result
–	–	–
0	X	No Interrupt, over-voltage protection not enabled
1	**0**	**BSTOVI Interrupt and Voltage Limiting,** the boost converter will pulse skip until the OV condition disappears
1	1	BSTOVI Interrupt + Automatic Power Down Sequence (see section about Boost Controller)

Table 40. PA OVER-TEMPERATURE PROTECTION TRUTH TABLE

PAOTEN	PAOTAP	Result
0	X	**No Interrupt**
1	0	PAOTI Interrupt
1	1	PAOTI Interrupt & Automatic Power Down Sequence

Table 41. PA OVER-CURRENT PROTECTION TRUTH TABLE

PAOCEN	PAOCAP	Result
0	X	**No Interrupt**
1	0	PAOCI Interrupt
1	1	PAOCI Interrupt & Automatic Power Down Sequence

Table 42. BOOST 1 REGISTER (Default in Bold)

Name: Boost1				Address: 1Ah			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
VBST[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
VBST[7:0]	VPA Boost Output Voltage Programmable from 9 V to 55.2 V in step of 200 mV. In Discriminator operating modes when the boost output voltage is controlled by the ITX pin the VBST programmed voltage is the Boost maximum output voltage (clamp) and no longer the boost effective output voltage. Below 18h down to 00h the output voltage is clamped at 9 V: **00000000b = 00h = 9 V** … 00011000b = 18h = 9 V 00011001b = 19h = 9.2 V … 01101000b = 68h = 25 V … 11100101b = E5h = 50 V … 11111111b = FFh = 55.2 V						

Table 43. BOOST 2 REGISTER (Default in Bold)

Name: Boost2				Address: 1Bh			
Type: Read/Write (R/W)				Default: 00110011b (33h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	BSTSPEED[2:0]			BSTPWR	BSTILIM[1:0]	
0	**0**	**1**	**1**	**0**	**0**	**1**	**1**
Bit	**Bit Description**						
BSTILIM	Programmable Peak Current Limit When **BSTPWR** = **0** then: 00 = 1.75 A typical 01 = 2.25 A typical 10 = 3.5 A typical **11 = 4.5 A typical** When BSTPWR = 1 then: 00 = 3.5 A typical 01 = 4.5 A typical 10 = 7 A typical 11 = 9 A typical						
BSTPWR	Boost Output Power Capability **0: Standard Range from 0 to 25 W** 1: High Power Range from 10 to 50 W						
BSTSPEED[2:0]	Boost Converter Output Voltage Ramping Speed: 000b = 00h = 9.4375 μs 001b = 01h = 18.875 μs 010b = 02h = 37.75 μs 011b = 03h = 75.5 μs 100b = 04h = 151 μs 101b = 05h = 302 μs **110b = 06h = 604 μs** 111b = 07h = 1208 μs						

Table 44. BOOST 3 REGISTER (Default in Bold)

Name: Boost3				Address: 1Ch			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	ITXMOD[1:0]		ITXSTEP[2:0]		
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ITXSTEP[2:0]	Induced DAC Change Step: **000b = 00h = 1 LSB** 001b = 01h = 2 LSB 010b = 02h = 3 LSB 011b = 03h = 4 LSB 100b = 04h = 5 LSB 101b = 05h = 6 LSB 110b = 06h = 7 LSB 111b = 07h = 8 LSB
ITXMOD[1:0]	ITX pin Discriminator Modes: **00b = 00h = Off** 01b = 01h = Window Mode 10b = 02h = Continuous Mode 11b = 03h = Test Mode

Table 45. BOOST 4 REGISTER (Default in Bold)

Name: Boost4				Address: 1Dh			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ITXPER[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ITXPER[7:0]	Programmable Sampling Speed Range from 18.88 μs to 4833 μs in 18.88 μs step: 00000000b = 00h = 18.88 μs 00000001b = 01h = 37.76 μs 00000010b = 02h = 56.64 μs … 01100011b = 63h = 1888 μs … 11111111b = FFh = 4833 μs

Table 46. BOOST 5 REGISTER (Default in Bold)

Name: Boost5				Address: 1Eh			
Type: Read/Write (R/W)				Default: 00000000b (01h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ITXHI[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ITXHI[7:0]	ITX Threshold High Value programmable from 0 to 3.5915 V in 14.084 mV step: 00000000b = 00h = 0 V 00000001b = 01h = 14.084 mV 00000010b = 02h = 28.168 mV … 11101010b = EAh = 3.295656 V … 11111111b = FFh = 3.5915 V

Table 47. BOOST 6 REGISTER (Default in Bold)

Name: Boost6				Address: 1Fh			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ITXLO[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
ITXLO[7:0]	ITX Threshold Low Value programmable from 0 to 3.5915 V in 14.084 mV step: **00000000b = 00h = 0 V** 00000001b = 01h = 14.084 mV 00000010b = 02h = 28.168 mV … 11101010b = EAh = 3.295656 V … 11111111b = FFh = 3.5915 V						

Table 48. PA DRIVE 1 REGISTER (Default in Bold)

Name: PADrive1				Address: 20h			
Type: Read/Write (R/W)				**Default: 00000000b (04h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PADRV12S[1:0]		PADRV1PH[1:0]		PADRV1EN	PADRV2PH[1:0]		PADRV2EN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
PADRV2EN	Power Amplifier Driver 2 Enable Bit **0: Disable** 1: Enable						
PADRV2PH[1:0]	Absolute Phase Shift PA Driver 2 **00b = 00h = 0°** 01b = 01h = 90° 10b = 02h = 180° 11b = 03h = 270°						
PADRV1EN	Power Amplifier Driver 1 Enable Bit **0: Disable** 1: Enable						
PADRV1PH[1:0]	Absolute Phase Shift PA Driver 1 **00b = 00h = 0°** 01b = 01h = 90° 10b = 02h = 180° 11b = 03h = 270°						
PADRV12S[1:0]	PA Driver Rise and Fall Times **00b = 00h = Fast (10 ns max)** 01b = 01h = Medium (20 ns max) 10b = 02h = Slow (40 ns max) 11b = 03h = Slow (40 ns max)						

Table 49. PA DRIVE 2 REGISTER (Default in Bold)

Name: PADrive2				Address: 21h			
Type: Read/Write (R/W)				**Default: 00000000b (04h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PADRV34S[1:0]		PADRV3PH[1:0]		PADRV3EN	PADRV4PH[1:0]		PADRV4EN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
PADRV4EN	Power Amplifier Driver 4 Enable Bit **0: Disable** 1: Enable						
PADRV4PH[1:0]	Absolute Phase Shift PA Driver 4 **00b = 00h = 0°** 01b = 01h = 90° 10b = 02h = 180° 11b = 03h = 270°						
PADRV3EN	Power Amplifier Driver 3 Enable Bit **0: Disable** 1: Enable						
PADRV3PH[1:0]	Absolute Phase Shift PA Driver 3 **00b = 00h = 0°** 01b = 01h = 90° 10b = 02h = 180° 11b = 03h = 270°						
PADRV34S[1:0]	PA Driver Rise and Fall Times **00b = 00h = Fast (10 ns max)** 01b = 01h = Medium (20 ns max) 10b = 02h = Slow (40 ns max) 11b = 03h = Slow (40 ns max)						

Table 50. IMPEDANCE 1 REGISTER (Default in Bold)

Name: Impedance1				Address: 22h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMP1EN	VIMP1HI[6:0]						
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
VIMP1HI[6:0]	Impedance Control Driver 1: Positive Power Supply Rail Programmable from 0 to 12.7 V in 100 mV step: **0000000b = 00h = 0 V** … 0110010b = 32h = 5 V … 1111111b = 7Fh = 12.7 V						
IMP1EN	Impedance Control Driver 1 Enable Bit **0: Disable** 1: Enable						

Table 51. IMPEDANCE 2 REGISTER (Default in Bold)

Name: Impedance2				Address: 23h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMP2EN	VIMP2HI[6:0]						
0	**0**	1	1	**0**	**0**	1	**0**
Bit	**Bit Description**						
VIMP2HI[6:0]	Impedance Control Driver 2: Positive Power Supply Rail Programmable from 0 to 12.7 V in 100 mV step: **0000000b = 00h = 0 V** … 0110010b = 32h = 5 V … 1111111b = 7Fh = 12.7 V						
IMP2EN	Impedance Control Driver 2 Enable bit **0: Disable** 1: Enable						

Table 52. IMPEDANCE 3 REGISTER (Default in Bold)

Name: Impedance3				Address: 24h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMP3EN	VIMP3HI[6:0]						
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
VIMP3HI[6:0]	Impedance Control Driver 3: Positive Power Supply Rail Programmable from 0 to 12.7 V in 100 mV step **0000000b = 00h = 0 V** … 0110010b = 32h = 5 V … 1111111b = 7Fh = 12.7 V						
IMP3EN	Impedance Control Driver 3 Enable bit **0: Disable** 1: Enable						

Table 53. IMPEDANCE 4 REGISTER (Default in Bold)

Name: Impedance4				Address: 25h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	–	IMPCPMOD[1:0]		IMPMEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
IMPMEN	Impedance Control Driver Master Enable Bit **0: Disable** 1: Enable						
IMPCPMOD[1:0]	Impedance Control Driver Power Supply Rail Configurations **00b = 00h : VIMPP = VDRV (bypass) & Negative Rail = GND** 01b = 01h : VIMPP = VDRV (bypass) & Negative Rail = VIMPN 10b = 02h : VIMPP = 3xVINLDO & Negative Rail = GND 11b = 03h : VIMPP = 3xVINLDO & Negative Rail = VIMPN						

Table 54. IMPEDANCE 5 REGISTER (Default in Bold)

Name: Impedance5				Address: 26h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IMPCDFS	IMPCDSS	–	–	IMPCD[1:0]		IMPCDFEN	IMPCDSEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
IMPCDSEN	Impedance Control Slow Resonance Detector Enable Bit **0: Disable** 1: Enable						
IMPCDFEN	Impedance Control Fast Resonance Detector Enable Bit **0: Disable** 1: Enable						
IMPCD[1:0]	Impedance Control Detector Reference (at IMPCDG pin) 0**0b = 00h = 0.2 x PAVDD** 01b = 01h = 0.4 x PAVDD 10b = 02h = 0.6 x PAVDD 11b = 03h = 0.8 x PAVDD						
IMPCDSS	PA Impedance Control Slow Resonance Detector Sense Bit **0: Normal Operation** 1: Slow Resonance Event Detected						
IMPCDFS	PA Impedance Control Fast Resonance Detector Sense Bit **0: Normal Operation** 1: Fast Resonance Event Detected						

Table 55. PEAK DETECT 1 REGISTER (Default in Bold)

Name: Peak_Detect1				**Address: 27h**			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PKPAP	PKPEN	PKPDAC[5:0]					
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
PKPDAC[5:0]	PA Peak Detector Digital Reference. The 6-bit DAC Range is from 0 mVp to 1562.5 mVp in steps of 31.25 mV. 000000b = 00h = 2.40625 V (corresponds to 6.25 mVp) 000001b = 01h = 2.43750 V (corresponds to 37.5 mVp) … 011100b = 1Ch = 3.28125 V (corresponds to 881.25 mVp) … 110010b to 111111b = 32h to 3F = 3.96875 V (corresponds to 1568.75 mVp)						
PKPEN	PA Peak Detector Enable Bit **0: Disable** 1: Enable						
PKPAP	Peak Detector Automatic Protection Bit **0: Automatic Protection Not Allowed** 1: Automatic Protection Allowed						

Table 56. PEAK DETECTOR AUTO-PROTECTION TRUTH TABLE

PKPEN	PKPAP	Result
0	X	**No Interrupt**
1	0	PKPI Interrupt and Voltage Limiting
1	1	PKPI Interrupt + Automatic Power Down Sequence

Table 57. PEAK DETECT 2 REGISTER (Default in Bold)

Name: Peak_Detect2				**Address: 28h**			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PKRFAP	PKRFEN	PKRFDAC[5:0]					
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
PKRFDAC[5:0]	RF Peak Detector Digital Reference. The 6-bit DAC Range is from 0 mVp to 1562.5 mVp in steps of 31.25 mV. 000000b = 00h = 2.40625 V (corresponds to 6.25 mVp) 000001b = 01h = 2.43750 V (corresponds to 37.5 mVp) … 011100b = 1Ch = 3.28125 V (corresponds to 881.25 mVp) … 110010b to 111111b = 32h to 3F = 3.96875 V (corresponds to 1568.75 mVp)						
PKRFEN	RF Peak Detector Enable Bit **0: Disable** 1: Enable						
PKRFAP	Peak Detector Automatic Protection Bit **0: Automatic Protection Not Allowed** 1: Automatic Protection Allowed						

Table 58. PEAK DETECTOR AUTO-PROTECTION TRUTH TABLE

PKRFEN	PKRFAP	Result
0	X	**No Interrupt**
1	0	PKRFI Interrupt and Voltage Limiting
1	1	PKRFI Interrupt + Automatic Power Down Sequence

Table 59. PEAK DETECT 3 REGISTER (Default in Bold)

Name: Peak_Detect3				Address: 29h			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PKTXAP	PKTXEN	PKTXDAC[5:0]					
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
PKTXDAC[5:0]	TX Peak Detector Digital Reference. The 6-bit DAC Range is from 0 mVp to 1562.5 mVp in steps of 31.25 mV. 000000b = 00h = 2.40625 V (corresponds to 6.25 mVp) 000001b = 01h = 2.43750 V (corresponds to 37.5 mVp) … 011100b = 1Ch = 3.28125 V (corresponds to 881.25 mVp) … 110010b to 111111b = 32h to 3F = 3.96875 V (corresponds to 1568.75 mVp)
PKTXEN	TX Peak Detector Enable Bit **0: Disable** 1: Enable
PKTXAP	Peak Detector Automatic Protection Bit **0: Automatic Protection Not Allowed** 1: Automatic Protection Allowed

Table 60. PEAK DETECTOR AUTO-PROTECTION TRUTH TABLE

PKTXEN	PKTXAP	Result
0	X	**No Interrupt**
1	0	PKTXI Interrupt and Voltage Limiting
1	1	PKTXI Interrupt + Automatic Power Down Sequence

Table 61. RELAY CONTROL REGISTER (Default in Bold)

Name: Relay_Control				Address: 2Ah			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	RLYPWMEN	RLYPWM[1:0]		RLYEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
RLYEN	Relay Driver Enable Bit **0: Disable** 1: Enable
RLYPWM[1:0]	Relay Driver PWM Duty Cycle **00b = 00h = 50% DC** 01b = 01h = 62.5 % DC 10b = 02h = 75% DC 11b = 03h = 87.5% DC
RLYPWMEN	Relay Driver PWM Operating Mode Enable Bit **0: PWM mode Disable, in that case equivalent PWM Duty Cycle = 100%** 1: PWM mode Enable

Table 62. GPIO CONTROL 1 REGISTER (Default in Bold)

Name: GPIO_Control1				**Address: 2Bh**			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	GPIO1CTRL[2:0]			GPIO1DAT[1:0]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
GPIO1DAT[1:0]	GPIO1 Routing Data: See Table 63						
GPIO1CTRL[2:0]	GPIO1 Routing Control: **000b = 00h = High Impedance** 001b = 01h = GPIO1 Configured as an Input To I^{2}C (GPIO1S sense bit) 010b = 02h = GPIO1 Configured as an Input To ADC Result 7 Register 011b = 03h = Not Applicable 100b = 04h = Dhi Discriminator Output 101b = 05h = Clock Output 110b = 06h = Output From I^{2}C 111b = 07h = Output From Peak Detect						

Table 63. ROUTING CONFIGURATION THROUGH GPIO1DAT

GPIO1DAT[1:0]	**00**	01	10	11
Clock Output Setting (GPIO1CTRL[2:0] = 101b)	27.12 MHz	6.78 MHz	27.12 MHz	6.78 MHz
I^{2}C Output Setting (GPIO1CTRL[2:0] = 110b)	Low	High	Low	High
Peak Detect Output Setting (GPIO1CTRL[2:0] = 111b)	PKPA	PKRF	PKTX	PKTX

Table 64. GPIO CONTROL 2 REGISTER (Default in Bold)

Name: GPIO_Control2				**Address: 2Ch**			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	GPIO2CTRL[2:0]			GPIO2DAT[1:0]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
GPIO2DAT[1:0]	GPIO2 Routing Data: See Table x75						
GPIO2CTRL[2:0]	GPIO2 Driver Control Setting: 000b = 00h = High Impedance 001b = 01h = GPIO2 Configured as an Input To I^{2}C (GPIO2S sense bit) 010b = 02h = GPIO2 Configured as an Input To ADC Result 8 Register 011b = 03h = Drain Detect 100b = 04h = Dlo Discriminator Output 101b = 05h = Signal Output 110b = 06h = Output From I^{2}C 111b = 07h = Output From Peak Detect Reference						

Table 65. ROUTING CONFIGURATION THROUGH GPIO2DAT

GPIO2DAT[1:0]	**00**	01	10	11
Drain Detect Setting (GPIO2CTRL[2:0] = 011b)	Drain Detect through 33 kΩ	Drain Detect through 33 kΩ + Route to ADC Input	Drain Detect through 33 kΩ	Drain Detect through 33 kΩ + Route to ADC Input
Signal Output Setting (GPIO2CTRL[2:0] = 101b)	27.12 MHz	6.78 MHz	27.12 MHz	6.78 MHz
I^{2}C Output Setting (GPIO2CTRL[2:0] = 110b)	Low	High	Low	High
Peak Detect Reference Output Setting (GPIO2CTRL[2:0] = 111b)	PAREF	RFREF	TXREF	TXREF

Table 66. LED/IO CONTROL 1 REGISTER (Default in Bold)

Name: LED/IO_Control1				**Address: 2Dh**			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	GPIO1CTRL[2:0]			GPIO1DAT[1:0]	
LED1PER[1:0]		LED1RATE[1:0]		LED2PER[1:0]		LED2RATE[1:0]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
LED2RATE[1:0]	Blinking Pattern Repetition Rate **00b = 00h = 500 ms (Very Fast)** 01b = 01h = 1000 ms (Fast) 10b = 02h = 2000 ms (Slow) 11b = 03h = 4000 ms (Very Slow)
LED2PER[1:0]	Blinking Pattern On Period **00b = 00h = 250 ms (Very Short)** 01b = 01h = 500 ms (Short) 10b = 02h = 1000 ms (Long) 11b = 03h = No Blinking
LED1RATE[1:0]	Blinking Pattern Repetition Rate **00b = 00h = 500 ms (Very Fast)** 01b = 01h = 1000 ms (Fast) 10b = 02h = 2000 ms (Slow) 11b = 03h = 4000 ms (Very Slow)
LED1PER[1:0]	Blinking Pattern On Period **00b = 00h = 250 ms (Very Short)** 01b = 01h = 500 ms (Short) 10b = 02h = 1000 ms (Long) 11b = 03h = No Blinking

Table 67. LED/IO CONTROL 2 REGISTER (Default in Bold)

Name: LED/IO_Control2				**Address: 2Eh**			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDIO1CTRL	LDIO1DAT[2:0]			LDIO2CTRL	LDIO2DAT[2:0]		
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
LDIO2DAT[2:0]	For LDIO2CTRL = 1: LED2 Current Range programmable from 2.5 mA to 20 mA in 2.5 mA Step **000b = 00h = 2.5 mA** 001b = 01h = 5.0 mA 010b = 02h = 7.5 mA 011b = 03h = 10 mA 100b = 04h = 12.5 mA 101b = 05h = 15 mA 110b = 06h = 17.5 mA 111b = 07h = 20 mA For LDIO1CTRL = 0 & LDIO2CTRL = 0 : USB detection configuration (Notes 50 & 51) **0xxb = 00h to 03h = Detector is disabled, input is Hi Z** 100b = 04h = Detect and sink 101b = 05h = Detect no sink 110b = 06h = Drive 0.6 V 111b = 07h = Drive VLDO (3.3 V)
LDIO2CTRL	LED Driver and IO 2 Control Bit **0: USB Detection Enabled if LDIO1CTRL = 0** 1: LDIO2 pin configured as LED driver with USB detector OFF
LDIO1DAT[2:0]	For LDIO1CTRL = 1: LED1 Current Range programmable from 2.5 mA to 20 mA in 2.5 mA Step **000b = 00h = 2.5 mA** 001b = 01h = 5.0 mA 010b = 02h = 7.5 mA 011b = 03h = 10 mA 100b = 04h = 12.5 mA 101b = 05h = 15 mA 110b = 06h = 17.5 mA 111b = 07h = 20 mA For LDIO1CTRL = 0 & LDIO2CTRL = 0 : USB detection configuration (Notes 50 & 51) **0xxb = 00h to 03h = Detector is disabled, input is Hi Z** 100b = 04h = Detect and sink 101b = 05h = Detect no sink 110b = 06h = Drive 0.6 V 111b = 07h = Drive VLDO (3.3 V)
LDIO1CTRL	LED Driver and IO 1 Control Bit **0: USB Detection Enabled if LDIO2CTRL = 0** 1: LDIO1 pin configured as LED driver with USB detector OFF

50. Only a single detector and single sink are physically available on-chip. This is sufficient for proper USB BC 1.2 detection. If both LDIO1 and LDIO2 are configured as being detectors, priority will be given to LDIO1.
51. When configured as USB detection, the LEDxRATE and LEDxPER settings in the LED_IO_Control1 register have no effect.

Table 68. AC POWER REGISTER (Default in Bold)

Name: ACPower				Address: 30h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	ACMOD	ACPH[2:0]			ACGAIN[1:0]		ACEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ACEN	AC Power Measurement Function Enable Bit **0: Disable** 1: Enable
ACGAIN[1:0]	AC Power Measurement Amplifier Gain **00b = 00h = 0 dB** 01b = 01h = 3 dB 10b = 02h = 6 dB 11b = 03h = 9 dB
ACPH[2:0]	AC Power Measurement Phase Control with VA = $V_{ACASP} - V_{ACASN}$ & VB = $V_{ACBSP} - V_{ACBSN}$ **000b = 00h = RE (VA + VB)** 001b = 01h = RE (VA – VB) 010b = 02h = RE (–VA + VB) 011b = 03h = RE (–VA – VB) 100b = 04h = IM (VA + VB) 101b = 05h = IM (VA – VB) 110b = 06h = IM (–VA + VB) 111b = 07h = IM (–VA – VB)
ACMOD	AC Power Measurement Operating Modes when ACEN = 1 **0: Low Power Mode: AC Power Measurement circuit block on under ADC conversion request** 1: AC Power Measurement circuit block always on if ACEN = 1

Table 69. ADC CONTROL 1 REGISTER (Default in Bold)

Name: ADC_Control1				Address: 31h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	TJSNSEN	VINSNSEN	ISNSGAIN[1:0]		ISNSEN	NTCEXT	NTCPUEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
NTCPUEN	Internal NTC Pull-Up Resistor Enable Bit. Applicable if NTCEXT = 0 **0: Disable** 1: Enable if NTCEXT = 0
NTCEXT	NTC Pull-Up Resistor Configuration **0: Internal** 1: External
ISNSEN	Current Sense Amplifier Enable Bit **0: Disable** 1: Enable
ISNSGAIN[1:0]	Current Sense Amplifier Voltage Gain **00b = 00h = bypass** 01b = 01h = x 20 10b = 02h = x 40 11b = 03h = x 40
VINSNSEN	AVIN Sense Enable Bit **0: Disable** 1: Enable
TJSNSEN	Junction Temperature Sense Enable Bit **0: Disable** 1: Enable

Table 70. ADC CONTROL 2 REGISTER (Default in Bold)

Name: ADC_Control2				Address: 32h			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	ADWAIT[1:0]		ADRATE[1:0]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ADRATE[1:0]	Conversion Repetition Rate in Auto Mode **00b = 00h = 0.5 ms (Very Fast)** 01b = 01h = 1.0 ms (Fast) 10b = 02h = 2.0 ms (Medium) 11b = 03h = 10 ms (Slow)
ADWAIT[1:0]	Conversion Request Wait Timer **00b = 00h = 0.5 ms (Very Short)** 01b = 01h = 1.0 ms (Short) 10b = 02h = 2.0 ms (Medium) 11b = 03h = 10 ms (Long)

Table 71. ADC CONTROL 3 REGISTER (Default in Bold)

Name: ADC_Control3				Address: 33h			
Type: Read/Write (R/W)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADCHMD[1:0]		ADCH[2:0]			ADTRMD[1:0]		ADTR
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit	Bit Description
ADTR	ADC Conversion Triggering **0: Cleared** 1: Initiate ADC Conversion; self cleared after conversion completed
ADTRMD[1:0]	Trigger Mode **00b = 00h = Not Trigger (ADC inactive)** 01b = 01h = Trigger Upon ADTR Bit 10b = 02h = Trigger on Exit Sleep Mode (pin SLP) 11b = 03h = Auto Mode
ADCH[2:0]	Channel Selection **000b = 00h = Channel 1** 001b = 01h = Channel 2 010b = 02h = Channel 3 011b = 03h = Channel 4 100b = 04h = Channel 5 101b = 05h = Channel 6 110b = 06h = Channel 7 111b = 07h = Channel 8
ADCHMD[1:0]	Channel Conversion Mode **00b = 00h = Conversion of One Specific Channel Selected by ADCH[2:0]** 01b = 01h = Conversion of 1 Same Channel repeated 8 times. Channel Selected Through ADCH[2:0] 10b = 02h = Conversion of all 8 Channels in Sequential Order 11b = 03h = Conversion of all 8 AC Power Measurement Combinations

Table 72. ADC COMPARATOR 2 REGISTER (Default in Bold)

Name: ADC_Comparator2				Address: 34h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CMPATR	CMPACNT[6:0]						
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
CMPACNT[6:0]	7-bit Counter Counts from 0 to 127						
CMPATR	Counter A Start Mode: **0: Counter Starts on the Falling Edge of the Comparator Output Transition** 1: Counter Starts on the Rising Edge of the Comparator Output Transition						

Table 73. ADC COMPARATOR 3 REGISTER (Default in Bold)

Name: ADC_Comparator3				Address: 35h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADCMPA[9:2]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
ADCMPA[9:2]	Channel A Pre-programmed Digital Reference. ADxR[9:2] compared w/ ADCMPA[9:2].						

Table 74. ADC COMPARATOR 4 REGISTER (Default in Bold)

Name: ADC_Comparator4				Address: 36h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CMPBTR	CMPBCNT[6:0]b						
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
CMPBCNT[6:0]	7-bit Counter Counts from 0 to 127						
CMPBTR	Counter B Start Mode: **0: Counter Starts on the Falling Edge of the Comparator Output Transition** 1: Counter Starts on the Rising Edge of the Comparator Output Transition						

Table 75. ADC COMPARATOR 5 REGISTER (Default in Bold)

Name: ADC_Comparator5				Address: 37h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADCMPB[9:2]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
ADCMPB[9:2]	Channel B Pre-programmed Digital Reference. ADxR[9:2] compared w/ ADCMPB[9:2].						

Table 76. ADC COMPARATOR 1 REGISTER (Default in Bold)

Name: ADC_Comparator1				Address: 38h			
Type: Read/Write (R/W)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	CMPCHA[1:0]		CMPAEN	CMPCHB[1:0]		CMPBEN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
CMPBEN	Comparator Channel B Enable **0: Disable** 1: Enable						
CMPCHB[1:0]	Comparator Channel A Assignment **00b = 00h = PA Voltage** 01b = 01h = PA Temperature 10b = 02h = PA Current 11b = 03h = GPIO1						
CMPAEN	Comparator Channel B Enable **0: Disable** 1: Enable						
CMPCHA[1:0]	Comparator Channel A Assignment **00b = 00h = PA Voltage** 01b = 01h = PA Temperature 10b = 02h = PA Current 11b = 03h = GPIO2						

Table 77. ADC RESULT1 LO REGISTER (Default in Bold)

Name: ADC_Result1_Lo				Address: 40h			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AD1R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD1R[7:0]	10 bit ADC Conversion Result MSB Section [7:0]						

Table 78. ADC RESULT1 HI REGISTER (Default in Bold)

Name: ADC_Result1_Hi				Address: 41h			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	–	AD1POL	AD1R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD1R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD1POL	Polarity Bit 0: + (plus) 1: – (minus)						

Table 79. ADC RESULT2 LO REGISTER (Default in Bold)

Name: ADC_Result2_Lo				Address: 42h			
Type: Read Only (R)				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AD2R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD2R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 80. ADC RESULT2 HI REGISTER (Default in Bold)

Name: ADC_Result2_Hi				Address: 43h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	AD2POL	AD2R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD2R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD2POL	Polarity Bit 0: + (plus) 1: – (minus)						

Table 81. ADC RESULT3 LO REGISTER (Default in Bold)

Name: ADC_Result3_Lo				Address: 44h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
AD3R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD3R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 82. ADC RESULT3 HI REGISTER (Default in Bold)

Name: ADC_Result3_Hi				Address: 45h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
			–	–	AD3POL	AD3R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD3R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD3POL	Polarity Bit 0: + (plus) 1: – (minus)						

Table 83. ADC RESULT4 LO REGISTER (Default in Bold)

Name: ADC_Result4_Lo				Address: 46h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
AD4R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD4R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 84. ADC RESULT4 HI REGISTER (Default in Bold)

Name: ADC_Result4_Hi				Address: 47h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	AD4POL	AD4R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD4R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD4POL	Polarity Bit 0: + (plus) 1: – (minus)						

Table 85. ADC RESULT5 LO REGISTER (Default in Bold)

Name: ADC_Result5_Lo				Address: 48h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
AD5R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	Bit Description						
AD5R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 86. ADC RESULT5 HI REGISTER (Default in Bold)

Name: ADC_Result5_Hi				Address: 49h			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	AD5POL	AD5R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	Bit Description						
AD5R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD5POL	Polarity Bit 0: + (plus) 1: – (minus)						

Table 87. ADC RESULT6 LO REGISTER (Default in Bold)

Name: ADC_Result6_Lo				Address: 4Ah			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
AD6R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	Bit Description						
AD6R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 88. ADC RESULT6 HI REGISTER (Default in Bold)

Name: ADC_Result6_Hi				Address: 4Bh			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	AD6POL	AD6R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	Bit Description						
AD6R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD6POL	Polarity Bit 0: + (plus) 1: – (minus)						

Table 89. ADC RESULT7 LO REGISTER (Default in Bold)

Name: ADC_Result7_Lo				Address: 4Ch			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	D6	D5	D4	D3	D2	D1	D0
AD7R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	Bit Description						
AD7R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 90. ADC RESULT7 HI REGISTER (Default in Bold)

Name: ADC_Result7_Hi				Address: 4Dh			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	–	AD7POL	AD7R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD7R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD7POL	Polarity Bit 0: + (plus) 1: - (minus)						

Table 91. ADC RESULT8 LO REGISTER (Default in Bold)

Name: ADC_Result8_Lo				Address: 4Eh			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AD8R[7:0]							
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD8R[7:0]	10 Bit ADC Conversion Result MSB Section [7:0]						

Table 92. ADC RESULT8 HI REGISTER (Default in Bold)

Name: ADC_Result8_Hi				Address: 4Fh			
Type: Read Only (R)				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	–	AD8POL	AD8R[9:8]	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit	**Bit Description**						
AD8R[9:8]	10 Bit ADC Conversion Result LSB Section [9:8]						
AD8POL	Polarity Bit 0: + (plus) 1: – (minus)						

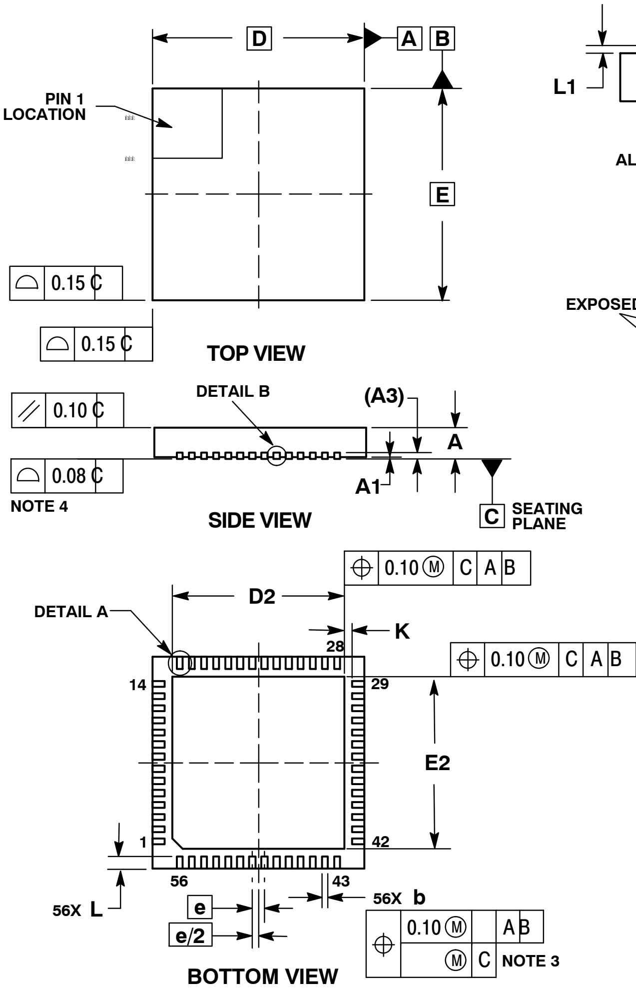
Table 93. ORDERING INFORMATION

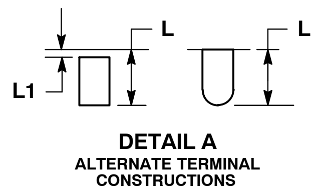
Device	Package	Shipping†
NCP6992AMWTXG	QFN−56 (Pb-Free)	2,500 / Tape & Reel
NCV6992AMWTXG	QFN−56 (Pb-Free)	2,500 / Tape & Reel

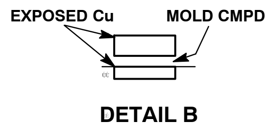
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN56 7x7, 0.4P
CASE 485BT
ISSUE A



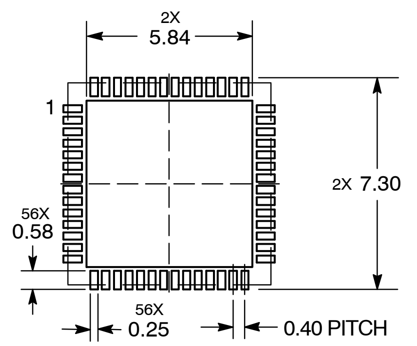




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAILS A AND B, ALTERNATE CONSTRUC– TION PERTAINING TO THE L1 DIMENSION, ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	7.00 BSC	
D2	5.60	5.80
E	7.00 BSC	
E2	5.60	5.80
e	0.40 BSC	
K	0.25 REF	
L	0.30	0.50
L1	0.05	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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