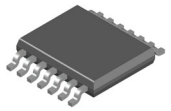
Self-Protected High Side Driver With IDLE Mode & Analog Current Sense

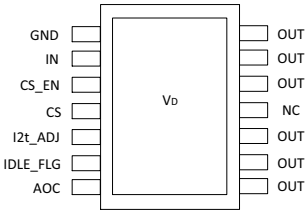
Product Preview

NCV84003G



TSSOP14 EP
CASE 948BZ

PINOUT



The NCV84003G is a fully protected single channel high side driver that can replace mechanical fuses and provide power in a smart power distribution architecture. It can also switch a wide variety of loads, such as bulk capacitors, bulbs, solenoids, and other actuators. The device incorporates advanced features designed for zonal applications such as a smart low power IDLE mode, a dedicated capacitive load charging mode, adjustable overcurrent thresholds and built−in I^2t profiles for fuse replacement. The device also features over−temperature shutdown with automatic latch−off. A Current Sense pin provides precision analog current monitoring of the output as well as fault indication.

Features

- 5 V/3.3 V compatible control input
- Low standby current
- Smart Low Power IDLE Mode with extremely low operating current & auto transition to Normal Mode
- Dual−purpose IDLE status feedback and control
- Capacitive charge mode for active inrush management with auto−entry and exit
- Adjustable overcurrent threshold
- Adjustable Intelligent I^2t protection
- Absolute and Differential thermal shutdown
- Intelligent retry with latch off in fault state
- Proportional analog current sense output multiplexed with discrete fault output levels for fault differentiation
- Off State Open Load and Short Circuit to V_{BATT} Detection
- Under−voltage shutdown and Over−voltage protection
- Protection against loss of ground and loss of V_{BATT}
- Inverse Current protection with FET turn on in inverse mode
- ESD protection
- Reverse battery protection with external components
- AEC−Q100 qualified

FEATURE SUMMARY

Nominal Operating Voltage Range	V_D	6 to 18	V
R_{ON} @ T_J = 25°C	R_{ON}	3	mΩ
Default Output Current Limit (typ)	I_{lim}	125	A
IDLE mode GND Operating Current @ T_J = 85°C	I_{GND}	80	μA

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Device	Package	Shipping†
NCV84003G	TSSOP14−EP (Pb−Free)	XXX

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Applications

- Replace fuses in zonal car platforms
- Power on Bulk Capacitors, Resistive, and Inductive Loads
- Automotive / Industrial

Table 1. PIN DESCRIPTIONS

Pin #	Symbol	Description
1	GND	Ground Reference
2	IN	Logic Level Input for Output Activation
3	CS_EN	Logic Level Input for Diagnosis Enable
4	CS	Current Sense/Diagnostic Output
5	I2t_ADJ	Adjustable I^2t Profile Input
6	IDLE_FLG	IDLE State Flag for MCU
7	AOC	Adjustable Over−Current Threshold Input
11	NC	No Connect
08−10, 12−14	OUT	Output
E−pad	VD	Battery Connection

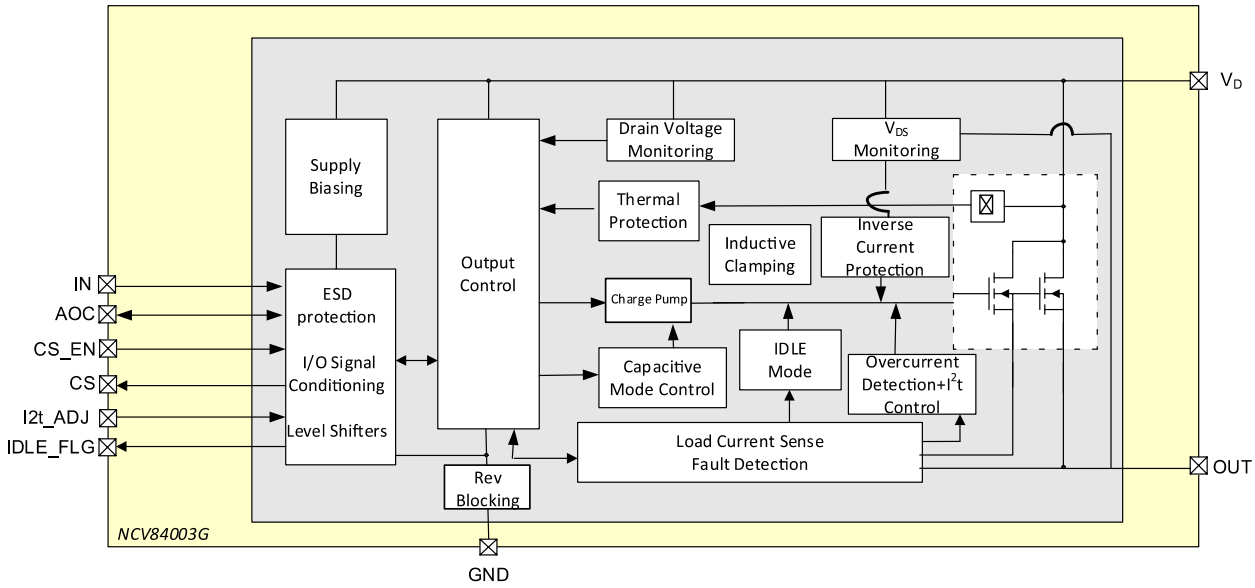


Figure 1. Block Diagram

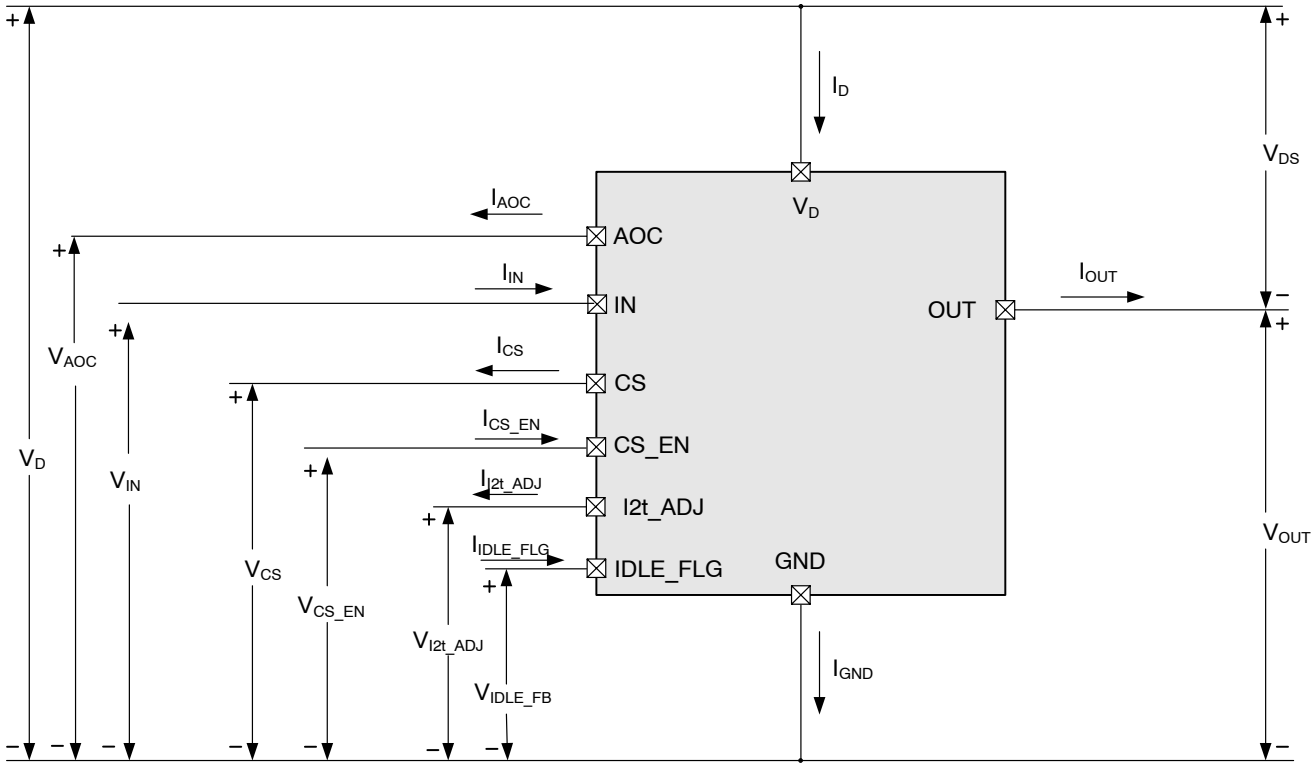


Figure 2. Voltage and Current Definitions

Electrical Specifications

Table 2. MAXIMUM RATINGS (Note 1)
$-40°C \le T_J \le 150°C$ unless otherwise specified

Rating	Symbol	Value		Unit
		Min	Max	
GENERAL				
Supply Voltage (Note 2)	V_D	−0.3	28	V
Supply Voltage for Load Dump Protection	V_{D_LD}		35	V
Supply Voltage for Short Circuit Protection	V_{D_SC}	0	24	V
Reverse Polarity Voltage, t < 2 min, load : 2 Ω, Setup : Refer to Figure 19	V_{D_REV}	0	16	V
SHORT CIRCUIT CAPABILITY				
Repetitive Short Circuit Capability per AEC Q100−12, LSC and TSC, 100 ppm, 300 ms	RSC	1000 Grade A	–	k cycles
DIGITAL INPUT PINS: IN, CS_EN				
Current at Input Pins	$I_{DIG\_IN\_MAX}$	−1	1	mA
Current at Input Pins in Rev Battery, t < 2 min	$I_{DIG\_IN\_MAX\_REV}$	−1	10	mA
Voltage at Input Pins	$V_{DIG\_IN\_MAX}$	−0.3	6.5	V
IDLE_FLG PIN				
Current at IDLE_FLG Pin	I_{IDLE_MAX}	−1	1	mA
Current at IDLE_FLG Pin in Rev Battery, t < 2 min	$I_{IDLE\_MAX\_REV}$	−1	10	mA
Voltage at IDLE_FLG Pin	V_{IDLE_MAX}	−0.3	6.5	V
CURRENT SENSE OUTPUT				
Current at Current Sense Output	I_{CS_MAX}	−25	$I_{CS\_Fault\_ILIM}$	mA
Voltage at Current Sense Output	V_{CS_MAX}	−0.3	V_D	V
ANALOG INPUT PINS: AOC PIN, I2T_ADJ PIN				
Current at input pin	$I_{ANA\_IN\_MAX}$	−1	1	mA
Voltage at input pin	$V_{ANA\_IN\_MAX}$	−0.3	6.5	V
OUTPUTS				
Power Dissipation T_A = 85°C, T_J = 150°C (Note 5)	P_{MAX}		3	W
Drain−Source Voltage at Power Transistor	V_{DS_MAX}		V_{ZCL}	V
Single Pulse Inductive Load Switching Energy (L = 1 mH, V_D = 13.5 V, I_{L_PEAK} = 6.5 A, T_{JSTART} = 150°C)	E_{AS}	TBD		mJ
GROUND TERMINAL				
Current through GND pin	I_{GND}	−50	50	mA
TEMPERATURES				
Operating Junction Temperature	T_J	−40	150	°C
Storage Temperature	$T_{J\_storage}$	−55	150	°C

Table 2. MAXIMUM RATINGS (Note 1)
$-40°C \le T_J \le 150°C$ unless otherwise specified

Rating	Symbol	Value		Unit
		Min	Max	
ESD				
ESD Susceptibility all pins HBM	V_{ESD_HBM}	−2	+2	kV
ESD Susceptibility OUTx to GND, V_D connected, HBM	$V_{ESD\_OUT\_HBM}$	−4	4	kV
ESD Susceptibility all pins CDM	V_{ESD_CDM}	−500	500	V
ESD Susceptibility pin (corner pins), CDM	V_{ESD_NC}	−750	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Not subject to production testing.
2. For transient application only. Extended operation at absolute maximum voltage may affect device reliability.
3. HBM test setup per AEC−Q100:EIA−JESD22−A114−B.
4. CDM test setup per AEC−Q100:EIA−JESD22−C101−A.
5. Board construction based on JEDEC JESD 51−7 for a four layer 2s2p board with forced air convection. Vias were added under the exposed pad as shown in Figure 3.

Table 3. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max Value	Unit
Thermal Resistance			
Junction−to−Top (Note 6)	P_{si_JT}	1.7	°C/W
Junction−to−EPAD (Note 6)	P_{si_e-PAD}	0.27	°C/W
Junction−to−Ambient − 1s0p min pad (Note 6)	R_{thJA}	144	°C/W
Junction−to−Ambient − 1s0p +1in^2 Cu (Note 6)	R_{thJA}	50	°C/W
Junction−to−Ambient − 2s2p min pad (Note 7)	R_{thJA}	34	°C/W
Junction−to−Ambient − 2s2p +1in^2 Cu (Note 7)	R_{thJA}	22	°C/W

6. Board construction based on JEDEC JESD 51−3 for a single layer 1s0p board with forced air convection.
7. Board construction based on JEDEC JESD 51−7 for a four layer 2s2p board with forced air convection. Vias were added under the exposed pad as shown below.

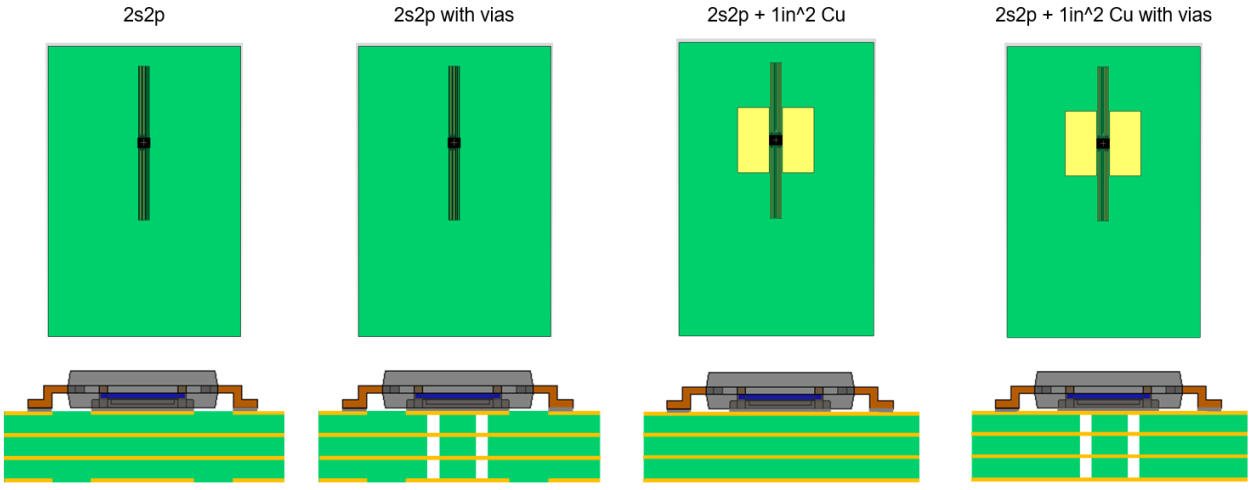


Figure 3. Board Construction for Thermal Performance

Table 4. SUPPLY ELECTRICAL CHARACTERISTICS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)
Typical Values measured @ V_D = 13.5 V, T_J = 25°C

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Nominal Supply Voltage Range (Note 8)	V_{D_NOM}		6	13.5	18	V
Extended Supply Voltage Range (Notes 8, 9)	V_{DS_EX}	V_{IN} = 5 V, R_L = 4 Ω, 3.1 V ≤ V_D ≤ 28 V Ramp down V_D from 28 V to 3.1 V			0.5	V
Under Voltage Shutdown	V_{D_UV}	V_{IN} = 5 V, V_D Falling, From V_{DS} < 0.5 V to I_{OUT} = 0	2.4	2.9	3.1	V
Minimum Operating Voltage	V_{D_MIN}	V_{IN} = 5 V, V_D Rising, From I_{OUT} = 0 to V_{DS} < 0.5 V	2.9	3.4	4.1	V
Under Voltage Shutdown Hysteresis	$V_{D\_UV\_HYS}$			0.5		V
Supply Undervoltage Recovery Time – Normal Mode (Note 8)	$t_{UV\_Recover\_Norm}$	V_{CS_EN} = 5 V, V_{IN} = 0V → 5V after t > t_{Norm}, V_D Rising, From V_D = 0 V → V_D ≥ V_{D_MIN} to V_{DS} < 0.5 V (See Figure 17)	2.5	5	7.5	ms
Supply Undervoltage Recovery Time – CL Mode (Note 8)	$t_{UV\_Recover\_CL}$	V_{CS_EN} = V_{IN} = 0 V 5 V, V_D Rising, From V_D = 0 V → V_D ≥ V_{D_MIN} to V_{DS} < 0.5 V (See Figure 17)	250	500	750	μs
Quiescent Current	I_{Q_85}	V_D = 18 V, T_J ≤ 85°C, V_{IN} = V_{CS_EN} = 0 V, V_{OUT} = 0 V			500	nA
Quiescent Current	I_{Q_150}	V_D = 18 V, T_J = 150°C, V_{IN} = V_{CS_EN} = 0 V, V_{OUT} = 0 V		5	20	μA
Quiescent Current, Diagnostic Active	I_{Q_DIAG}	V_D = 18 V, V_{IN} = 0 V, V_{CS_EN} = 5 V		1.8	2.4	mA
Normal Operating Current	I_{GND_ON}	V_D = 18 V, V_{IN} = V_{CS_EN} = 5 V, V_{CS} < 5 V		5	6	mA
Operating Current in IDLE Mode	I_{GND_IDLE}	V_D = 18 V, V_{IN} = 5 V, V_{CS_EN} = 0V, I_{OUT} = 0.5 A, T_J ≤ 85°C			80	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Not subject to production testing.
9. Extended operation outside the nominal supply voltage range may affect device reliability. Parametric performance not guaranteed.

Table 5. POWER OUTPUT ELECTRICAL CHARACTERISTICS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)
Typical Values measured @ V_D = 13.5 V, T_J = 25°C

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
On−state Resistance	R_{ON_25}	$I_{OUT} = I_{NOM}$ = 15 A, V_{IN} = 5 V, T_J = 25°C		3		mΩ
On−state Resistance	R_{ON_150}	$I_{OUT} = I_{NOM}$ = 15 A, V_{IN} = 5 V, T_J = 150°C			5	mΩ
On−state Resistance − Low Voltage	R_{ON_LV}	I_{OUT} = 2 A, V_D = 3.4V, T_J = 150°C			6	mΩ
On−state Resistance − Inverse Current	$R_{ON\_INV\_25}$	I_{OUT} = −4 A, V_D = 13.5 V, T_J = 25°C		3		mΩ
On−state Resistance − Inverse Current	$R_{ON\_INV\_150}$	I_{OUT} = −4 A, V_D = 13.5 V, T_J = 150°C			6	mΩ
On−state Resistance − IDLE Mode	$R_{ON\_IDLE\_85}$	I_{OUT} = 0.5 A, V_D = 13.5 V, $T_J \le$ 85°C			300	mΩ
Normal Mode Threshold	V_{DS_Norm}	V_{IN} = 0 V, V_{CS_EN} = 5 V		1		V
Output Leakage Current	I_{LEAK_85}	$V_{IN} = V_{CS\_EN}$ = 0 V, V_{OUT} = 0 V, T_J < 85°C			0.5	μA
Output Leakage Current	I_{LEAK_150}	$V_{IN} = V_{CS\_EN}$ = 0 V, V_{OUT} = 0 V, T_J < 150°C			15	μA
IDLE Mode Enable Threshold − Falling	I_{IDLE_TF}	V_{IN} = 5 V, V_{IDLE_FLG} = Low → High	1.3	1.5	1.7	A
IDLE Mode Disable Threshold − Rising	I_{IDLE_TR}	V_{IN} = 5 V, V_{IDLE_FLG} = High → Low	1.8	2.5	3.5	A
Drain−to−Source Clamping Voltage ($V_D - V_{OUT}$)	V_{ZCL}	I_{OUT} = 5 mA, V_{IN} = 0 V	35	36	39	V
Body Diode Forward Voltage	V_F	I_{OUT} = −1 A, T_J = 150°C, $V_F = V_{OUT} - V_D$			0.7	V
OUT slew in H−Bridge Configuration (Note 10)	$\lvert dV_{OUT}/dt \rvert$				10	V/μs

10. Not subject to production testing.

Input Pins

All low−voltage control inputs are compatible with 3.3 V and 5 V microcontroller supply voltages. All inputs comprise of a voltage Schmitt−trigger circuit to enable direct drive from voltage sources and prevent uncontrolled oscillations due to slow transitions at the inputs. Each input features a pull−down element to prevent uncontrolled input states in case of an open pin condition. Unused inputs should be left open or connected to device GND through a 4.7 kΩ resistor.

Table 6. DIGITAL INPUT (IN, CS_EN), AND IDLE_FLG PIN CHARACTERISTICS
($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Low Level Digital Input Voltage	$V_{DIG\_IN\_L}$				0.8	V
High Level Digital Input Voltage	$V_{DIG\_IN\_H}$		2			V
Digital Input Voltage Hysteresis	$V_{DIG\_IN\_HYS}$			0.25		V
Digital Input Pull−down Current	I_{IN_PD}	$0.8\ V \le V_{IN} \le 2\ V$	1		25	μA
IDLE_FLG Pin Output Voltage Low	V_{IDLE_low}	$I_{IDLE\_FLG} = 0.5$ mA		0.2	0.5	V
IDLE_FLG Pin Leakage Current	$I_{IDLE\_leakage}$	$V_{IDLE\_FLG} = 5\ V$, $V_{IN} = V_{CS\_EN} = 0\ V$		0.5	2	μA

Table 7. SWITCHING CHARACTERISTICS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified) (See Figure 11)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Turn ON Delay − CL Mode (V_{IN} Lo → Hi to V_{OUT} = 10% V_D)	$t_{D\_ON\_CL}$	$V_D = 13.5\ V$, $R_L = 2\ \Omega$	80	200	400	μs
Turn ON Time − CL Mode (V_{IN} Lo → Hi to V_{OUT} = 90% V_D)	t_{ON_CL}		200	700	1200	μs
Turn ON Delay − Normal Mode (V_{IN} Lo → Hi to V_{OUT} = 10% V_D)	$t_{D\_ON\_Norm}$		20	70	140	μs
Turn ON Time − Normal Mode (V_{IN} Lo → Hi to V_{OUT} = 90% V_D)	t_{ON_Norm}		50	130	200	μs
Turn OFF Delay (V_{IN} Hi → Lo to V_{OUT} = 90% V_D)	t_{D_OFF}		10	50	130	μs
Turn OFF time (V_{IN} Hi → Lo to V_{OUT} = 10% V_D)	t_{OFF}		30	100	200	μs
Turn ON / OFF Matching − Normal Mode: $t_{ON} - t_{OFF}$	Δt_{ON-OFF}		−20	20	60	μs
Slew Rate ON − CL Mode (V_{OUT} = 30% to 70% V_D)	SR_{ON_CL}		0.015	0.03	0.045	V/μs
Slew Rate ON − Normal Mode (V_{OUT} = 30% to 70% V_D)	SR_{ON_Norm}		0.15	0.3	0.45	V/μs
Slew Rate OFF (V_{OUT} = 70% to 30% V_D)	SR_{OFF}		−0.45	−0.3	−0.15	V/μs
Slew Rate Matching Normal Mode: $SR_{ON\_Norm} - SR_{OFF}$	ΔSR		−0.15	0	0.15	V/μs
Turn ON Energy − Normal Mode (Note 11)	W_{ON}	$V_D = 18\ V$, $R_L = 2\ \Omega$, V_{OUT}: 10% V_D ←→ 90%V_D		1.5		mJ
Turn OFF Energy − Normal Mode (Note 11)	W_{OFF}			1.5		mJ

11. Not subject to production testing.

Protection

Table 8. PROTECTION CHARACTERISTICS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Over−current Detection (Adjustable) (Note 12)	I_{LIM}	V_D = 15V, R_{AOC} = 4.7 kΩ, Setup based on AECQ100−012 Load Short Circuit	112	125	138	A
		V_D = 15V, R_{AOC} = 10 kΩ, Setup based on AECQ100−012 Load Short Circuit	90	100	110	
		V_D = 15V, R_{AOC} = 20 kΩ, Setup based on AECQ100−012 Load Short Circuit	64	75	86	
		V_D = 15V, R_{AOC} = 30 kΩ, Setup based on AECQ100−012 Load Short Circuit	40	50	60	
Normalized Over−current detection at High V_{DS} (Note 12)	$I_{LIM(FB)}$	$V_{DS} \ge 17$ V		0.6*I_{LIM}		A
Normalized Over−current detection at High V_D for Jump Start (Note 12)	$I_{LIM(JS)}$	$V_D > V_{D\_JS}$		0.6*I_{LIM}		A
Differential Thermal Shutdown Threshold − Normal Mode (Note 12)	T_{DTSD}			80		°C
Differential Thermal Shutdown Threshold − Capacitive load Mode (Note 12)	T_{DTSD_CL}			30		°C
Max allowed time in capacitive switching mode (Note 12)	t_{max_Cap}			50		ms
Thermal Shutdown Threshold (Note 12)	T_{TSD}		150	175	200	°C
Thermal Shutdown Hysteresis (Note 12)	T_{TSD_HYS}			15		°C
Over−Voltage Protection Clamp	V_{ZOV}	Current into the V_D pin, I_D = 5 mA, V_{IN} = 0 V	35	36	39	V
Drain Voltage for Current Limitation Reduction in Jump Start (Note 12)	V_{D_JS}		20.5	22.5	24	V

12. Not Subject to production testing.

Table 9. RETRY STRATEGY (See Figure 17)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Number of Retries in Fault after Counter Reset (Notes 13, 14)	n_{COUNT}	$I_{OUT} = I_{LIM}$, or $T_{J(ABS)} > T_{TSD}$, or $T_{J(DIFF)} > T_{DTSD}$, I^2t Monitor = 100%		1		
IN based Counter Reset Time (Note 13)	$t_{IN(Rst)}$	V_{IN} = 0 V, Fault Counter > 0	40	70	100	ms
CS_EN based Counter Reset Time (Note 13)	$t_{CS\_EN(Rst)}$	V_{IN} = 0 V, Fault Counter > 0	150			μs

13. Not Subject to production testing.
14. Not valid in Capacitive load mode.

Table 10. I^2t PROTECTION THRESHOLDS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I^2t Current Thresholds (Notes 15, 16)	I_{I2t_1}	R_{I2t_ADJ} = 4.7 kΩ	TBD	0.2 * I_{I2t_11}	TBD	A
	I_{I2t_2}		TBD	0.25 * I_{I2t_11}	TBD	A
	I_{I2t_3}		TBD	0.3 * I_{I2t_11}	TBD	A
	I_{I2t_4}		TBD	0.35 * I_{I2t_11}	TBD	A
	I_{I2t_5}		TBD	0.4 * I_{I2t_11}	TBD	A
	I_{I2t_6}		TBD	0.5 * I_{I2t_11}	TBD	A
	I_{I2t_7}		TBD	0.6 * I_{I2t_11}	TBD	A
	I_{I2t_8}		TBD	0.7 * I_{I2t_11}	TBD	A
	I_{I2t_9}		TBD	0.8 * I_{I2t_11}	TBD	A
	I_{I2t_10}		TBD	0.9 * I_{I2t_11}	TBD	A
	I_{I2t_11}			125		A
	I_{I2t_11}	R_{I2t_ADJ} = 10 kΩ	TBD	100	TBD	A
	I_{I2t_11}	R_{I2t_ADJ} = 20 kΩ	TBD	75	TBD	A
	I_{I2t_11}	R_{I2t_ADJ} = 30 kΩ	TBD	50	TBD	A

15. Not Subject to production testing.
16. R_{AOC} = 4.7 kΩ to ensure full I^2t range.

Table 11. I^2t PROTECTION THRESHOLDS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I^2t Time Control (Notes 17, 18)	t_{I2t_1}	$I_{OUT} = I_{I2t\_1}$	TBD	31.6	TBD	ms
	t_{I2t_2}	$I_{OUT} = I_{I2t\_2}$	TBD	21.2	TBD	ms
	t_{I2t_3}	$I_{OUT} = I_{I2t\_3}$	TBD	15.1	TBD	ms
	t_{I2t_4}	$I_{OUT} = I_{I2t\_4}$	TBD	11.4	TBD	ms
	t_{I2t_5}	$I_{OUT} = I_{I2t\_5}$	TBD	7.9	TBD	ms
	t_{I2t_6}	$I_{OUT} = I_{I2t\_6}$	TBD	5.3	TBD	ms
	t_{I2t_7}	$I_{OUT} = I_{I2t\_7}$	TBD	3.8	TBD	ms
	t_{I2t_8}	$I_{OUT} = I_{I2t\_8}$	TBD	2.8	TBD	ms
	t_{I2t_9}	$I_{OUT} = I_{I2t\_9}$	TBD	2.2	TBD	ms
	t_{I2t_10}	$I_{OUT} = I_{I2t\_10}$	TBD	1.8	TBD	ms
	t_{I2t_11}	$I_{OUT} = I_{I2t\_11}$		1.6		ms
I^2t Time Control Accuracy (Note 17)	t_{I2t_acc}		−20		20	%

17. Not Subject to production testing.
18. R_{AOC} = 4.7 kΩ to ensure full I^2t range.

Diagnostic Functions

NCV84003G provides diagnostic information and dynamic current sensing on the diagnostic output pin CS.

Table 12. DIAGNOSTIC TRUTH TABLE

Operating Condition	IN	CS_EN	IDLE MODE	Output Voltage	CS Output
Normal Operation	L	H	X	~ GND	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Short Circuit to GND – Overcurrent				GND	HiZ, if Fault Counter = 0 $I_{CS\_FAULT\_ILIM}$ if Fault Counter > 0
Over Temperature				~ GND	HiZ, if Fault Counter = 0 $I_{CS\_FAULT\_TSD}$ if Fault Counter > 0
Short Circuit to V_{BATT}				V_{BATT}	$I_{CS\_FAULT\_OSOL}$, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Open Load				< V_D – V_{DS_OSOL}	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
				> V_D – V_{DS_OSOL}	$I_{CS\_FAULT\_OSOL}$, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Inverse Current				> V_D	$I_{CS\_FAULT\_OSOL}$, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Normal Operation	H		Disabled	~ V_D	$I_{CS} = I_{OUT} / K_{NOM}$
			Enabled		$I_{CS} = I_{OUT} / K_{NOM}$ if $I_{OUT} > I_{IDLE\_TF}$, HiZ if $I_{OUT} \le I_{IDLE\_TF}$
Short Circuit to GND – Over Current Detection			X	~ GND	$I_{CS\_FAULT\_ILIM}$
Over Temperature (Absolute or Differential)			X	~ GND	$I_{CS\_FAULT\_TSD}$
Short Circuit to V_{BATT}			Disabled	V_{BATT}	ICS_OL < ICS < IOUT / K_{NOM}
			Enabled	V_{BATT}	HiZ
Open Load			Disabled	~ V_D	$I_{CS} \le I_{CS(OL)}$
			Enabled	~ V_D	HiZ
Underload			Disabled	~ V_D	ICS(OL) < ICS < IOUT / K_{NOM}
			Enabled	~ V_D	HiZ
Inverse Current			X	> V_D	HiZ
Diagnostics Disabled	X	L	X	X	HiZ

Current Sense Ratio K

The accuracy in load current estimation through sensed current can be improved by performing a calibration routine during end of line (EOL) testing. The calibration procedure can be performed at the nominal load current at one single temperature (25°C).

Diagnostics

Table 13. CURRENT SENSE CHARACTERISTICS ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
CS Leakage Current, CS Output Disabled	$I_{Q\_CS\_DIS}$	V_{IN} = 5 V, V_{CS_EN} = 0 V, I_L = 15 A			0.5	μA
CS Leakage Current, CS Output Enabled	$I_{Q\_CS\_EN}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I_L = 0 A			1	μA
CS Operation Voltage for nominal operation (Note 19)	$V_{CS\_SAT(NOM)}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, I_L = 15 A, $I_{CS} > 0.5 * I_{CS\_NOM}$	0	0.5	1	V
CS Operation Voltage for in−fault operation (Note 19)	$V_{CS\_SAT(Fault)\_ILIM}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, $I_{CS} > 0.5*I_{CS\_Fault\_ILIM}$	0	0.5	1	V
CS Operation Voltage for in−fault operation (Note 19)	$V_{CS\_SAT(Fault)\_TSD}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, $I_{CS} > 0.5*I_{CS\_Fault\_TSD}$	0	0.5	1	V
CS Operation Voltage for in−fault operation (Note 19)	$V_{CS\_SAT(Fault)\_I2t}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, $I_{CS} > 0.5*I_{CS\_Fault\_I2t}$	0	0.5	1	V
CS Operation Voltage for OFF State Open Load operation (Note 19)	$V_{CS\_SAT(Fault)\_OSOL}$	V_D = 6 V, V_{IN} =0 V, V_{CS_EN} = 5 V, I_L = 0 A, $I_{CS} > 0.5*I_{CS\_Fault\_OSOL}$	0	0.5	1	V
CS Saturation Current in normal mode (Note 19)	I_{CS_SAT}		8	10		mA
CS Fault Indication Current: Overcurrent detection (Note 19)	$I_{CS\_FAULT\_ILIM}$	V_{IN} = 5 V, V_{CS_EN} = 5 V Fault Counter > 0, $I_{OUT} = I_{LIM}$	6.7	8.5	10	mA
CS Fault Indication Current: TSD/DTSD (Note 19)	$I_{CS\_FAULT\_TSD}$	V_{IN} = 5 V, V_{CS_EN} = 5 V Fault Counter > 0, $T_J > T_{TSD}$ or $T_{J(DIFF)} > T_{DTSD}$	3.8	5	6.5	mA
CS Fault Indication Current: I^2t Activation (Note 19)	$I_{CS\_FAULT\_I2t}$	V_{IN} = 5 V, V_{CS_EN} = 5 V Fault Counter > 0, I^2t Monitor = 100%	1	1.4	1.8	mA
CS Fault Indication Current in OFF State Open Load	$I_{CS\_FAULT\_OSOL}$	V_{IN} = 0 V, V_{CS_EN} = 5 V Fault Counter = 0, $V_{DS} < V_{DS\_OSOL}$	1.9	2.5	3.5	mA
CS Pin Clamp to Power Supply	V_{CS_CL}	I_{CS} = 1 mA	35	36	39	V
Current Sense Ratio 1	K_1	I_{OUT} = 0.5 A	14000	20000	26000	
Current Sense Ratio 2	K_2	I_{OUT} = 0.75 A	16000	20000	24000	
Current Sense Ratio 3	K_3	I_{OUT} = 2 A	18000	20000	22000	
Current Sense Ratio 4	K_4	I_{OUT} = 8.5 A	19000	20000	21000	
Current Sense Ratio 5	K_5	I_{OUT} = 15 A	19400	20000	20600	
Max Current Sense Ratio Drift After Two−Point Calibration (Note 20)	K_{rel4}	K_4 / K_5, including temperature drift	0.97	1	1.03	

19. Not Subject to production testing.
20. Not subjected to production testing. For more information, refer to the AND9733/D Applications Note.

Table 14. CURRENT SENSE TIMING ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified) (See Figure 29)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Current Sense Settling Time after Diagnostic Activation, Stable Output and Load Conditions – Nominal Load (Note 21)	$t_{S\_CS\_ENH}$	V_{IN} = 5 V, V_{CS_EN} = 0 V → 5 V V_D = 13.5 V, I_L = 15 A, I_{CS} = 90% I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Current Sense Settling Time after Diagnostic Activation, Stable Output and Load Conditions – Light Load (Note 21)	$t_{S\_CS\_ENL}$	V_{IN} = 5 V, V_{CS_EN} = 0 V → 5 V V_D = 13.5 V, V_{IDLE_FLG} = 5 V, I_L = 0.75 A, I_{CS} = 90 % I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			60	µs
Current Sense Settling Time after Load Current Change (Note 21)	$t_{S\_CS\_LOAD\_U}$	V_{IN} = V_{CS_EN} = 5 V, V_D = 13.5 V I_L = 10 A → 15 A, I_{CS} = 90 % I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Current Sense Output Disable Time (Note 21)	$t_{S\_CS\_DIS}$	V_{IN} = 5 V, V_{CS_EN} = 5 V → 0 V V_D = 13.5 V, I_L = 15A, I_{CS} = 10% I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Current Sense Output Disable Time– In Fault (Note 21)	$t_{S\_CS\_DIS\_F}$	V_{IN} = 0 V, V_{CS_EN} = 5 V → 0 V V_D = V_{OUT} = 13.5V, I_{CS} = 10% I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Standby Mode activation after Diagnostic activation (Note 21)	t_{Norm}	V_{CS_EN} = 0 V → 5 V to V_{IN} = 0 V → 5 V for normal mode entry (See Figure 11)	200			µs

21. Not Subject to production testing.

Table 15. OPEN LOAD / UNDERLOAD DETECTION AND TIMING
($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Open Load Detection Threshold, OFF State (Note 22)	V_{DS_OSOL}	V_{IN} = 0 V, V_{CS_EN} = 5 V	1.3	1.8	2.3	V
Open Load Detection Delay OFF State	t_{OSOL_Blank}	V_{IN} = 5 V → 0 V, V_{CS_EN} = 5 V V_D = V_{OUT} = 13.5 V, I_{CS} = 90% I_{CS_FAULT} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF	70	150	250	µs
Open Load Detection Threshold, ON State (IDLE Mode Disabled) (Note 23)	I_{OL_ON}	VIN = 5 V, VCS_EN = 5 V ICS = ICS(OL) = 4 µA	30		150	mA

22. Not subject to production testing.
23. Limits may be widened.

Table 16. IDLE MODE DETECTION AND TIMING ($6 \le V_D \le 18$ V; $-40°C \le T_J \le 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
IDLE Mode Exit Detection Delay	t_{IDLE_Ext}	V_{IN} = 5 V, I_{OUT} = 0.5 A → 15 A to V_{IDLE_FLG} = 10% max V_{IDLE_FLG}		50		µs
IDLE Mode Entry Detection Delay	t_{IDLE_Ent}	V_{IN} = 5 V, I_{OUT} = 15 A → 0.5 A to V_{IDLE_FLG} = 90% max V_{IDLE_FLG}, I^2t Monitor = 0%		250		µs
IDLE Mode Entry Blanking Time	t_{IDLE_Blk}	V_{IN} = 0 → 5V, V_{CS_EN} = 5 V, I_{OUT} = 0.5 A V_{IDLE_FLG} = 90% max V_{IDLE_FLG}		350		µs

Application Diagram and Pin Description

NCV84003G is a single channel smart high−side driver with a very low resistance n−channel output transistor. The required gate overdrive voltage for the transistor is generated by a charge pump that is integrated into the device. The output driver's protection scheme is designed to support linear resistive loads as well as loads with high inrush current, e.g. bulk capacitors and lighting bulbs. The embedded control and protection functions provide full protection to the device as well as full−featured load diagnostic for open load, underload and short circuit through a current sense output that delivers a fraction of the load current in nominal operation multiplexed with a fixed current output in a fault state. An accurate slew rate control is provided to minimize conducted EMI in case of a constant PWM operation. The device features an ultra−low operating current in IDLE mode to address system leakage requirements in zonal applications.

The device provides direct control input (IN) and a diagnostic enable input (CS_EN) to control the information to be provided at the current sense output.

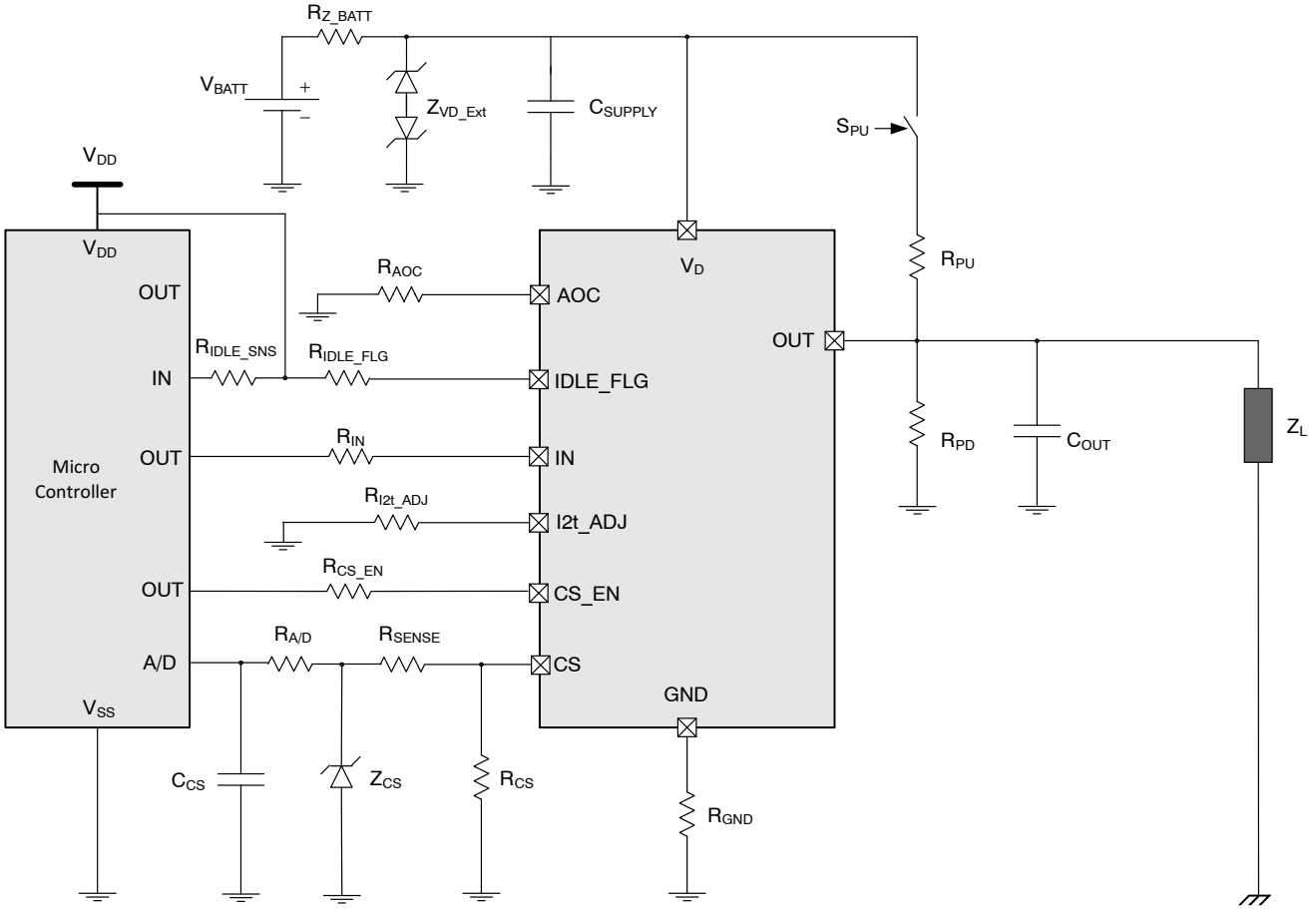


Figure 4. Application Diagram

NCV84003G is supplied by the V_D pin, which can be directly connected to the battery net. The V_D pin is used as power supply to the control circuitry as well as the common drain supply for output channels. In order to support all board net transients following ISO7637−1, an external protection concept as shown in Figure 4 is recommended.

The zener diode Z_{VD_Ext} is used to clamp overvoltage events as well as to provide a free−wheeling path in the event of loss of battery (V_D) with charged inductive loads. R_{GND} is required to limit the maximum current flowing through Z_{VD} (see Figure 18) in case of an over−voltage event. Since all low−voltage I/O pins feature input protection diodes, it is required to insert series resistances into the connection lines between the controlling device (e.g. microcontroller) and NCV84003G.

Table 17. RECOMMENDED EXTERNAL COMPONENTS

Reference	Value	Function
R_{IN}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{CS_EN}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{I2t_ADJ}	4.7 kΩ ~ 30 kΩ	Recommended range for selecting I^2t. Open circuit and short to GND not recommended (See Overcurrent Shutdown).
R_{IDLE_FLG}	10 kΩ	Open drain resistor to logic level voltage.
R_{IDLE_SNS}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{AOC}	4.7 kΩ ~ 30 kΩ	Recommended range for selecting overcurrent threshold. Open circuit and short to GND not recommended (See Overcurrent Shutdown).
R_{CS}	1.2 kΩ	Current Sense resistor.
R_{SENSE}	4.7 kΩ	Provides protection against overvoltage, reverse polarity, and loss of GND. The value of this resistor should be selected with the micro controller specification.
C_{CS}	100 pF	Current Sense signal filtering.
$R_{A/D}$	4.7 kΩ	Current Sense signal filtering.
Z_{CS}	10 V Zener Diode	Provides protection micro controller during overvoltage at CS. Should be selected with the micro controller specification.
R_{PU}	1.5 kΩ	Polarizes the NCV84003G output during OFF state open load diagnosis.
R_{PD}	47 kΩ	Output polarization. Improves the NCV84003G immunity to electromagnetic noise and also used for short to V_{BATT} detection.
S_{PU}	BC807	Switches the battery voltage for OFF state open load diagnostic.
R_{GND}	47 Ω	Provides protection during overvoltage.
Z_{VD_Ext}	30 V Zener Diode	Provides protection of the device during overvoltage.
C_{SUPPLY}	100 nF	Filtering of voltage spikes on the battery line.
C_{OUT}	4.7 nF	Protection during ESD and BCI on output.

Modes of Operation

NCV84003G is designed to operate in the following distinct modes of operation as stated below. Irrespective of the modes below, it should be noted that if $V_D < V_{D(UV)}$, then the internal logic may be reset to default, and values of timers/counters cannot be guaranteed.

a. Sleep Mode

If IN and CS_EN have been observed as low for a duration longer than $t_{IN(Rst)}$ and I^2t Monitor is zero, then the device enters sleep mode. The output FET is off, and the internal reference blocks are shut down and digital logic is reset (as in case of supply−based reset) in this mode to offer extremely low quiescent current (See Table 4).

b. Standby Mode

If IN has been observed low for a duration more than $t_{IN(Rst)}$ and CS_EN is high then device operates in standby mode. The output FET is off, and the off state diagnosis for open load and short circuit to V_{BATT} are available and I^2t monitor is active in this mode. If CS_EN continues to be high, device stays in standby mode.

c. Capacitive Load (CL) Mode

If IN is set to high, the output stage is powered on, and device enters normal or CL mode of operation depending on the state prior to turn on. In case of turn on (IN = Lo → Hi) from sleep mode, the device automatically transitions into CL (capacitive load) mode where the turn on slew rate is reduced and corresponding turn on time is increased. This allows for a delayed turn on profile to charge any capacitive loads connected to the output of the device. The retry strategy and protection features are tailored to charge a capacitive load as described in the section Capacitive Load Switching. Further, the exit conditions from CL mode are also described in this section. In case of PWM operation, device stays in CL mode unless one of the exit conditions is met. PWM frequency and duty cycle should be set externally to ensure that load is sufficiently charged in required time. If CS_EN is set to High, then diagnosis is available in CL mode.

d. Normal Mode

Once the capacitive load is fully charged, the device transitions to normal mode. The turn on timing and slew in this mode are designed to support faster switching operation. The current sense pin outputs a current proportional to the load current if CS_EN is set to high. In case the capacitive load switching is not required in the application, it is recommended to switch on CS_EN before forcing the input Lo → Hi from sleep. This ensures that device enters normal mode once input is enabled. The minimum time between CS_EN: Lo → Hi and IN: Lo → Hi should be more than $t_{Norm.}$ for the output stage to turn subsequently on in normal mode. If already in CL mode, the normal mode can still be entered by meeting one of the exit conditions described in Capacitive Load Switching mode. Similar to the CL mode, device can be driven in PWM operation in normal mode. If IN and CS_EN are both forced low for a period greater than $t_{IN(Rst)}$ and I^2t monitor equals zero, then device enters sleep mode.

e. Protect Mode

While operating in normal mode, the device may observe either of the fault conditions described in Protection Features, that trigger protect mode and lead to latching−off of the output stage. A fault current output on the CS pin will be provided if CS_EN is enabled. The reset conditions for the fault counter are described in section ON State Fault Retry Strategy. If any of the reset conditions are met, device exits protect mode. ON state fault takes precedence over Off State Open Load (OSOL) in off state if fault counter is greater than zero.

f. IDLE mode

A dedicated IDLE mode has been designed in NCV84003G for applications that require reduced operating current while the output stage is turned on (at relatively small output current levels) over extended periods. These applications may, for example, involve the SmartFET providing power to electronic modules that require a software routine to be executed while the car is parked. In such case, limiting the operating current is very critical to reduce the current consumption of the automotive system. The open drain IDLE_FLG pin allows the microcontroller to control the IDLE functionality as explained below.

If IDLE mode is desired in an application, IDLE_FLG pin needs to be supplied with logic level voltage with a pull−up resistor. As the internal logic is activated from sleep mode (by asserting either/both IN/CS_EN high), it executes an internal routine to sense the voltage referenced at this pin. If the sensed voltage is greater than the threshold described in Table 6, then IDLE mode detection is enabled. This routine is associated with a blanking time, per Table 14, during which, a decision to enable IDLE functionality is still being determined.

Once the blanking time has elapsed and IDLE functionality is enabled, NCV84003G automatically detects an entry into IDLE mode by sensing the level of output current. Current thresholds for IDLE mode entry and exit are defined in Table 5. If the output current falls below I_{IDLE_TF} while IN = Hi, then device enters IDLE mode. The R_{ON} of the output stage in this mode is higher than normal mode R_{ON} (See Table 5) while conducting extremely low operating current out of the GND pin (See Table 4). Protection mechanisms in the form of overcurrent, undervoltage and thermal shutdown are not available during operation in this mode. In addition, the current sense output and diagnosis are turned off. The CS_EN input is recommended to be forced low in this mode to limit the operating current.

If the IDLE_FLG pin is connected to GND (via a resistor), then IDLE functionality is disabled, and device continues to operate in normal mode even if load transitions to current levels below I_{IDLE_TF} while IN = High. Current sense output and protection features also operate as usual in such case. This implementation lets the application microcontroller to decide if IDLE functionality should be present or not by controlling the reference supply to IDLE_FLG pin.

It should be noted that the internal routine for activating IDLE mode detection is only performed once at exit from sleep mode, or in case of digital logic reset with $V_D < V_{D\_UV}$, i.e., the reference supply at IDLE_FLG pin will not be continuously sensed for in normal operation. Therefore, for applications that do require IDLE mode functionality, this pin should always be supplied with logic voltage before attempting to switch on the output or activate any diagnostics.

Further, an entry into IDLE mode is prohibited, a.) in CL mode, or b.) if I2t monitor is greater than zero or c.) if the sensed current is low because of a fault counter being latched in case of an ON−State fault (See ON State Fault Retry Strategy). For example, if $I_{OUT} < I_{IDLE\_TF}$ as the output stage is turned on from sleep into CL mode, the decision to enter IDLE mode will not be made until the IDLE blanking time (as defined above) has elapsed and the device has transitioned to normal mode. In typical cases, this time is at−least $t_{ON\_CL} + t_{IDLE\_Ent}$, where t_{IDLE_Ent} is the transition time to IDLE mode from normal mode (note that IDLE blank routine executes in parallel with the output stage turn on).

The IDLE_FLG pin serves a dual purpose by also indicating the status of the IDLE mode in the application. If the IDLE mode functionality is enabled and the output current reduces below I_{IDLE_TF}, then open drain IDLE_FLG output observes a logic high voltage to indicate operation in IDLE mode, and vice versa. The state of this pin should be

disregarded during the IDLE blanking time during which IDLE functionality is being sensed for.

While operating in IDLE mode, if the output current increases above I_{IDLE_TR}, such as in case of overload, short circuit to GND or normal load activation, then device exits into Normal mode and all the protection features are enabled. The voltage at IDLE_FLG pin is asserted low indicating an entry into normal mode. The response time for the device to enter normal mode is described in Table 7.

If the input is asserted high → low during operation in IDLE mode to switch off the output stage, then the device directly enters the sleep mode.

The following timing diagram depicts the transitions in and out of IDLE mode and the block diagram in Figure 6 describes IDLE operation internal to the device.

The flowchart in Figure 8 summarizes the sequence of operations associated with IDLE functionality.

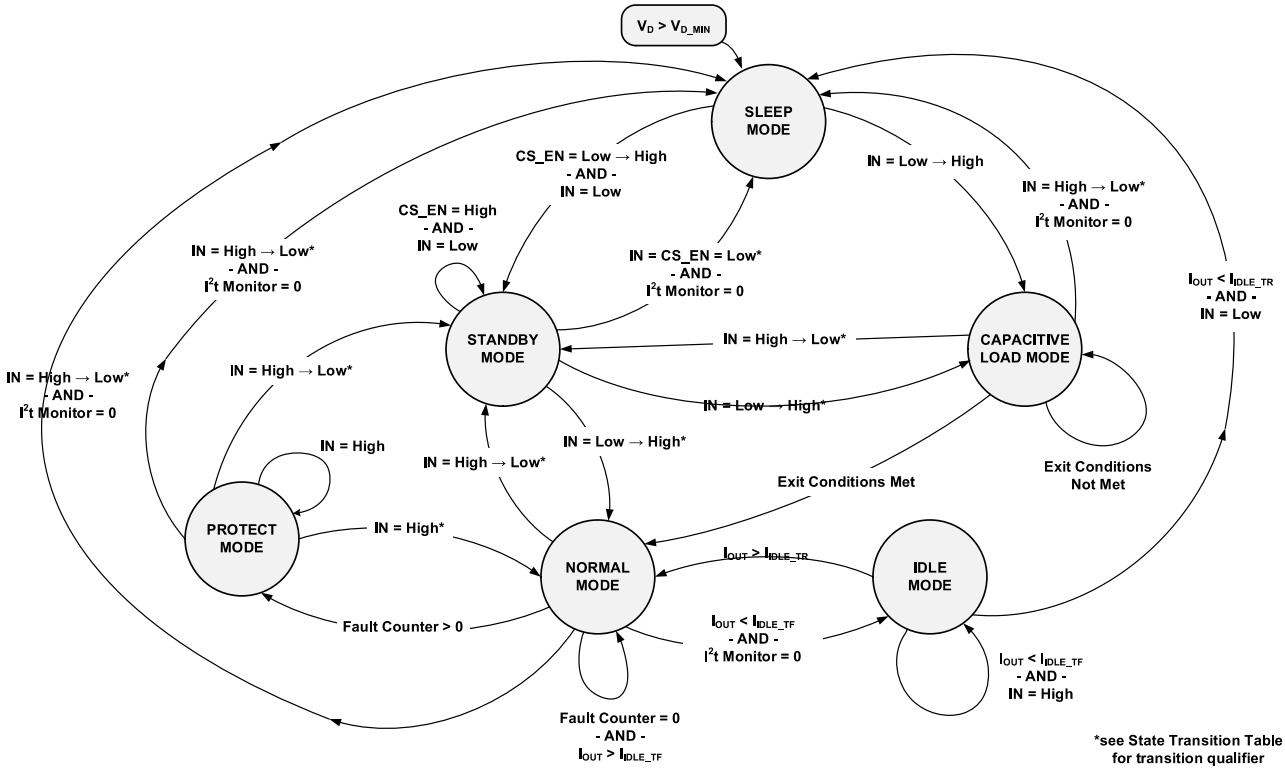


Figure 5. NCV84003G Operation Modes and Transitions

Table 18. STATE TRANSITION TABLE

Present State	Target State	Transition Criteria	Transition Qualifier
UNPOWERED	SLEEP MODE	$V_D > V_{D\_MIN}$	–
SLEEP MODE	CAPACITIVE LOAD MODE	IN = Low → High	–
SLEEP MODE	STANDBY MODE	CS_EN = Low → High – AND – IN = Low	–
NORMAL MODE	IDLE MODE	$I_{OUT} < I_{IDLE\_TF}$	I^2t Monitor = 0
NORMAL MODE	PROTECT MODE	Fault Counter > 0	–
NORMAL MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired
NORMAL MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$ – AND – I^2t Monitor = 0

Table 18. STATE TRANSITION TABLE

Present State	Target State	Transition Criteria	Transition Qualifier
STANDBY MODE	NORMAL MODE	IN = Low → High	$t > t_{Norm}$
STANDBY MODE	SLEEP MODE	IN = CS_EN = Low	$t_{IN(Rst)}$ Expired – AND – I^2t Monitor = 0
STANDBY MODE	CAPACITIVE LOAD MODE	IN = Low → High	$t < t_{Norm}$
IDLE MODE	SLEEP MODE	$I_{OUT} < I_{IDLE\_TR}$ – AND – IN = Low	–
IDLE MODE	NORMAL MODE	$I_{OUT} > I_{IDLE\_TR}$	–
PROTECT MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = High/CE_EN = Low for $t < t_{IN(Rst)}$
PROTECT MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$ – AND – I^2t Monitor = 0
PROTECT MODE	NORMAL MODE	IN = High	$t_{IN(Rst)}$ Not Expired – AND – $t_{CS\_EN(Rst)}$ Expired
CAPACITIVE LOAD MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = High/CE_EN = Low for $t < t_{IN(Rst)}$
CAPACITIVE LOAD MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$ – AND – I^2t Monitor = 0
CAPACITIVE LOAD MODE	NORMAL MODE	Exit Conditions Met (Note 24)	–

24. Refer to section Resistive and Capacitive Load Switching Characteristics.

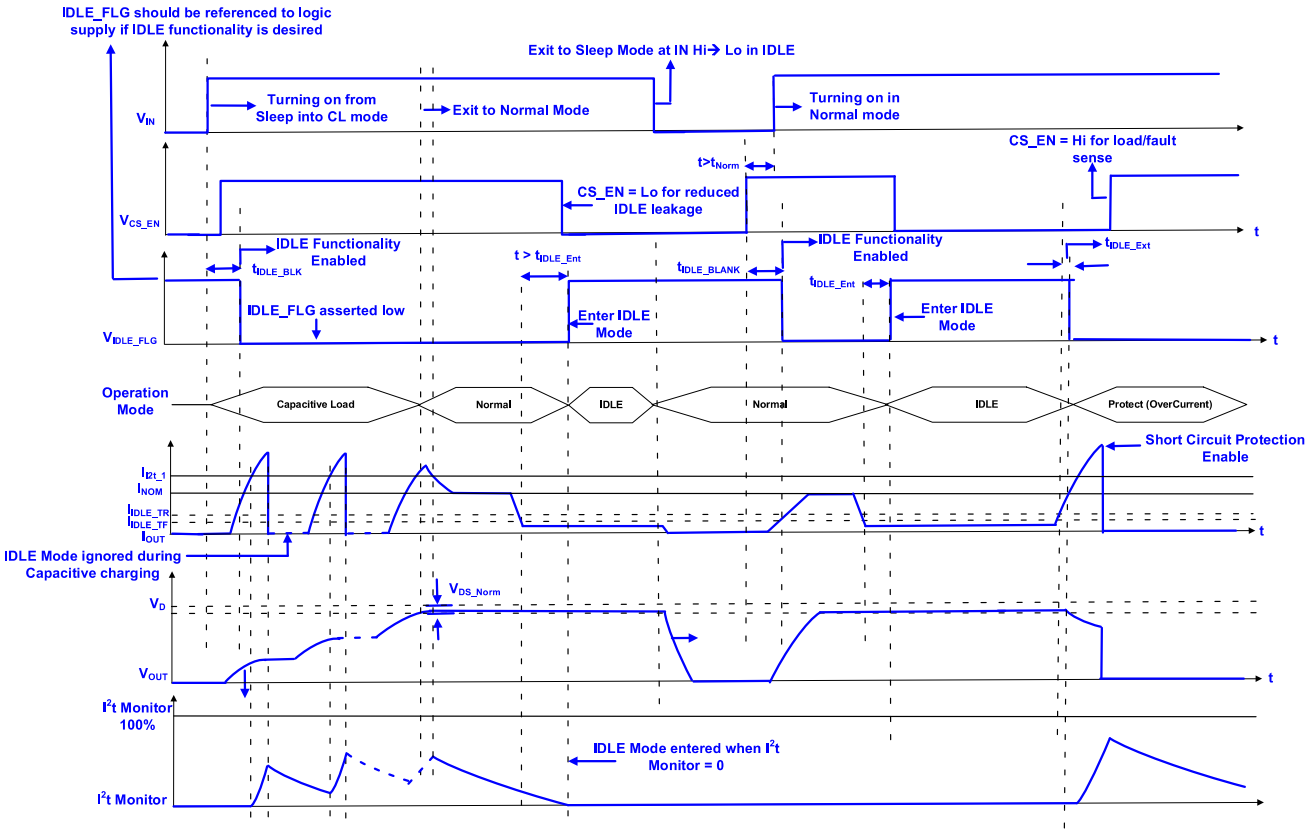


Figure 6. IDLE Mode Timing Diagram

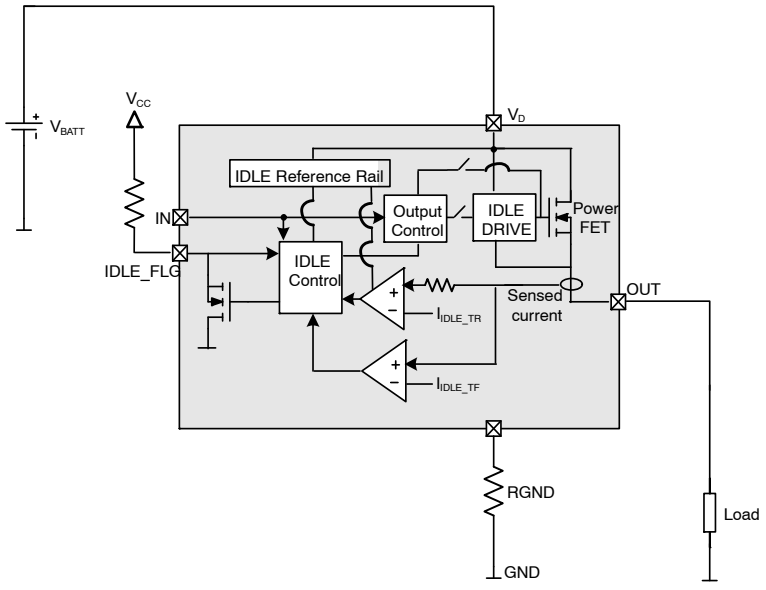


Figure 7. IDLE Mode Operational Block Diagram

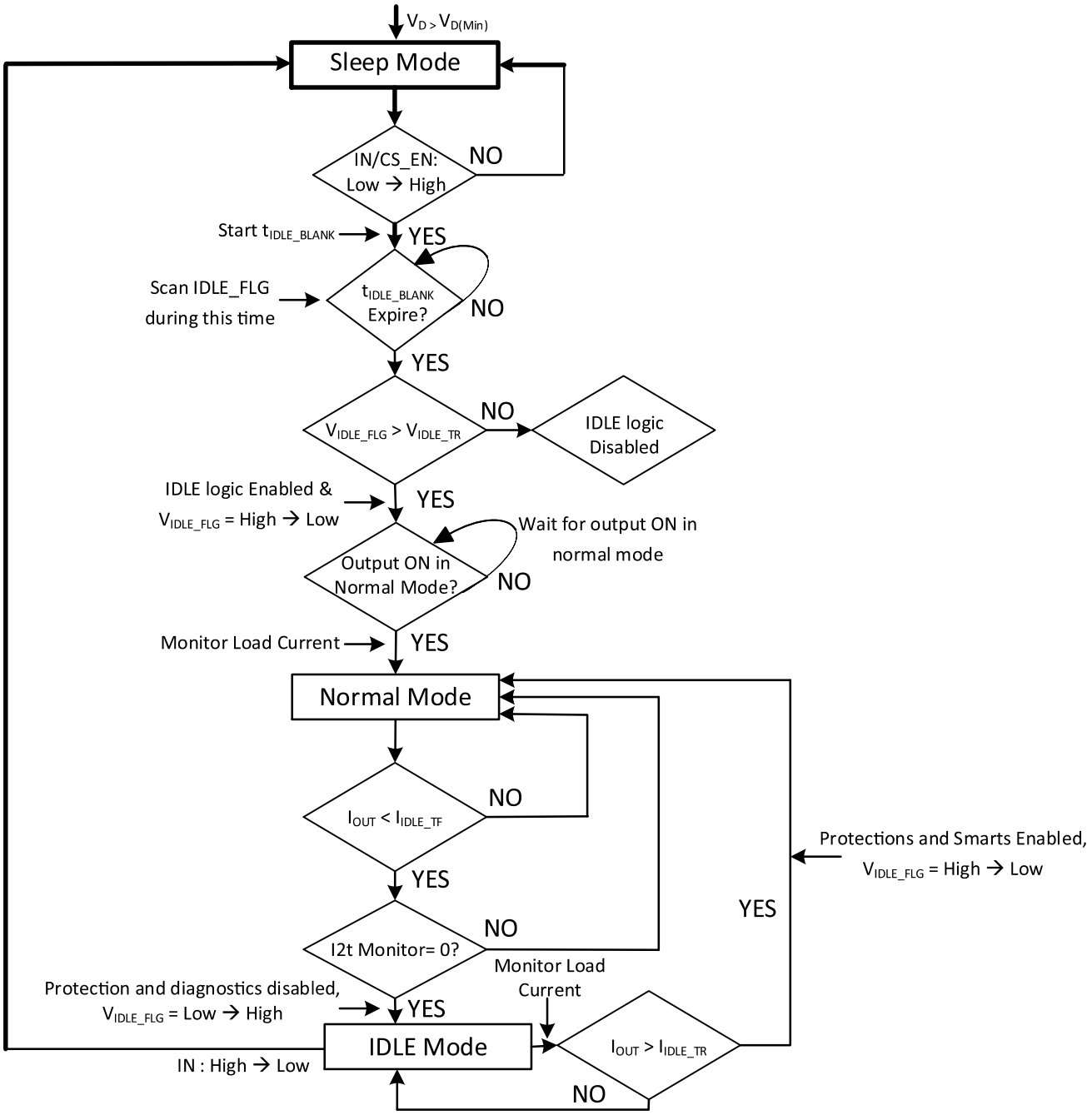


Figure 8. NCV84003G IDLE Mode Flowchart

Power Stage

NCV84003G provides output power through an integrated N−channel vertical power MOSFET. The gate overdrive is provided by an integrated charge pump.

Output ON−state Resistance

Like any MOSFET, the output's ON−state resistance R_{ON} increases with the junction temperature T_J. R_{ON} also depends on the supply voltage V_S (Figure 9).

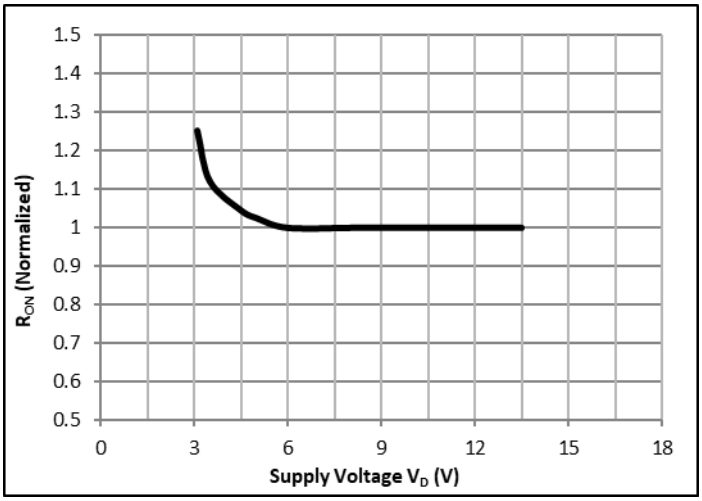


Figure 9. ON−state Resistance

In the idle mode of operation, the R_{ON} of the power stage increases to a higher value (See Table 5) as the internal controls are re−configured to allow for a reduced operating current consumption at lighter loads.

Resistive and Capacitive Load Switching Characteristics:

NCV84003G provides an integrated slew−rate control mechanism to minimize EMC in case of device switching. The turn on profiles are actively adjusted between CL mode and normal mode to differentiate a capacitive load from other types of loads.

As a default turn on strategy from sleep mode, the device automatically enters CL mode when IN is enabled. While switching on into CL mode, the slew rate is reduced leading to a gradual turn on of the output stage. The delayed turn on allows the device to charge a capacitive load by providing more power to meet the inrush requirements of the capacitor. The load levels in the initial phase of capacitor charging can be quite high causing a severe transient stress on the device. To avoid such stress, the differential thermal shutdown threshold is reduced during operation in CL mode (See Table 8). The high capacitive inrush may trigger the DTSD or overcurrent trip threshold and invoke a shutdown of the output stage. To ensure that the load is fully charged, the control circuit allows for multiple retries (See Figure 11), thereby overriding the fault retry strategy described in the ON−State Fault Retry Strategy section.

As the capacitive load is being charged, the output voltage gradually increases. The drain−source voltage drop V_{DS} is continuously sensed and once it reaches the threshold defined by V_{DS_Norm}, the device exits to normal mode with normally defined DTSD threshold and retry strategy. Further, a max time specified by t_{max_Cap} is designed in to avoid extended operation in this condition.

Since there may be applications that do not require capacitive charging, the following design implementations allow the device to operate in normal mode.

If CS_EN is forced low → high before turning on the input by a time period longer than t_{NORM}, then the device automatically enters normal mode upon enabling the input. Further, if already in CL mode, applying a CS_EN pulse longer than $t_{CS\_EN(Rst)}$ while IN = low will force the device into normal mode of operation. Such an implementation is similar to the exit from fault mode (See the Fault Retry Strategy section).

The exit conditions to Normal Mode are summarized below:

1. Auto exit at $V_{DS} < V_{DS\_Norm}$, indicating that capacitive load has sufficiently charged.
2. t_{max_Cap} expire as auto−exit to prevent extended operation in capacitive load mode.
3. Forcing CS_EN low → high before IN low → high by at least t_{NORM}.
4. Applying CS_EN pulse that is longer than $t_{CS\_EN(Rst)}$ while IN = low.

The waveforms below depict the difference in turn on slew rates and turn on profiles when switching on a nominal resistive load from sleep vs standby mode.

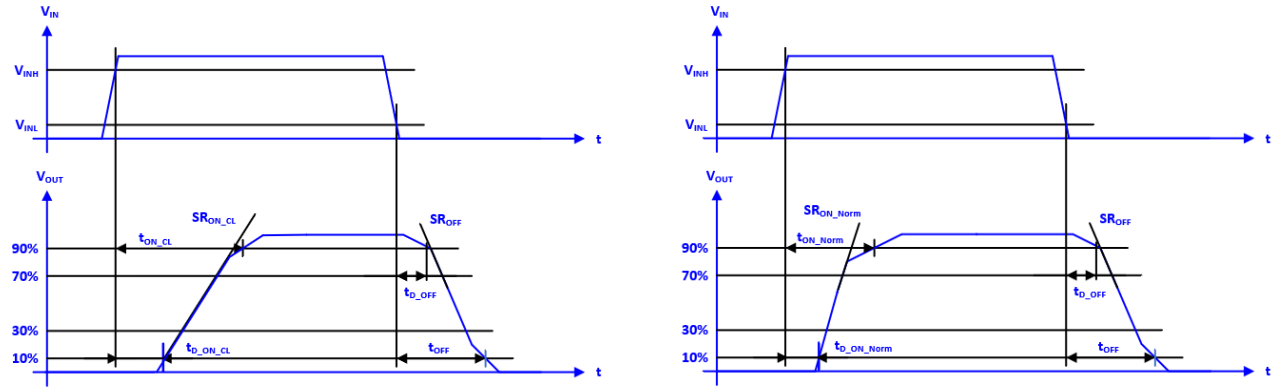


Figure 10. Resistive Load Switching Timing in turning on into a) Capacitive Load and b) Normal Mode

The transition between modes and the exit conditions cited above are described in the idealized wave−set below.

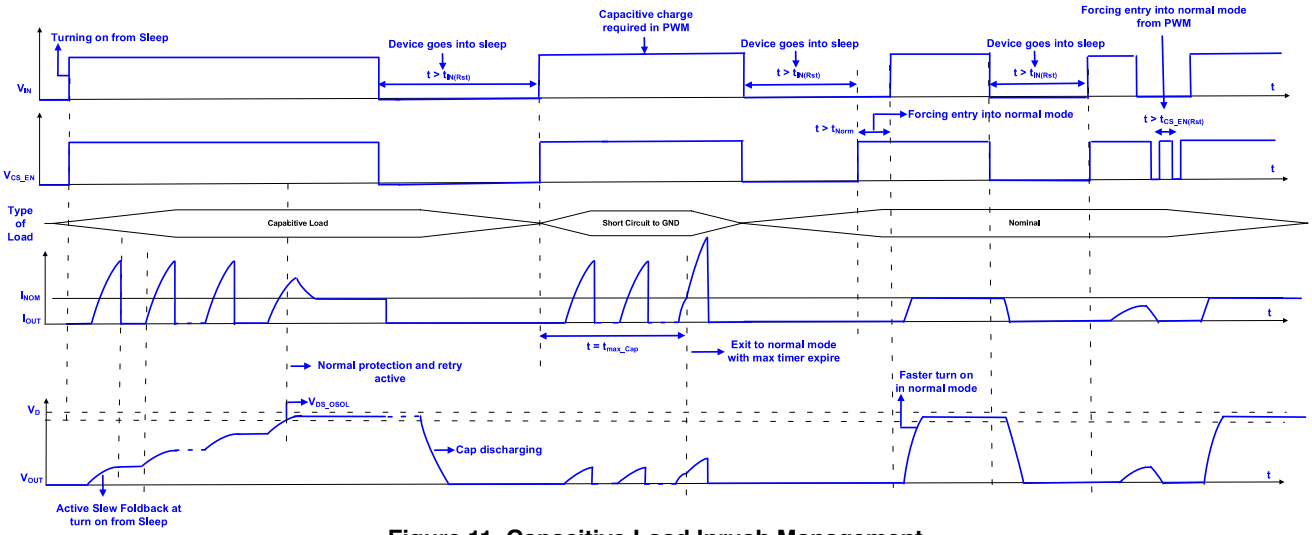


Figure 11. Capacitive Load Inrush Management

Output Clamping with Inductive Load Switch Off

The output voltage V_{OUT} drops below GND potential when switching off inductive loads. This is because the inductance develops a negative voltage across the load in response to a decaying current. The integral clamp diode (Z_{CL}) clamps the negative output voltage to a defined level relative to the supply voltage V_D. During output clamping with inductive load switch off, the energy stored in the inductance is rapidly dissipated in the device resulting in high power dissipation. This is a stressful condition for the device and the maximum energy allowed for a given load inductance should not be exceeded in any application.

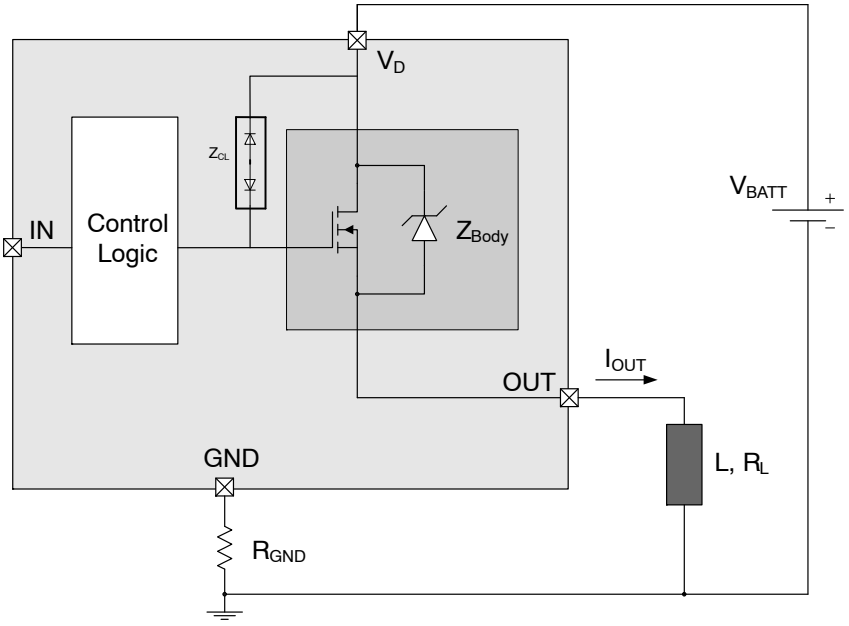


Figure 12. Output Clamping

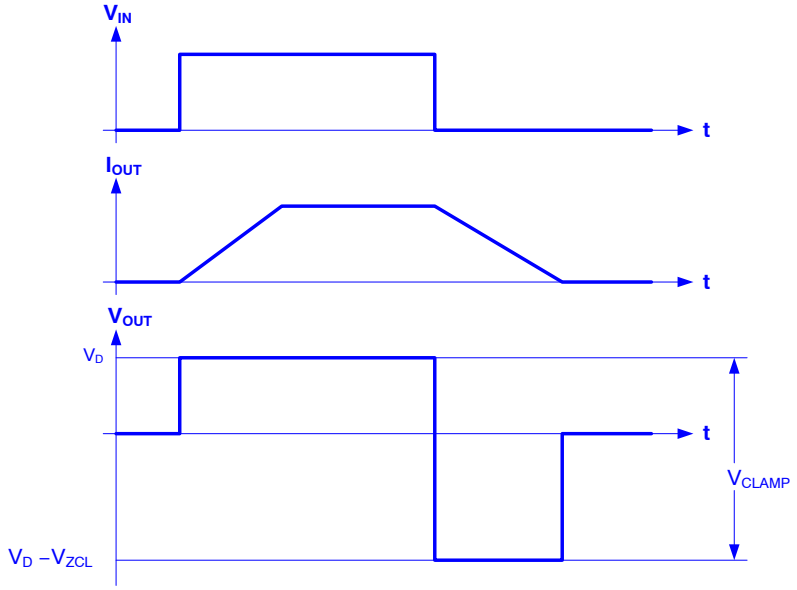


Figure 13. Inductive Load Switching Timing

The channel's energy capability [J] for inductive switching is given as follows, referring to Figure 12:

$$E = (V_D - V_{OUT}) \cdot \left[\frac{V_D - V_{OUT}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_{OUT}}{V_D - V_{OUT}}\right) + I_{OUT} \right] \cdot \frac{L}{R_L} \quad \text{(eq. 1)}$$

Protection Features

In application, the device can be subject to stressful conditions which are outside of normal operating range. To prevent damage and destruction of the device from these fault conditions, several protection functions are integrated in device design. It is important to diagnose and remove any fault condition that may exist since the protection functions cannot prevent damage over sustained fault state operation.

Inverse Current

The protection logic in the device detects when the output voltage V_{OUT} rises above the supply voltage V_D and adjusts the output stage to be turned on in an inverted configuration, thereby shunting the body diode and limiting the losses in case of an inverse current flow. The parameter R_{ON_INV} (See Table 5) specifies the resistance offered by the output stage in an inverted configuration. The current sense output stays low during inverse current conduction at the output stage. During Inverse Current operation, protection features as discussed in the ON−State Fault Retry Strategy section may not be available.

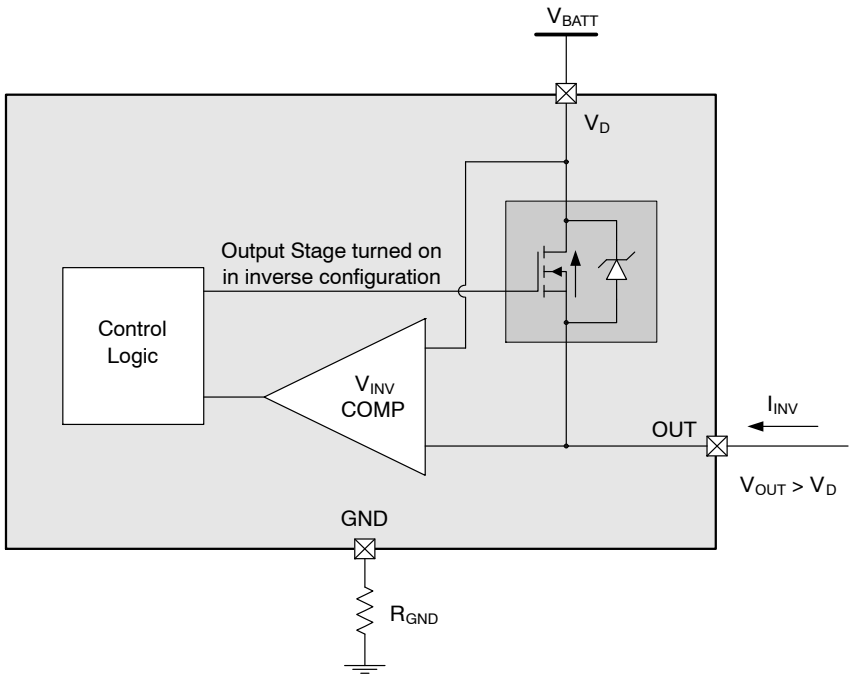


Figure 14. Inverse Current

Loss of Ground Protection

When device or ECU ground connection is lost and the load is still connected to ground, the device will turn the output OFF. In loss of ground state, the output stage is held OFF independent of the state of the input. Protection mechanisms and current sense output of the device will not be available during loss of device ground. Series resistors are recommended between the device and microcontroller to prevent the I/O pins from providing a parasitic GND path through microcontroller. Finally, it should be noted that loss of device ground protection is not guaranteed if the device is operating in IDLE mode.

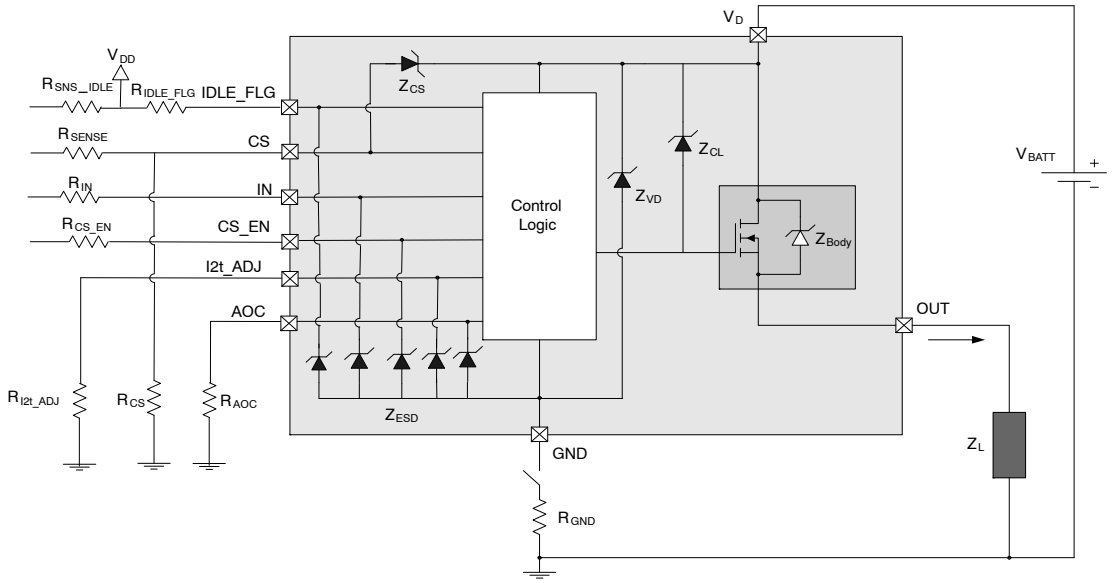


Figure 15. Loss of Ground Protection

Undervoltage Protection

The device has two under voltage threshold levels, V_{D_MIN} and V_{D_UV}. Switching function (ON/OFF) requires supply voltage to be at least V_{D_MIN}. The device features a lower supply threshold V_{D_UV}, above which the output can remain in ON state, if already ON. The protection and diagnostic features are available and functional down to V_{D_UV} (if switch already ON), however, may deviate from the nominally specified parametric performance.

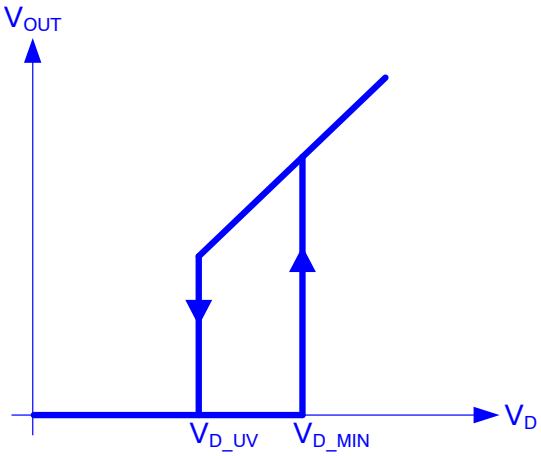


Figure 16. Under−voltage Behavior

In case the supply voltage drops below V_{D_UV} while the channel is ON (V_{IN} = High), the output stage shuts off and a delay time $t_{UV\_Recover}$ is incorporated before turning on the output again once the supply increases more than V_{D_MIN}. Such a protection scheme precludes fast repetitive turn on and turn off events and reduces the transient stress on the device as the supply periodically increases or decreases around the under−voltage threshold while conducting high currents. Once initiated, this delay timer is independent of the transitions at the IN pin as shown in the figure below. The delay $t_{UV\_Recover}$ is not present if the power supply voltage is greater than V_{D_MIN} at the time of turning the channel ON (V_{IN}: Low → High).

Further, this delay time is shortened in capacitive load mode (See Table 4) to allow fast inrush required for charging capacitive loads at low battery conditions such as cranking at cold temperatures. The waveforms below depict the behavior in case of an under−voltage event.

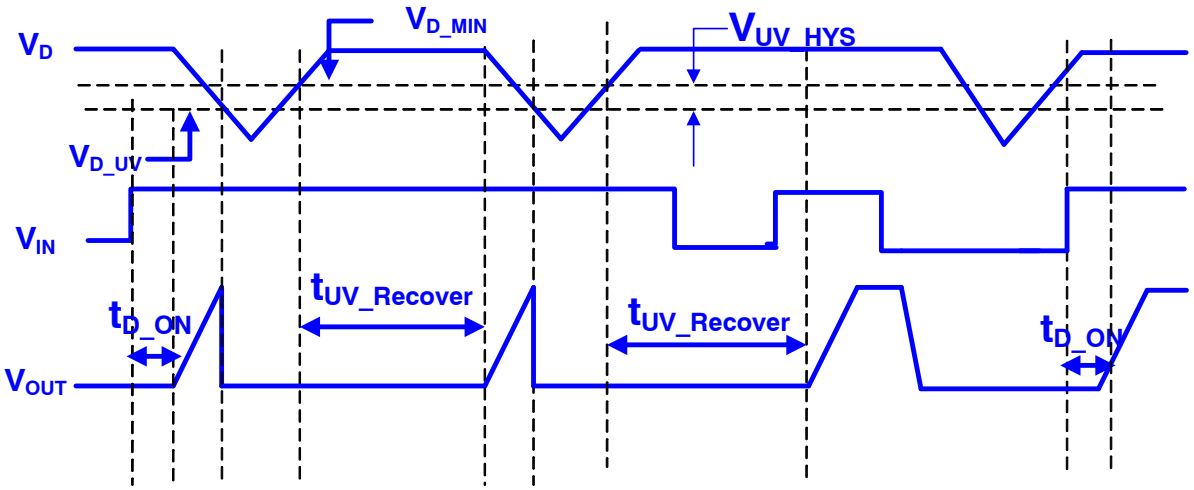


Figure 17. Under−voltage Recovery Timing

Overvoltage Protection

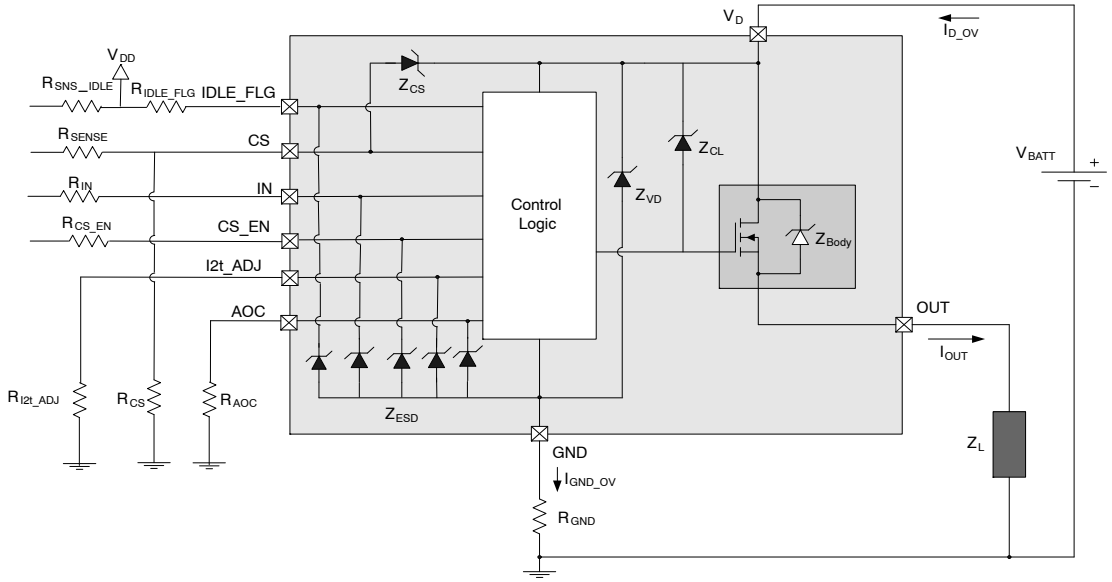


Figure 18. Overvoltage Protection Circuit

The NCV84003G employs a set of over−voltage protection zener clamp diodes− Z_{VD}, Z_{CL}, Z_{ESD} and Z_{CS}, which protect the device against abnormal high voltage events. Z_{VD} protects the logic part by clamping the voltage between supply pin V_D and ground pin GND to V_{ZVD}. Z_{CS} limits the voltage at current sense pin to $V_D - V_{ZCS}$. The output power MOSFET has an integrated drain to gate clamp Z_{CL} that provides protection by actively clamping the voltage across the MOSFET to ~V_{ZCL}. During overvoltage protection, current flowing through Z_{VD}, Z_{CS} and Z_{CL} must be limited. Load impedance Z_L limits the current in output clamp. In order to limit the current in Z_{VD}, a resistor, R_{GND}, is required in the GND path. External resistors R_{CS} and R_{SENSE} limit the current flowing through Z_{CS} and out of the CS pin into the micro−controller I/O pin. With R_{GND}, GND pin voltage is elevated to R_{GND}*I_{GND} during normal operation and must be accounted for while driving the logic inputs referenced to GND. ESD diodes Z_{ESD} clamp the voltage at logic inputs IN, CS_EN and I2t_ADJ, analog input AOC, as well as at open drain IDLE pin relative to the GND pin voltage. External resistors R_{IN}, R_{AOC}, R_{CS_EN}, R_{I2t_ADJ} and R_{IDLE_FLG} are required to limit the current flowing out of these pins. During overvoltage exposure, the device transitions into a self−protection state, with automatic recovery after the supply voltage comes back to the normal operating range. The parametric spec, diagnostic capability as well as short circuit robustness and energy capability of the output MOSFET cannot be guaranteed during overvoltage exposure.

Reverse Battery Protection

In case of Reverse Battery connection, the external load limits the current through the body diode of the output FET. An integrated blocking mechanism blocks the reverse current flowing into the GND and reduces the constraints on the value of R_{GND}. The diagnostic output stays OFF in a reverse battery configuration and no protection feature such as over−current detection or over−temperature shutdown is available. A typical application setup for reverse battery protection is shown in Figure 19. The current in the ESD protection diodes at logic pins and AOC input are limited by resistors R_{IN}, R_{CS_EN}, R_{SNS_IDLE}, R_{I2t_ADJ} and R_{AOC} respectively. Resistors R_{CS} and R_{SENSE} limit the current flowing in the CS pin. The resistor values have to be chosen to limit the current within the current ratings specified in the absolute maximum rating section.

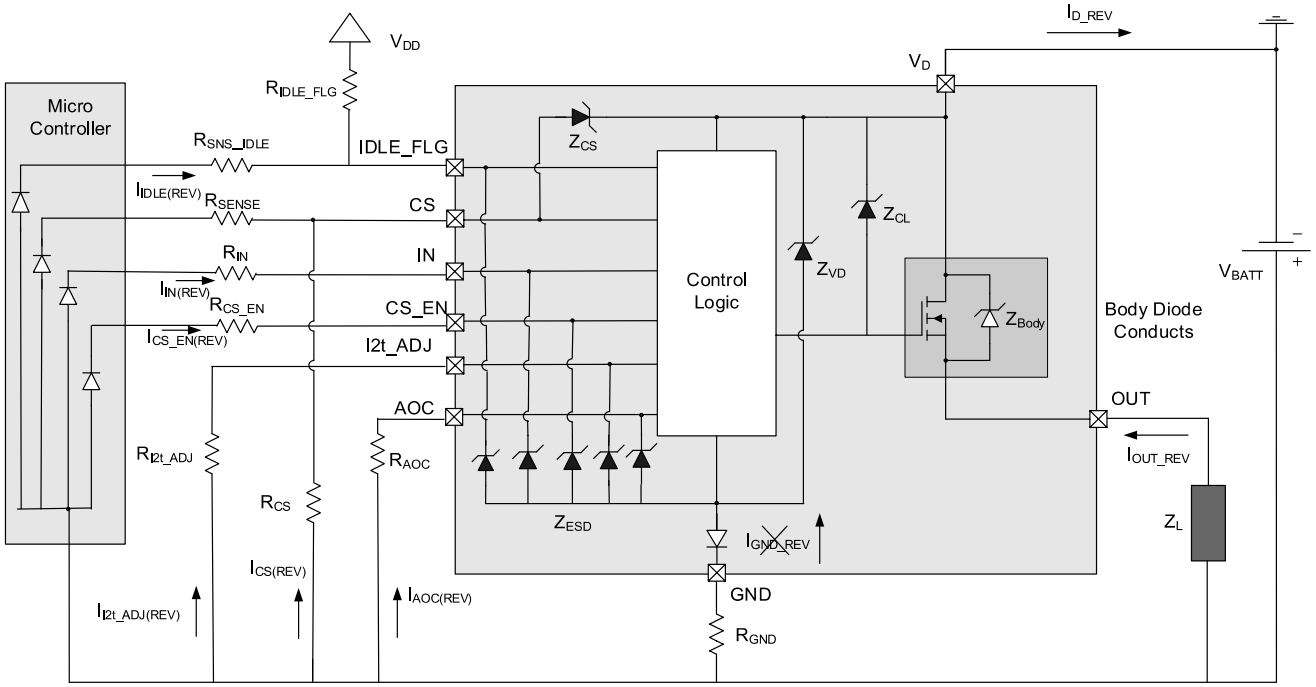


Figure 19. Reverse Battery Protection Circuit

Overload Protection

Overcurrent, I^2t, and over temperature shutdown mechanisms are integrated into NCV84003G to provide protection from overload, capacitive inrush or output short to ground conditions.

Overcurrent Shutdown

To serve multiple applications with different current and power requirements, NCV84003G offers an adjustable overcurrent detection mechanism. The overcurrent detection threshold can be adjusted by the user externally with the help of a resistor at AOC pin referenced to GND. The overcurrent threshold is designed to fold back with the AOC resistor between 80% (for R_{AOC} = 10 kΩ) and 40% (for R_{AOC} = 30 kΩ) of its maximum value. Every 1 kΩ increase in R_{AOC} in the linear range (See Figure 20) folds back the overcurrent threshold by 2% of its maximum value. Table 8 provides thresholds specific to R_{AOC} = 10 kΩ, 20 kΩ and 30 kΩ which are folded back to 80%, 60% and 40% of the highest overcurrent threshold respectively. An R_{AOC} resistor outside the linear range sets the threshold at its maximum value. Figure 20 depicts the dependence of overcurrent detection threshold on R_{AOC} resistor.

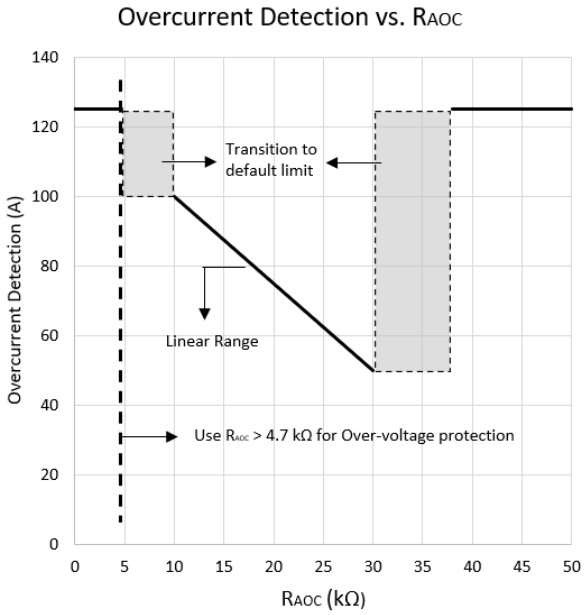


Figure 20. Adjustable Overcurrent Detection vs R_{AOC}

As shown in Figure 20, to set the threshold to its default maximum value, it is recommended to use a resistor at AOC pin that is sufficiently smaller than 10 kΩ or sufficiently greater than 30 kΩ while avoiding the resistors close to transitions in and out of linear range. For example, R_{AOC} = 4.7 kΩ or R_{AOC} = 40 kΩ will ensure that overcurrent detection threshold is set to its maximum value. Further, an R_{AOC} ≥ 4.7 kΩ is recommended to protect the ESD structures at this pin against reverse battery and overvoltage events. It is not recommended to short AOC pin to GND in order to protect the internal ESD from stresses inflicted in such events. Further, leaving this pin floating, or open in the application can lead the internal interface susceptible to inadvertent high frequency injections and is also therefore not recommended.

It's possible for the current profile to observe some overshoot beyond the specified I_{LIM} threshold (especially in case of extremely low impedance shorts) because of the delay between current detection and consequent shut−off of the output stage. The safety of the device, will, nevertheless be ensured in a short circuit event.

The overcurrent detection threshold is reduced to a lower value in case of high drain−source voltage. This is done to limit the amount of power dissipation in the device and consequential thermal transients. The curve below depicts the trend in normalized I_{LIM} where the value "1" represents the peak measured at V_{DS} = 5 V. A similar protection logic is applied at high Drain voltages, specifically for conditions such as Jump Start (See Table 8). The corresponding I^2t profiles (as described below), are specifically designed for harness protection and do not change with applied V_D or V_{DS}.

Finally, the over−current detection is designed to be relatively independent of junction temperature to ensure that it does not infringe with the I^2t protection.

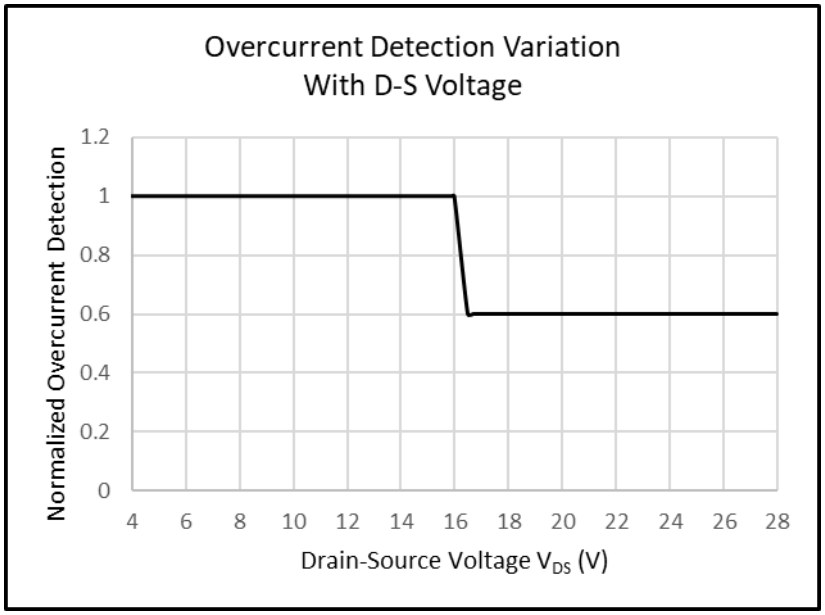


Figure 21. Over−Current Detection Variation with Drain−Source Voltage

I^2t Protection

In addition to overcurrent shutdown, NCV84003G comprises of a smart overload protection in the form of an I^2t function that emulates the current vs time profile of a conventional fuse. The built−in circuit forces a shutdown of the output stage when high current is conducted over extended intervals exceeding the I^2t limit of the device per the curve depicted in Figure 22 below. Table 10 specifies the I^2t profile in the form of maximum ON time permitted at different current thresholds. As the current level increases above the minimum threshold I_{I2t_1}, the internal I^2t monitor increases in value as well. Further, the I^2t monitor accounts for the changes in load level by integrating the timing response as output current increases through multiple thresholds, thereby keeping track of the "accumulated heat" as in case of a fuse. The intelligent monitor also reduces in value in case the output current falls below the threshold I_{I2t_1} to account for the "heat lost" in applications such as PWM at overload. When the I^2t monitor reaches 100% of the designed in limit, the output stage is safely shut off. Once shut off, the retry strategy is defined in the section ON State Fault Retry Strategy. This response allows proper sizing of the harness in an application by ensuring that a given current will never exceed over a given time threshold thereby keeping the harness insulation within the defined safe operating limits.

The I^2t function is bound on the lower end by highest allowed steady state current I_{I2t_1} below which the I^2t protection is inactive. It is also bound on the upper end by the maximum I^2t threshold, I_{I2t_11} that is associated with the minimum allowed ON time.

Similar to the adjustability in overcurrent detection NCV84003G offers adjustability in I^2t profiles that allow the user to choose wire harness size for different applications with the same device. The external resistor at I2t_ADJ pin allows scalable profiles in a foldback pattern as depicted in the figure below. Similar to AOC dependence on external resistor, the I^2t profile also folds back with the I2t_ADJ resistor between 80% (for R_{I2t_ADJ} = 10 kΩ) and 40% (for R_{I2t_ADJ} = 30 kΩ) of the highest designed profile (outermost curve per Figure 22). Every 1 kΩ increase in R_{I2t_ADJ} in the linear range (See Figure 22) folds back the I^2t profile by 2%. Table 10 provides maximum current thresholds for I^2t profiles specific to R_{I2t_ADJ} = 10 kΩ, 20 kΩ and 30 kΩ which are folded back to 80%, 60% and 40% respectively of the maximum current threshold for the highest I^2t profile. Other current thresholds for the selected profile, thereby, scale commensurately by the same percentage of the corresponding threshold for the highest profile. Figure 23 plots the I^2t profiles for the specified resistor values. It should be noted that these curves are only representatives of the allowed range, and any I^2t profile can be selected between these curves by varying the R_{I2t_ADJ} resistor based on the requirements of the application. The internal logic defaults to the highest I^2t profile if the R_{I2t_ADJ} resistor is less than or equal to 4.7 kΩ, and defaults to the lowest I^2t profile if the RI2t_ADJ resistor is greater than or equal to 40 kΩ (Refer to Figure 22).

To select the highest I^2t profile in the application, it is recommended to use a resistor at I2t_ADJ pin that is sufficiently smaller than 10 kΩ while avoiding the resistors close to transitions in to linear range. For example, R_{I2t_ADJ} = 4.7 kΩ will ensure the selection of highest profile. In case of an inadvertent open circuit, or a high "leakage" resistance observed at this pin will cause the selection of lowest I^2t profile to guarantee safety of application harness, PCB traces etc.

Lastly, as in case of AOC pin, it is not recommended to short I2t_ADJ pin to GND in order to protect the internal ESD from stresses inflicted in reverse battery, or

over−voltage events. Leaving this pin floating, or open in the application can lead the internal interface susceptible to high frequency injections and is also therefore not recommended.

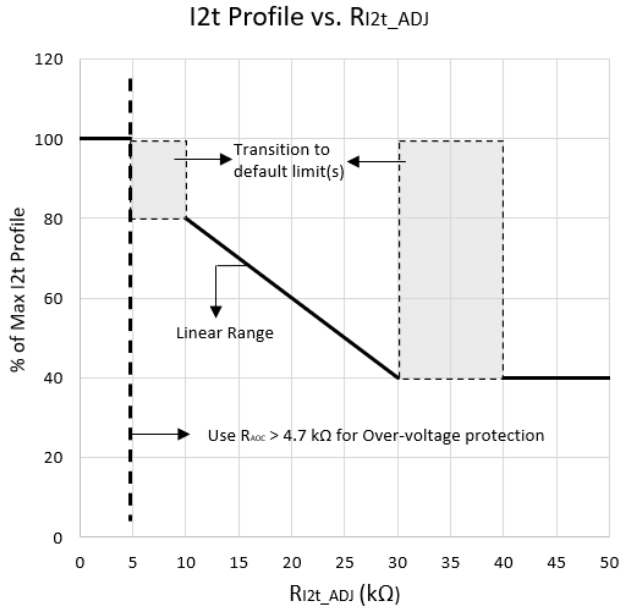


Figure 22. Adjustable I^2t Profiles vs R_{I2t_ADJ}

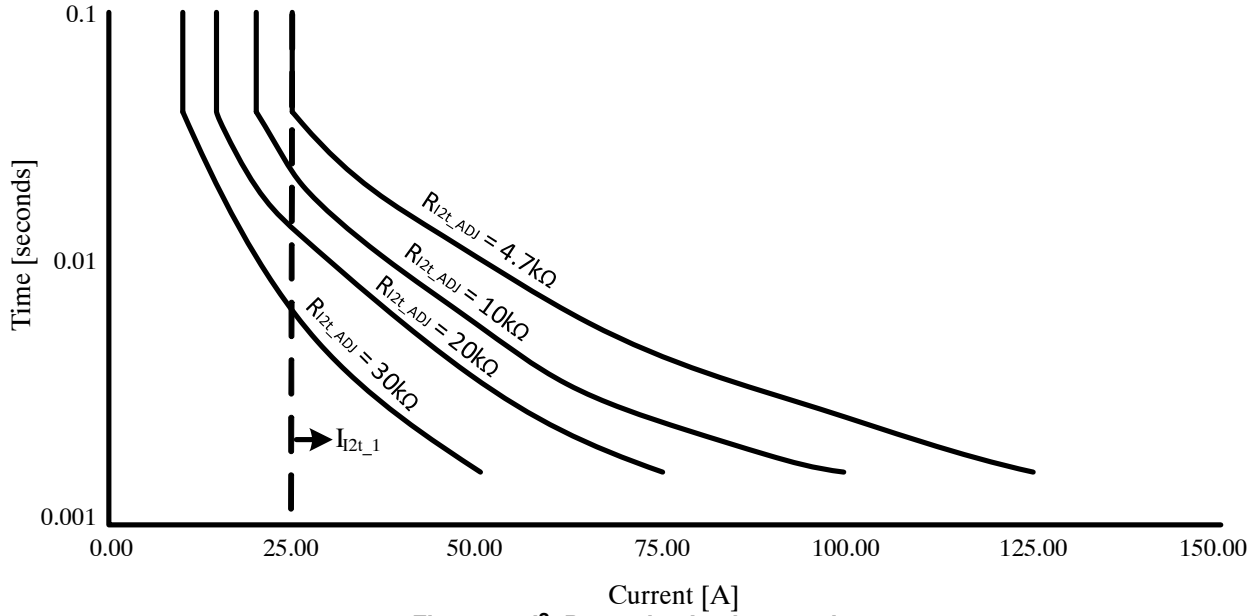


Figure 23. I^2t Protection Implementation

It should also be noted that the profiles depicted in Figure 23 are assuming $T_{J(start)} \leq 100°C$ for each current step and that the device is mounted on a four−layer 2s2p board based on JEDEC JESD 51−7 specification (See Table 3). Having inadequate external heat sinking in the application may cause the junction temperature to rise rapidly and output stage may be shut off sooner than the times indicated because of thermal shutdown.

NCV84003G can serve multiple load and harness conditions by allowing independent adjustability of over−current detection threshold and I^2t profile. For example, if a high I^2t capability is desired with a reduced over−current threshold for the load, or a high load inrush is desired while keeping the I^2t profile for the harness at minimum, then the example profiles as depicted in Figure 24 can be referenced. Caution must be exercised while selecting an overcurrent trip threshold that is significantly greater than the maximum current threshold (I_{I2t_11}) for the selected I^2t profile. In such a case, the I^2t monitor will enforce the same allowed ON time − t_{I2t_11} for

any current greater than I_{I2t_11} until the overcurrent protection is triggered.

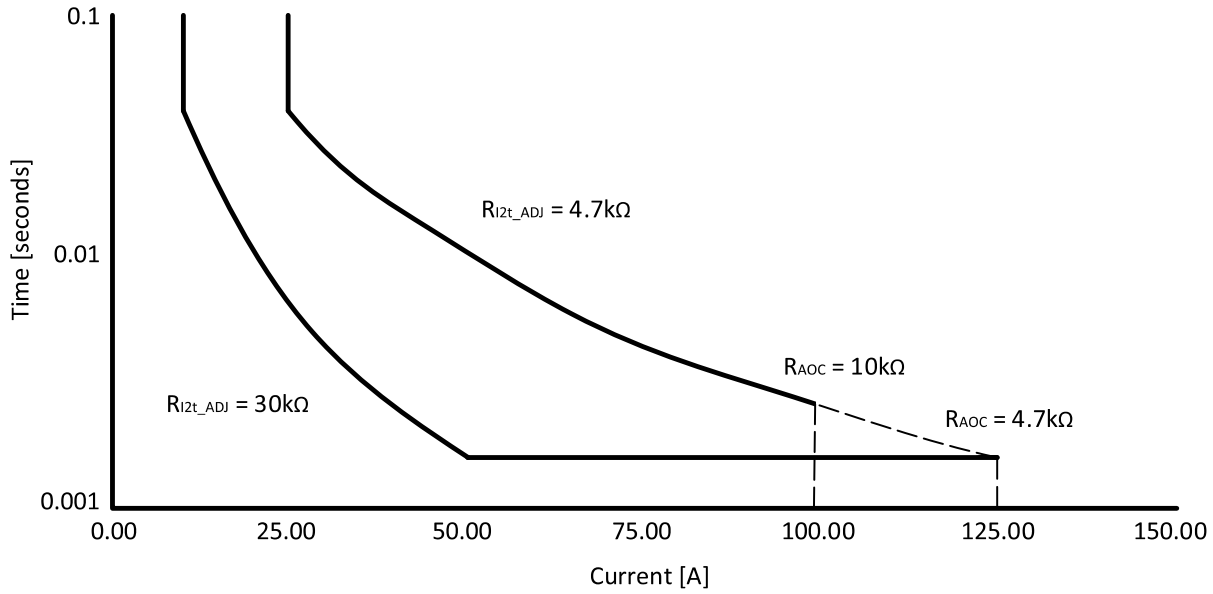


Figure 24. I^2t Maximum Overcurrent Adjustability

Over Temperature Protection

NCV84003G has two over temperature shutdown mechanisms. They are implemented by incorporating an absolute and a differential temperature sensor. To prevent damage and/or destruction, when either of the two sensors is activated, the output will be switched OFF. In case of a prolonged high power dissipation condition, a rapid increase in the junction temperature creates a severe temperature gradient within the device. When this differential temperature swing reaches the defined threshold (T_{DTSD}, per Table 8), the differential temperature sensor is activated thereby switching OFF the device. In case if the junction temperature reaches thermal shutdown temperature T_{TSD}, the absolute temperature sensor is activated, and the output stage will be switched OFF. The output will be allowed to turn back ON when the differential temperature drops to a safe value determined by the hysteresis T_{TSD_HYS} (See Table 8) with a retry strategy presented in the next section.

It should be noted that in capacitive load mode, the DTSD threshold is reduced to T_{DTSD_CL} (See Table 8) to limit the transient stress on the device while charging a capacitive load. Further, the thermal protections as described above will override the I^2t protection in case the differential or absolute thermal limits of the die are exceeded.

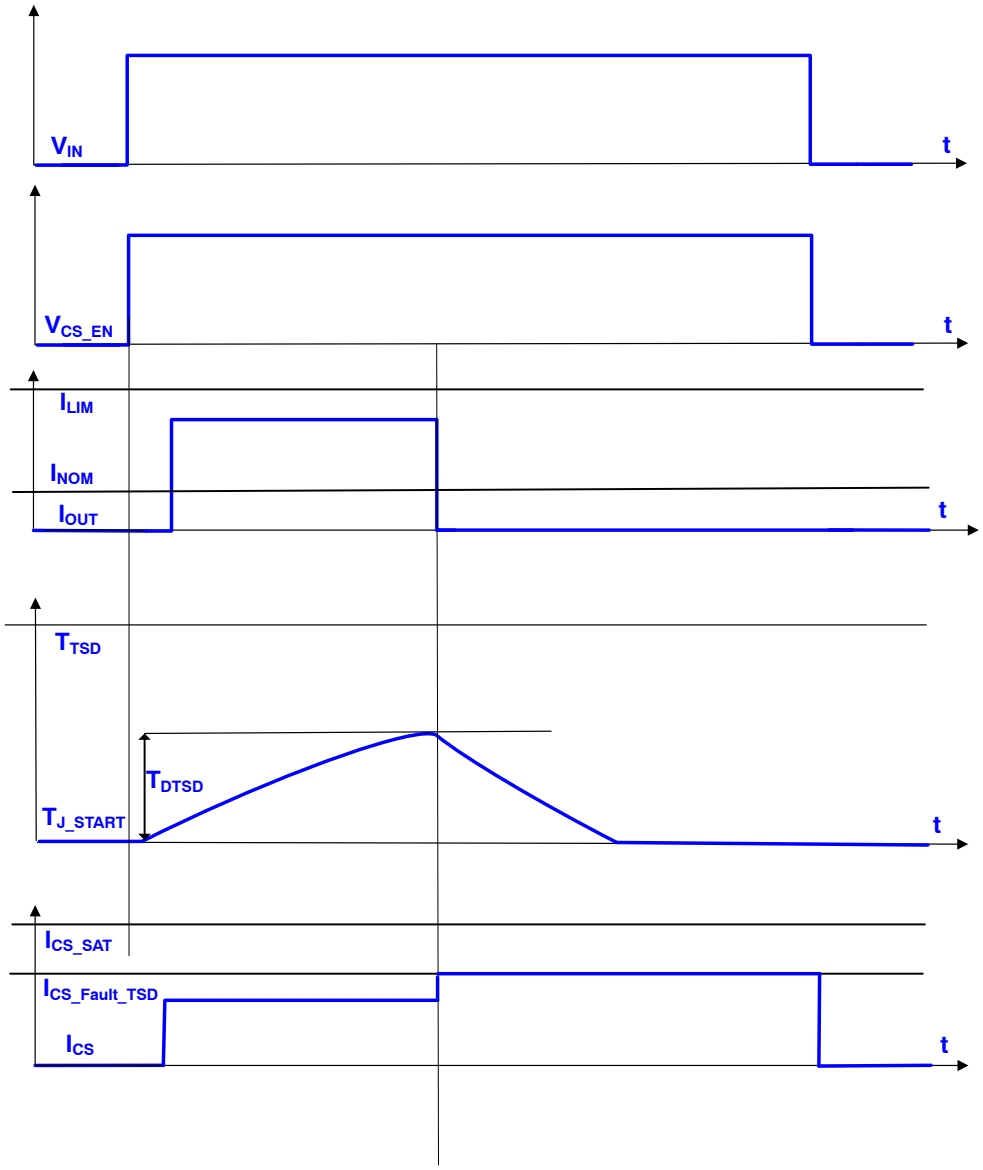


Figure 25. Over−Temperature Protection

ON State Fault Re−try Strategy

The timing diagram below explains the re−try strategy in case of an overcurrent and/or over−temperature fault state. It should be noted that while the particular example below considers an overcurrent detection condition in case of short circuit to GND, the same philosophy can be applied to re−try strategy in case of an over−temperature shutdown event as well.

When exposed to the fault conditions mentioned above, the device emulates the behavior of a fuse and the output stage is latched off after incrementing the fault counter once to protect the device from subsequent high power re−try pulses. The fault counter can be reset to zero (default) by forcing IN low for a time period $t > t_{IN(Rst)}$, or by forcing a diagnostic enable pulse while IN = low as shown above. If the IN pin is switched Low → High before the $t_{IN(Rst)}$ timer expires, then the output stage is forced to stay off. The timer is reset and starts over again when the input goes low the next time. A diagnostic enable based reset provides a faster solution to reset the counter (typically used in cases where the application microcontroller detects a normal operating condition, and a quick re−start is desired).

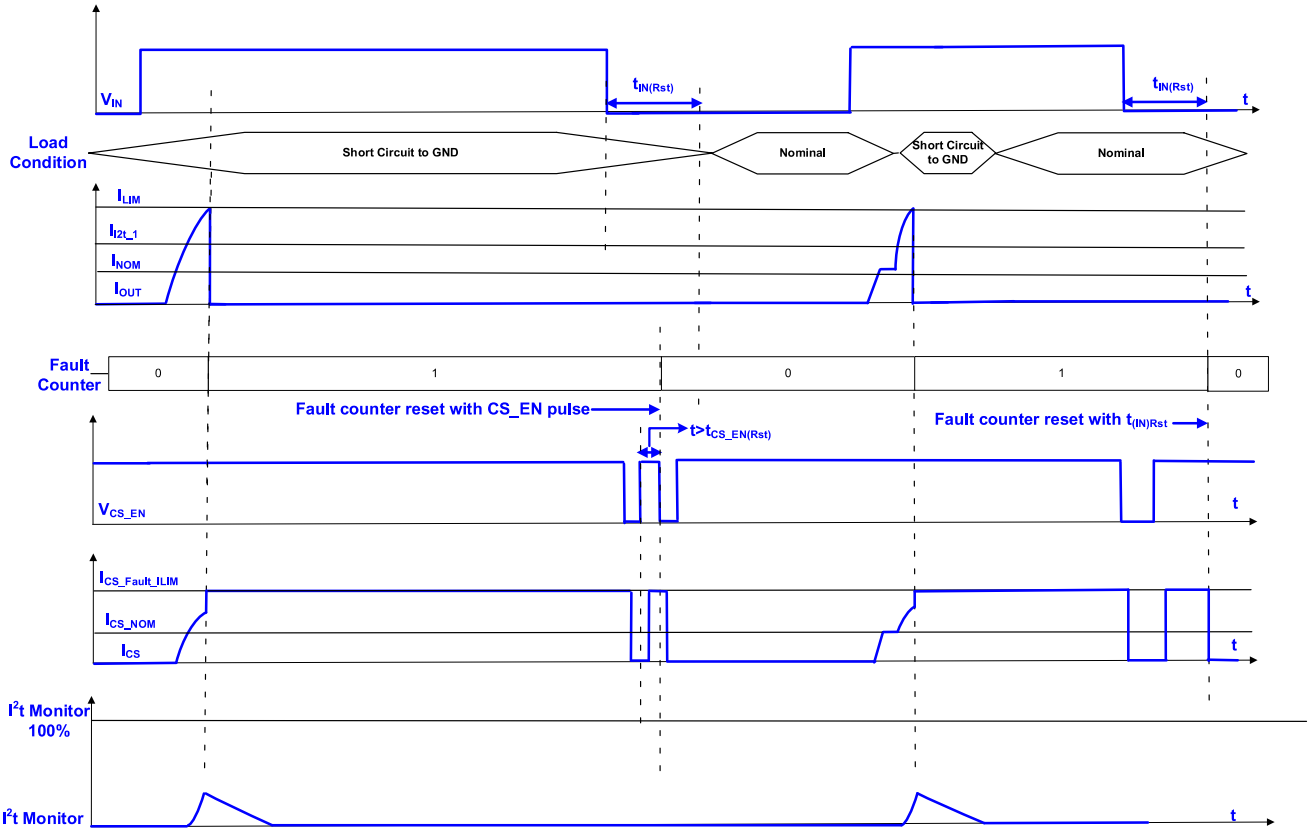


Figure 26. Re−try Strategy in Case of Current Limit and/or Over−Temperature

The retry strategy as defined above is overridden while turning on into capacitive load mode to allow multiple retries while charging a capacitive load. It is therefore recommended to exit the capacitive charging mode with an IN pulse (See Resistive and Capacitive Charging) in case of a shorted load to prevent the device from repetitive transient stresses in this mode. The current sense fault output and voltage at the output node should be sensed to make this decision.

In case of extended overload condition applied to the device, the I^2t monitor increases in value and eventually reaches 100% of the designed limit which then latches off the output stage. The condition is depicted in the wave−set below.

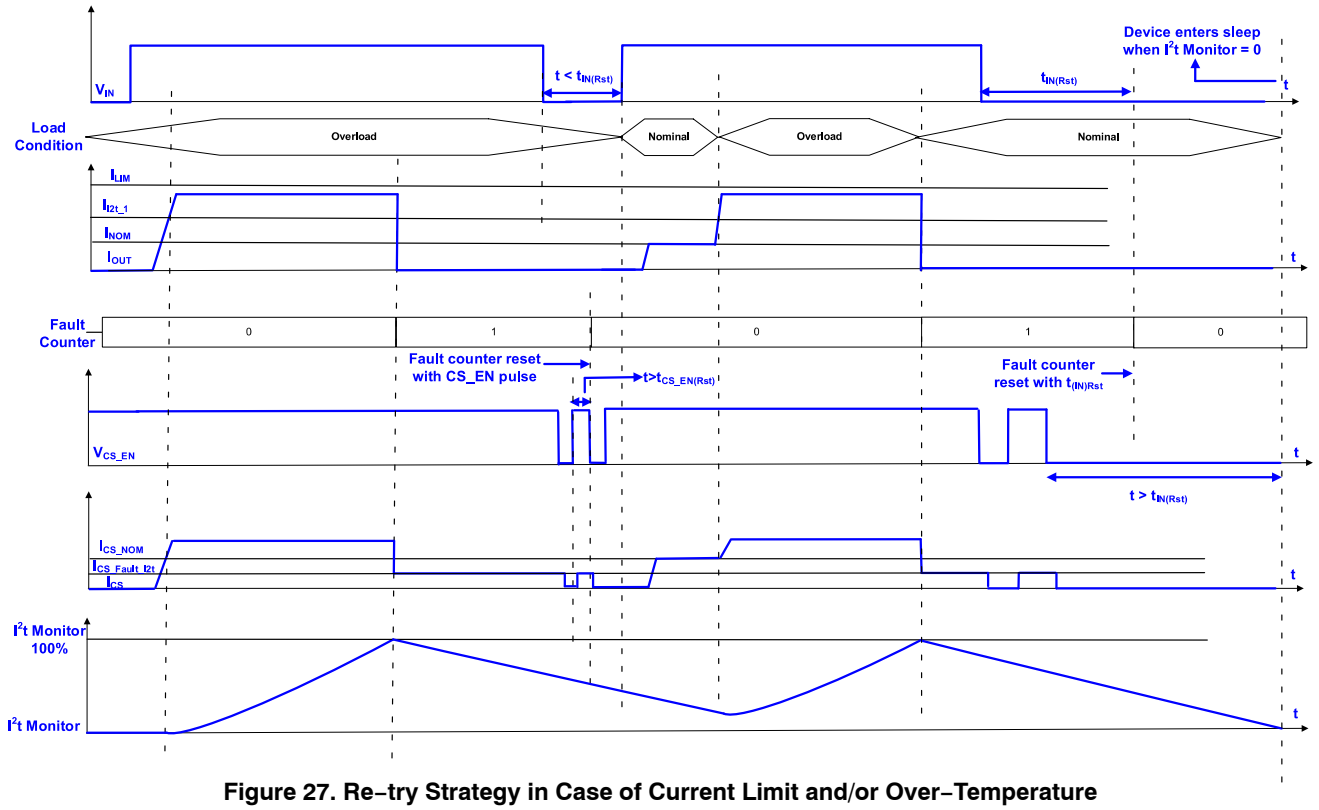


Figure 27. Re−try Strategy in Case of Current Limit and/or Over−Temperature

The flowchart in Figure 28 below summarizes the operation in case of an ON−state fault.

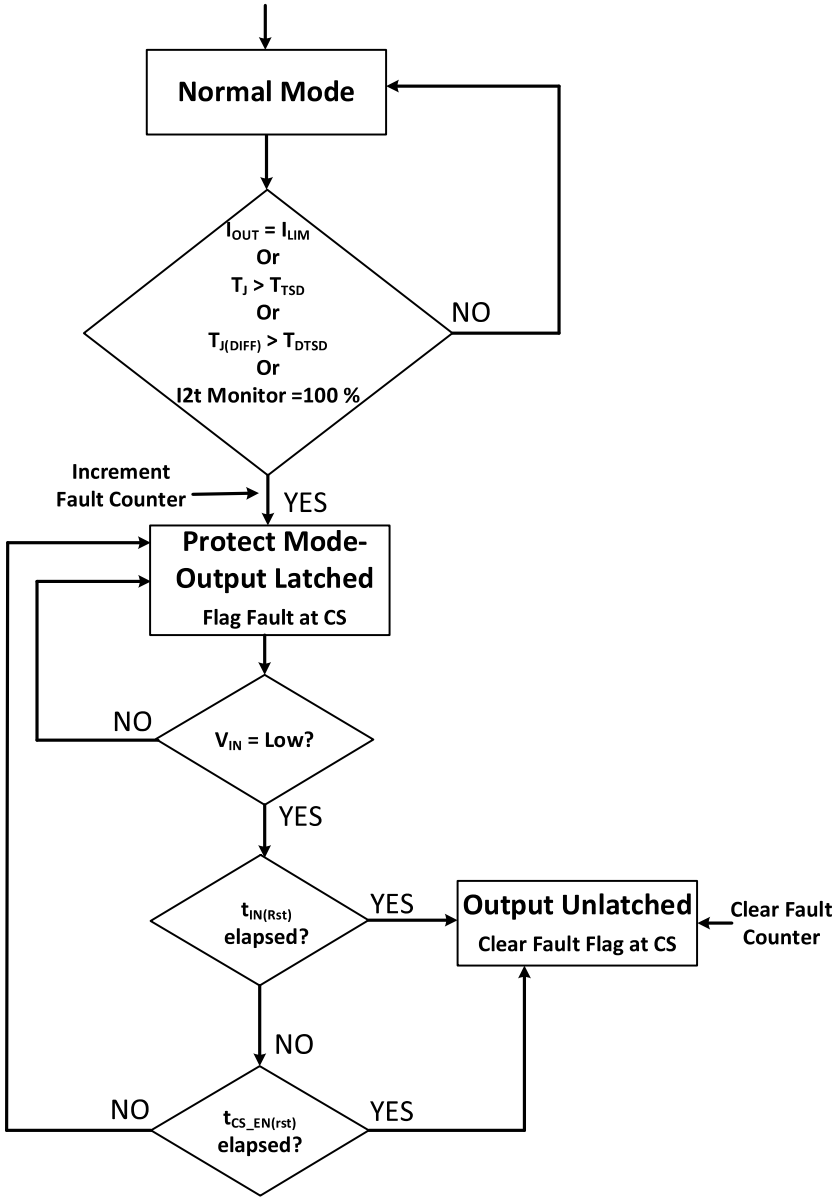


Figure 28. On−State Re−try Strategy Flowchart

Current Sense Output Timing

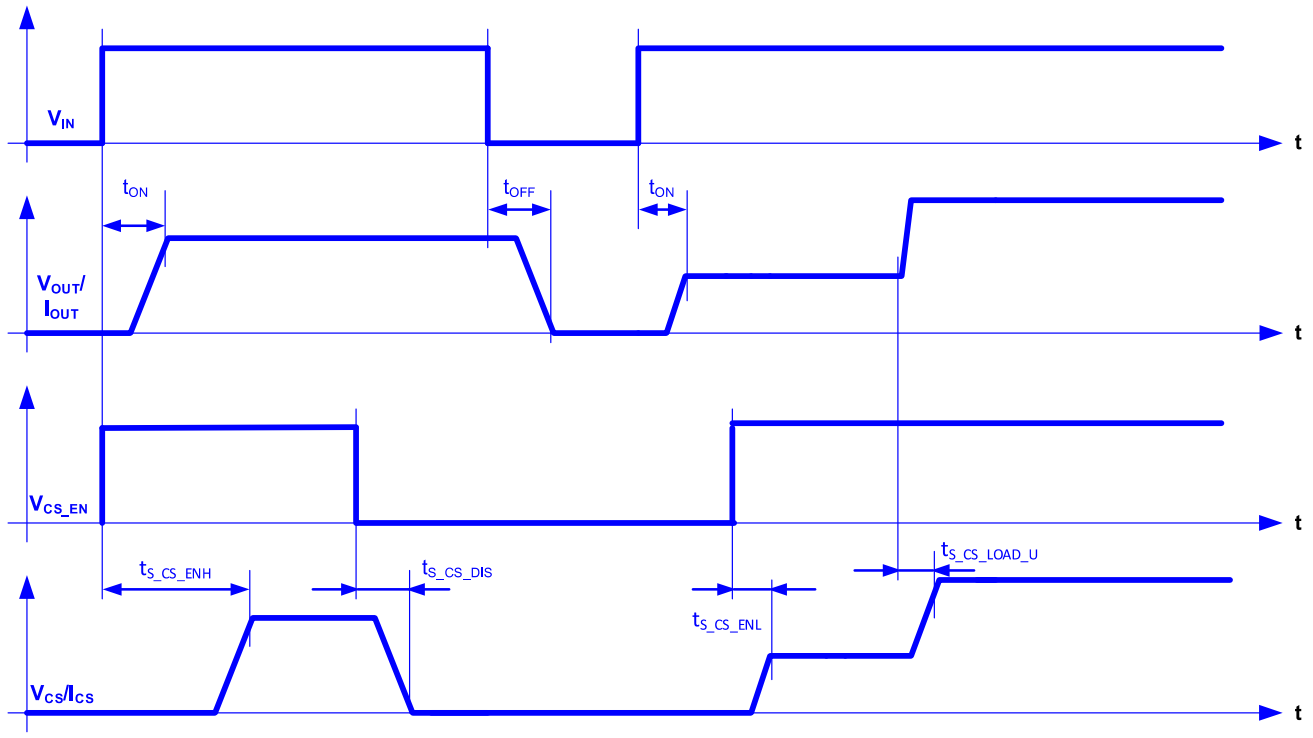


Figure 29. Current Sense Timings

Open Load/Short to V_{BATT} Detection in OFF State

OFF State Open Load (OSOL) diagnosis can be performed by activating an external resistive pull−up path (R_{PU}) to V_{BATT}. To calculate the pull−up resistance, external leakage currents (designed pull−down resistance, humidity−induced leakage etc.) as well as the open load threshold voltage V_{DS_OSOL} have to be considered. A switch can be used open the battery connection to R_{PU} to prevent undesired leakage through this path in case an open load diagnostic is not required.

A short circuit to V_{BATT} in off state is also detected by the same analog circuit block.

It should be noted that OSOL Fault current range is exclusive to and lower than other fault conditions such as a TSD or a current limit. This segregation of fault levels will help user to distinguish an OSOL fault from a case where a fault is being flagged high in OFF state due to an un−expired Fault counter (See Table 12).

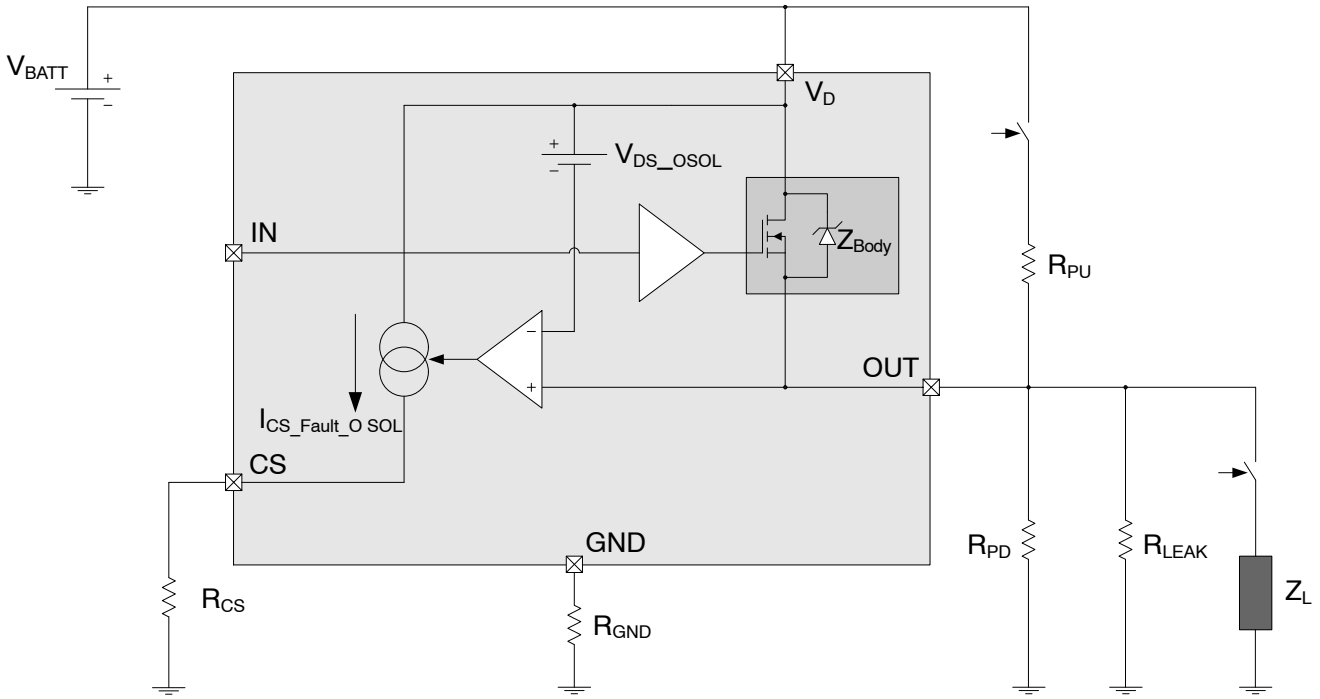


Figure 30. Off State Open Load Detection Circuit

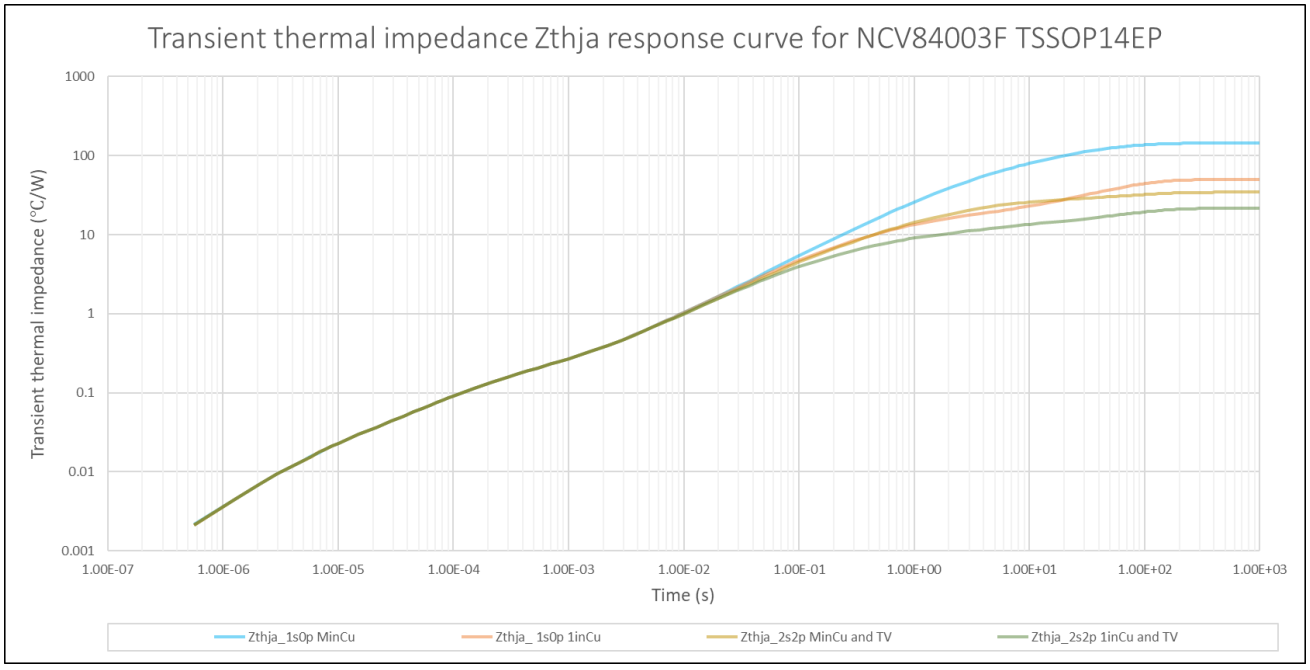
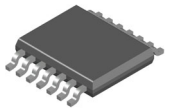


Figure 31. Transient Thermal Response

PACKAGE DIMENSIONS



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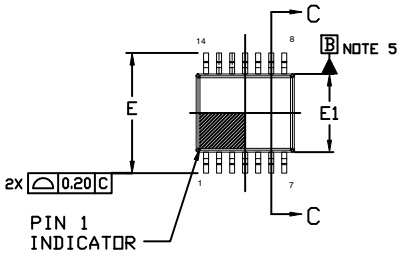
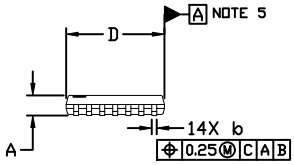
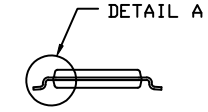


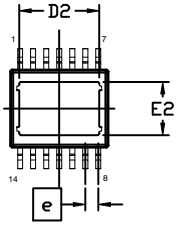
TOP VIEW



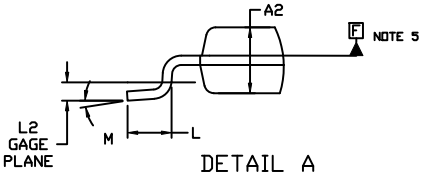
SIDE VIEW



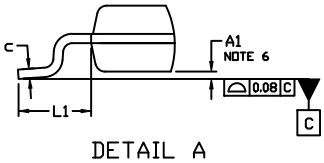
SECTION C-C



BOTTOM VIEW



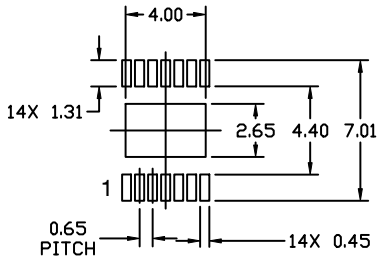
DETAIL A



DETAIL A
(SUPPLEMENTAL)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.127 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. LEAD THICKNESS (c) AND LEAD WIDTH (b) INCLUDE PLATING THICKNESS.

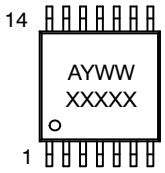
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.15
A1	0.00	---	0.10
A2		0.95 REF	
b	0.20	---	0.30
c		0.20 REF	
D	4.80	4.90	5.00
D2	3.90	4.00	4.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.55	2.65	2.75
e		0.65 BSC	
L	0.42	---	---
L1		1.05 REF	
L2		0.25 REF	
M	0°	---	8°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales