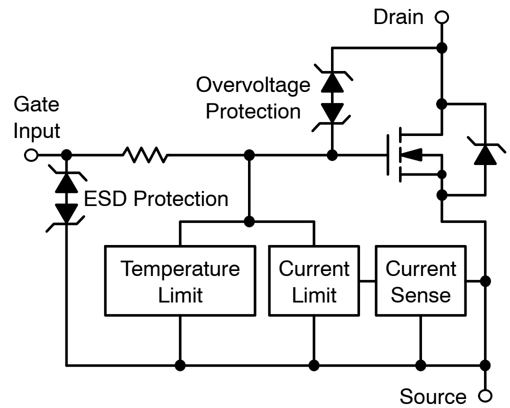
# Self-Protected Low Side Driver with Temperature and Current Limit

## 65 V, 7.0 A, Single N−Channel

# NCV8406A, NCV8406B

| $V_{DSS}$ (Clamped) | $R_{DS(on)}$ TYP | $I_D$ TYP (Limited) |
|---|---|---|
| 65 V | 210 mΩ | 7.0 A |




NCV8406A/B is a three terminal protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

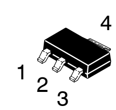
### Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- These Devices are Faster than the Rest of the NCV Devices
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

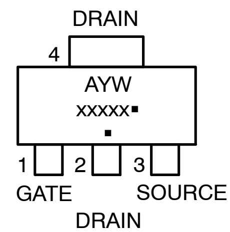
### Typical Applications

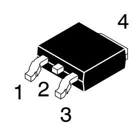
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

### MARKING DIAGRAM

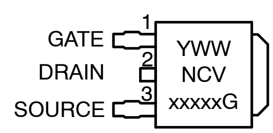



**SOT−223
CASE 318E
STYLE 3**




**DPAK
CASE 369C**




A = Assembly Location
Y = Year
W, WW = Work Week
xxxxx = 8406A or 8406B
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information page 10 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 10.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain−to−Source Voltage Internally Clamped | | $V_{DSS}$ | 60 | Vdc |
| Gate−to−Source Voltage | | $V_{GS}$ | ± 14 | Vdc |
| Drain Current | Continuous | $I_D$ | Internally Limited | |
| Total Power Dissipation − SOT−223 Version<br>@ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2) | | $P_D$ | <br>1.25<br>1.81 | W |
| Total Power Dissipation − DPAK Version<br>@ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2) | | $P_D$ | <br>1.31<br>2.31 | W |
| Thermal Resistance − SOT−223 Version<br>Junction−to−Soldering Point<br>Junction−to−Ambient (Note 1)<br>Junction−to−Ambient (Note 2) | | <br>$R_{\theta JS}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>7.0<br>100<br>69 | °C/W |
| Thermal Resistance − DPAK Version<br>Junction−to−Soldering Point<br>Junction−to−Ambient (Note 1)<br>Junction−to−Ambient (Note 2) | | <br>$R_{\theta JS}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>95<br>54 | °C/W |
| Single Pulse Inductive Load Switching Energy<br>(Starting $T_J$ = 25°C, $V_{DD}$ = 50 Vdc, $V_{GS}$ = 5.0 Vdc,<br>$I_L$ = 2.1 Apk, L = 50 mH, $R_G$ = 25 Ω) | | $E_{AS}$ | 110 | mJ |
| Load Dump Voltage ($V_{GS}$ = 0 and 10 V, $R_I$ = 2 Ω, $R_L$ = 7 Ω, $t_d$ = 400 ms) | | $V_{LD}$ | 75 | V |
| Operating Junction Temperature Range | | $T_J$ | −40 to 150 | °C |
| Storage Temperature Range | | $T_{stg}$ | −55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.
2. Mounted onto 1” square pad size (700 sq/mm) FR4 PCB, 1 oz cu.

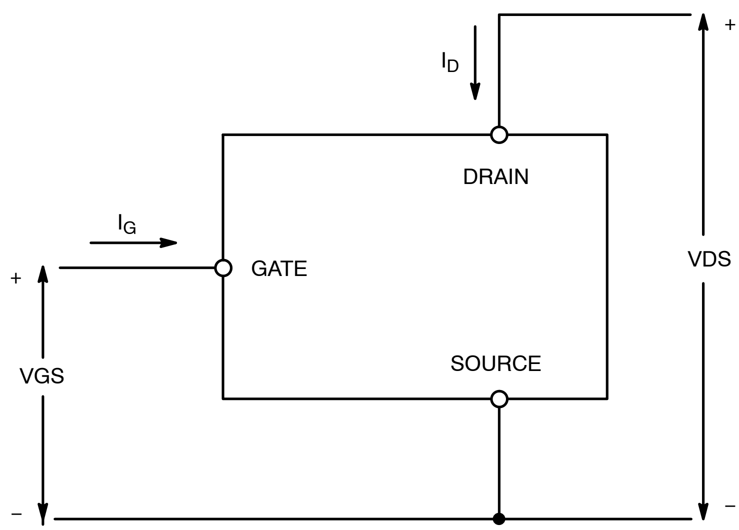



**Figure 1. Voltage and Current Convention**

**MOSFET ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Clamped Breakdown Voltage ($V_{GS}$ = 0 V, $I_D$ = 2 mA) | | $V_{(BR)DSS}$ | 60 | 65 | 70 | V |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 52 V, $V_{GS}$ = 0 V) | | $I_{DSS}$ | – | 22 | 100 | μA |
| Gate Input Current ($V_{GS}$ = 5.0 V, $V_{DS}$ = 0 V) | | $I_{GSS}$ | – | 30 | 100 | μA |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 150 μA)<br>Threshold Temperature Coefficient | | $V_{GS(th)}$ | 1.2<br>– | 1.66<br>4.0 | 2.0<br>– | V<br>−mV/°C |
| Static Drain−to−Source On−Resistance (Note 3) ($V_{GS}$ = 10 V, $I_D$ = 2.0 A, $T_J$ @ 25°C) | | $R_{DS(on)}$ | – | 185 | 210 | mΩ |
| Static Drain−to−Source On−Resistance (Note 3)<br>($V_{GS}$ = 5.0 V, $I_D$ = 2.0 A, $T_J$ @ 25°C)<br>($V_{GS}$ = 5.0 V, $I_D$ = 2.0 A, $T_J$ @ 150°C) | | $R_{DS(on)}$ | –<br>– | 210<br>445 | 240<br>520 | mΩ |
| Source−Drain Forward On Voltage ($I_S$ = 7.0 A, $V_{GS}$ = 0 V) | | $V_{SD}$ | – | 0.9 | 1.1 | V |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | |
| Turn−on Delay Time | $R_L$ = 6.6 Ω, $V_{in}$ = 0 to 10 V, $V_{DD}$ = 13.8 V, $I_D$ = 2.0 A, 10% $V_{in}$ to 10% $I_D$ | $td_{(on)}$ | – | 127 | – | ns |
| Turn−on Rise Time | $R_L$ = 6.6 Ω, $V_{in}$ = 0 to 10 V, $V_{DD}$ = 13.8 V, $I_D$ = 2.0 A, 10% $I_D$ to 90% $I_D$ | $t_{rise}$ | – | 486 | – | ns |
| Turn−off Delay Time | $R_L$ = 6.6 Ω, $V_{in}$ = 0 to 10 V, $V_{DD}$ = 13.8 V, $I_D$ = 2.0 A, 90% $V_{in}$ to 90% $I_D$ | $td_{(off)}$ | – | 1600 | – | ns |
| Turn−off Fall Time | $R_L$ = 6.6 Ω, $V_{in}$ = 0 to 10 V, $V_{DD}$ = 13.8 V, $I_D$ = 2.0 A, 90% $I_D$ to 10% $I_D$ | $t_{fall}$ | – | 692 | – | ns |
| Slew Rate ON | $R_L$ = 6.6 Ω, $V_{in}$ = 0 to 10 V, $V_{DD}$ = 13.8 V, $I_D$ = 2.0 A, 70% to 50% $V_{DD}$ | $dV_{DS}/dT_{on}$ | – | 79 | – | V/μs |
| Slew Rate OFF | $R_L$ = 6.6 Ω, $V_{in}$ = 0 to 10 V, $V_{DD}$ = 13.8 V, $I_D$ = 2.0 A, 50% to 70% $V_{DD}$ | $dV_{DS}/dT_{off}$ | – | 27 | – | V/μs |
| **SELF PROTECTION CHARACTERISTICS** (Note 4) | | | | | | |
| Current Limit | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 25°C (Notes 5, 7)<br>$V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 150°C (Notes 5, 6, 7)<br>$V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 25°C (Notes 5, 7) | $I_{LIM}$ | 5.0<br>3.5<br>6.5 | 7.0<br>4.5<br>8.5 | 9.5<br>6.0<br>10.5 | A |
| Temperature Limit (Turn−off) | $V_{GS}$ = 5.0 V (Notes 6, 7) | $T_{LIM(off)}$ | 150 | 180 | 200 | °C |
| Thermal Hysteresis | $V_{GS}$ = 5.0 V | $\Delta T_{LIM(on)}$ | – | 10 | – | °C |
| Temperature Limit (Turn−off) | $V_{GS}$ = 10 V (Notes 6, 7) | $T_{LIM(off)}$ | 150 | 180 | 200 | °C |
| Thermal Hysteresis | $V_{GS}$ = 10 V | $\Delta T_{LIM(on)}$ | – | 20 | – | °C |
| Input Current during Thermal Fault | $V_{DS}$ = 0 V, $V_{GS}$ = 5.0 V, $T_J$ = $T_J$ > $T_{(fault)}$ (Note 6)<br>$V_{DS}$ = 0 V, $V_{GS}$ = 10 V, $T_J$ = $T_J$ > $T_{(fault)}$ (Note 6) | $I_{g(fault)}$ | –<br>– | 5.9<br>12.3 | – | mA |
| **ESD ELECTRICAL CHARACTERISTICS** | | | | | | |
| Electro−Static Discharge Capability<br>Human Body Model (HBM)<br>Machine Model (MM) | | ESD | 6000<br>500 | –<br>– | –<br>– | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Current limit measured at 380 μs after gate pulse.
6. Not subject to production test.
7. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

## TYPICAL PERFORMANCE CURVES

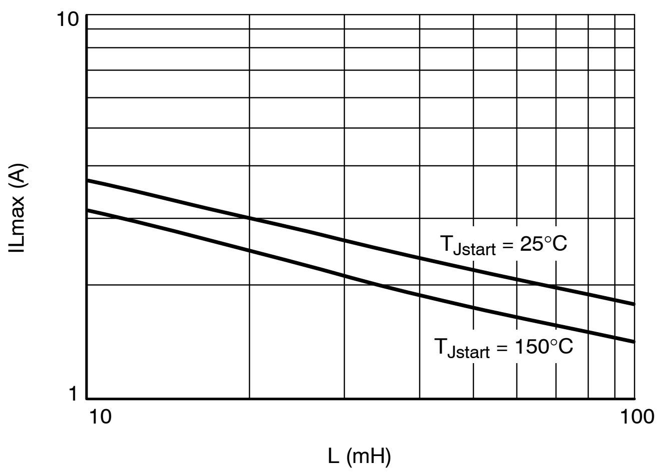



**Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance**

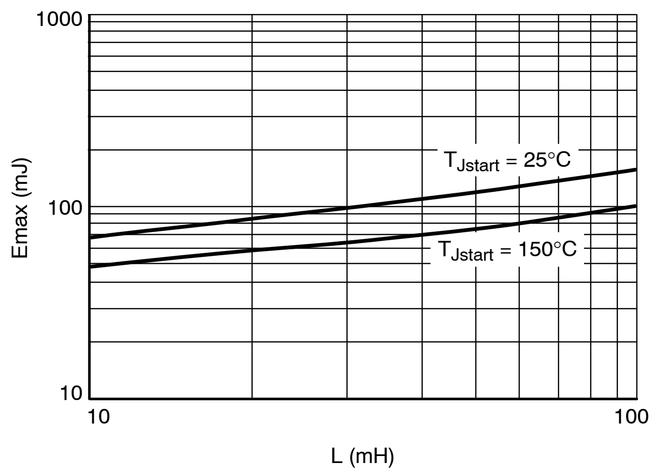



**Figure 3. Single−Pulse Maximum Switching Energy vs. Load Inductance**

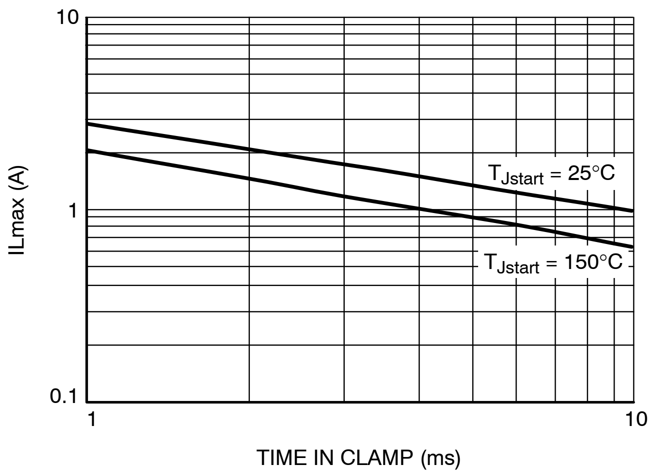



**Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp**

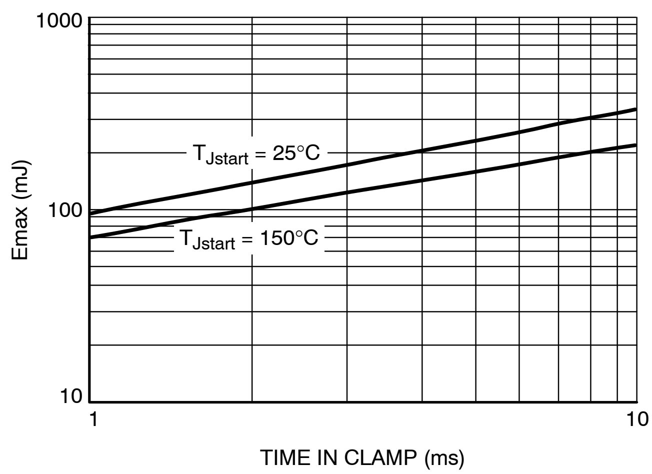



**Figure 5. Single−Pulse Maximum Inductive Switching Energy vs. Time in Clamp**

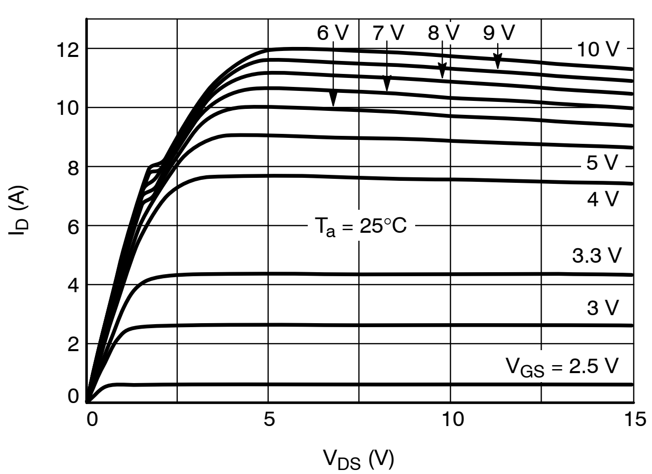



**Figure 6. On−state Output Characteristics**

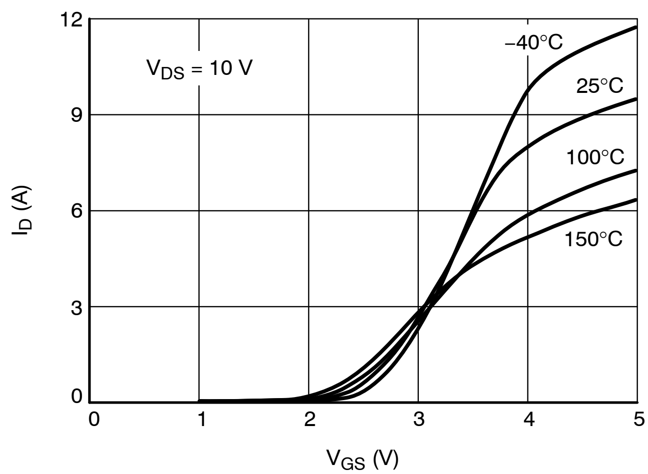



**Figure 7. Transfer Characteristics**

## TYPICAL PERFORMANCE CURVES

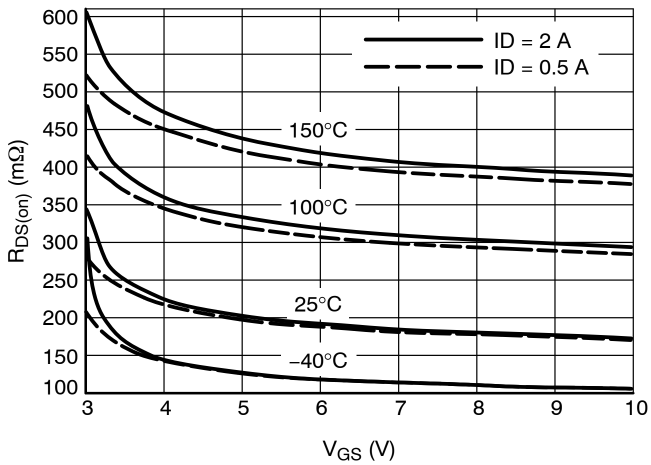



**Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage**

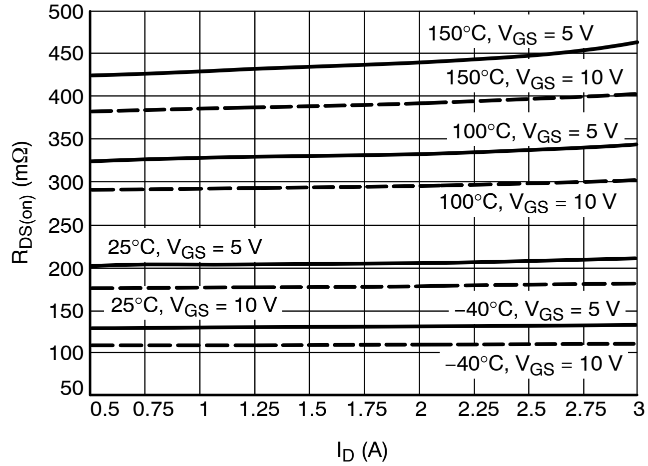



**Figure 9. $R_{DS(on)}$ vs. Drain Current**

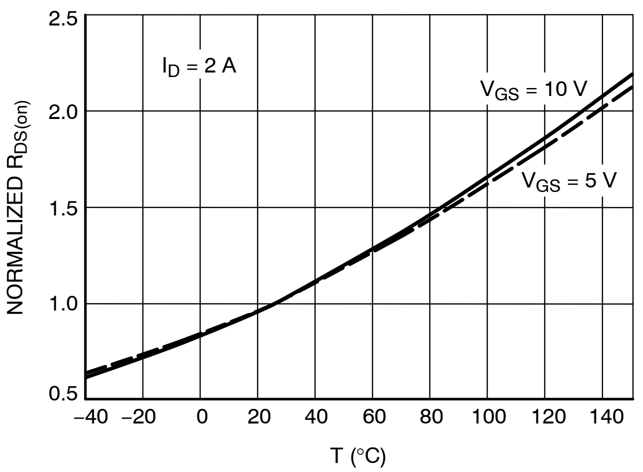



**Figure 10. Normalized $R_{DS(on)}$ vs. Temperature**

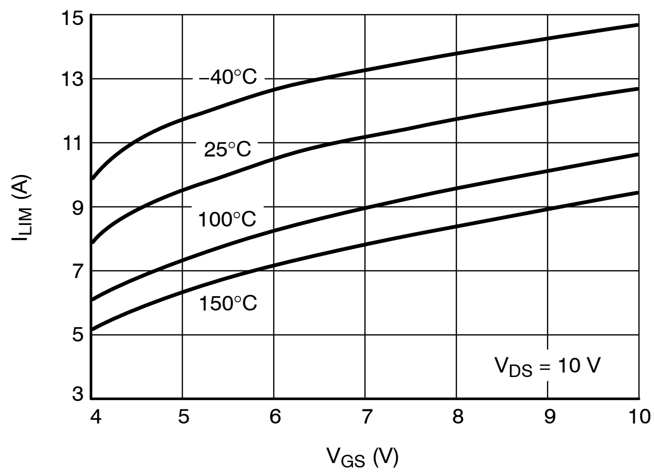



**Figure 11. Current Limit vs. Gate−Source Voltage**

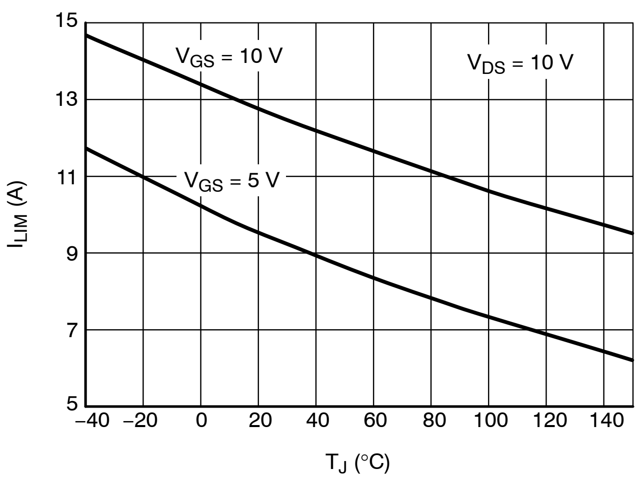



**Figure 12. Current Limit vs. Junction Temperature**

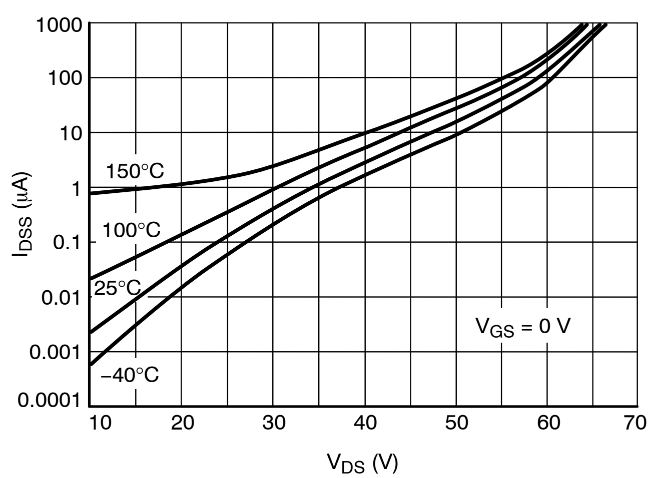



**Figure 13. Drain−to−Source Leakage Current**

## TYPICAL PERFORMANCE CURVES

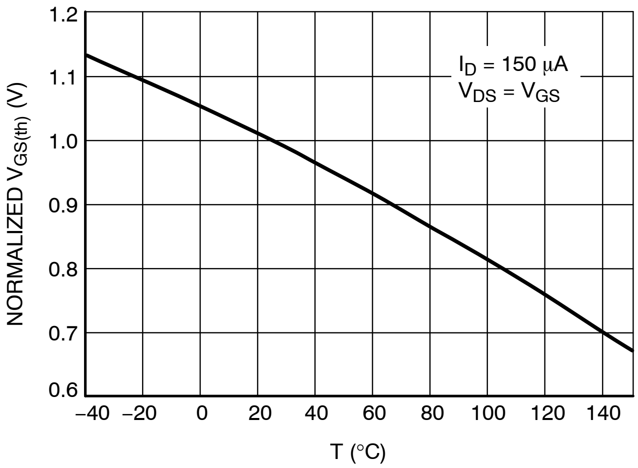



**Figure 14. Normalized Threshold Voltage vs. Temperature**

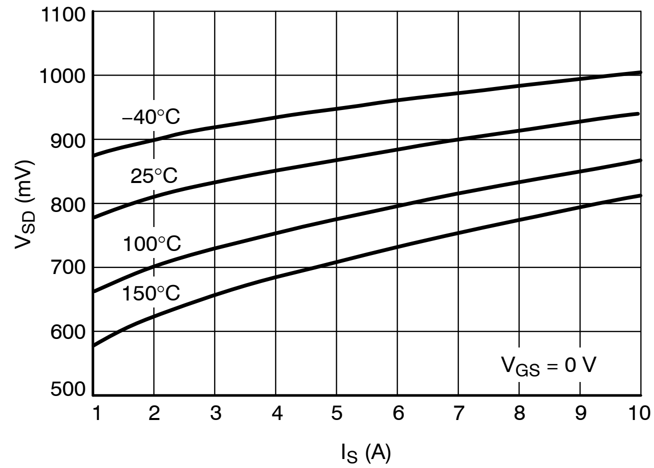



**Figure 15. Source−Drain Diode Forward Characteristics**

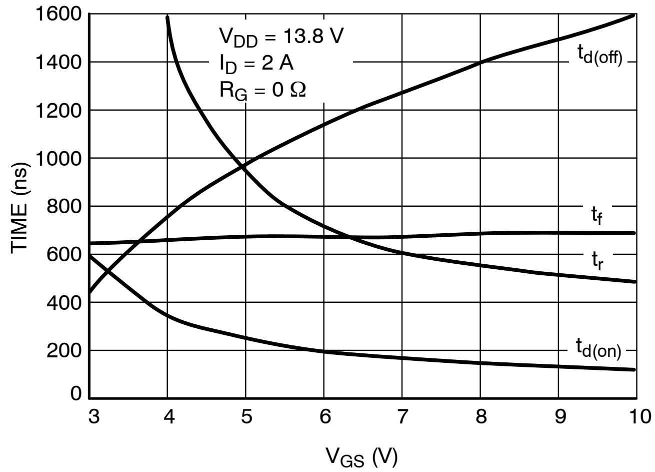



**Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage**

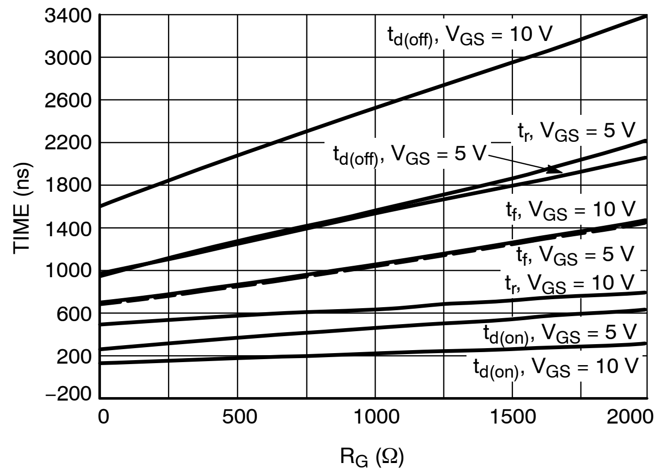



**Figure 17. Resistive Load Switching Time vs. Gate Resistance**

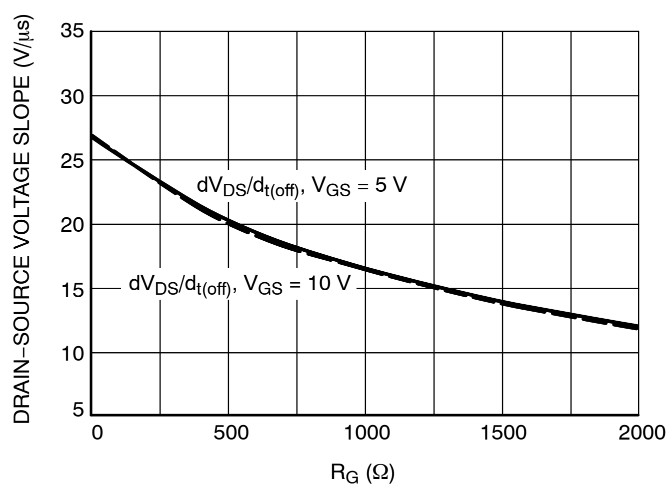



**Figure 18. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance**

## TYPICAL PERFORMANCE CURVES

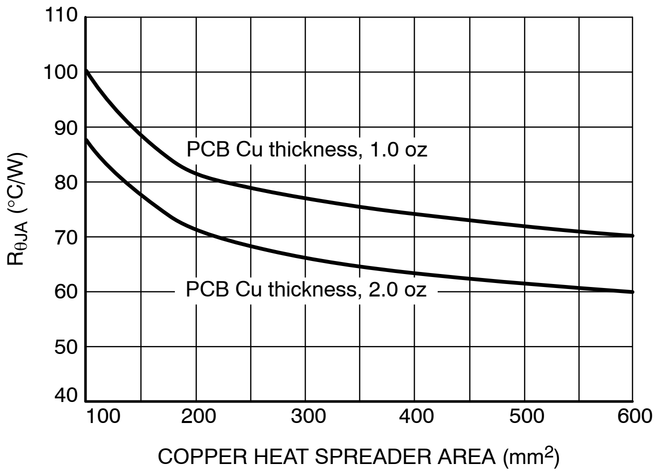



**Figure 19. $R_{\theta JA}$ vs. Copper Area – SOT−223**

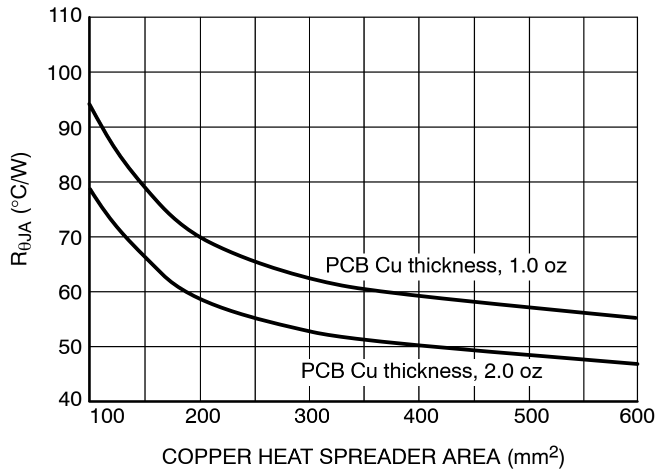



**Figure 20. $R_{\theta JA}$ vs. Copper Area – DPAK**

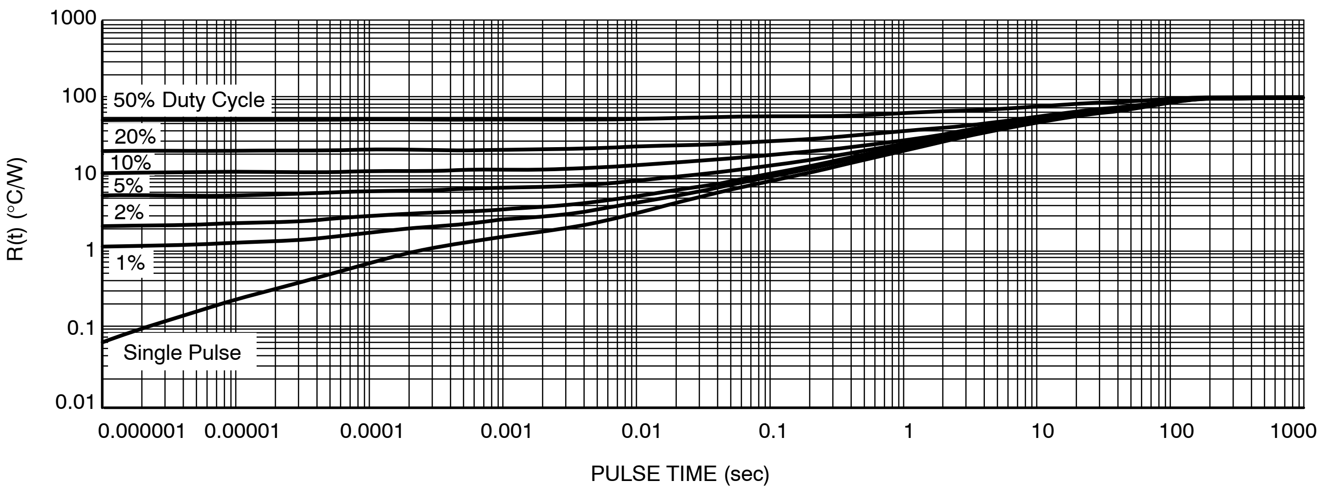



**Figure 21. Transient Thermal Resistance – SOT−223 Version**

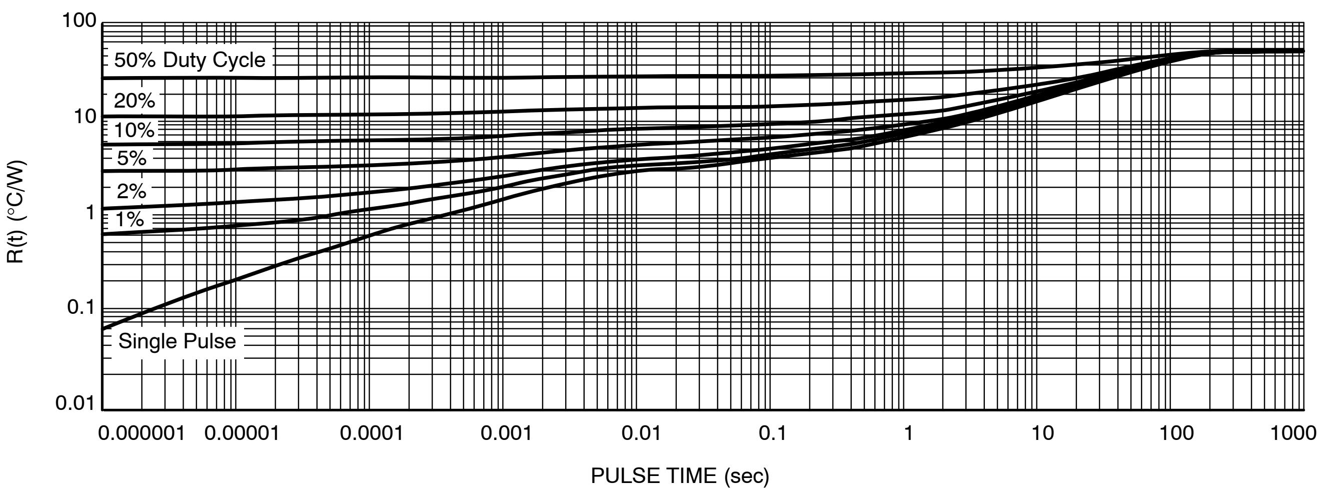



**Figure 22. Transient Thermal Resistance – DPAK Version**

## TEST CIRCUITS AND WAVEFORMS

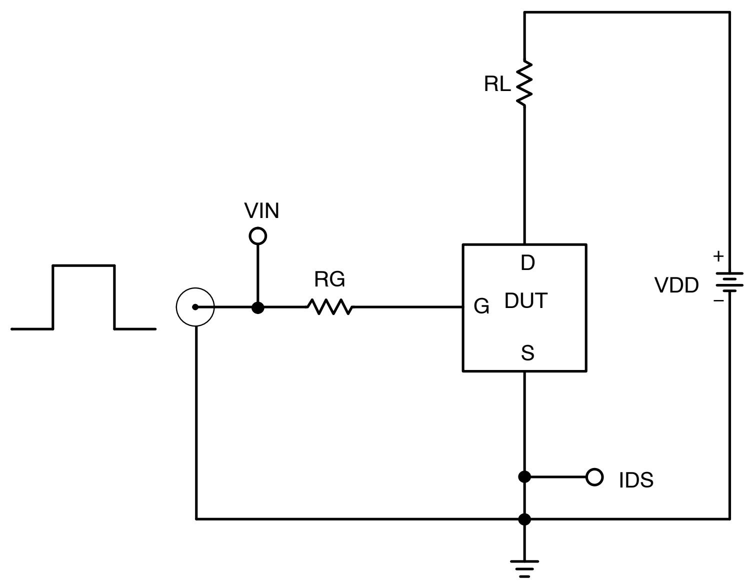



**Figure 23. Resistive Load Switching Test Circuit**

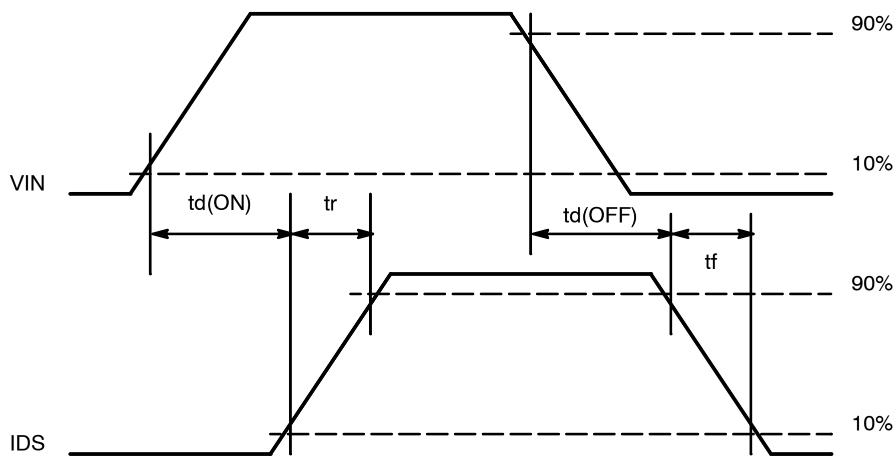



**Figure 24. Resistive Load Switching Waveforms**

## TEST CIRCUITS AND WAVEFORMS

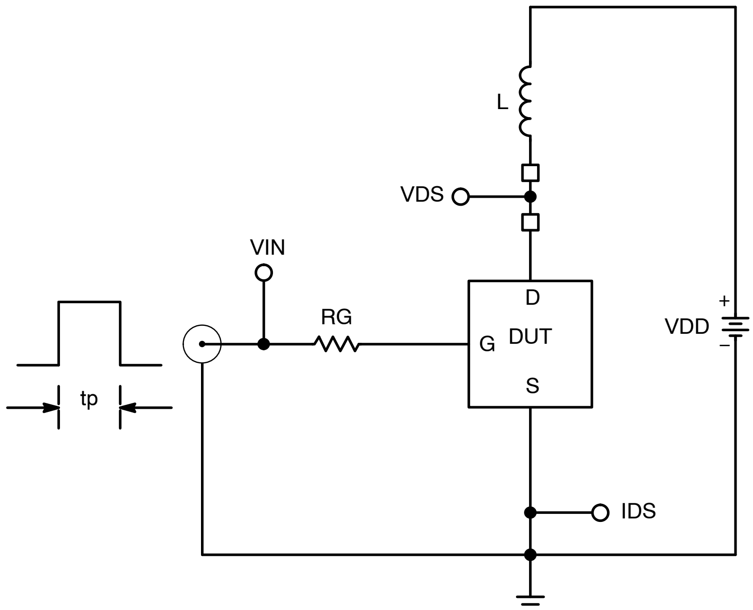



Figure 25. Inductive Load Switching Test Circuit

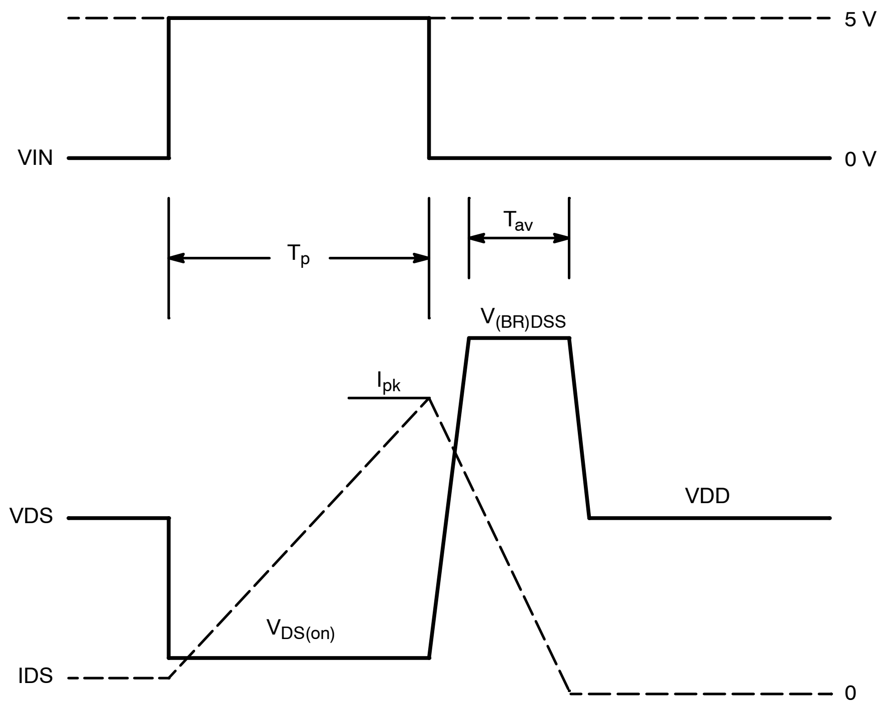



Figure 26. Inductive Load Switching Waveforms

## ORDERING INFORMATION

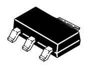
| Device | Package | Shipping† |
|---|---|---|
| NCV8406ASTT1G | SOT−223 (Pb−Free) | 1000 / Tape & Reel |
| NCV8406ASTT3G | SOT−223 (Pb−Free) | 4000 / Tape & Reel |
| NCV8406BDTRKG | DPAK (Pb−Free) | 2500 / Tape & Reel |

**DISCONTINUED** (Note 8)

| | | |
|---|---|---|
| NCV8406ADTRKG | DPAK (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

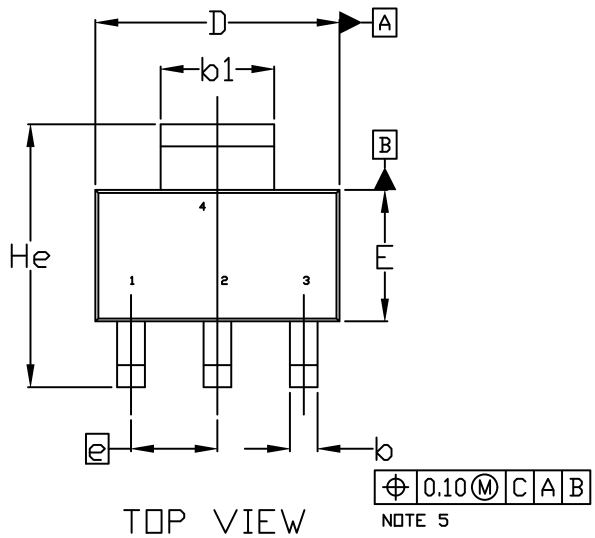
8. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



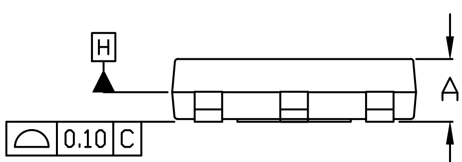
SCALE 1:1

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

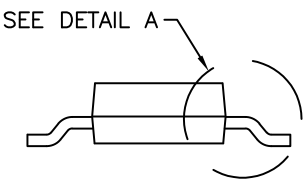
DATE 02 OCT 2018



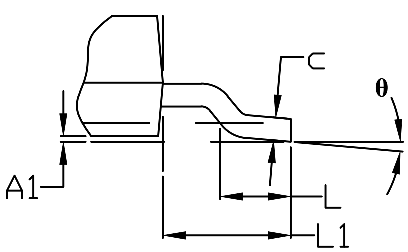

TOP VIEW




SIDE VIEW



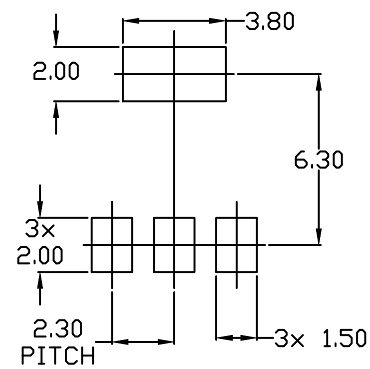

FRONT VIEW




DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |




RECOMMENDED MOUNTING FOOTPRINT

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42680B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **SOT−223 (TO−261)** | **PAGE 1 OF 2** |

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

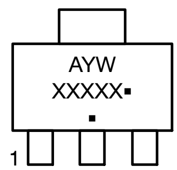
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAM*




A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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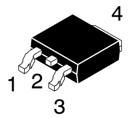
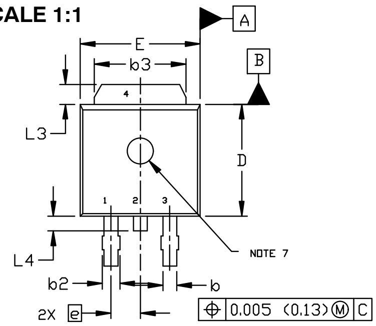
| **DESCRIPTION:** | **SOT−223 (TO−261)** | **PAGE 2 OF 2** |



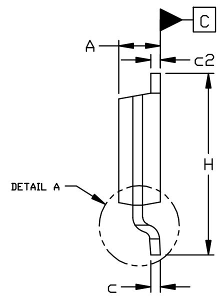

**SCALE 1:1**

# DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023




TOP VIEW

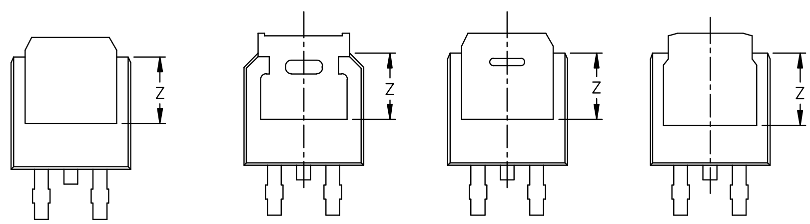



SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

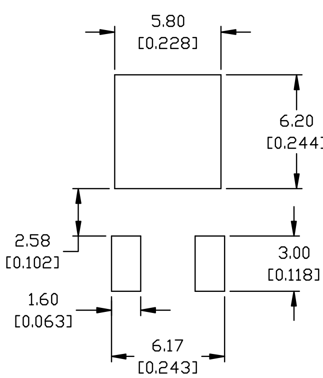
| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | | 2.90 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | ---- | 0.040 | --- | 1.01 |
| Z | 0.155 | ---- | 3.93 | --- |




BOTTOM VIEW

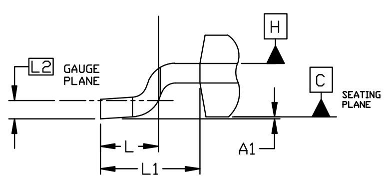
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



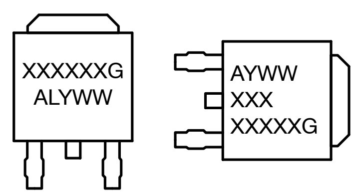

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.




DETAIL A
ROTATED 90° CW

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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|---|---|---|
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT:** www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

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