ND3260

Print Circuit Board Design Guidelines

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The information contained herein is subjected to change without notice.

Contents:

0. Revision History

Date of Revision	Revision	Description
May/12/2003	*DG1.0*	*Initial Design guidelines*
May/15/2003	*DG1.1*	*Updated xD-Picture Card circuit.*

1. Introduction

This document provides guideline for the design of ND3260 print circuit boards. The material includes demo board placement, schematics, layout guidelines, general USB 2.0 considerations, BOM, Flash ROM supporting list. For more detail please refer to ND3260 the Multi-Format Flash Memory Card Reader with USB2.0 HS Interface Specification.

2. PCB Overview

2.1 PCB Placement

The following figure is the overview of ND3260 DEMO BOARD ver1.0.

Figure 1 is the top side of the demo board and Figure 2 is the bottom side of the demo board. Most of the components are placing on the top side of the PCB. Only SM and SD connector are placing on the solder side.

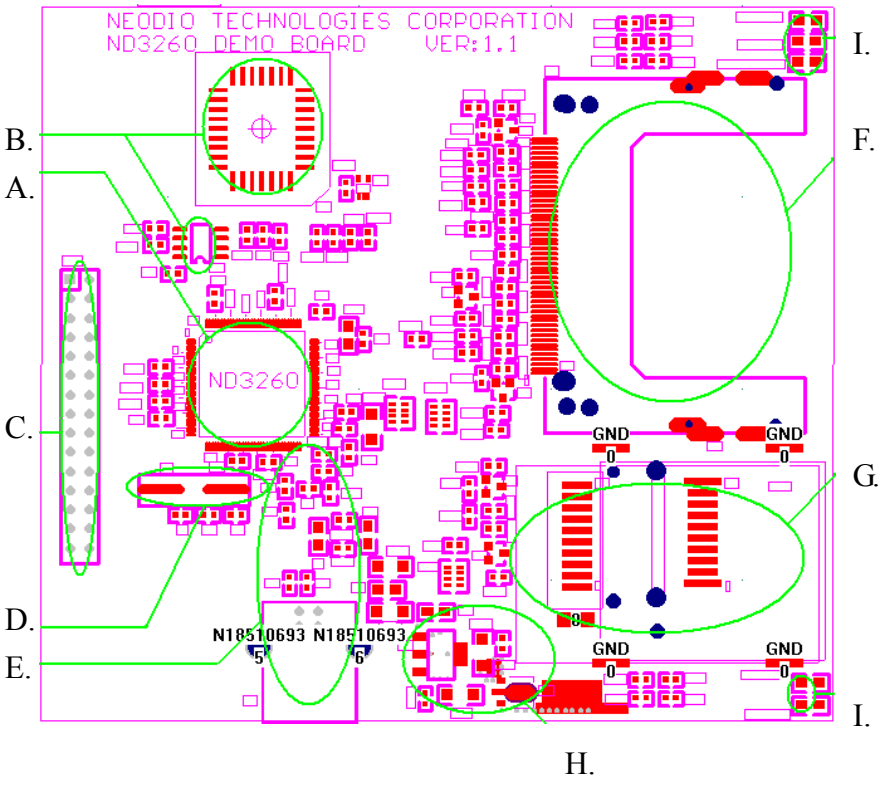


Figure 1 Top Side View

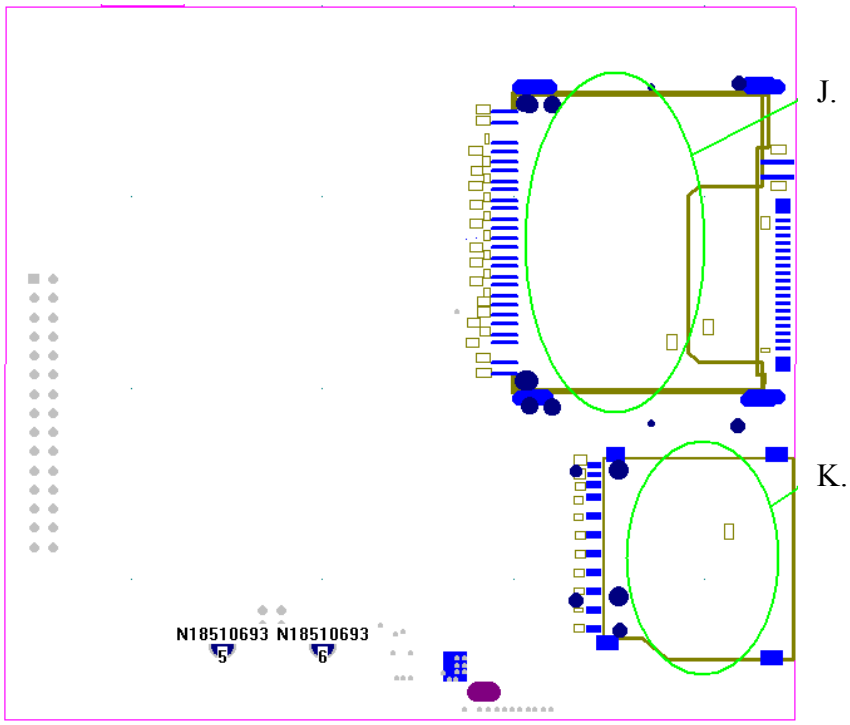


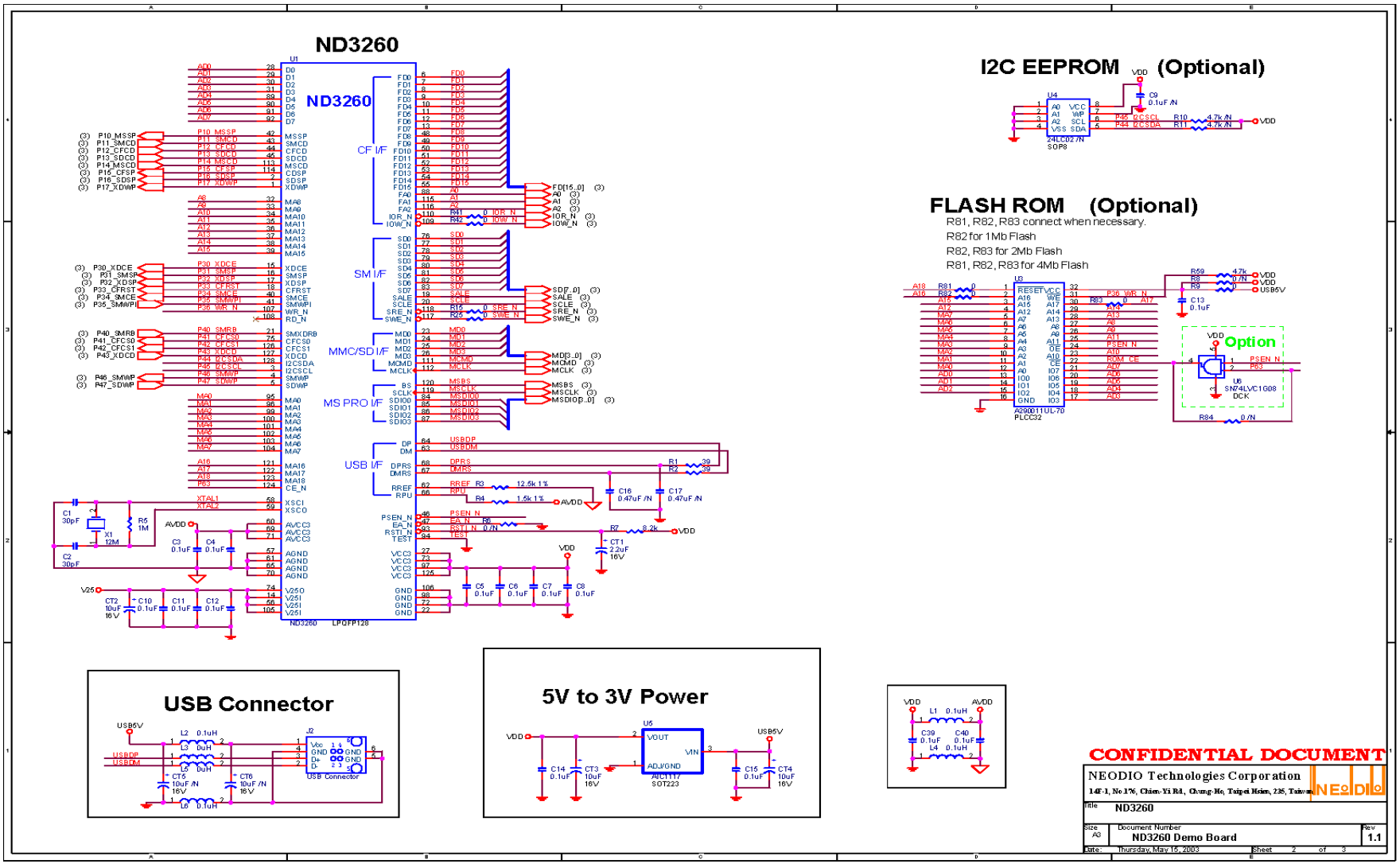
Figure 2 Bottom Side View

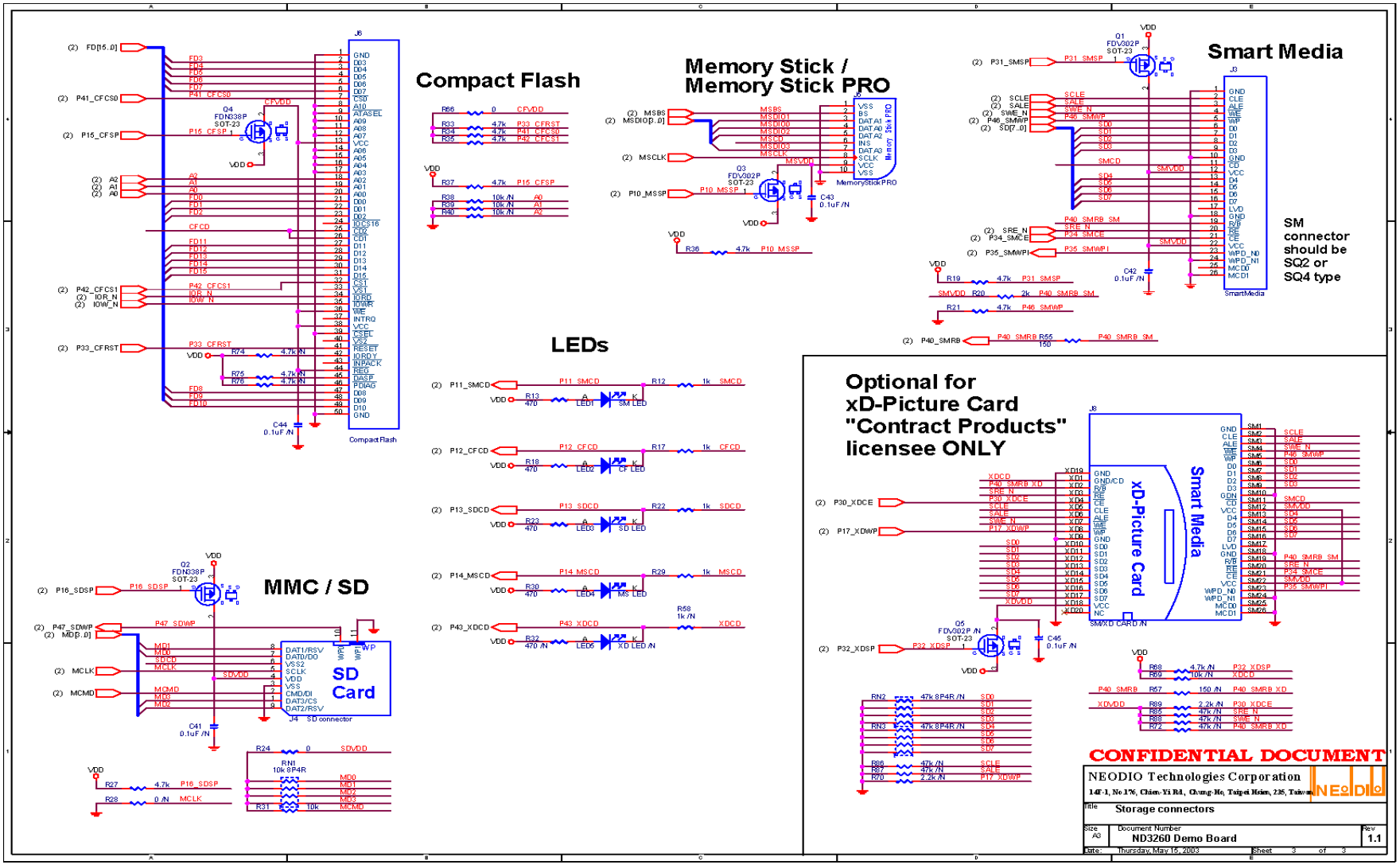
2.2 PCB Detail

A. ND3260 USB2.0 Card Reader Controller.
B. Flash memory and I2C EEPROM.
C. Debug Port. (For Neodio debug only).
D. Crystal.
E. USB signals and connector.
F. CF Card Slot type I/type II.
G. MS card Slot.
H. Power regulator.
I. LEDs.
J. SM/xD Card Slot.
K. SD Card Slot.

3. Schematic Circuit

3.1 Schematic





3.2 Schematic Detail

The value of all component parts on the schematic with /N means NO LOAD and reserved the location.

Schematic Page 1

1. U1 is ND3260 Card Reader controller. The package is LQFP128.
2. X1 is a Crystal. The crystal is 12MHz.
3. J2 is USB connector. The related of filter circuit should be placed as close connector as possible. USBDP and USBDM are very critical and should be careful on layout. For detail, please see following Layout Guidelines.
4. U3 and U4 are I2CEEPROM and Flash ROM. To have the ISP function, use Flash ROM. To cost down the reader solution, use I2C EEPROM.

Schematic Page 2

1. J8 is a combination connector for SmartMedia Card or xD-Picture Card. The related circuits are for xD-Picture Card license ONLY.
2. LED1 to LED4 are 4 LEDs for 4 slots. If only 1 LED is needed, reserve LED2 and related circuits.
3. LED5 and related circuits are also for xD-Picture Card license ONLY.

4. Layout Guidelines

For ND3260 Card Reader's PCB layout, the most important signals are USB2.0 differential signals. For more detail please refer to the Universal Serial BUS Specification Revision 2.0.

4.1 USB Layout Guidelines

4.1.1 USB Placement and Routing

1. Place the USB 2.0 device and connector on the un-routed board first.
2. With minimum trace lengths, as equal as possible (D+, D-), route high-speed clock and USB 2.0. Differential signal pair first. Keep maximum distance between high-speed signals to USB 2.0 differential signal pair.
3. Route the USB 2.0 differential signal pair on the component side, which is adjacent to the ground plane layer. Vias to different signal trace layers or

routing to close to breaks in the ground plane will adversely affect the differential trace impedance.

4. Route USB 2.0 differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change.
5. If it's necessary to turn 90°, it' better to use two 45° turn or an arc, instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.
6. Please don't route USB 2.0 differential signal pair trace under crystal, oscillator, clock-synthesizers, magnetic devices or ICs. It will cause interference.
7. Stubs on USB 2.0 differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200mils.
8. Route USB 2.0 differential signal pair traces over continuous ground and power planes. Avoid crossing anti-etch areas or any break in the underlying planes.
9. Avoid routing the USB 2.0 differential signal pair near the edge of the PCB or power planes.
10. Keep parallelism between D+ and D- with the trace spacing, which achieves 90Ω differential impedance.
11. Provide adequate trace width to handle the current requirements of power control devices.

4.1.2 Differential Signal Pair Impedance Control and Connect

The USB 2.0 D+/D- differential pair, which can operate at a rate of 480MHz (High-Speed), are some of the most critical signals on a USB 2.0 PCB. Its implementation on the PCB requires special considerations. The impedance of the PCB differential trace pair is the ratio of voltage to current, of an electrical signal moving down along the traces. The inductive and capacitive reactance, resistance, and conductance of a PCB differential pair will determine the impedance of the trace pair at any point along the PCB track. The value of differential impedance will be a function of the physical dimensions of the trace, as detail below.

For a USB 2.0 differential pair, an impedance of 90Ω is optimal.

4.1.3 USB2.0 Trace Spacing

The physical construction of differential PCB traces as Figure 3, determines the differential impedance. The primary physical characteristics are summarized as following.

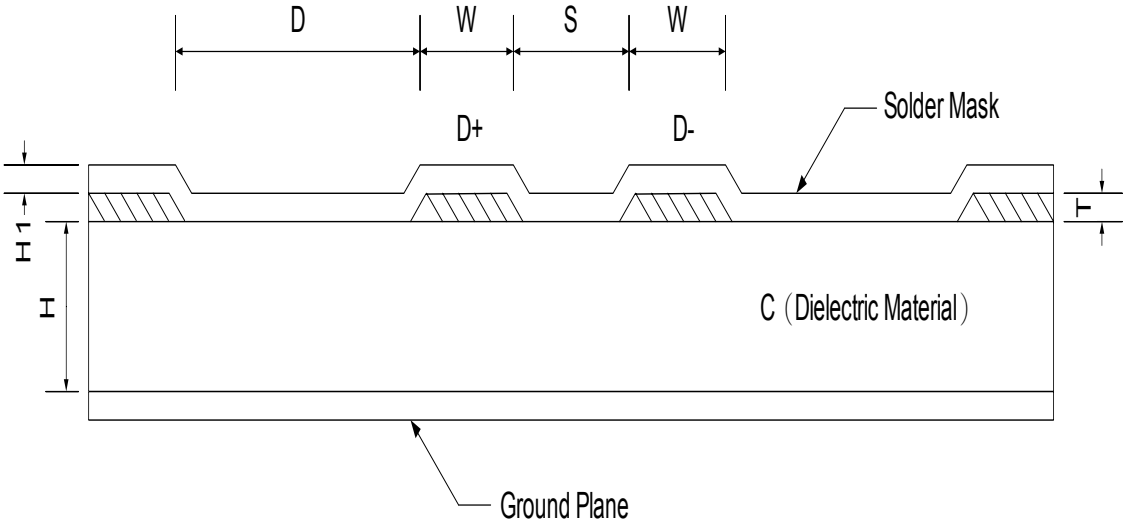


Figure 3 PCB stack up configuration (partial)

1. W = Width of the trace
2. S = Separation from D+ to D-
3. H = Dielectric thickness, distance of trace from the ground plane.
4. T = Thickness of the trace
5. D = Ground Separation
6. H1 = Solder mask thickness
7. Er = Dielectric constant (depend on C, example: FR4 Er = 4.5)

4.2 Power and Ground Planes Layout Guideline

4.2.1 PCB Layer Stack-up

In USB 2.0 applications, a PCB with a minimum of 4 layers is required. Because it needs to control the impedance of the USB 2.0 differential signal pair and supply a clear power and ground. The 4 layers are typically configured as described as below.

Layer	Description	Signification Features
1.	Component Side (Top)	Contains differential signal pair and other signal routing and primary surface-mounted components.
2.	Ground Layer	Ground plane (include AGND and DGND). Also, It is reference layer for differential

		signal pair.
3.	Power Layer	Power plane (include AVCC and DVCC).
4.	Solder Side (Bottom)	Contains signal routing and secondary surface-mounted components.

The PCB designer should use an impedance calculator to determine the differential trace impedance of USB2.0 differential signal pair. Note that the calculations to determine the differential impedance are somewhat different from those used to calculate the impedance of a signal trance. The appropriate software should be selected.

W = 7.5 mils
S = 8 mils
D ≥ 20 mils
H ≈ 4.5 mils (prepreg)
T = 1 ounce copper
Er ≈ 4.5 (FR4 material)
Board thickness ≈ 63 mils (1.6 mm)

4.2.2 Summary Key Point for Power and Ground

1. Route high-speed signals above a continuous, unbroken ground plane
2. Provide ample power and ground planes
3. Ensure the power supply is rated for the load
4. Filter and shield DC-DC converters, oscillators, etc
5. Avoid breaks in the ground plane, especially in areas where it is shielding high-frequency signals
6. Filter the analog power circuits. The filters may be removed if performance testing proves they are unnecessary

4.3 Crystal Layout Guidelines

The Crystal is 12MHz. Therefore, place the crystal nearby ND3260 pin58, 59 and keep the clock traces as short as possible. Route the clock signals above a continuous, unbroken ground plane.

5. Bill of Material

The following table is the engineer BOM for your reference. This BOM do NOT include the component for xD-Picture Card.

Item	Quantity	Reference	Part
1	1	CT1	2.2uF
2	3	CT2,CT3,CT4	10uF
3	2	C1,C2	30pF
4	14	C3,C4,C5,C6,C7,C8,C10, C11,C12,C13,C14,C15,C39, C40	0.1uF
5	1	J2	USB Connector
6	1	J3	SmartMedia
7	1	J4	SD connector
8	1	J5	MemoryStickPRO
9	1	J6	CompactFlash
10	1	LED1	SM LED
11	1	LED2	CF LED
12	1	LED3	SD LED
13	1	LED4	MS LED
14	4	L1,L2,L4,L6	0.1uH
15	2	L5,L3	0uH
16	2	Q1,Q3	FDV302P
17	2	Q2,Q4	FDN338P
18	1	RN1	10k 8P4R
19	2	R1,R2	39
20	1	R3	1.25k 1%
21	1	R4	1.5k 1%
22	1	R5	1M
23	1	R7	8.2k
24	10	R9,R15,R24,R25,R41,R42, R66,R81,R82,R83	0
25	4	R12,R17,R22,R29	1k
26	4	R13,R18,R23,R30	470
27	9	R19,R21,R27,R33,R34,R35, R36,R37,R59	4.7k
28	1	R20	2k
29	1	R31	10k
30	1	R55	150
31	1	U1	ND3260
32	1	U3	A290011UL-70
33	1	U5	AIC1117
34	1	U6	SN74LVC1G08
35	1	X1	12M

6. Flash ROM Supporting List

To support In Application Programming through USB port, the card reader should build an external Flash ROM. The Flash ROM should be 8 bit COMS flash memory. For the Flash ROM, please refer to following table.

Brand	Size	Component
AMD	2MB	AM29F002NBB-55JC
AMD	4MB	AM29F040B-70JC
AMIC	2MB	A290021UL-70
AMIC	1MB	A290011TL-70
EON	2MB	EN29F002NT
MXIC	1MB	MX29F001BQC-70
MXIC	4MB	MX29F040-90
SST	2MB	SST39VF020-90
SST	1MB	SST39SF010A-70
SST	2MB	SST39SF020A-70
SST	512KB	SST39SF512-70
SST	4MB	SST39SF020A-70
Winbond	512KB	W39L512P-90
Winbond	2MB	W49F002UP70B
ATMEL	512KB	AT49BV512-90JC
ATMLE	2MB	AT49F002NT-70JC
ATMLE	4MB	AT49F040-90JC
PMC	512KB	Pm39LV512R-90JC