ND7060

A Multi-Format Flash Card Reader/Writer Controller for Embedded Applications Specification

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Overview

ND7060 is a highly integrated, Smart Media Card/Memory Stick Card/Memory Stick PRO Card/Memory Stick Duo Card/Compact Flash Card/Security Digital Card/Mini Secure Digital card/MultiMedia Card/RS-MultiMedia Card/xD-Picture Card, compatible reader/writer controller IC with PCMCIA/IDE interface. It integrates an enhanced 8 bit MCU, an internal program/data memory, and numerous of peripherals into single monolithic SOC. ND7060 can provide up to 20 Mbps access speed on Flash memory cards. In Application Programming (IAP), which supports software upgrades through either the PCMCIA /IDE bus or flash memory cards, makes it possible for the customers to update the flash reader/writers in field without any technical assistance. With a 128-pin LQFP package and very few external passive components for implementation, ND7060 is the most suitable solution for embedded flash card reader/writer products.

Feature

Turbo 8052 central process unit

- Standard 8052 instruction compatible core
- 4-cycle instruction with 2.5X performance improvement
- Internal maximum 32K x 8 code memory
- Two sets of data pointers (DPTR) to speed up the transfer of large amount data
- 0ne 16-bit timers/counters
- 12 vectors interrupt structure with 2 priority level
- Built-in watchdog timer
- Low EMI (ALE is inhibited automatically when executing internal code)

PCMCIA-ATA / IDE interface

- Conform to PC-ATA Card and IDE-ATA/ATAPI specification
- 3.3 V single power supply operation
- Read/Write unit is 512 bytes (sector) sequential access
- Support 3 variations of mode access
  --- PC Card Memory mode
  --- PC Card I/O mode
  --- True IDE mode
- Support PIO0~PIO3 mode in Host data transfer.
- Support Multi word DMA (Mode 1) in ATA/IDE mode

Smart Media/xD-Picture Card interface

- Fully compatible with Smart Media™ Electrical Specification Version 1.4, Physical Format Specification Version 1.3, Logical Format Specification Version 1.3 and xD-Picture Technical Specification Version 1.1
- Support Error Correction Code (ECC) function
- Support interface for Toshiba/Samsung NAND type flash memory
- Max. Support capacity: SM: 512MB & xD: 2GB

Memory Stick interface

- Fully compatible with the Memory Stick Format Specification Version 1.4 and Memory Stick PRO Format Specification Version 1.00
- Support serial/parallel data bus (4 bit) interface
- Auto data CRC generating & checking
- Max. Support capacity: MS: 128MB & MS-PRO: 32GB
- Maximum clock rate up at 20 MHz

MultiMedia card/Secure Digital memory card interface

- Fully compatible with MultiMedia Card (MMC) system specification version 3.31 and Secure Digital (SD) memory card specification physical layer version 1.01
- Support serial/parallel data (4 bit) bus interface
- Auto data CRC generating & checking
- Max. Support capacity: MMC: 2199GB & SD: 2199GB

Compact Flash interface

- Fully compatible with Compact Flash specification version 2.0
- Support standard IDE/ATA host interface (compatible with most HDD/CDROM/DVD drives)
- Programmable transfer mode that can set varied access speed
- Full task file register set support
- Max. Support capacity: 2199GB

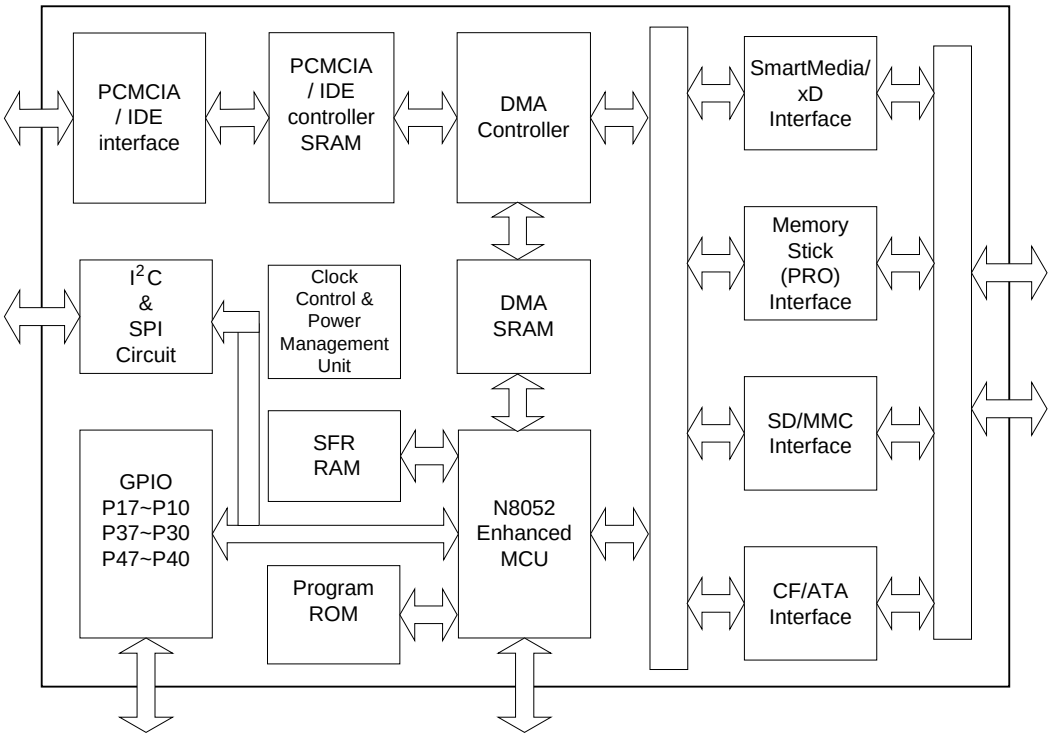
DMA Controller

- Neodio's proprietary high-performance SOC bus architecture
- Support 4 independent DMA channels
- Address Increment or decrement
- Independent polarity control for REQ and ACK signals
- Support 3 modes of transfer (Single, Block and Demand mode)
- 1024 X16 bit internal SRAM
- SRAM is accessible as the standard 8052 SRAM

Other features

- External NOR flash support for IAP.
- Internal 32KB Mask ROM for firmware storage when IAP is not required.
- Software configurable I^2C bus with optional external serial EEPROM for customization with Mask ROM configuration
- Provide LED indicator while flash card is busy, and power ready
- Only one 3.3V operating voltage required
- 128-pin LQFP package

Block Diagram



Pin Descriptions

Pin No.	Name	I/O	Descriptions
Pin66, Pin65	HCE1_N, HCE2_N (PC Card Memory mode)	I	1.Host mode: PCMCIA HCE1_N and HCE2_N are low active card select signals. Even/Word/Odd byte mode is defined by combination of HCE1_N, HCE2_N and HA0.
	HCE1_N, HCE2_N (PC Card I/O mode)	I	These signals the same as PC Card Memory mode
	HCS0_N, HCS1_N (True IDE mode)	I	CS1_N is used for select the Alternate Status Register and the Device Control Register while CS0_N is the chip select for the other task file registers.
	HCS0_N, HCS1_N	I	2.Host mode: IDE CS1_N is used for select the Alternate Status Register and the Device Control Register while CS0_N is the chip select for the other task file registers.

Pin59	HCSEL_N (PC Card Memory mode)	I	1.Host mode: PCMCIA This signal is not used.
	HCSEL_N (PC Card I/O mode)	I	This signal is not used.
	HCSEL_N (True IDE mode)	I	This signal is used to configure this device as a Master or a Slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a Master. When the pin is open or pull up to VCC, this device is configured as a Slave.
	HCSEL_N	I	2.Host mode: IDE The device is configured as either Device 0 or Device 1 depending upon the value of HCSEL: If HCSEL is 0 then the device address is 0 If HCSEL is 1 then the device address is 1
Pin70~ Pin85	HDD0~HDD15	I/O	Data bus is HD15 to HD0. HD0 is the LSB of the even byte of the word. HD8 is the LSB of the odd byte of the word.
Pin63	BVD2 (PC Card Memory mode)	O	1.Host mode: PCMCIA BVD2 (Battery Voltage Detect2) outputs the battery voltage status in the card. This output line is constantly driven to a high state if a battery is not required for this product.
	SPKR_N (PC Card I/O mode)	O	SPKR_N (Audio Digital Waveform) outputs speaker signals. This output line is constantly driven to a high state if this product does not support the audio function.
	HDASP_N (True IDE mode)	I/O	HDASP_N is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
	HDASP_N	I/O	2.Host mode: IDE HDASP_N is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.

Pin67~Pin69	HA0~HA2	I	Host side address bus bit 2 ~ bit 0
Pin86	HRDY/BSY_N (PC Card Memory mode)	O	1.Host mode: PCMCIA The signal is RDY/-BSY pin. RDY/BSY_N pin turns low level during the card internal initialization operation at VCC applied or reset applied, so next access to the card should be after the signal turned high level.
	HIREQ _N (PC Card I/O mode)	O	This signal is active low IREQ_N pin. The signal of low level indicates that the card is requesting software service to host, This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
	HINTRQ (True IDE mode)	O	This signal is the active high Interrupt Request to the host.
	HINTRQ	O	2.Host mode: IDE This signal is the active high Interrupt Request to the host
Pin60	HIOR_N (PC Card Memory mode)	I	1.Host mode: PCMCIA This signal is not used.
	HIOR_N (PC Card I/O mode)	I	HIOR_N is used for control of read data in I/O task file area. This card does not respond to HIOR_N until I/O card interface setting up .
	HIOR_N (True IDE mode)	I	HIOR_N is used for control of read data in I/O task file area. This card does not respond to HIOR_N until True DE interface setting up.
	HIOR_N	I	2.Host mode: IDE HIOR_N is active low by the host to read device registers or the data port.
Pin61	HIOW_N (PC Card Memory mode)	I	1.Host mode: PCMCIA This signal is not used.

	HIOW_N (PC Card I/O mode)	I	HIOW_N is used for control of data write in I/O task file area. This card does not respond to HIOW_N until I/O card interface setting up.
	HIOW_N (True IDE mode)	I	HIOW_N is used for control of data write in I/O task file area. This card does not respond to HIOW_N until True IDE interface setting up.
	HIOW_N	I	2.Host mode: IDE HIOW_N is active low by the host to write device registers or the data port.
Pin87	HWAIT_N (PC Card Memory mode)	O	1.Host mode: PCMCIA This signal is to signal the host to delay completion of a memory cycle in progress.
	HWAIT_N (PC Card I/O mode)	O	This signal is to signal the host to delay completion of an I/O cycle in progress.
	HIORDY_N (True IDE mode)	O	This signal may be used as IORDY.
	HIORDY_N	O	2.Host mode: IDE This signal may be used as IORDY.
Pin64	BVD1 (PC Card Memory mode)	O	1.Host mode: PCMCIA BVD1 outputs the battery voltage status in the card. This output line is constantly driven to a high state if a battery is not required for this product.
	STSCHG_N (PC Card I/O mode)	O	STSCHG_N is used for changing the status of Configuration and status register in attribute area. Its use is controlled by the Card Configuration and Status register.
	HPDIAG (True IDE mode)	I/O	HPDIAG is the Pass Diagnostic signal in Master/Slave handshake protocol. This line shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics.

Pin91	HREG_N (PC Card Memory mode)	I	1.Host mode: PCMCIA HREG_N is used during memory cycles to distinguish between task file and attribute memory accesses. High for task file, Low for attribute memory is accessed.
	HREG_N (PC Card I/O mode)	I	HREG_N is constantly low when task file or attribute memory is accessed.
	HDMACK_N (True IDE mode)	I	This input signal is used in IDE Multi-Word DMA acknowledge.
	HDMACK_N	I	2.Host mode: IDE The signal is used in IDE Multi-Word DMA acknowledge.
Pin92	HINPACK_N (PC Card Memory mode)	O	1.Host mode: PCMCIA This signal is not used and should not be connected at the host.
	HINPACK_N (PC Card I/O mode)	O	This signal is asserted low by this card when the card is selected and responding to an I/O read cycle at the address that is on the address bus during HIOR_N is low. This signal is used for the input data buffer control.
	HDMARQ (True IDE mode)	O	This signal is used in IDE Multi-Word DMA request signal.
	HDMARQ	O	2.Host mode: IDE This signal is used in IDE Multi-Word DMA request signal.
Pin94	HOE_N (PC Card Memory mode)	I	1.Host mode: PCMCIA HOE_N is used for the control of reading register's data in attribute area or task file area.
	HOE_N (PC Card I/O mode)	I	HOE_N is used for the control of reading register's data in attribute area.
	HATASEL (True IDE mode)	I	To enable True IDE mode this input should be ground by the host.

	HATASEL	I	2.Host mode: IDE To enable True IDE mode this input should be ground by the host.
Pin93	HWE_N (PC Card Memory mode)	I	1.Host mode: PCMCIA HWE_N is used for the control of writing register's data in attribute memory area or task file area.
	HWE_N (PC Card I/O mode)	I	HWE_N is used for the control of writing register's data in attribute memory area.
	None (True IDE mode)	I	This input signal is not used and should be connected to VCC by the host.
Pin33	SALE MCMD	O	1.Host mode: PCMCIA a.) NAND-type Flash/Smart Media address latch enable b.) SD/MMC card Command signal.
	FA0 SALE MCMD	O	2.Host mode: IDE a.) Compact Flash/IDE address bus [0]: It is asserted to access a register or data port in the Compact Flash/IDE device. b.) NAND-type Flash/Smart Media address latch enable c.) SD/MMC card Command signal.
Pin34	SCLE	O	1.Host mode: PCMCIA NAND-type Flash/Smart Media command latch enable
	FA1 SCLE	O	2.Host mode: IDE a.) Compact Flash/IDE address bus [1]: It is asserted to access a register or data port in the Compact Flash/IDE device. b.) NAND-type Flash/Smart Media command latch enable
Pin35	BS	O	1.Host mode: PCMCIA Memory Stick serial protocol bus state signal.
	FA2 BS	O	2.Host mode: IDE a.) Compact Flash/IDE address bus [2]: It is asserted to access a register or data port in the Compact Flash/IDE device. b.) Memory Stick serial protocol bus state signal.

Pin38	SRE_N	O	1.Host mode: PCMCIA NAND-type Flash/Smart Media read enable.
	IOR_N SRE_N	O	2.Host mode: IDE a.) Compact Flash/IDE I/O read signal b.) NAND-type Flash/Smart Media read enable.
Pin37	SWE_N	O	1.Host mode: PCMCIA NAND-type Flash/Smart Media write enable.
	IOW_N SWE_N	O	2.Host mode: IDE a.) Compact Flash/IDE I/O write signal. b.) NAND-type Flash/Smart Media write enable.
Pin9~Pin12	SD0~SD3 MD0~MD3	I/O	1.Host mode: PCMCIA a.) NAND-type Flash/Smart Media data I/O bus with internal 75K pull-downs. (2) b.) MMC/SD data bus with internal 75K pull-ups. (2)
	FD0~FD3 SD0~SD3 MD0~MD3	I/O	2.Host mode: IDE a.) Compact Flash/IDE data bus with internal 75K pull-downs. (2) b.) NAND-type Flash/Smart Media data I/O bus with internal 75K pull-downs. (2) c.) MMC/SD data bus with internal 75K pull-ups. (2)
Pin13~Pin16	SD4~SD7 SDIO0~SDIO3	I/O	1.Host mode: PCMCIA a.) NAND-type Flash/Smart Media data I/O bus with internal 75K pull-downs. (2) b.) Memory Stick serial data signal with internal 75K pull-down. (2)
	FD4~FD7 SD4~SD7 SDIO0~SDIO3	I/O	2.Host mode: IDE a.) Compact Flash/IDE data bus with internal 75K pull-downs. (2) b.) NAND-type Flash/Smart Media data I/O bus with internal 75K pull-downs. (2) c.) MMC/SD data bus with internal 75K pull-ups. (2)Memory Stick serial data signal with internal 75K pull-down. (2)
Pin17~Pin24	HA3~HA10	I	1.Host mode: PCMCIA Host side address bus bit 10 ~ bit 3

	FD8~FD15	I/O	2.Host mode: IDE IDE data bus bit 3 ~bit10 with internal 75K pull-downs.
Pin36	SCLK	O	Memory Stick serial protocol clock signal.
Pin47	MCLK	O	MMC/SD host to card clock signal.
Pin97	EA_N	I	External access enable: EA_N is an input configuration pin of N8052 core. It must be externally held low to enable the device to fetch code from external code memory.
Pin98	PSEN_N	O	Program strobe enable: PSEN_N is the read strobe signal to external code memory while fetching programs or performing MOVC instruction.
Pin95	RSTI_N	I	Reset input: A low on this pin for two machine cycles while the oscillator is running that resets the device.(1,2)
Pin115~Pin122	P0.0~P0.7	I/O	Port0: Port 0 is an 8-bit open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory. (2)
Pin41, 42, 4, 43, 44, 5, 45, 46	P1.0~P1.7	I/O	Port1: Port 1 is an 8-bit bi-directional I/O port with internal 75K pull-ups. They are the general-purpose I/O pins.
Pin107~Pin114	P2.0~P2.7	I/O	Port2: Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. (2)
Pin29~32, Pin39, 40, 127,128	P3.0~P3.7	I/O	Port3: Port 3 is an 8-bit bi-directional I/O port with internal 75K pull-ups. All bits have alternate functions, which are described below: (2) RxD (P3.0) : Serial Port 0 input TxD (P3.1) : Serial Port 0 output INT0_N (P3.2) : External Interrupt 0 INT1_N (P3.3) : External Interrupt 1 T0 (P3.4) : Timer 0 External Input T1 (P3.5) : Timer 1 External Input WR_N (P3.6) : External Data Memory Write Strobe RD_N (P3.7) : External Data Memory Read Strobe
Pin1~3, Pin48~52	P4.0~P4.7	I/O	Port4: Port 4 is an 8-bit bi-directional I/O port. The higher 2 bits are implemented the same with Port 1. The lower 6 bits are implemented as the I^2C and SPI interfaces respectively, which are described below. (2) SCL (P4.5) : I^2C bus serial clock output SDA (P4.4) : I^2C bus serial data input/output (open-drain) SS_N (P4.3) : SPI slave select input SCK (P4.2) : SPI master clock output/slave clock input MOSI (P4.1) : SPI master data output/slave data input MISO (P4.0) : SPI master data input/slave data output SS_N, MOSI, MISO 3 pins are implemented with internal pull-ups. When used in the I2C-related applications, SCL and SDA must be connected with external 4.7K pull-ups. And when used in the SPI-related applications, SCK has to be set to push-pull mode (by clear P4WOR register). In the other cases, it

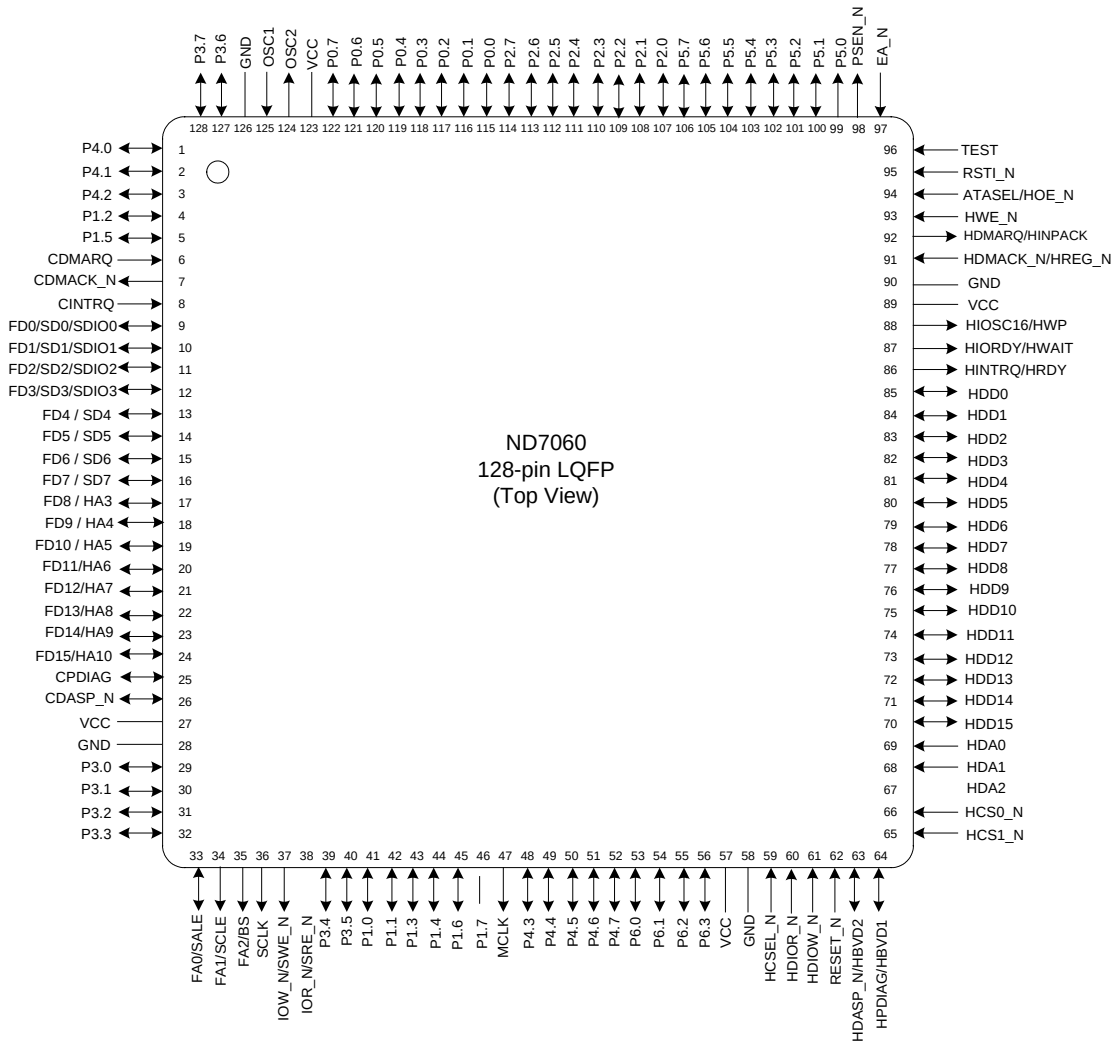
			is recommended to connect these 3 pins, SCL, SDA, and SCK, to external 75K pull-ups to avoid the signal floating.
Pin99~Pin106	P5.0~P5.7	I/O	Port5: Port 5 is an 8-bit bi-directional I/O port with internal pull-ups. This port also provides the lower address bits for accesses to external memory. (2)
Pin99~Pin106	P6.0~P6.3	I/O	Port6: Port 6 is an 4-bit bi-directional I/O port with internal pull-downs. A16 (P6.0) : High address A16 A17 (P6.1) : High address A17 A18 (P6.2) : High address A18
Pin6	CDMARQ	I	No use. Special function for tester. Please connect to VDD.
Pin7	CDMACK_n	O	No use. Special function for tester
Pin8	CINTRQ	I	No use. Special function for tester. Please connect to VDD.
Pin25	CPDIAG	I/O	No use. Special function for tester.
Pin26	CDASP_N	I/O	No use. Special function for tester.
Pin96	TEST	I	Test input pin. These pins are used only in the IC test mode, and should be connected to GND when in normal mode.
Pin125	OSC1	I	Crystal Oscillator Input (20MHz)
Pin126	OSC2	O	Crystal Oscillator Output (20MHz)
Pin27, 57, 89, 123	VCC	P	Power pin (3.3V)
Pin28, 58, 90, 126	GND	G	Ground. Pin

I: digital input direction; O: digital output direction; I/O: digital bi-direction;

Note (1) Schmitt triggered input buffer

Note (2) 5V tolerant input (bi-directional) buffer

Pin Assignment



Electrical Specification:

Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	DC supply voltage	-0.3	3.6	V
V_{IN}	DC input voltage	-0.3	V_{CC}+0.3	V
V_{OUT}	DC output voltage	-0.3	V_{CC}+0.3	V
T_{STG}	Storage temperature range	-55	150	^{o}C

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	3.0	3.3	3.6	V
V_{IN}	DC input voltage	0.0		V_{CC}	V
Tj	Commercial junction operating temperature	0	25	115	^{o}C

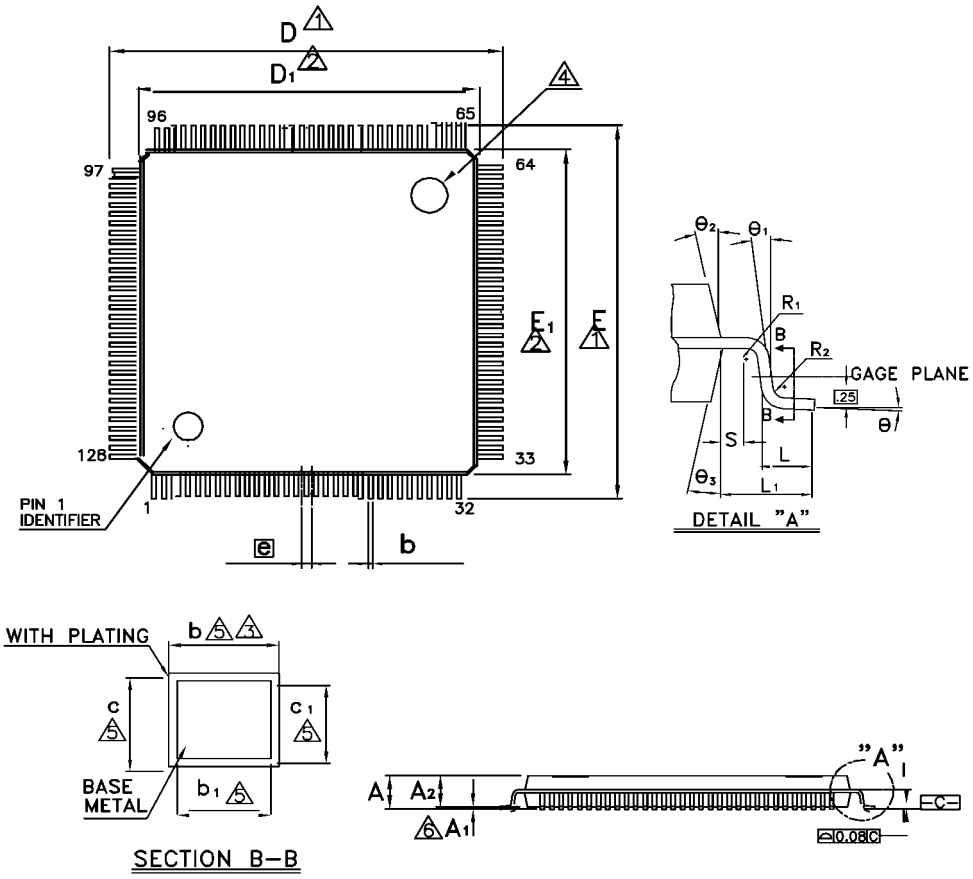
DC Characteristics

(Measured under the recommended operation conditions V_{CC}=3.0V~3.6V, Tj=0 ^{o}C ~115 ^{o}C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input leakage current	w/o pull-up/down	-1.0		1.0	uA
I_{OZ}	Tri-state leakage current		-1.0		1.0	uA
V_{IL}	Input low voltage				0.3*V_{CC}	V
V_{IH}	Input high voltage		0.7*V_{CC}			V
V_{t-}	Schmitt trigger negative going threshold voltage			TBD		V
V_{t+}	Schmitt trigger positive going threshold voltage			TBD		V
V_{OL}	Output low voltage	I_{OL}=2mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2mA	2.4			V
R_I	Input pull-up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}		75		KOhm
I_{OP}	Operating current	(1)		TBD		mA
I_{PWD}	Power down current	V_{IH}=V_{CC} V_{IL}=0.0V(1)		TBD		uA

Note (1) Measured within the assembled application circuits operating in internal 20MHz frequency

PACKAGE



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	--	--	1.60	--	--	0.063
A_1	0.05	--	--	0.002	--	--
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	--	0.20	0.004	--	0.008
c_1	0.09	--	0.16	0.004	--	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	--	--	0.003	--	--
R_2	0.08	--	0.20	0.003	--	0.008
S	0.20	--	-	0.008	--	--
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	--	--	0°	--	--
θ_2	12° TYP			12° TYP		
θ_3	12° TYP			12° TYP		

Supported ATA command set:

ND7060 for ATA Device Command List

General Feature Set			
Item	**Command Name**	**Code**	**Remarks**
1	Identify Device	0xEC	
2	Initialize Device Parameters	0x91	
3	Read Sector(s)	0x20	
4	Read Verify Sector(s)	0x40	
5	Set Features	0xEF	
6	Set Multiple Mode	0xC6	
7	Write Sector(s)	0x30	