

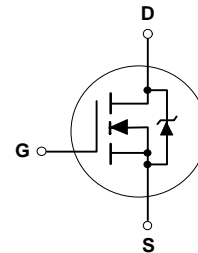
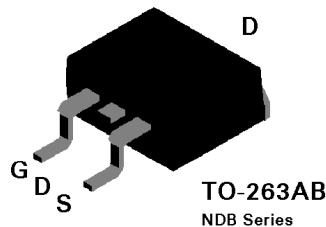
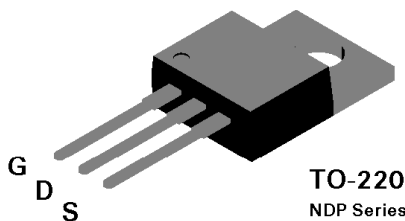
NDP7052L / NDB7052L N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 75 A, 50 V. $R_{DS(ON)} = 0.010 \Omega @ V_{GS} = 5 \text{ V}$
 $R_{DS(ON)} = 0.0075 \Omega @ V_{GS} = 10 \text{ V}$.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)} < 2.0\text{V}$.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2 PAK) package for both through hole and surface mount applications.



Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDP7052L	NDB7052L	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive ($t_p < 50 \mu\text{s}$)	± 25		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Maximum Power Dissipation @ $T_c = 25^\circ\text{C}$	150		W
	Derate above 25°C	1		
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
DRAIN-SOURCE AVALANCHE RATINGS (Note)								
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25\text{ V}, I_D = 75\text{ A}$			550	mJ		
I_{AR}	Maximum Drain-Source Avalanche Current				75	A		
OFF CHARACTERISTICS								
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	50			V		
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		0.075		$V/^\circ\text{C}$		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			250	μA		
			$T_J = 125^\circ\text{C}$		1	mA		
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 16\text{ V}, V_{DS} = 0\text{ V}$			100	nA		
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -16\text{ V}, V_{DS} = 0\text{ V}$			-100	nA		
ON CHARACTERISTICS (Note)								
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-0.005		$V/^\circ\text{C}$		
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1	1.3	2	V	
			$T_J = 125^\circ\text{C}$	0.8	0.85	1.6		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 5\text{ V}, I_D = 37.5\text{ A}$			0.0085	0.01	Ω	
			$T_J = 150^\circ\text{C}$			0.014	0.018	
			$V_{GS} = 10\text{ V}, I_D = 37.5\text{ A}$			0.0065	0.0075	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$	60			A		
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 37.5\text{ A}$		69		S		
DYNAMIC CHARACTERISTICS								
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		4030		pF		
C_{oss}	Output Capacitance			1260		pF		
C_{rss}	Reverse Transfer Capacitance			450		pF		
SWITCHING CHARACTERISTICS (Note)								
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 25\text{ V}, I_D = 37.5\text{ A},$ $V_{GS} = 5\text{ V}, R_{GEN} = 10\text{ }\Omega$ $R_{GS} = 10\text{ }\Omega$		25	50	nS		
t_r	Turn - On Rise Time			215	400	nS		
$t_{D(off)}$	Turn - Off Delay Time			110	200	nS		
t_f	Turn - Off Fall Time			170	300	nS		
Q_g	Total Gate Charge	$V_{DS} = 24\text{ V}$ $I_D = 75\text{ A}, V_{GS} = 5\text{ V}$		92	130	nC		
Q_{gs}	Gate-Source Charge			15		nC		
Q_{gd}	Gate-Drain Charge			45		nC		
DRAIN-SOURCE DIODE CHARACTERISTICS								
I_S	Maximum Continuous Drain-Source Diode Forward Current				75	A		
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				180	A		
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 37.5\text{ A}$ (Note)		0.9	1.3	V		
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 37.5\text{ A}$ $di_F/dt = 100\text{ A}/\mu\text{s}$	40		150	ns		
I_{rr}	Reverse Recovery Current		2		10	A		

Note:
Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

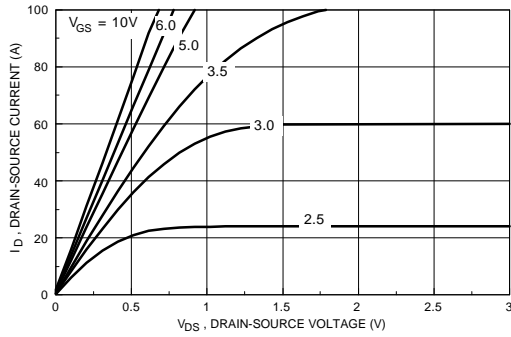


Figure 1. On-Region Characteristics.

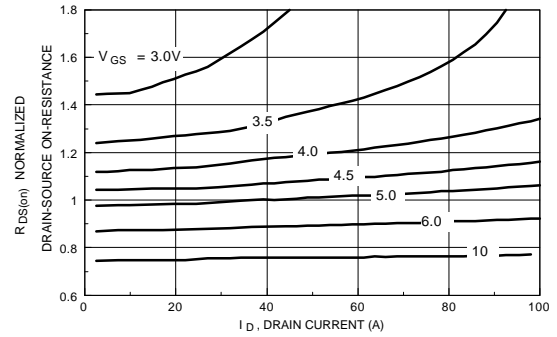


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

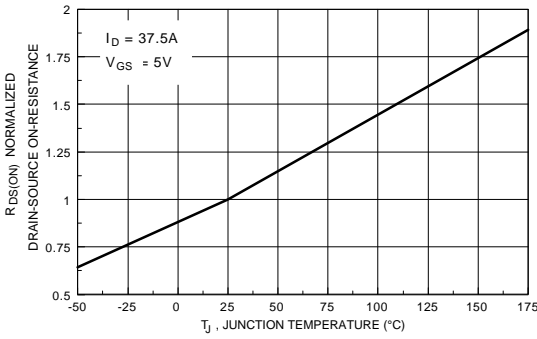


Figure 3. On-Resistance Variation with Temperature.

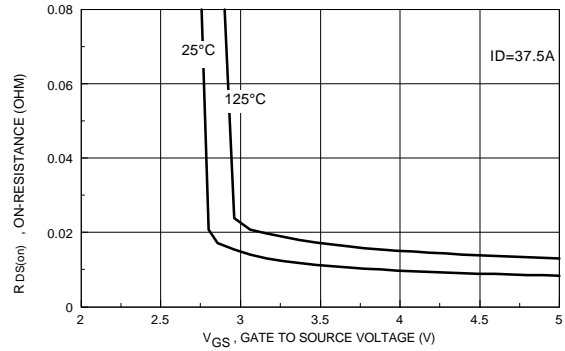


Figure 4. On Resistance Variation with Gate-To-Source Voltage.

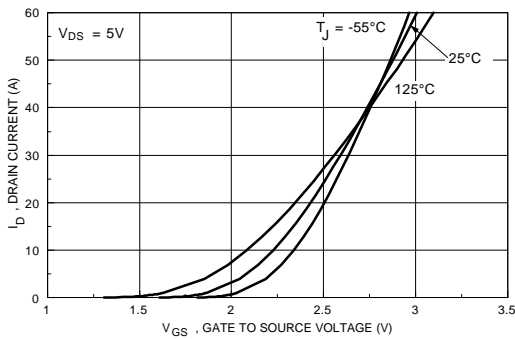


Figure 5. Transfer Characteristics.

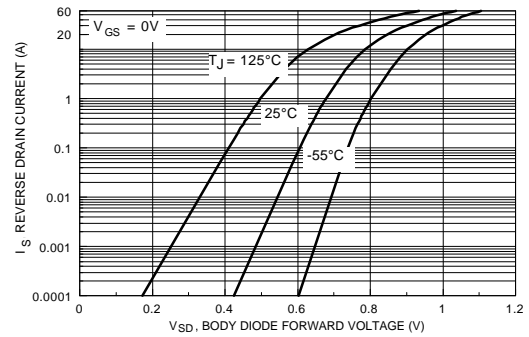


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

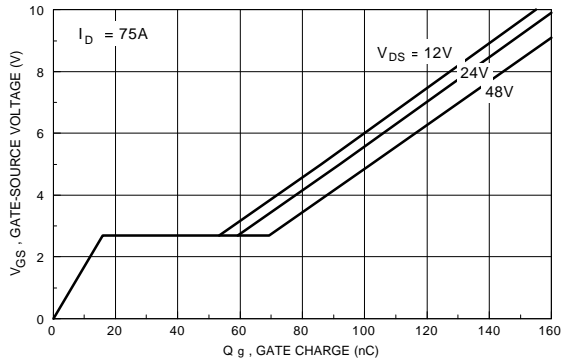


Figure 7. Gate Charge Characteristics.

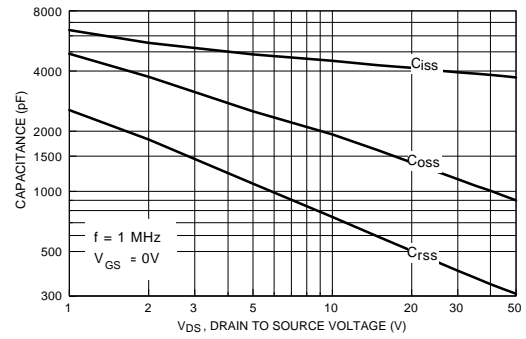


Figure 8. Capacitance Characteristics.

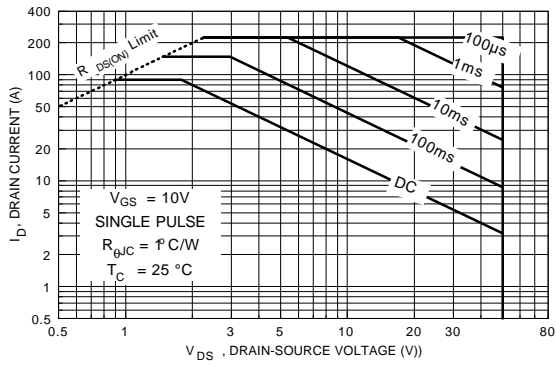


Figure 9. Maximum Safe Operating Area.

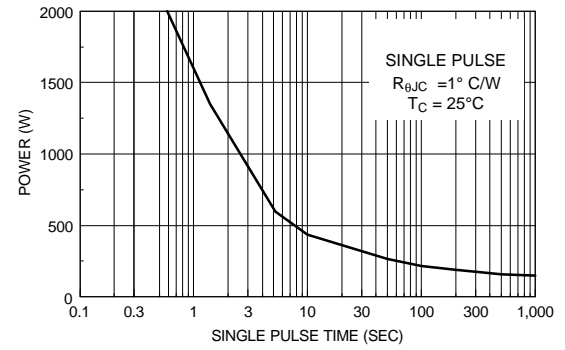


Figure 10. Single Pulse Maximum Power Dissipation.

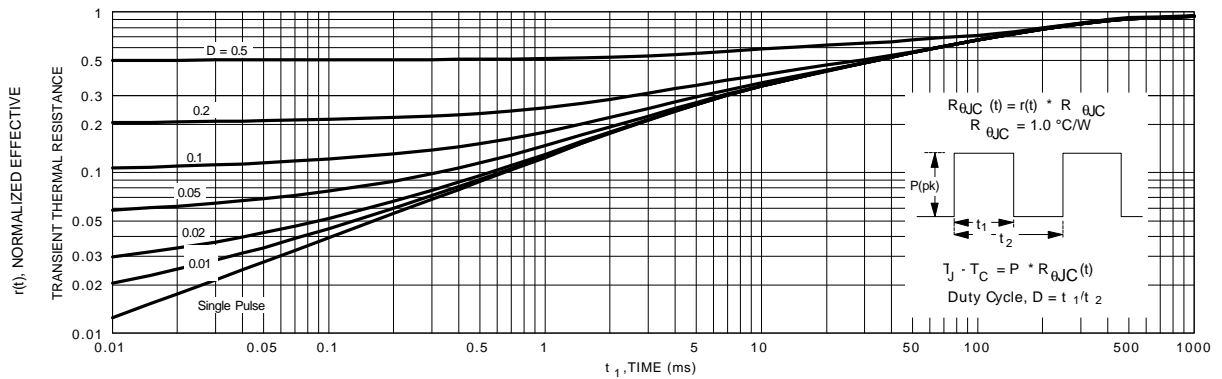


Figure 11. Transient Thermal Response Curve.