



**Description**

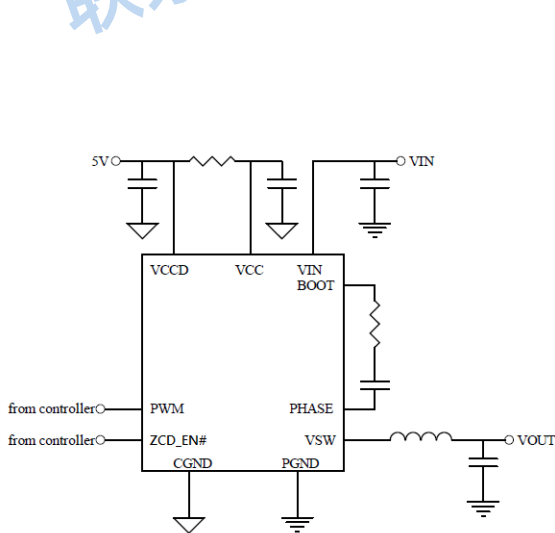
The NDC301RA integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package. The driver and MOSFETs have been optimized for high-current DC-DC buck power conversion applications. The NDC301RA integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

**Features**

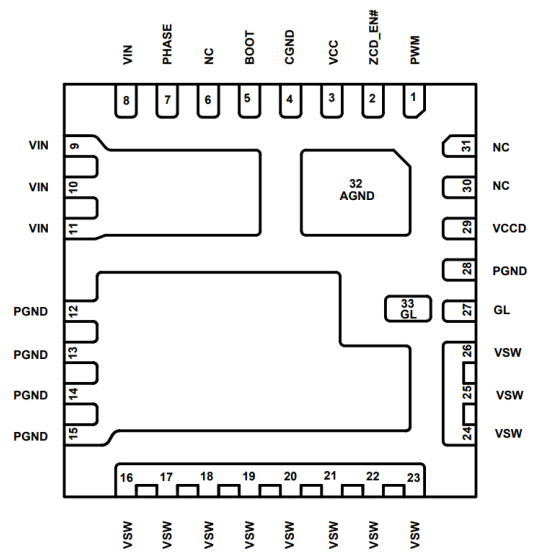
- Capable of Average Currents up to 60 A.
- Capable of Switching at Frequencies up to 1 MHz.
- Compatible with 5V PWM Input.
- Good 30V HS/LS MOSFET Characteristics
- The QFN5x5 Package of Low Impedance design.
- Zero Current Detection for High Efficiency at Light Load.
- Internal Bootstrap Diode.
- Under voltage Protection.
- Thermal Shutdown.
- Supports Intel® Power State 4.

**Applications**

- Desktop & Notebook Microprocessors V-Core and Non-V-Core DC-DC Converters.



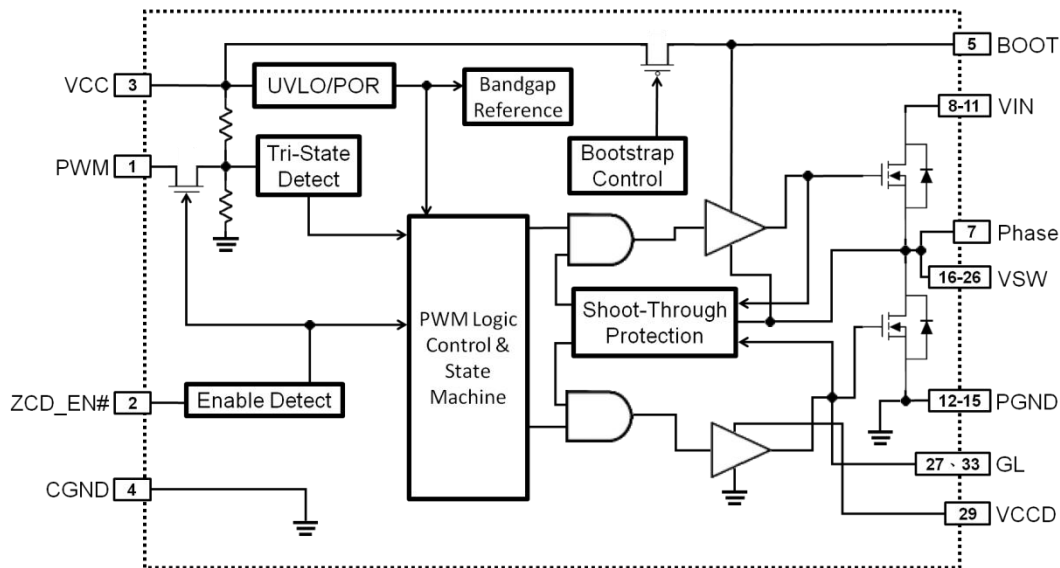
**Figure 1. Application Schematic**



**PINOUT DIAGRAM**

**Table 1. PIN LIST AND DESCRIPTIONS**

Pin No.	Symbol	Description
1	PWM	PWM Signal Input. Connect this pin to the PWM output of the controller.
2	ZCD_EN#	ZCD_EN# is used to control diode emulation mode. When ZCD_EN# is "LOW", diode emulation mode is allowed . When ZCD_EN# is "HIGH", continuous conduction mode is forced. ZCD_EN# can also be put in a high impedance mode by floating the pin. If both ZCD_EN# and PWM are floated, the device shuts down and operates at low current consumption mode.
3	VCC	Power supply of internal control logic. The required bias voltage for VCC is 5V. For avoiding noise disturbance, the supplied bias voltage must be stable.
4,32	CGND, AGND	Signal Ground (pin 4 and pad 32 are internally connected)
5	BOOT	Bootstrap Supply for High Side Gate Drive.
6	NC	No Connect
7	PHASE	Phase pad. Connect this pad to the Source of the high side FET and the Drain of the low side FET.
8-11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12-15, 28	PGND	Power Ground.
16-26	VSW	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27,33	GL	Low Side FET Gate Access (pin 27 and pad 33 are internally connected)
29	VCCD	Power supply of gate driver. The required bias voltage for VCCD is 5V.
30	NC	No Connect
31	NC	No Connect



**Figure 2. Block Diagram**

**POR (Power On Reset)**

POR block detects the voltage of the VCC pin. When the VCC pin voltage is higher than POR rising hreshold, POR block output is high. POR output is low when VCC is not higher than POR rising threshold. When the POR block output is high, UGATE and LGATE can be controlled by PWM input voltage. If the POR block output is low, both UGATE and LGATE will be pulled to low.

**Enable Detect**

When ZCD\_EN# pin input voltage is higher/lower than ZCD\_EN# rising threshold, MOSFET driver is enabled/disabled. When the ZCD\_EN# input and POR output are high, UGATE and LGATE can be controlled by PWM input voltage. When ZCD\_EN# input is low, both UGATE and LGATE are pulled to low, and the PWM input terminal is opened.

**Tri-State Detect**

When both POR block output and ZCD\_EN# pin voltages are high, UGATE and LGATE can be controlled by PWM input. There are three PWM input modes, which are high, low, and tri-state. If PWM input is within the tri-state window, both UGATE and LGATE outputs are low. When PWM input is higher than its rising threshold, UGATE is high and LGATE is low. When PWM input is lower than its falling threshold, UGATE is low and LGATE is high

**Bootstrap Control**

Bootstrap control block controls the integrated bootstrap switch. When LGATE is high (low side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor connected to the BOOT pin. When LGATE is low (low side MOSFET is turned off), the bootstrap switch is turned off to disconnect the VCC pin and BOOT pin

**Turn-Off Detection**

Turn-off detection block detects whether high side MOSFET is turned off by monitoring PHASE pin voltage. To avoid shoot-through between high side and low side MOSFETs, low side MOSFET can be turned on only after high side MOSFET is effectively turned off.

**Shoot-Through Protection**

Shoot-through protection block implements the dead time when both high side and low side MOSFETs are turned off. With shoot-through protection block, high side and low side MOSFETs are never turned on simultaneously. Thus, shoot through between high side and low side MOSFETs is prevented.

**Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information-all signals referenced to PGND unless noted otherwise)**

Pin Name/Parameter	Min	Max	Unit
Supply Voltage	-0.3	6.5	V
VIN	-0.3	30	V
BOOT to PHASE	-0.3	6.8	V
PHASE to GND	-0.3	30	V
LGTAE to GND	-0.3	6.8	V
UGATE to PHASE	-0.3	6.8	V
EN, PWM to GND	-0.3	6.8	V
Tstg	-65	150	°C
T <sub>J</sub>		150	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. THERMAL INFORMATION**

Rating	Symbol	Value	Unit
Thermal Resistance	$\theta_{JA}$	12.5	°C/W
Maximum Power Dissipation		10.4	W
Moisture Sensitivity Level	MSL	1	

1. JESD 51-5 (1S2P Direct-Attach Method) with 0 LFM.
2. JESD 51-7 (1S2P Direct-Attach Method) with 0 LFM.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

Parameters	Pin Name	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>CC</sub>		4.5		5.5	V
Power Stage Power Supply	V <sub>IN</sub>		4.5		24	V
Junction Temperature Range			-10		105	°C
Continuous Output Current		F <sub>SW</sub> = 1 MHz, V <sub>IN</sub> = 12 V, V <sub>OUT</sub> = 1.0 V, T <sub>A</sub> = 25°C			60	A

Peak Output Current		$F_{SW} = 500 \text{ kHz}$ , $V_{IN} = 12 \text{ V}$ , $V_{OUT} = 1.0 \text{ V}$ , Duration = 10 ms.			75	A
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Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 5. ELECTRICAL CHARACTERISTICS**

$V_{IN} = 12 \text{ V}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $125 \text{ }^\circ\text{C}$ , unless otherwise noted. ( $U_{G\_CISS} = 6000\text{pF}$ ,  $L_{G\_CISS} = 10000\text{pF}$ ).

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>POWER SUPPLY</b>						
PS4 power supply current	$I_{IN \text{ Sby}}$	PWM=Hi-Z, $V_{ZCD\_EN\#} = \text{Hi-Z}$			5	uA
Control Logic Supply Current	$I_{VCC}$	$V_{PWM} = \text{FLOAT}$		20		
		$V_{PWM} = \text{FLOAT}$ , $V_{ZCD\_EN\#} = 0 \text{ V}$		112		
Drive Supply Current	$I_{VCCD}$	$f_s = 1\text{MHz}$ , $D = 0.1$		131		mA
		$f_s = 300 \text{ kHz}$ , $D = 0.1$		9		
		$f_s = 1 \text{ MHz}$ , $D = 0.1$		31		
<b>PWM CONTROL INPUT</b>						
Rising Threshold(5V logic)	$V_{TH\_PWM\_R}$		3.55	3.8	4.05	V
Falling Threshold(5V logic)	$V_{TH\_PWM\_F}$		0.72	1	1.3	V
PWM Tri-state Threshold window (5V logic)	$V_{TRI\_TH}$	$V_{PWM} = \text{FLOAT}$	1.2		3.7	V
Tri-state Voltage	$V_{TRI}$	$V_{PWM} = \text{FLOAT}$		1.8		V
PWM Input Current	$I_{PWM}$	$V_{PWM} = 5\text{V}$			350	uA
		$V_{PWM} = 0\text{V}$			-350	uA
<b>ZCD_EN# CONTROL INPUT</b>						
Rising Threshold(5V logic)	$V_{TH\_ZCD\_EN\#\_R}$		3.55	3.8	4.05	V
Falling Threshold(5V logic)	$V_{TH\_ZCD\_EN\#\_F}$		0.72	0.9	1.3	
ZCD_EN# Tri-state Threshold window (5V logic)	$V_{TRI\_TH\_ZCD\_EN\#}$	$V_{ZCD\_EN\#} = \text{FLOAT}$	1.2		3.7	
Tri-state Voltage	$V_{TRI\_ZCD\_EN\#}$	$V_{ZCD\_EN00\#} = \text{FLOAT}$		1.7		
ZCD_EN# Input Current	$I_{ZCD\_EN\#}$	$V_{ZCD\_EN\#} = 5\text{V}$			100	uA
		$V_{ZCD\_EN\#} = 0\text{V}$			-100	

TIMING SPECIFICATIONS						
Minimum UG On-time	TONmin			52		ns
Dead time(rising/falling)	DT			30		ns
Tri-State Hold-Off Time	tTSHO			50		ns
Tri-State to GH/GL Rising Propagation Delay	tPD_TRI_R			20		ns
GH - Turn Off Propagation Delay	tPD_OFF_GH			14		ns
GL - Turn Off Propagation Delay	tPD_OFF_GL			5		ns
PROTECTION						
Under Voltage Lockout	VUVLO	VCC rising, on threshold		4	4.3	V
		VCC falling, off threshold	3.6	3.7		
Under Voltage Lockout Hysteresis	VUVLO_HYST			335		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

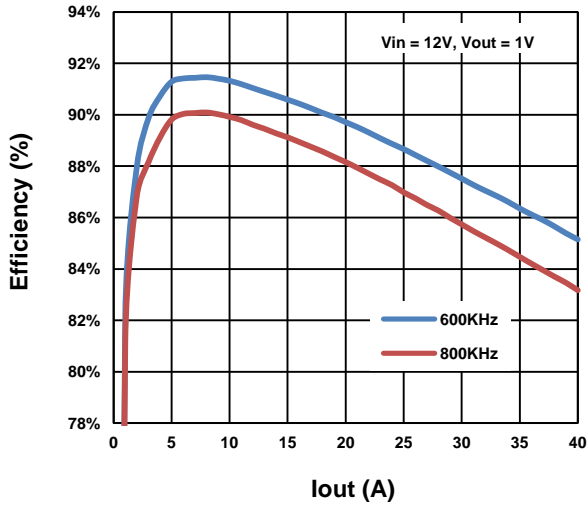
**Table 6. LOGIC TABLE**

ZCD_EN#	PWM	GH	GL
L	L	L	H, I <sub>L</sub> >0A L, I <sub>L</sub> <0A
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L

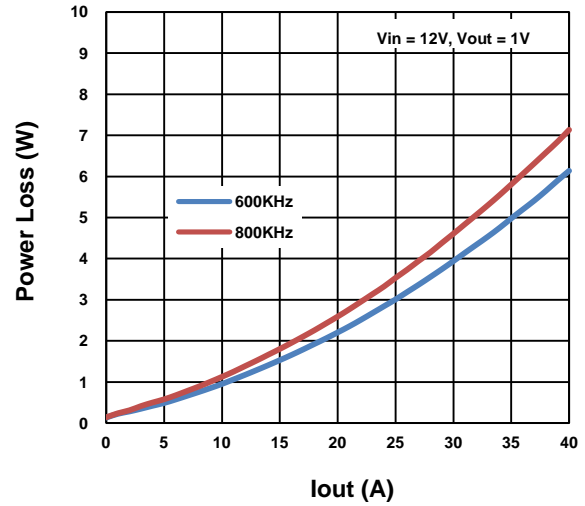
**Typical Performance Characteristics**

(Test Conditions:  $V_{IN} = 12\text{ V}$ ,  $V_{CC} = PV_{CC} = 5\text{ V}$ ,  $V_{OUT} = 1\text{ V} \text{ \& } 1.8\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

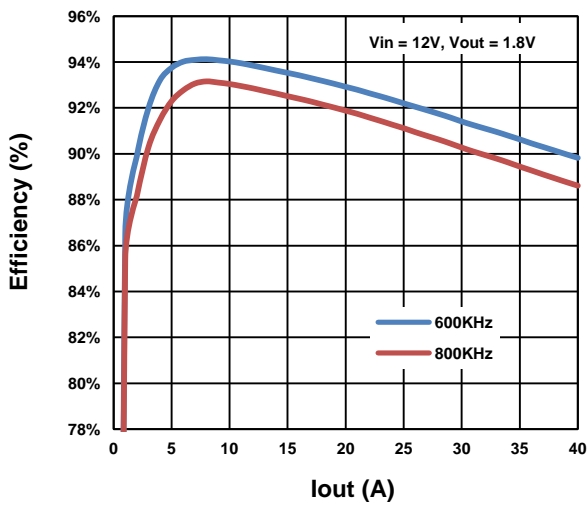
**Figure 3. Efficiency**



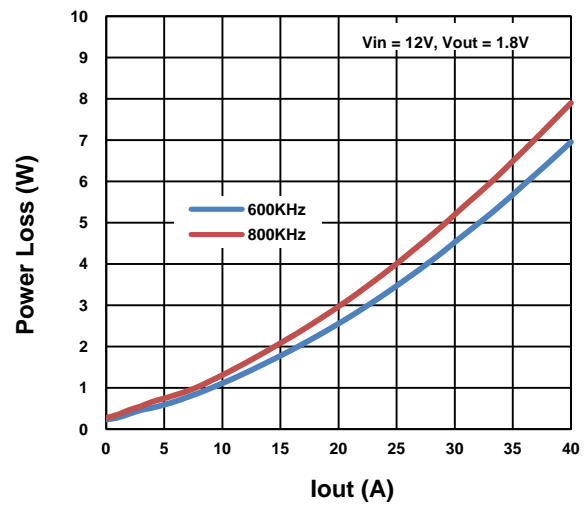
**Figure 4. Power Loss vs. Output Current**



**Figure 5. Efficiency**



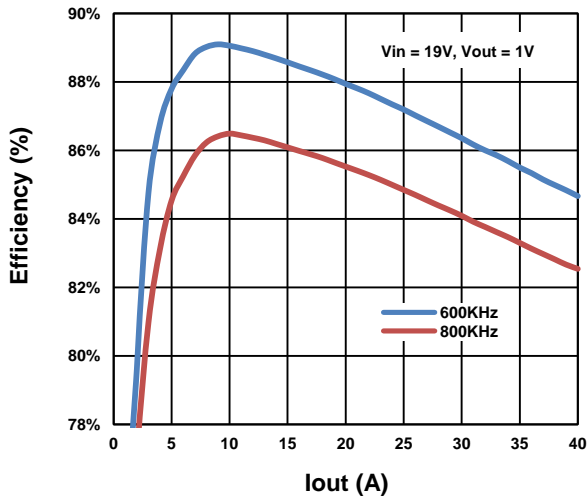
**Figure 6. Power Loss vs. Output Current**



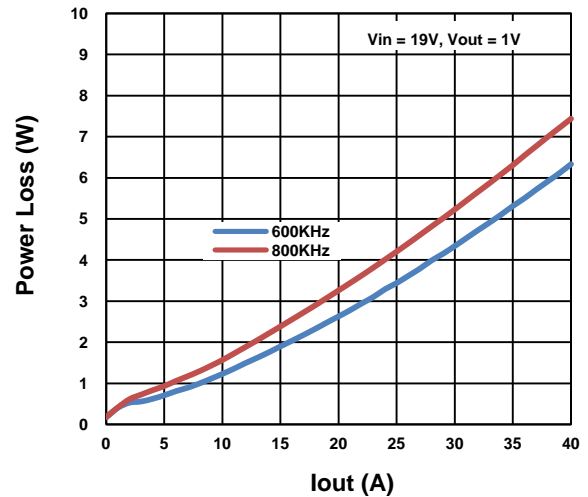
**Typical Performance Characteristics**

(Test Conditions:  $V_{IN} = 19\text{ V}$ ,  $V_{CC} = PV_{CC} = 5\text{ V}$ ,  $V_{OUT} = 1\text{ V}$  &  $1.8\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

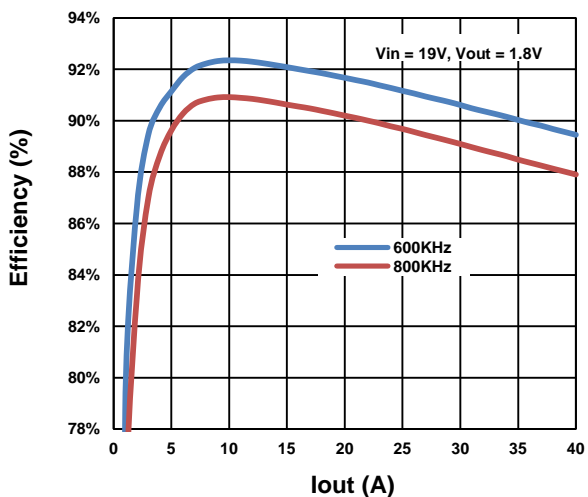
**Figure 7. Efficiency**



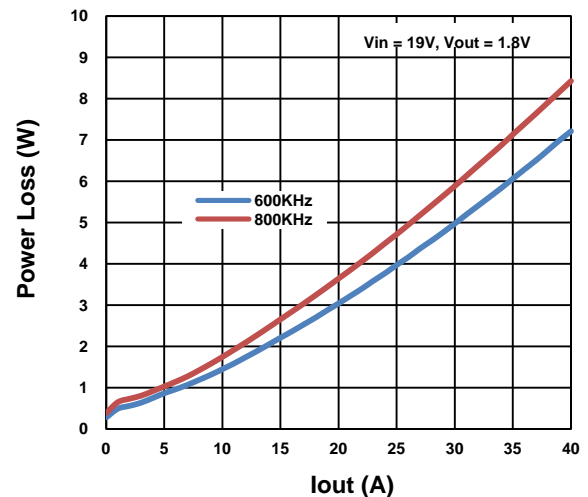
**Figure 8. Power Loss vs. Output Current**



**Figure 9. Efficiency**

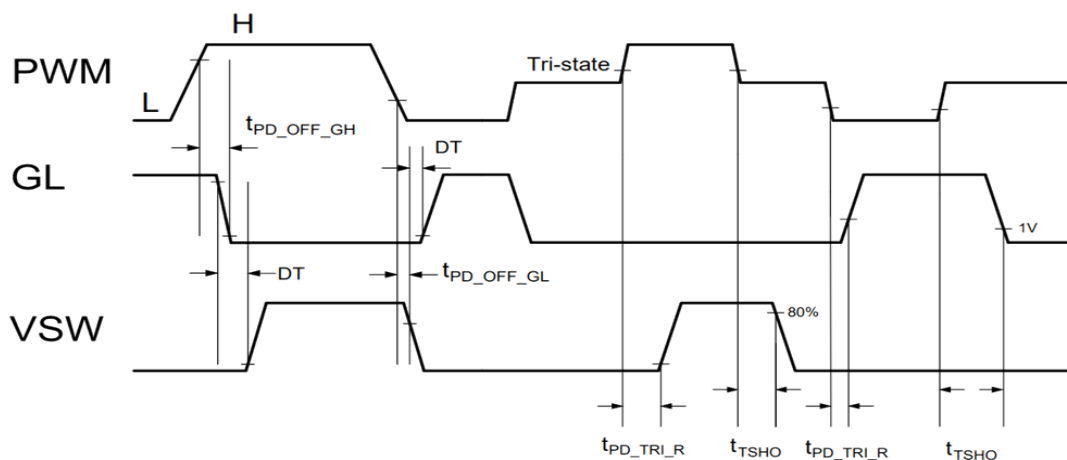


**Figure 10. Power Loss vs. Output Current**





**Timing Diagram**



**Figure 11. Timing Diagram**

**Application Information**

The NDC301RA is a high frequency, synchronous rectified, single phase dual MOSFET driver containing advanced MOSFET driver technologies. The NDC301RA is designed to be able to adapt from normal MOSFET driving applications to high performance CPU/GPU VR driving capabilities.

**Supply Voltage and Power On Reset**

The NDC301RA can be utilized under VCC = 5V application. The NDC301RA is designed to drive both high side and low side N-MOSFET through external input PWM control signal. It has a power on protection function which held UGATE and LGATE low before the VCC voltage rises to higher than rising threshold voltage.

**Enable and Disable**

The NDC301RA includes a ZCD\_EN# pin for sequence control. When the ZCD\_EN# pin rises above the V<sub>TH\_ZCD\_EN#\_R</sub> trip point, the NDC301RA begins a new initialization and follows the PWM command to control the UGATE and LGATE. When the ZCD\_EN# pin falls below the V<sub>TH\_ZCD\_EN#\_F</sub> trip point, the NDC301RA shuts down to keep UGATE and LGATE low and keep the PWM input terminal open. To avoid noise coupled, EN pin is recommended adding a bypass capacitor with de-glitch time of 400ns for the EN shutdown function.

**Tri-state PWM Input**

After the initialization, the PWM signal takes control. The rising PWM signal first forces the LGATE signal to turn low then the UGATE signal is allowed to go

high just after a non-overlapping time to avoid shoot-through current. The falling of the PWM signal first forces UGATE to go low. When UGATE and PHASE signals reach a predetermined low level, LGATE signal is allowed to turn high. The PWM signal acted as “High” if the signal is above the rising threshold and acted as “Low” if the signal is below the falling threshold. When the PWM signal level enters and remains within the tri-state window, the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWM signal is left floating, the pin will be kept around 2.5V by the internal divider and provide the PWM controller with a recognizable level.

**Internal Bootstrap Power Switch**

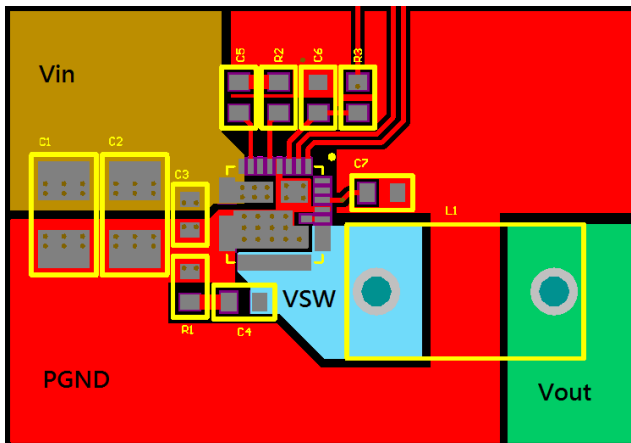
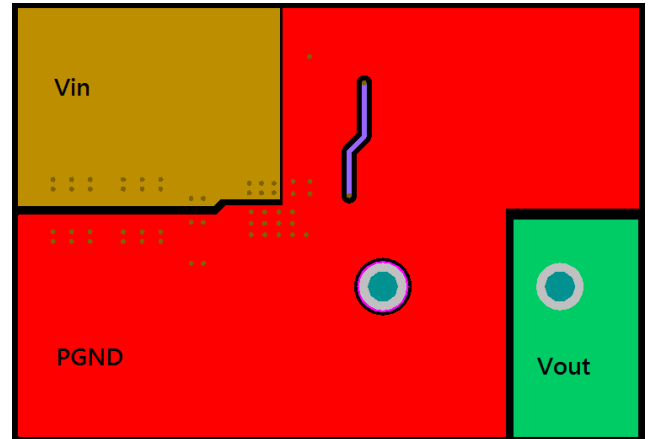
The NDC301RA builds in an internal bootstrap power switch to replace the external bootstrap diode, and this can facilitate PCB design and reduce the total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

**NDC301RA PCB layout guide**

NDC301RA is a high-current-rated device capable of operating up to 1 MHz. Achieving such high frequency requires extremely fast switching speeds to keep switching losses and device temperatures within limits. Integrating a robust gate driver with MOSFETs in one package eliminates the parasitic components or PCB associated with the driver-to-MOSFET and between high side and low side MOSFETs, thus resulting in excellent switching speeds. However, correspondingly high levels of  $dv/dt$  and  $di/dt$  will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients.

The PCB design is somewhat simplified because of the package integration and optimized pin assignment. The VIN and PGND pins are located adjacent to each other, and the input bypass capacitors (C1, C2, C3) should be placed as close as possible to these pins. The PHASE switching loop, formed by PHASE (VSW), output inductor (L1), and output capacitor COUT is the next critical current loop. This requires a second layer with an uninterrupted PGND plane with sufficient GND vias placed as close as possible to the bypass capacitor PGND pads.

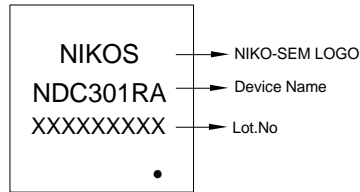
PGND plane, and a via should be used to connect CVCCD directly to the PGND plane. Finally, CBOOT (C5) and RBOOT(R2) should be connected directly to pins 5, and 7.



To simplify thermal management, both VIN and GND pads should be attached to larger VIN and PGND planes directly using a number of vias. These vias provide a thermal connection to the copper layers under the NDC301RA, which then conduct heat away from the heat source, whereby the “electrical vias” also function as “thermal vias”. It is essential to ensure that the copper plane is not interrupted by tracks that run perpendicular to the thermal path away from the power component. The VCCD bypass capacitor CVCCD (C7) should connect directly to the

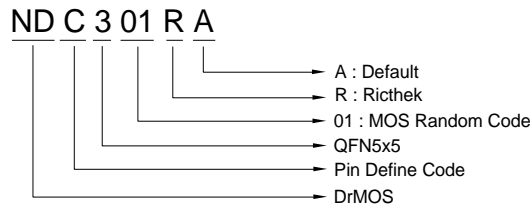
**Marking Information:(Please see the corresponding data sheet)**

1.零件Marking 文字面說明

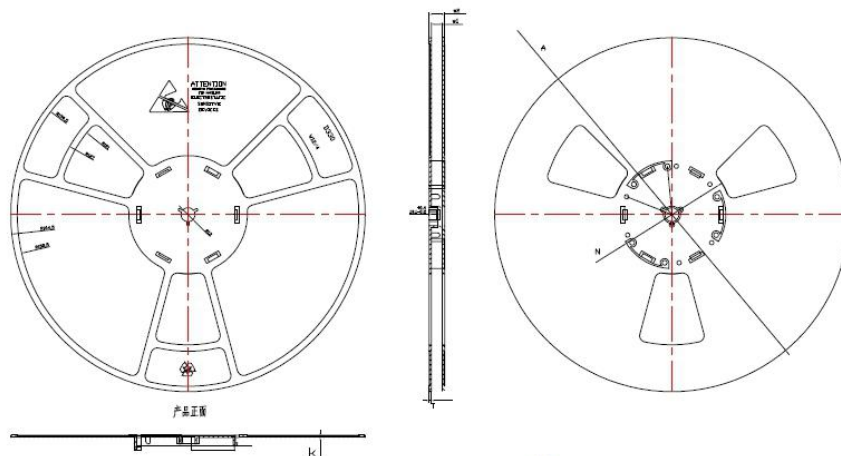
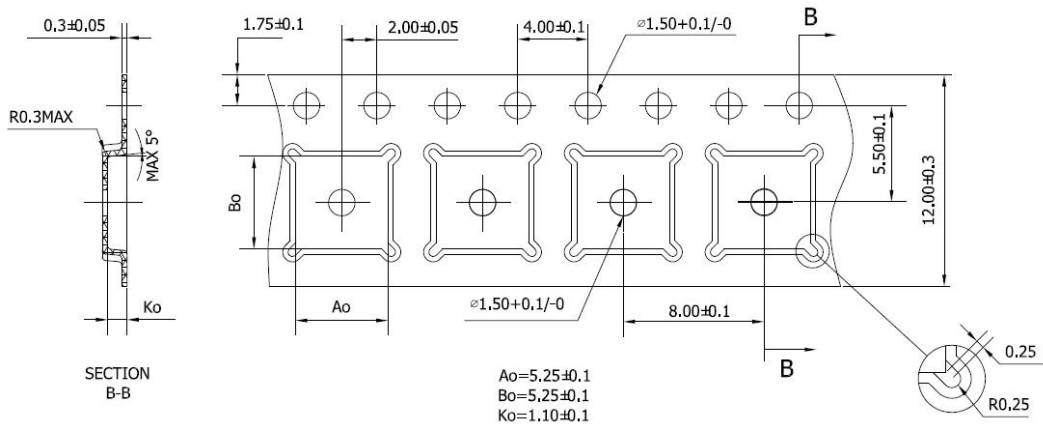


#1

2.零件 Part number 說明



**Tape&Reel Information:5000pcs/Reel**

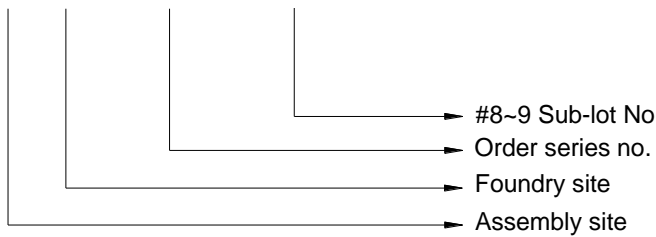


附註:All Dimension in millimeter

**Lot.No. & Date Code rule**

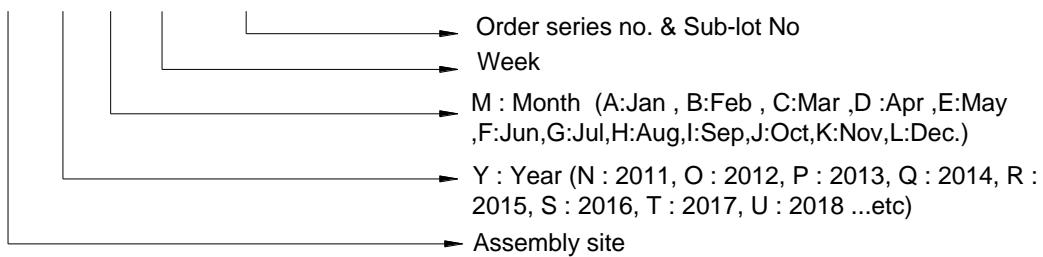
1.LOT.NO.

M N 15M21 03



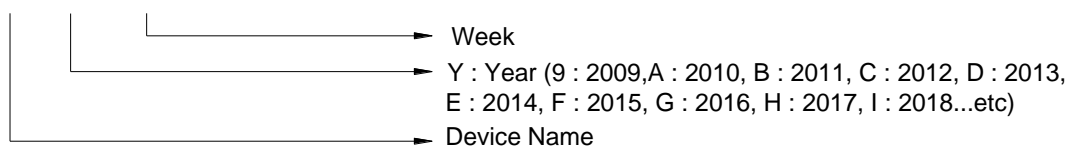
2.Date Code

D Y M X XXX



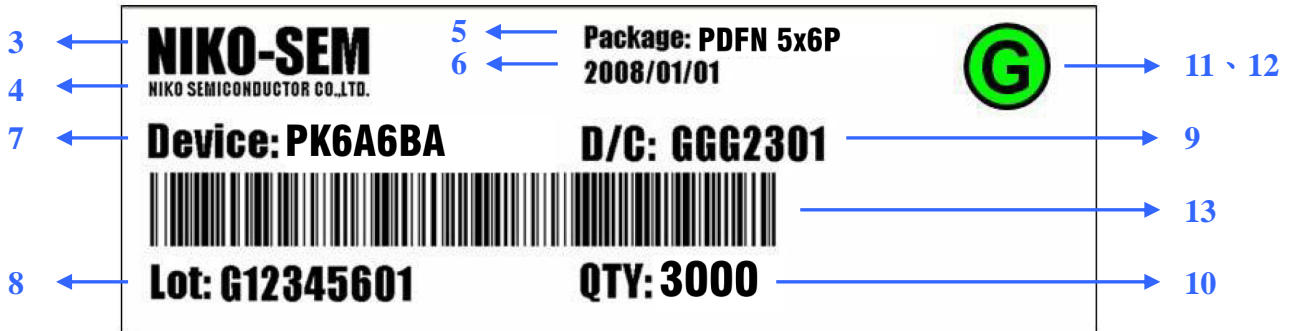
3.Date Code (for Small package)



XX Y WW

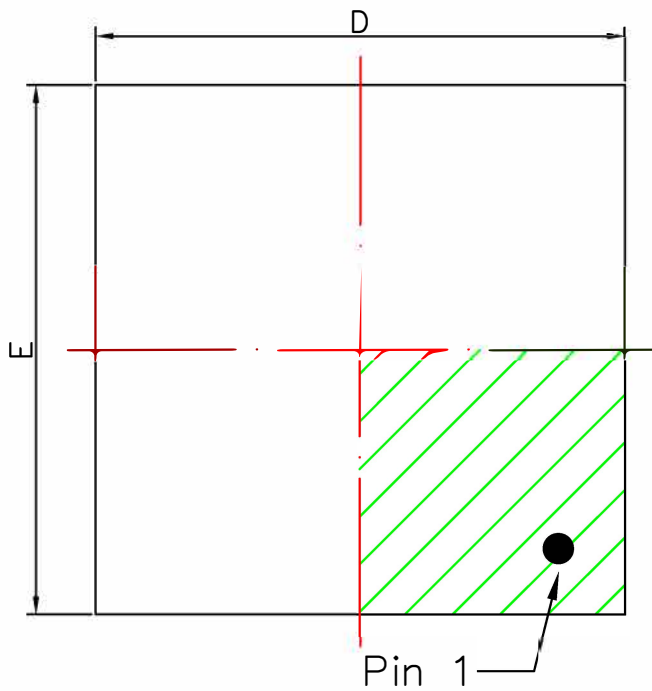


**Label rule**

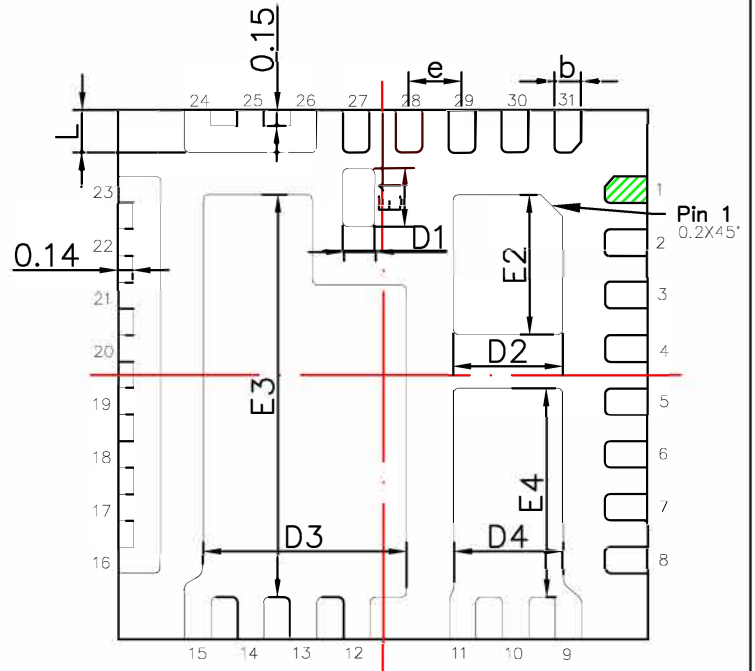
標籤內容 (Label content)



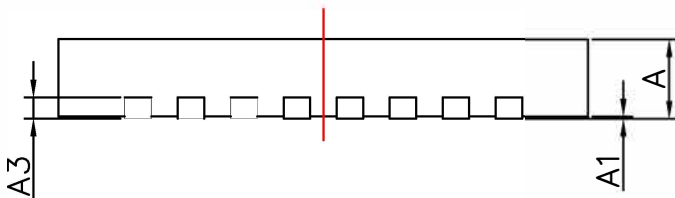
1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可區分英文”O”和數字”0”，”G 和”Q”的字型即可) (Or any font capable of being distinguished for Letter O and digital 0, and for G and Q))
3	NIKO-SEM	Height: 4 mm
4	NIKO SEMICONDUCTOR CO., LTD.	Height: 1 mm
5	Package	Height: 2 mm
6	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
7	Device	Height: 3 mm (Max: 16 Digit) Device Name not including Rev.
8	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
9	D/C	Height: 3 mm (Max: 7 Digit)
10	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
11	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
13	Scan info	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least



**Top View**



**Bottom View**

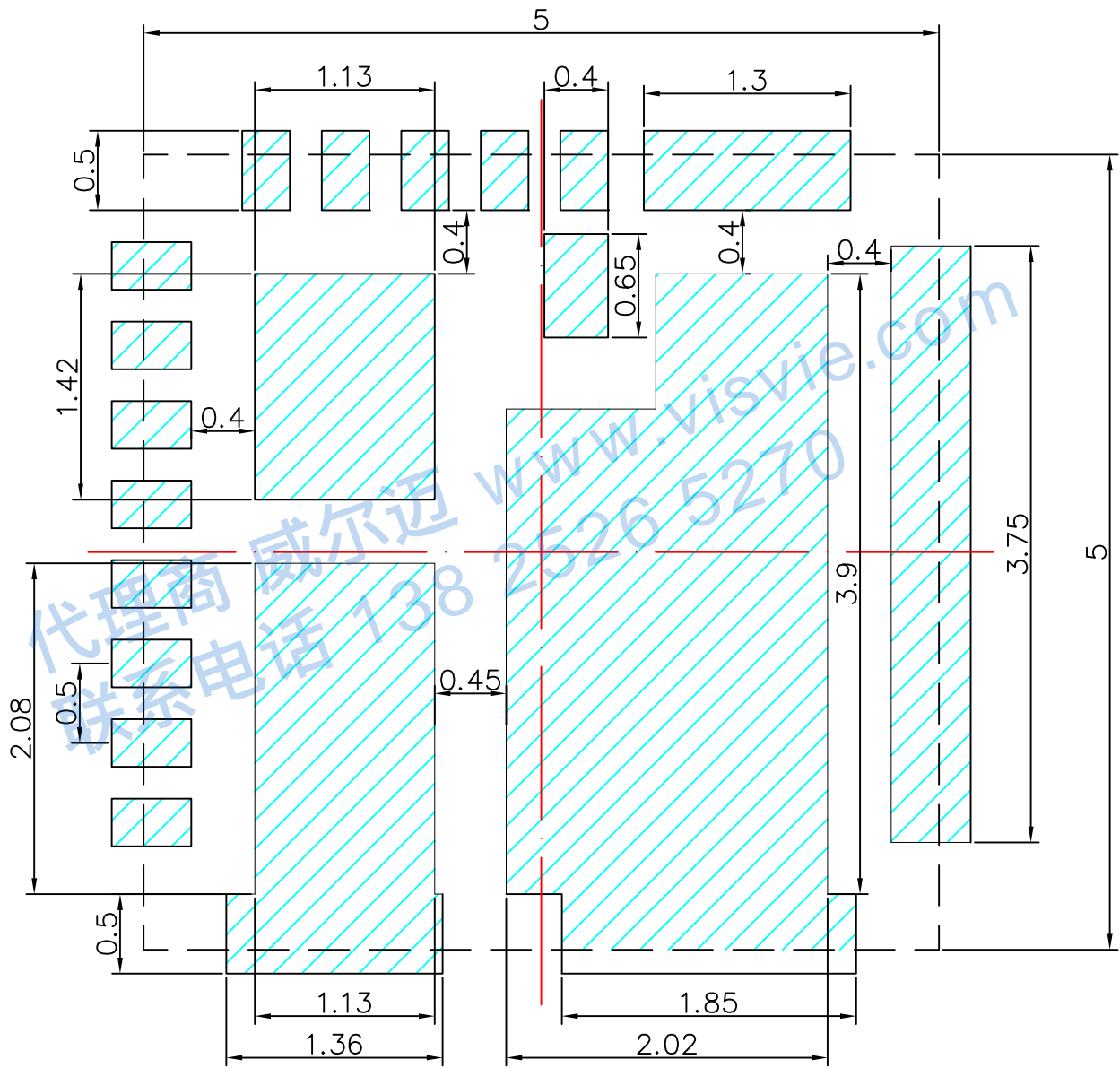


**Side View**

SYMBOL	DIMENSIONS IN MM			SYMBOL	DIMENSIONS IN MM		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.70	0.75	0.80	D4	0.93	1.03	1.13
A1	0	0.02	0.05	E	5.00 BSC		
A3	0.20 REF.			E1	0.45	0.55	0.65
b	0.20	0.25	0.30	E2	1.22	1.32	1.42
D	5.00 BSC			E3	3.70	3.80	3.90
D1	0.20	0.30	0.40	E4	1.88	1.98	2.08
D2	0.93	1.03	1.13	e	0.50 BSC		
D3	1.82	1.92	2.02	L	0.30	0.40	0.50

**\* Dimensions Are Exclusive Of Burrs , Mold Flash And Tie Bar Protrusions**

Package Dimension		PQFN31-5x5		REV.	1.1	Q'TY	1 OF 2
UNIT	MM	SCALE	15 : 1	DATE	Aug.10.2023		



**Land Pattern  
(Only for reference)**

Package Dimension		PQFN31-5x5		REV.	1.1	Q'TY	2 OF 2
UNIT	MM	SCALE	25 : 1	DATE	Aug.10.2023		