**FAIRCHILD**

SEMICONDUCTOR ™

NDS355N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMICA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.6A, 30V. $R_{DS(ON)} = 0.125\Omega$ @ $V_{GS} = 4.5V$.

- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.

- High density cell design for extremely low $R_{DS(ON)}$.

- Exceptional on-resistance and maximum DC current capability.

- Compact industry standard SOT-23 surface mount package.

SuperSOT™-3
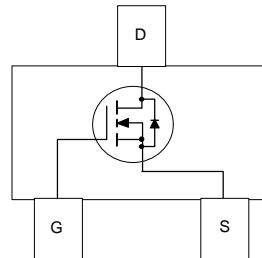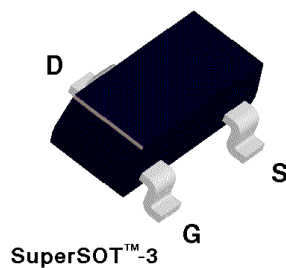
Absolute Maximum Ratings $T_A = 25°C$ unless otherwise noted

Symbol	Parameter		NDS355N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage - Continuous		20	V
I_D	Drain Current - Continuous	(Note 1a)	± 1.6	A
	- Pulsed		± 10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to -Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V				1	µA
			T_J=125°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS}= 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA		1	1.6	2	V
			T_J=125°C	0.5	1.3	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 1.6 A				0.125	Ω
			T_J=125°C			0.25	
		V_{GS} = 10 V, I_D = 1.9 A				0.085	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V		6			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.6 A			3.5		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz			245		pF
C_{oss}	Output Capacitance				130		pF
C_{rss}	Reverse Transfer Capacitance				20		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω			15	30	ns
t_r	Turn - On Rise Time				14	30	ns
$t_{D(off)}$	Turn - Off Delay Time				12	25	ns
t_f	Turn - Off Fall Time				4	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.6 A, V_{GS} = 5 V			3.5	5	nC
Q_{gs}	Gate-Source Charge					1	nC
Q_{gd}	Gate-Drain Charge					2	nC

Electrical Characteristics $(T_A = 25°C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				0.6	A
I_{SM}	Maximum Pulse Source Current (Note 2)				6	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 1.6$ A		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)}@T_J$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz cpper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz cpper.

1 a   **1b**
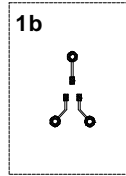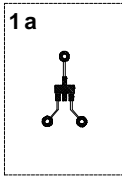
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq$ 300µs, Duty Cycle $\leq$ 2.0%.

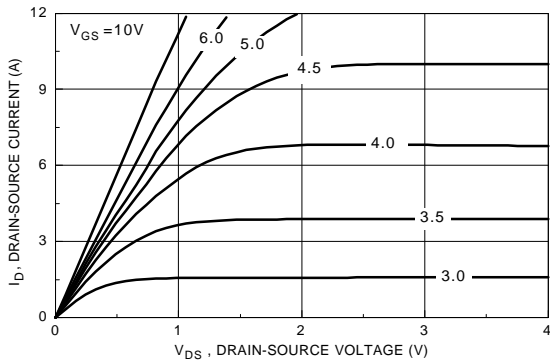## Typical Electrical Characteristics
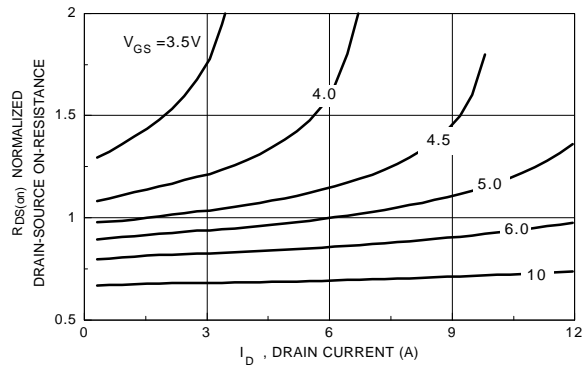
Figure 1. On-Region Characteristics

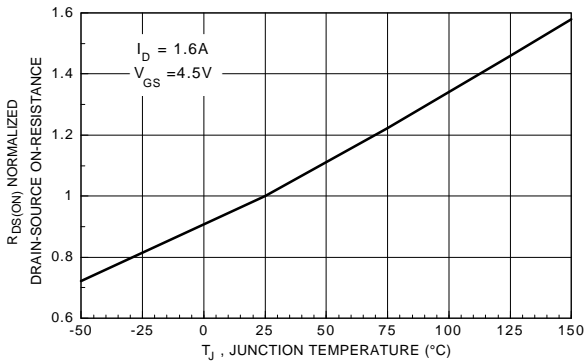**Figure 2. On-Resistance Variation with Gate Voltage and Drain Current**

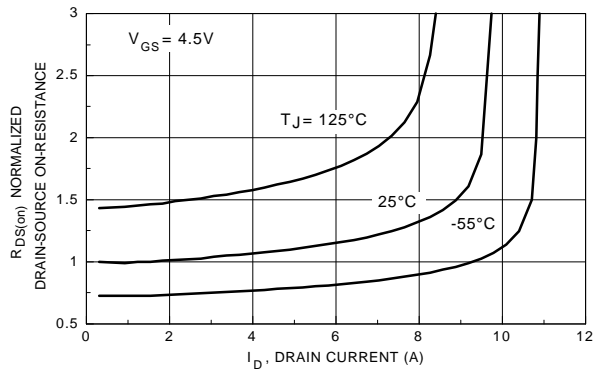**Figure 3. On-Resistance Variation with Temperature**

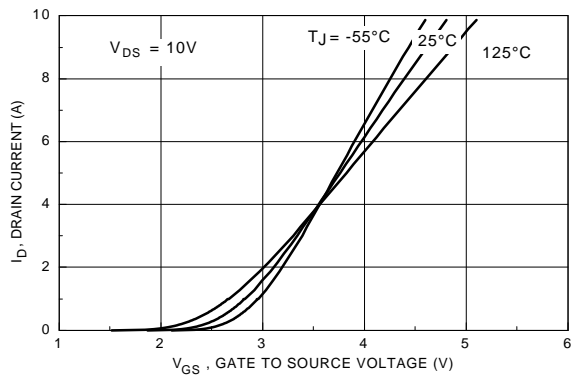**Figure 4. On-Resistance Variation with Drain Current and Temperature**
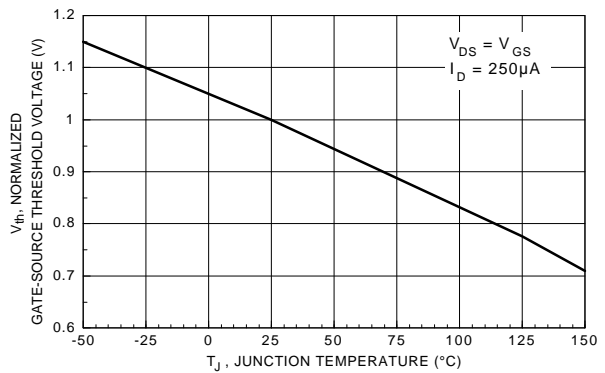
Figure 5. Transfer Characteristics

Figure 6. Gate Threshold Variation with Temperature
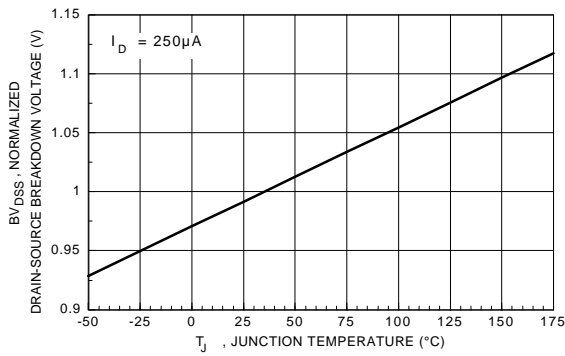
Typical Electrical Characteristics (continued)

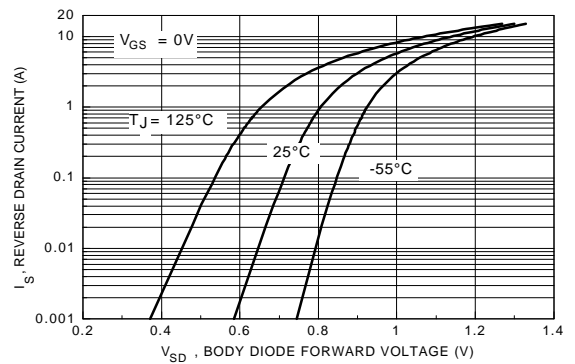**Figure 7. Breakdown Voltage Variation with Temperature**

X-axis: T_J, JUNCTION TEMPERATURE (°C)
Y-axis: BV_{DSS}, NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE (V)
$I_D = 250\mu A$

Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

X-axis: V_{SD}, BODY DIODE FORWARD VOLTAGE (V)
Y-axis: I_S, REVERSE DRAIN CURRENT (A)
$V_{GS} = 0V$
$T_J = 125°C$, 25°C, -55°C
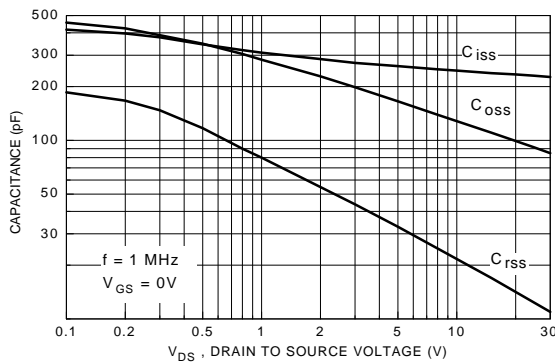
Figure 9. Capacitance Characteristics

X-axis: V_{DS}, DRAIN TO SOURCE VOLTAGE (V)
Y-axis: CAPACITANCE (pF)
C_{iss}, C_{oss}, C_{rss}
$f = 1$ MHz
$V_{GS} = 0V$
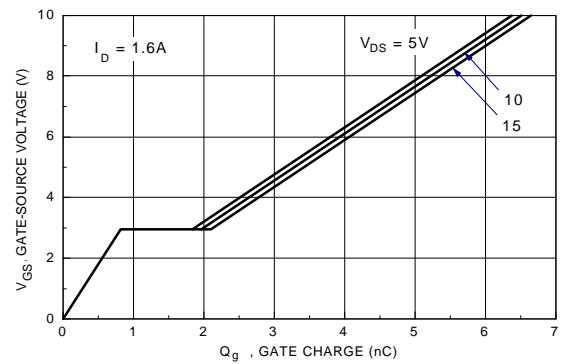
Figure 10. Gate Charge Characteristics

X-axis: Q_g, GATE CHARGE (nC)
Y-axis: V_{GS}, GATE-SOURCE VOLTAGE (V)
$I_D = 1.6A$
$V_{DS} = 5V$
10, 15
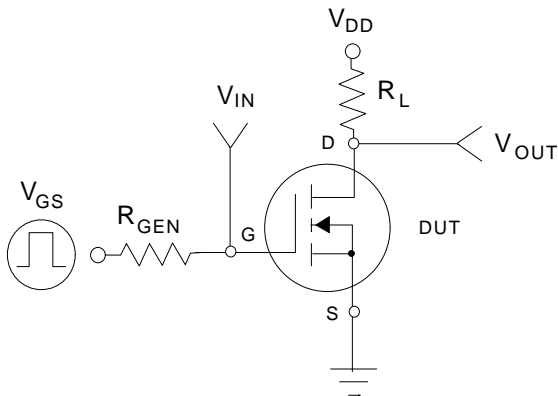
Figure 11. Switching Test Circuit

V_{DD}, V_{IN}, R_L, V_{OUT}, V_{GS}, R_{GEN}, G, D, S, DUT

Figure 12. Switching Waveforms

t_{on}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_{off}, t_f
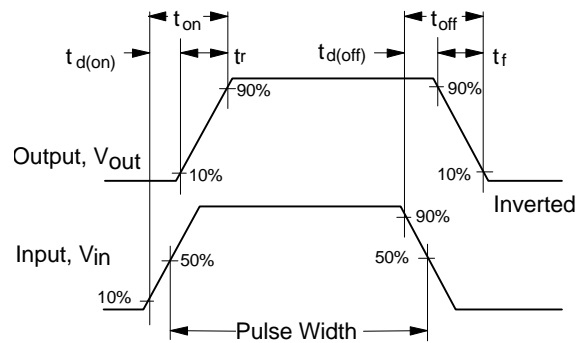Output, V_{out}, 90%, 10%, Inverted
Input, V_{in}, 90%, 50%, 10%
Pulse Width

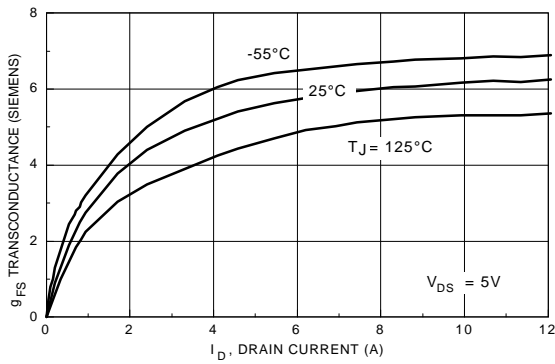## Typical Electrical Characteristics (continued)

Figure 13. Transconductance Variation with Drain Current and Temperature
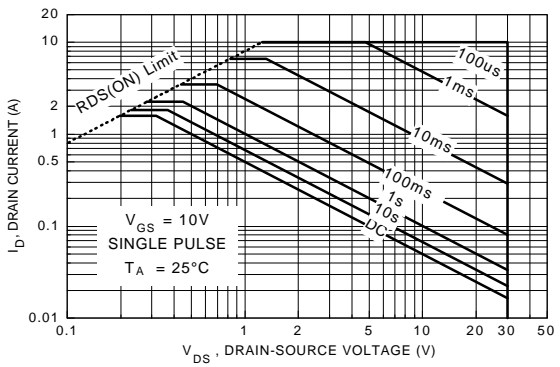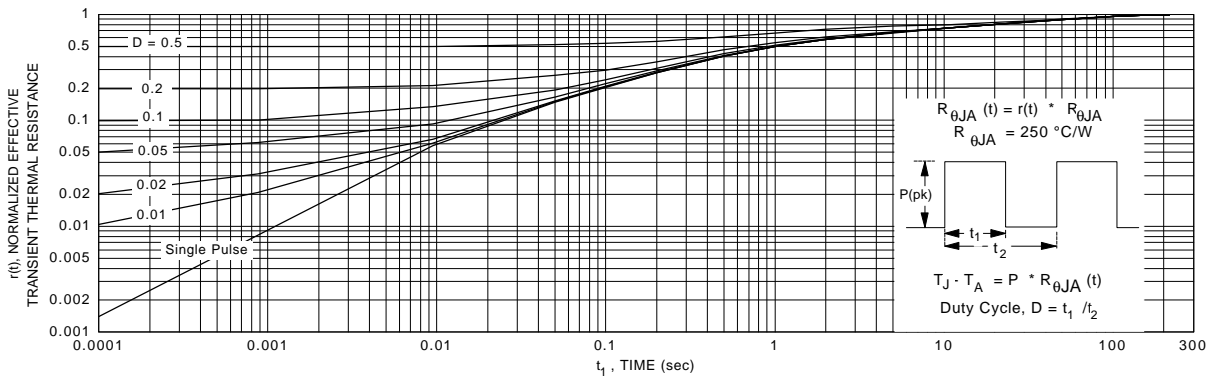

Figure 14. Maximum Safe Operating Area

Figure 15. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.