NE156QUM-NZ3

HW:V3.0

Product Specification

Rev. P0

BOE TECHNOLOGY CO.,LTD

REVISION HISTORY

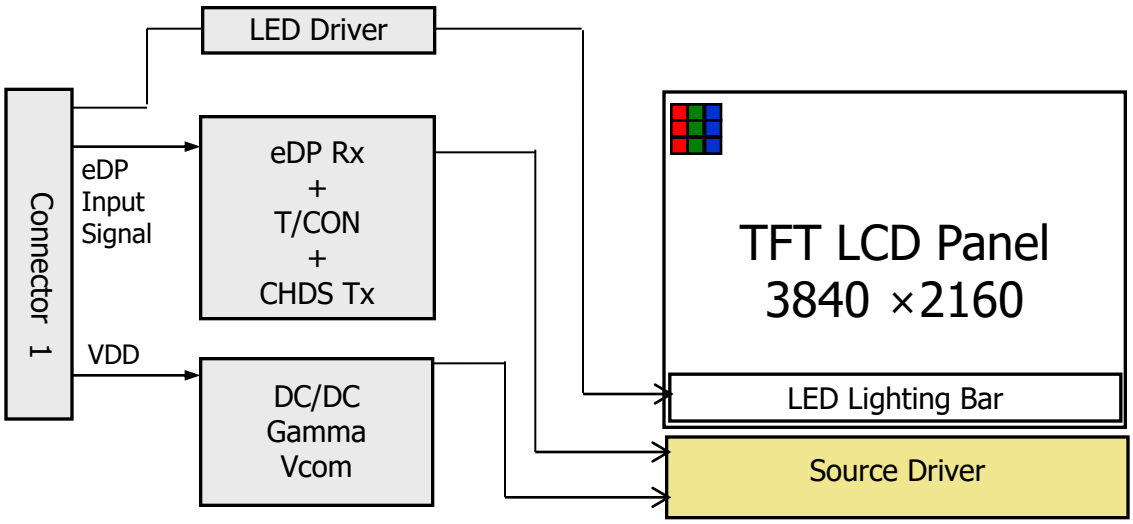
REV.	ECN No.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0	-	Initial Release	2020.04.22	李彬

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NE156QUM-NZ3 V3.0 is a color active matrix TFT LCD module using amorphous IGZO TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16,777,216 colors. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED Driver for back-light driving is built in this model.
All input signals are eDP 1.4 interface compatible.



1.2 Features

- 4 lane eDP Interface with 8.1Gbps Gbps Link Rates
- Thin and light weight
- 8-bit color depth, display 16.7M colors, color gamut 100%sRGB
- Single LED Lighting Bar. (Down side/Horizontal Direction)
- Green Product (RoHS & Halogen free product)
- On board LED Driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE156QUM-NZ3 V3.0. (listed in Table 1.)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.2176 (H) ×193.6224 (V)	mm	
Number of pixels	3840 (H) ×2160 (V)	pixels	
Pixel pitch	0.08964(H) X 0.08964 (V)	mm	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M	colors	
Color gamut	sRGB 100% Typ，95%Min		
Display mode	Normally Black		
Dimensional outline	350.66±0.3(H)*216.12±0.5(V) (W/PCB)*2.6(Max)	mm	
Weight	320 (max)	g	
Surface treatment	AG		
Surface hardness	3H		
Back-light	Lower Down side, 1-LED Lighting Bar type		Note 1
Power consumption	PD : 3.0 (max.)	W	@ mosaic 120Hz
	PBL :5.94(max)	W	
	Ptotal :8.94 (max)	W	@ mosaic

Notes : 1. LED Lighting Bar (72*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

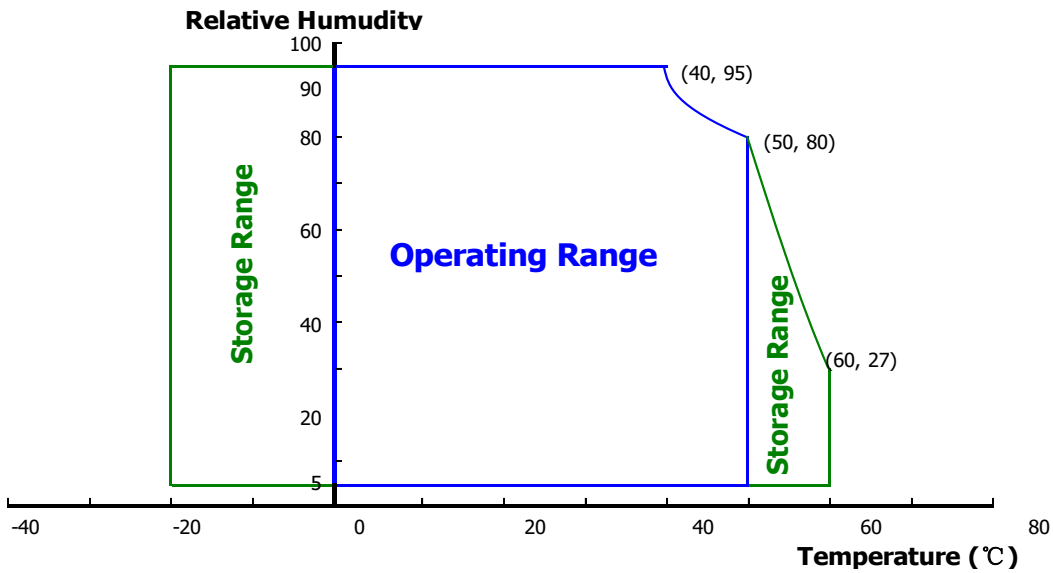
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings> Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	5.3	V	Note 1
Logic Supply Voltage	V_{IN}	V_{ss}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	℃	Note 2
Storage Temperature	T_{ST}	-20	+60	℃	

Notes : 1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 ^{O}C ≥ Ta)
Maximum wet - bulb temperature at 39 ^{O}C or less. (Ta > 40 ^{O}C) No condensation.



3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical specifications > Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	VDD	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	VRF	-	-	600	mV	@ VDD = 3.3V
Power Supply Current	IDD	-	909	-	mA	Note 1
Power Supply Inrush Current	In rush	-	-	2	A	Note3
Power Consumption	PD	-	-	3.0	W	Note 1
	PBL	-	-	5.94	W	Note 2
	Ptotal	-	-	8.94	W	Note 1

Notes :
1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 °C.
   Pattern type : Mosaic pattern
2. Calculated value for reference (VLED × ILED)
3. Measure condition (Figure 4)

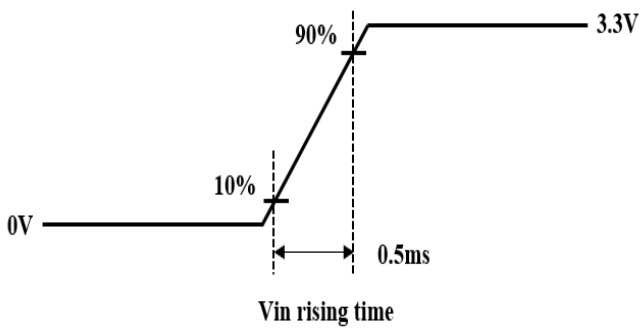


Figure 4. Inrush Measure Condition

3.2 Backlight Unit

< Table 4. LED Driving guideline specifications > Ta=25+/-2°C

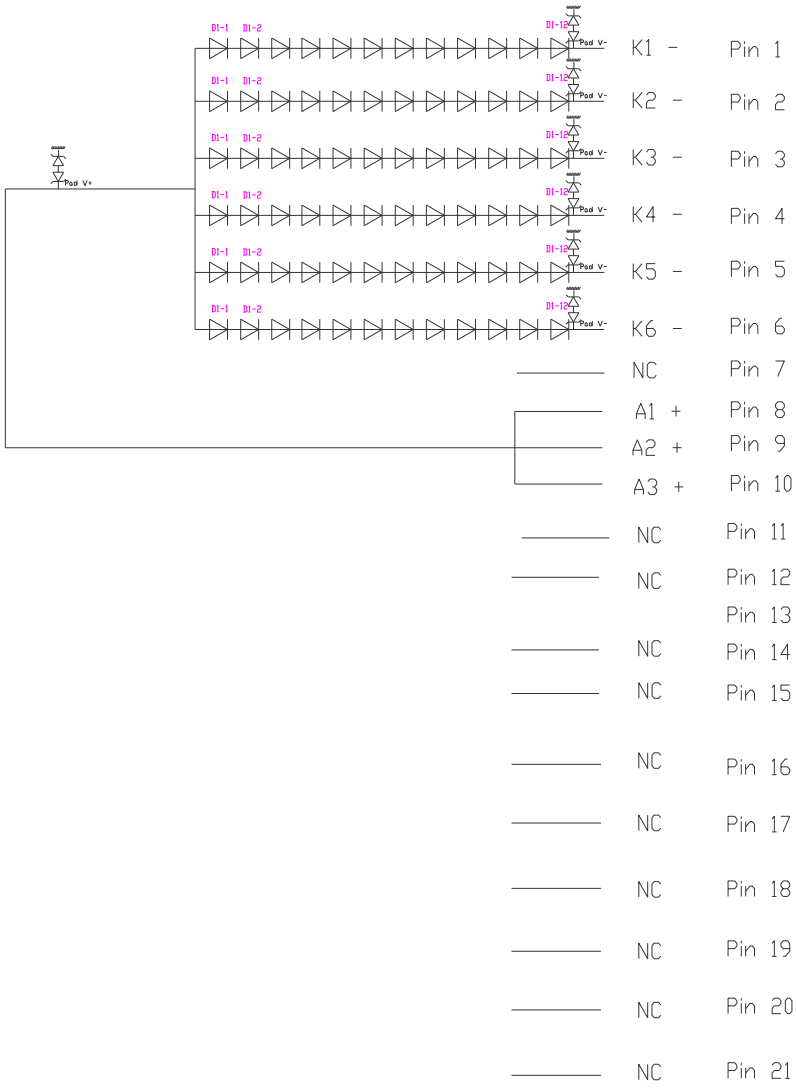
Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		VF	-	-	2.9	V	-
LED Forward Current		IF	-	24.3	-	mA	-
LED Power Input Voltage		VLED	5	12	20	V	
LED Power Input Current		ILED	-	-	404	mA	
LED Power Consumption		PLED		-	5.94	W	Note 1
LED Life-Time		N/A	15,000	-	-	Hour	IF = 20mA
Power supply voltage for LED Driver		VLED	5	12	21	V	
EN Control Level	Backlight on		2.5		5.0	V	
	Backlight off		0		1.0	V	
PWM Control Level	PWM High Level		2.5		5.0	V	
	PWM Low Level		0		0.1	V	
PWM Control Frequency		FPWM	200	-	2,000	Hz	
Duty Ratio		-	5	-	100	%	Note3

Notes : 1. Power supply voltage12V for LED Driver

Calculator Value for reference $I_F \times VF \times 72$/ efficiency = P_{LED}

2. The LED Life-time define as the estimated time to 50% degradation of initial luminous.
3. 1% duty cycle is achievable with a dimming frequency less than 1KHz.

3.3 LED structure



4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and SR3) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	900	1200			Note 2
Luminance of White	Center	Y_w	Θ = 0°	340	400	-	cd/m^2	Note 3
White Luminance uniformity	5 Points	ΔY5		80%	-	-		Note 4
	13 Points	ΔY13		65%	-	-		
White Chromaticity		x_w	Θ = 0°	0.283	0.313	0.343		Note 5
		y_w		0.299	0.329	0.359		
Reproduction of color	Red	x_R	Θ = 0°	Typ.-0.03	0.64	Typ.+0.03		
		y_R			0.33			
	Green	x_G			0.30			
		y_G			0.60			
	Blue	x_B			0.150			
		y_B			0.060			
Gamut				95	100	-	%	
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	10	15	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state .
(see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.
(see FIGURE 2 and FIGURE 3).

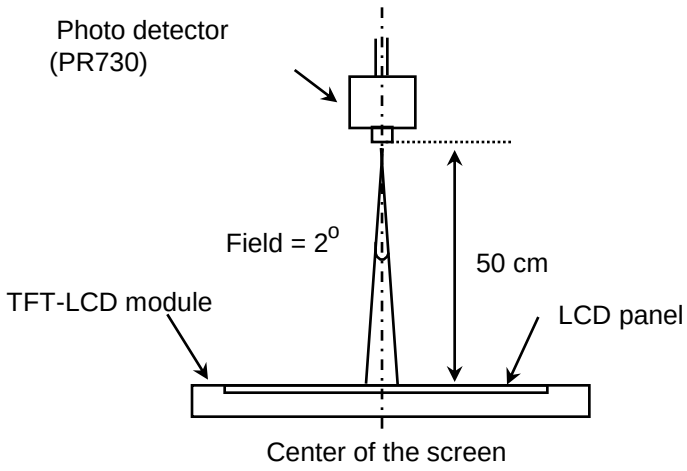
5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as FIGURE 4 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.
(See FIGURE 5).

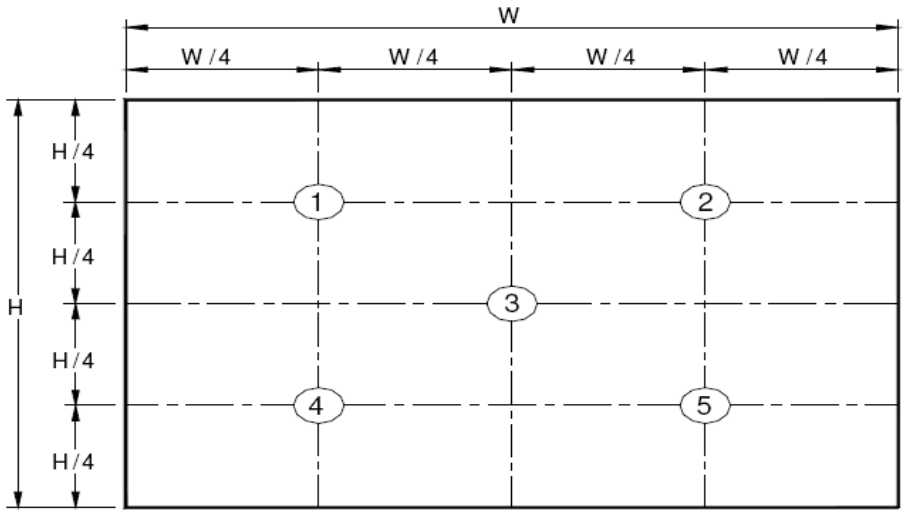
4.3 Optical measurements

Figure 1. Measurement Set Up



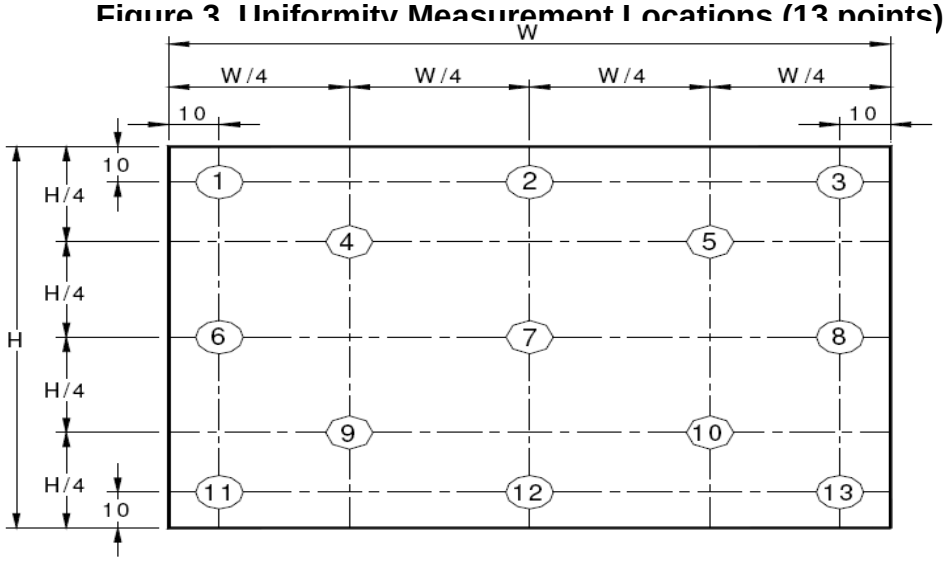
Optical characteristics measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations (5 points)



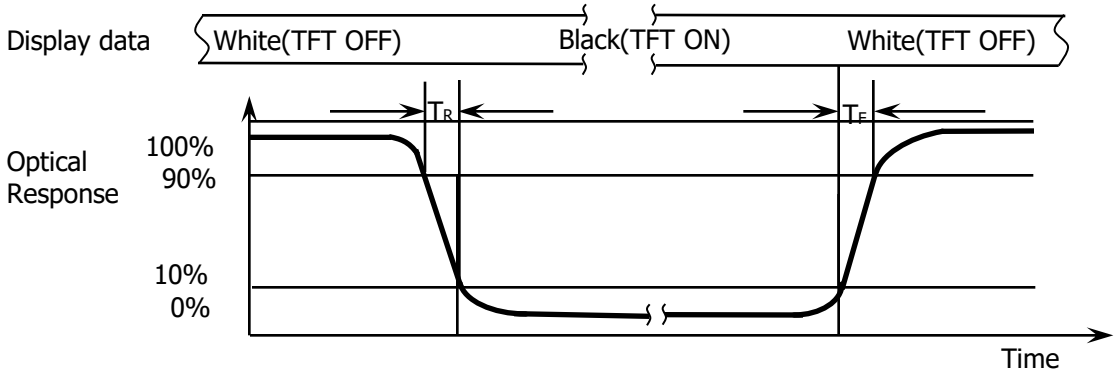
Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

Figure 3. Uniformity Measurement Locations (13 points)



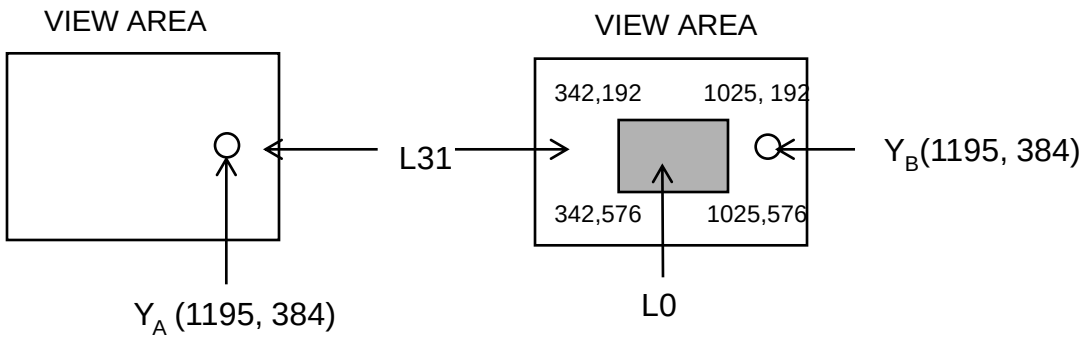
The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see FIGURE 2) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see FIGURE 3).

Figure 4. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 4 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td and 90% to 10% is Tr.

Figure 5. Cross Modulation Test Description



$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns

Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark (Refer to FIGURE 5).

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

The electronics interface connector is is IPEX 20455-040E-66.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	G-SYNC	G-SYNC
2	H_GND	Ground
3	LANE3_N	eDP RX Channel 3 Negative
4	LANE3_P	eDP RX Channel 3 Positive
5	H_GND	Ground
6	LANE2_N	eDP RX Channel 2 Negative
7	LANE2_P	eDP RX Channel 2 Positive
8	H_GND	Ground
9	LANE1_N	eDP RX Channel 1 Negative
10	LANE1_P	eDP RX Channel 1 Positive
11	H_GND	Ground
12	LANE0_N	eDP RX Channel 0 Negative
13	LANE0_P	eDP RX Channel 0 Positive
14	H_GND	Ground
15	AUX_CH_P	eDP AUX CH Positive
16	AUX_CH_N	eDP AUX CH Negative
17	H_GND	Ground
18	LCD_VCC	Power Supply, 3.3V (Typ.)
19	LCD_VCC	Power Supply, 3.3V (Typ.)
20	LCD_VCC	Power Supply, 3.3V (Typ.)

Terminal	Symbol	Functions
Pin No.	Symbol	Description
21	LCD_VCC	Power Supply, 3.3V (Typ.)
22	NC	No Connection
23	LCD GND	Ground
24	LCD GND	Ground
25	LCD GND	Ground
26	LCD GND	Ground
27	HPD	Hot Plug Detect Output
28	BL_GND	LED Ground
29	BL_GND	LED Ground
30	BL_GND	LED Ground
31	BL_GND	LED Ground
32	BL_Enable	LED Enable Pin(+3.3V Input)
33	BL_PWM	System PWM Signal Input
34	NC	No Connection
35	NC	No Connection
36	BL_PWR	LED Power Supply 5V-21V
37	BL_PWR	LED Power Supply 5V-21V
38	BL_PWR	LED Power Supply 5V-21V
39	BL_PWR	LED Power Supply 5V-21V
40	NC reserved	No Connection

5-2. eDP Interface

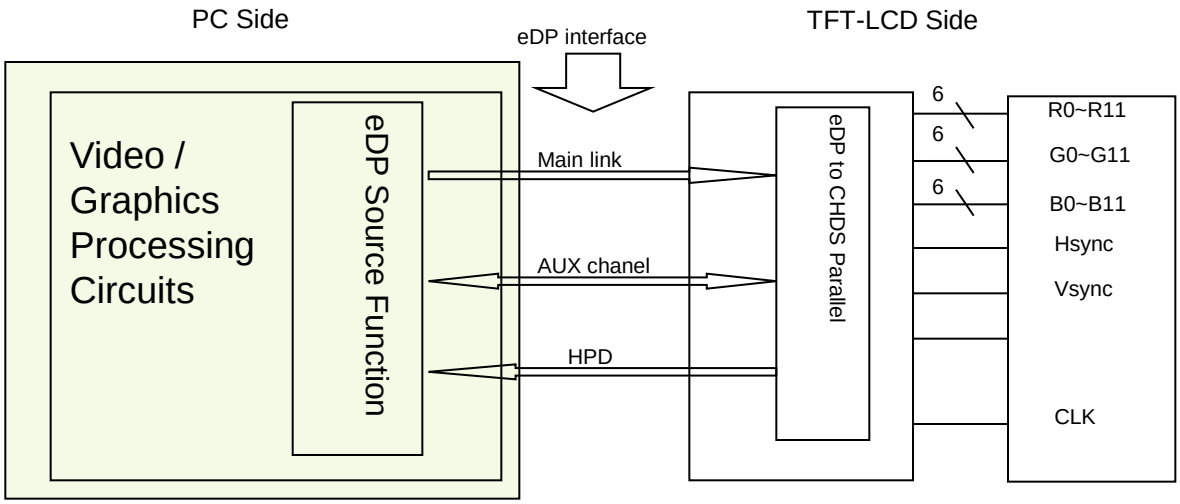


Figure 12. eDP Interface Architecture

Note:
Transmitter : NT71872.
Transmitter is not contained in module.

eDP Input signal

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

5.3 Data Input Format

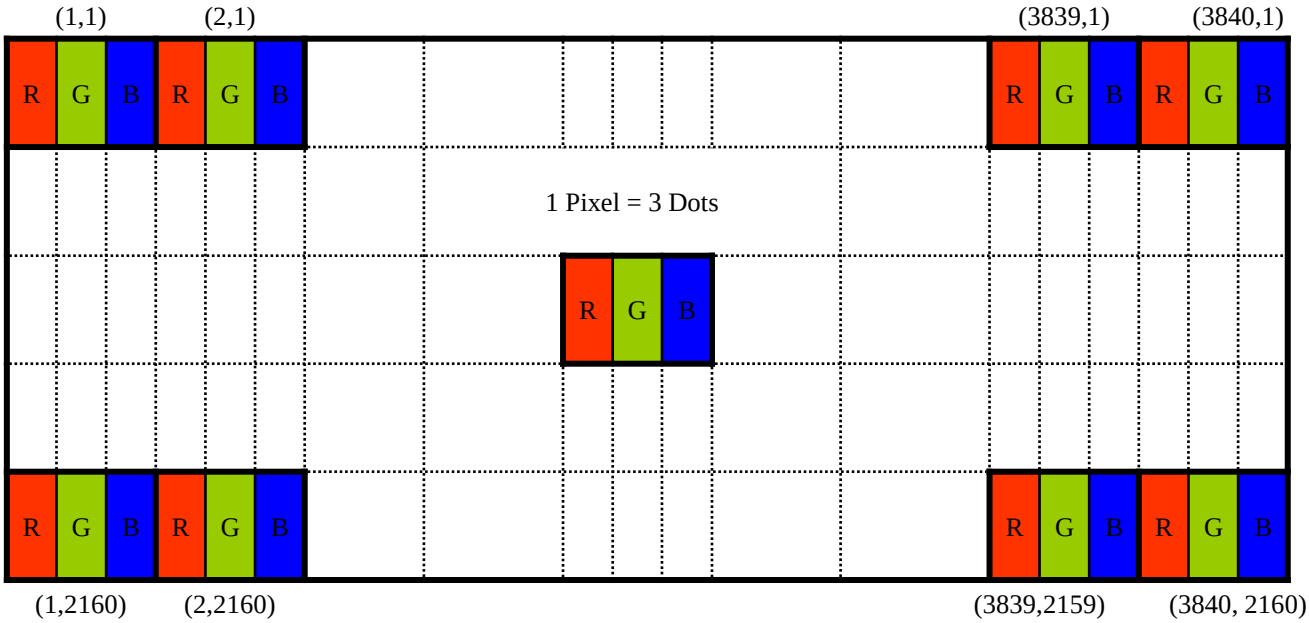


Figure 13. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector**: IPEX_20599-021E-01**.

<Table 7. Pin Assignments for the BLU & LCM Connector>

Pin No.	Symbol	Description
1	LED1-	LED1 cathode connection
2	LED2-	LED2 cathode connection
3	LED3-	LED3 cathode connection
4	LED4-	LED4 cathode connection
5	LED5-	LED5 cathode connection
6	LED6-	LED6 cathode connection
7	NC	NC
8	LED+	LED anode connection
9	LED+	LED anode connection
10	LED+	LED anode connection
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	NC
15	NC	NC
16	NC	NC
17	NC	NC
18	NC	NC
19	NC	NC
20	NC	NC
21	NC	NC

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NE156QUM-NZ3 V3.0 is operated by the DE only.

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	533.3	1066.56	-	MHz
	High Time	Tch	-	4/7	-	Tc
	Low Time	Tcl	-	3/7	-	Tc
Frame Period		Tv	-	2222	-	lines
			60	120	-	Hz
			16.7	8.33		ms
Vertical Display Period		Tvd	-	2160	-	lines
One line Scanning Period		Th	-	4000		clocks
Horizontal Display Period		Thd	-	3840	-	clocks

Note※: The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	70	-	1320	mV	
Rx input DC common mode voltage	VRX_DC_CM	-	GND	-	V	
Differential termination resistance	RRX-DIFF	80	-	100	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_INTRA_PAIR	-	-	50	ps	

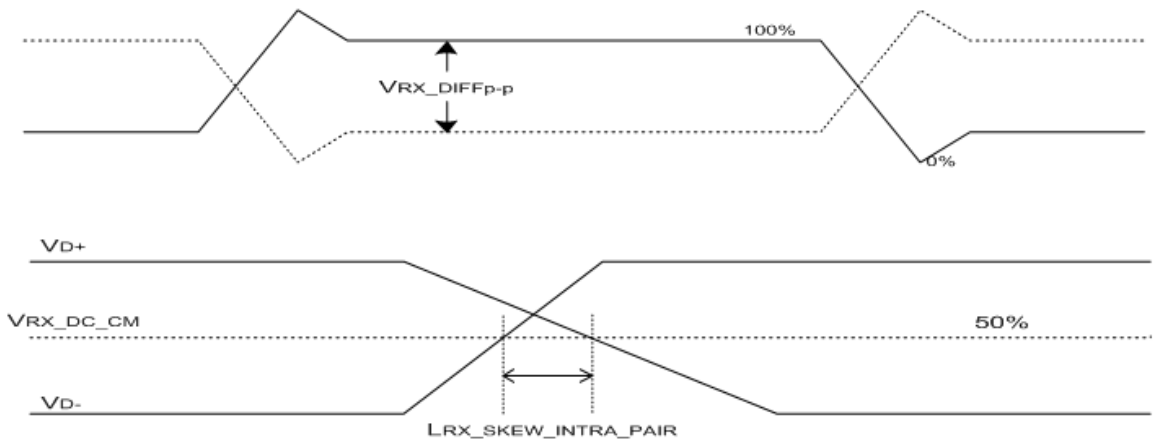


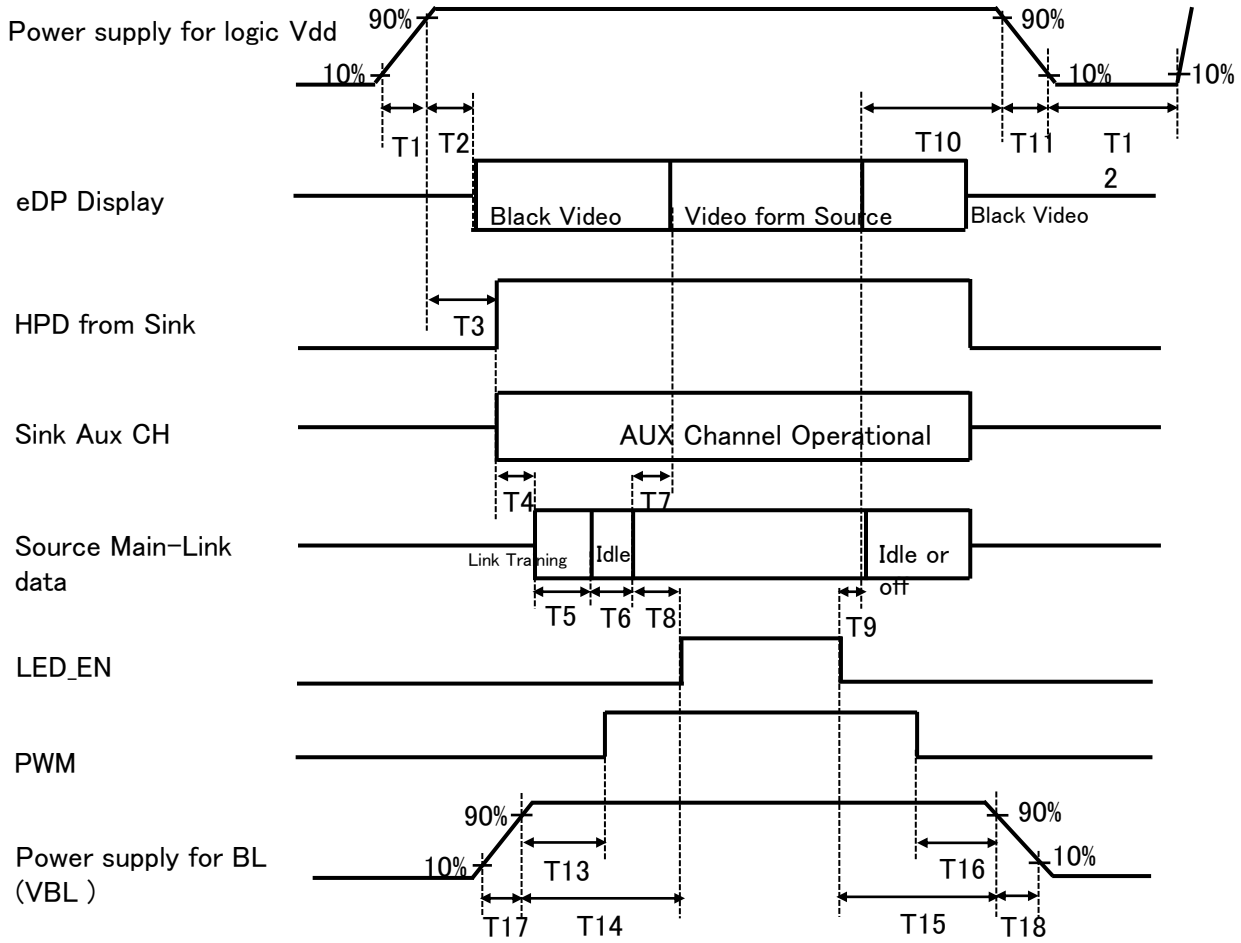
Figure 14. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off seq uence shall be as shown in below



- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T3+T4+T5+T6+T8>200ms
- 0ms < T7 ≤ 50ms
- T7 < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

Connector Name /Description	**For Signal Connector**
Manufacturer	I-PEX
Type/ Part Number	IPEX-20455-040E-66
Mating housing/ Part Number	IPEX-20455-040T or equivalent

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

FIGURE 6 shows mechanical outlines for the model NE156QUM-NZ3 V3.0.
Other parameters are shown in Table 9.

<Table 9. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.2176 (H) ×193.6224(V)	
Number of pixels	3840 (H) X 2160 (V) (1 pixel = R + G + B dots)	
Pixel pitch	0.08964 (H) X 0.08964 (V)	mm
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M	
Display mode	Normally Black	
Dimensional outline	350.66±0.3(H)*216.12±0.5(V) (W/PCB)*2.6(Max)	mm
Weight	320(Max)	gram
Back Light	Connector :IPEX-20599-021E-01	
	LED, Horizontal-LED Array type	

10.2 Mounting

See FIGURE 6.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an AG coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 10. Reliability test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240 hrs
4	High temperature operation test	Ta = 50 ℃, 240 hrs
5	Low temperature operation test	Ta = 0 ℃, 240 hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Vibration test (non-operating)	1.47Grms, 1~200Hz, Random +X, +Y, ±Z per 30min
8	Shock test (non-operating)	220G, Half Sine Wave 2msec ±X,±Y,±Z Once for each direction
9	Electro-static discharge test (non-operating)	Air : 150 pF, 340Ω, 15 KV Contact : 150 pF, 340Ω, 8 KV

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) MDL label

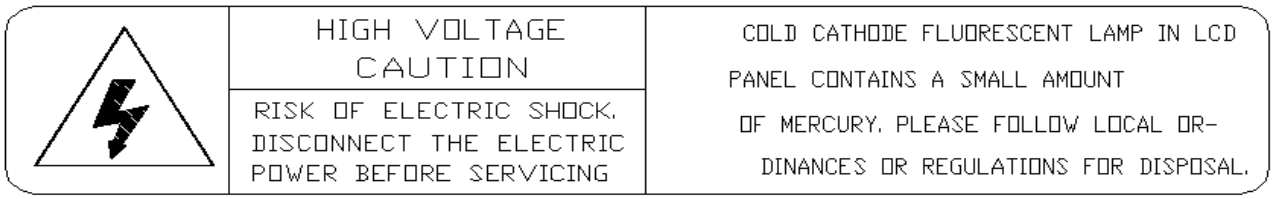
Label Size: 48mm × 12mm
1. FG-CODE: NE156QUM-NZ3 V3.0
2. MDL ID
3. Customer PPID
4. MDL ID Bar code
5. PPID QR code
6. Made In CHINA (产地)

Customer material number:L86732-LD1
A.CODE:JPDV

MDL ID code rule

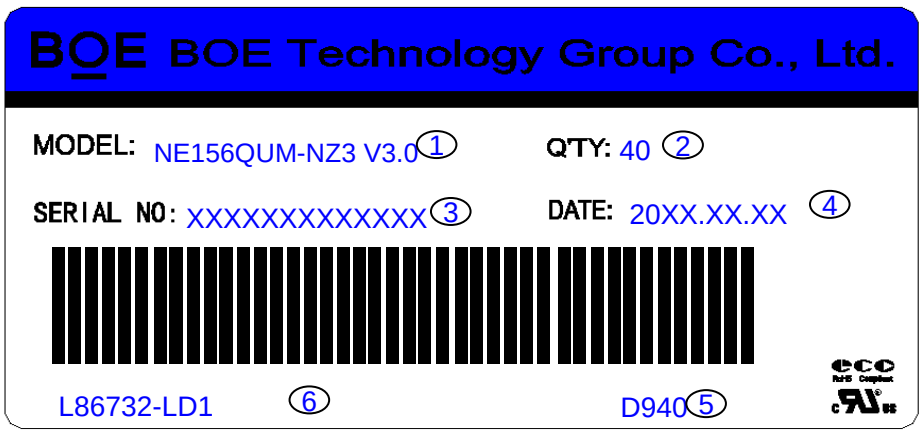
序列号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	X	X	P	3	5	2	7	X	X	X	X	0	0	1	E	E	J
描述	生管指定		等级 S,A,P,Q 等	工厂 B3	年		月	FG Code后四位				流水码 36进制(无I和O)					

(2) High voltage caution label



(3) Box label

- Label Size :115mm*80mm
- Contents
  1. FG-CODE : NE156QUM-NZ3 V3.0
  2. Box QTY
  3. Box ID,
  4. Box Packing date
  5. FG CODE four digit
  6. Customer material number



BOX ID naming rule

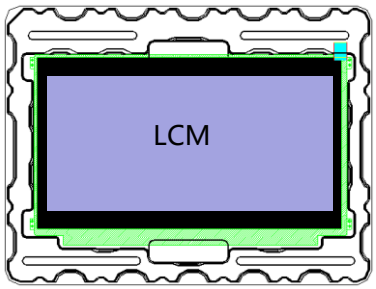
序列号	1	2	3	4	5	6	7	8	9	10	11	12	13
代码	X	X	S	3	1	5	B	0	0	0	1	H	D
描述	GBN CODE		grade	B3	year		month	Rev	Serial Number				

15.0 PACKING INFORMATION

15.1 Packing order

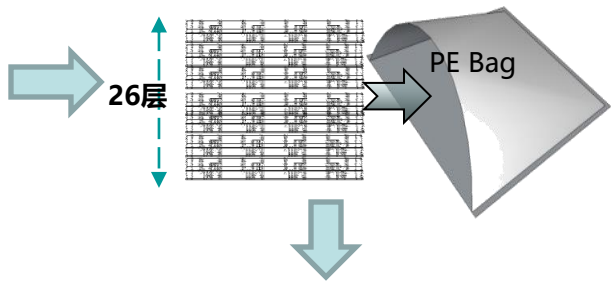
-. Put 1pcs MDL in Tray,

-. Put 1pcs EPE Spacer on MDL



-. Put 26pcs PET Tray into PE Bag

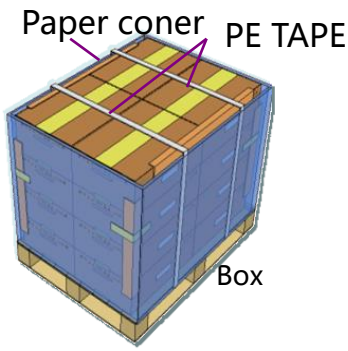
top 1pcs empty Tray



-. 3 layer Box/Pallet

4 Box/layer, total 12ea Box

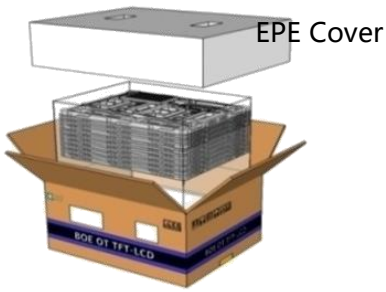
-. capicity: 300pcs/Pallet



- . Put PET Tray into Inner Box

top and bottom 1pcs EPE Cover

-. capicity：25pcs/Inner Box



15.2 Notes

- Box Dimension: 500mm(W) x 400mm(D) x 300mm(H)
- Package Quantity in one Box: 25pcs

16.0 MECHANICAL OUTLINE DIMENSION

Figure 6. TFT-LCD Module Outline Dimension (Front View)

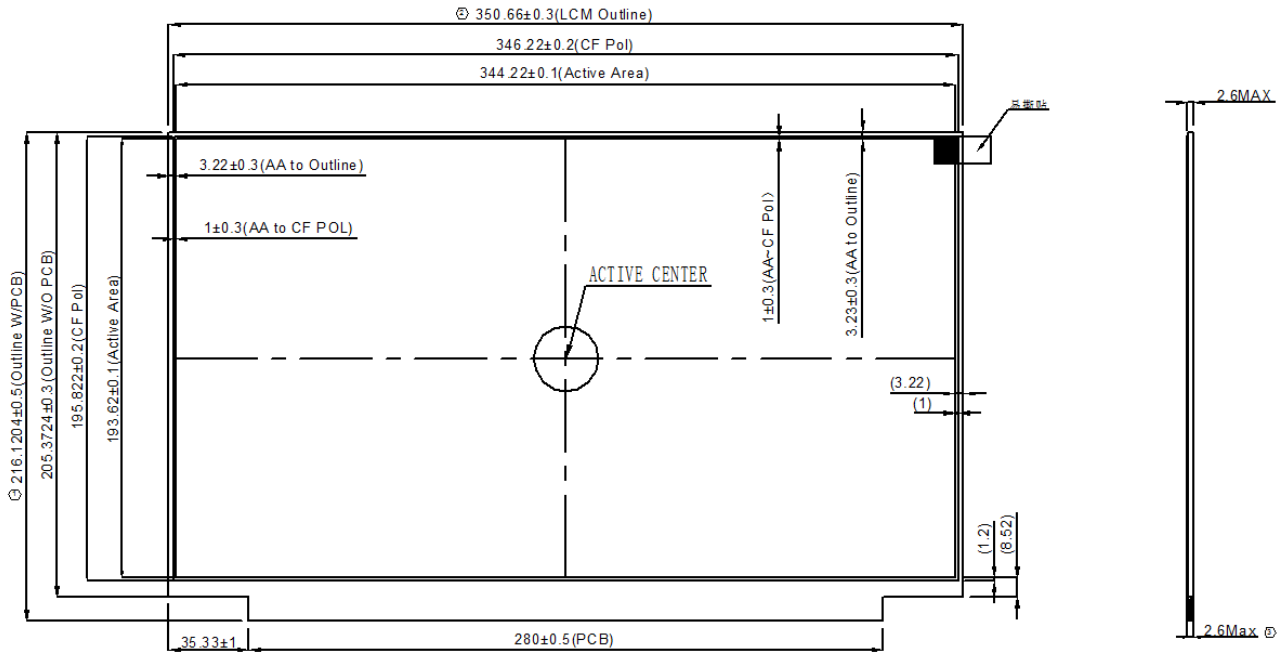
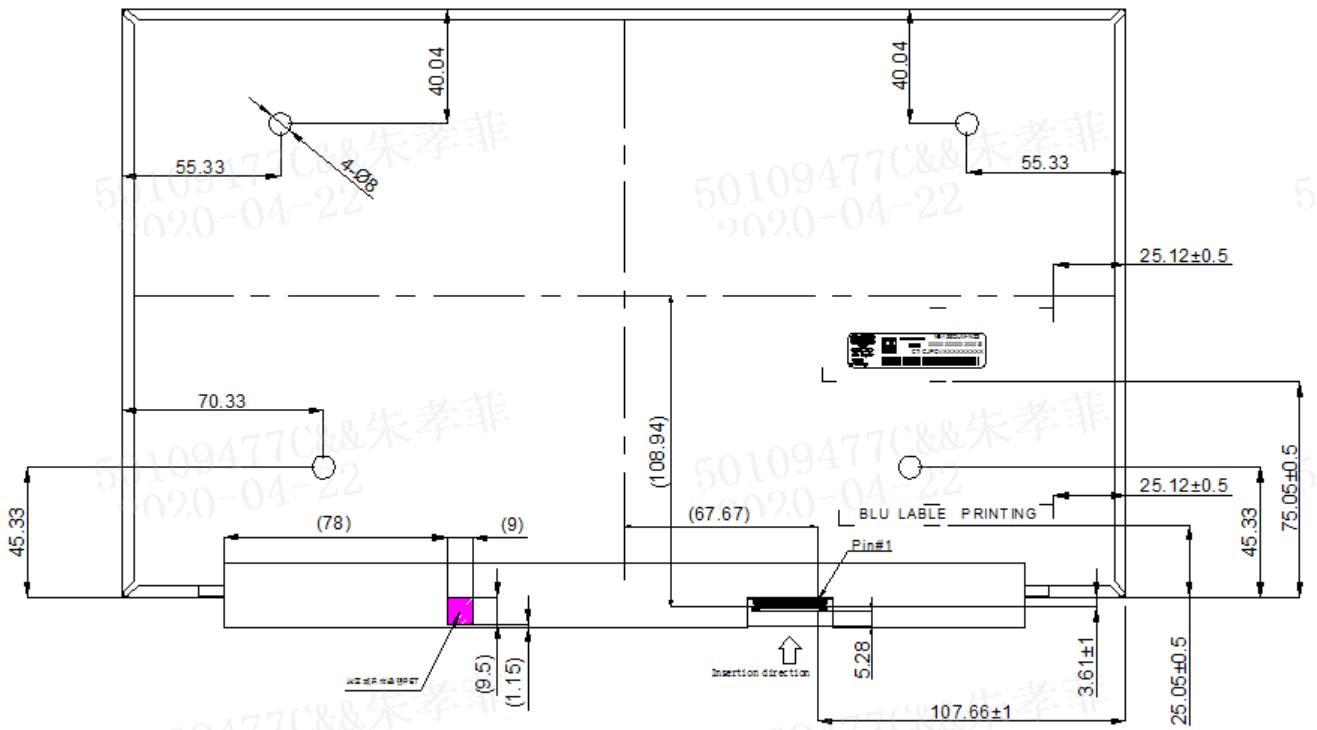


Figure 7. TFT-LCD Module Outline Dimensions (Rear view)



17.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	E0	224		2272	ID = 2272
0B		08	8			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	25	37		37	
11	Year of Manufacture	1D	29		2019	Manufactured in 2019
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	22	34		34	34.4 cm (Approx)
16	Max V image size	13	19		19	19.4 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	EE	238		-	Red / Green Low Bits
1A	Blue/White low bits	95	149		-	Blue / White Low Bits
1B	Red x high bits	A3	163	655	0.640	Red (x) = 10100011 (0.64)
1C	Red y high bits	54	84	338	0.330	Red (y) = 01010100 (0.33)
1D	Green x high bits	4C	76	307	0.300	Green (x) = 01001100 (0.3)
1E	Green y high bits	99	153	614	0.600	Green (y) = 10011001 (0.6)
1F	Blue x high bits	26	38	154	0.150	Blue (x) = 00100110 (0.15)
20	BLue y high bits	0F	15	61	0.060	Blue (y) = 00001111 (0.06)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	52	82		533.3	533.3MHz Main clock
37		D0	208			
38		00	0		3840	Hor Active = 3840
39		A0	160		160	Hor Blanking = 160
3A		F0	240		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		70	112		2160	Ver Active = 2160
3C		3E	62		62	Ver Blanking = 62
3D		80	128		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		35	53		3	V sync Offset = 3 line
41		00	0		5	V Sync Pulse width : 5 line
42		58	88		344	Horizontal Image Size = 344 mm (Low 8 bits)
43		C2	194		194	Vertical Image Size = 194 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table
48	Detailed timing/monitor descriptor #2	00	0			MHz Main clock
49		00	0			
4A		00	0			Hor Active =
4B		00	0			Hor Blanking =
4C		00	0			4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		00	0			Ver Active =
4E		00	0			Ver Blanking =
4F		00	0			4 bits of Ver. Active + 4 bits of Ver. Blanking
50		00	0			Hor Sync Offset =
51		00	0			H Sync Pulse Width =
52		00	0			V sync Offset = line
53		00	0			V Sync Pulse width : line
54		00	0			Horizontal Image Size = mm (Low 8 bits)
55		00	0			Vertical Image Size = mm (Low 8 bits)
56		00	0			4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0			Hor Border (pixels)
58		00	0			Vertical Border (Lines)
59		1A	26			Refer to right above table

5A	Detailed timing/monitor descriptor #3	00	0			Nvidia nvDPS (Refer the tab of nvDPS) Lowest refresh rate that does not cause any visual/optical side effect
5B		00	0			
5C		00	0			
5D		00	0			
5E		00	0			
5F		00	0			
60		00	0			
61		00	0			
62		00	0			
63		00	0			
64		00	0			
65		00	0			
66		00	0			
67		00	0			
68		00	0			
69		00	0			
6A		00	0			
6B		00	0			
6C	Detailed timing/monitor descriptor #4	00	0			Detailed Timing Description #4
6D		00	0			Flag
6E		00	0			Reserved
6F		02	2			For Brightness Table and Power consumption
70		00	0			Flag
71		07	7		-	PWM % [7:0] @ Step 0
72		28	40		-	PWM % [7:0] @ Step 5
73		FF	255		-	PWM % [7:0] @ step 10
74		0A	10		-	Nits [7:0] @ Step 0
75		3C	60		-	Nits [7:0] @ Step 5
76		C8	200		-	Nits [7:0] @ Step 10
77		4B	75		-	Panel Electronics Power @32x32 Chess Pattern = 3000mW
78		17	23		-	Backlight Power @60 nits = 943.411764705882mW
79		4A	74		-	Backlight Power @Step 10 = 5940mW
7A		C8	200		-	Nits @ 100% PWM Duty = 400nit
7B		00	0			Format : terminate with ASCII code 0Ah and pad field with ASCII code 20h
7C		00	0			
7D		00	0			
7E	Extension flag	01	1			0 : 1個EDID; N-1: N个EDID
7F	Checksum	**D6**	**214**	**214**	-	

80	EDID Extension Block Tag	70	112		112	
81	Display ID version	13	19		19	
82	section size	79	121		121	
83	product Type identifier	00	0		0	
84	extension count	00	0		0	
85	block tag	03	3		3	
86	block rev	01	1		1	
87	rayload	14	20		20	
88	pixel clock	A0	160		1067	1066.56MHz Main clock
89		A0	160			
8A		01	1			
8B	timing options	84	132		132	
8C	H-Active	FF	255		3840	Hor Active =3840
8D		0E	14			
8E	H-Blanking	9F	159		160	Hor Blanking =160
8F		00	0			
90	H-offset	2F	47		48	Hor Sync Offset =48
91		00	0			
92	H-sync pulse width	1F	31		32	H Sync Pulse Width =32
93		00	0			
94	V-Active	6F	111		2160	Ver Active =2160
95		08	8			
96	V-Blanking	3D	61		62	Ver Blanking =62
97		00	0			
98	V-offset	02	2		3	V sync Offset =3
99		00	0			
9A	V-sync pulse width	04	4		5	V Sync Pulse width =5
9B		00	0			
FE	Checksum(81~FD)	E3	227		-	
FF	Checksum(80~FE)	90	144			