# High-speed FSK modem receiver — NE5081

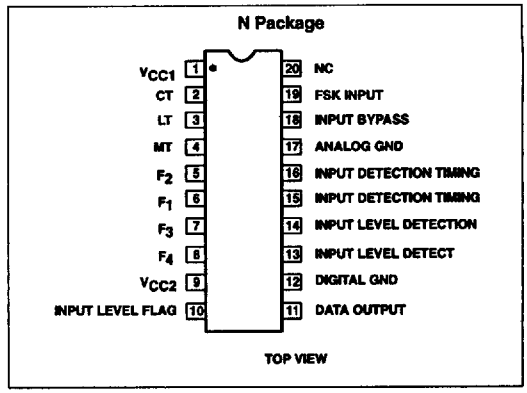
## DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies given in the 802 standard. However, the receiver will work at other frequencies.

## FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Low bit rate error ($10^{-12}$ typical)

## PIN CONFIGURATION



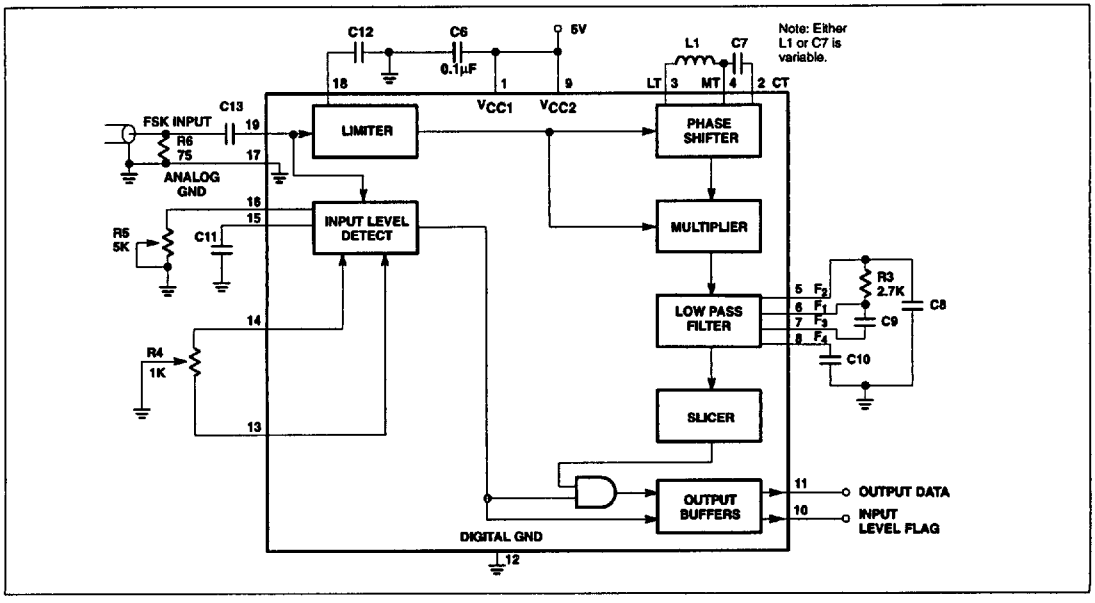

## APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|---|---|---|---|
| 20-Pin Plastic Dual In-Line Package (DIP) | 0°C to +70°C | NE5081N | 0408B |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC1}$ $V_{CC2}$ | Supply voltage | +6 | V |
| $V_{IN}$ | Input voltage range | –0.3 to +$V_{CC}$ | V |
| $I_{DO}$ | Output (Data, Level detect) Max sink current | 20 | mA |
| $P_D$ | Maximum power dissipation, $T_A$ = 25°C, (still-air)[1] N package | 1690 | mW |
| $T_A$ | Operating temperature range | 0 to +70 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_{SOLD}$ | Lead soldering temperature (10 sec. max) | 300 | °C |
| | Max differential voltage between analog and digital grounds | 100 | mV |

**NOTE:**
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1, 2}$ = 4.75–5.25V. External LC circuit tuned to 5MHz. Input level detect set at 16$mV_{RMS}$, $T_A$ = 0°C +70°C.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_0$ | Logic Low Frequency | External LC tuned to 5MHz | 3.67 | 3.75 | 3.83 | MHz |
| $f_1$ | Logic High Frequency | External LC tuned to 5MHz | 6.17 | 6.25 | 6.33 | MHz |
| $IN_{DL}$ | Minimum Input Detect Level | Minimum input level that is detected as carrier (See Note 2 in General Description) | 5 | | 50 | $mV_{RMS}$ |
| | Logic Levels: | | | | | |
| $V_{OL}$ | Data Output | $I_{OL}$ = 4.0mA $V_{IN}$ > 16$mV_{RMS}$ Freq = $f_0$ | | | 0.4 | V |
| $V_{OH}$ | Data Output | $I_{OH}$ = –400µA $V_{IN}$ > 16$mV_{RMS}$ Freq = $f_1$ | 2.4 | | | V |
| $V_{OH}$ | Data Output | $I_{OH}$ = –400µA $V_{IN}$ < 5$mV_{RMS}$ Freq = $f_0$ | 2.4 | | | V |
| $V_{OL}$ | Input Detect Flag | $I_{OL}$ = 4.0mA $V_{IN}$ = 0$V_{RMS}$ | | | 0.4 | V |
| $V_{OH}$ | | $I_{OH}$ = –400µA $V_{IN}$ > 16mV | 2.4 | | | V |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.25V ($V_{CC1}$ connected to $V_{CC2}$) $V_{IN}$ = 1.0$V_{RMS}$ Freq = $f_1$ or $f_0$ | | | 50 | mA |
| BER | Bit Error Rate | Input Signal > 16$mV_{RMS}$ maximum in-band noise = 1.6$mV_{RMS}$ | | $10^{-12}$ | $10^{-9}$ | |

## AC ELECTRICAL CHARACTERISTICS (AN195, Figure 5 with a 100KHz 1$V_{P-P}$)

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_B$ | Delay Time | Input Level Detect Flag | Input On | Figure 1 | | 0.05 | 1 | µs |
| $t_C$ | Delay Time | Input Level Detect Flag | Input Off | Figure 1 | 0.5 | 1.5 | 2.5 | µs |
| $t_D$ | Delay Time | Output Enabled | Input On | Figure 2 | | | 2 | µs |
| $t_E$ | Delay Time | Output Disabled | Input Off | Figure 2 | 0.5 | 1.5 | 2.5 | µs |
| | Required Delay | Carrier Turn Off | Valid Data End | | 2 | | | µs |

# High-speed FSK modem receiver | NE5081

## GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4—Token-Passing Single-Channel Phase-Continuous-FSK Bus—(i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from 16mV$_{RMS}$ to 1V$_{RMS}$. This can be adjusted.[2]

The receiver will yield an undetected "Bit Error Rate" of $10^{-9}$ or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

**NOTES:**

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV$_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

## FUNCTION TABLE

| PIN | FUNCTION |
|---|---|
| 1 | **$V_{CC1}$:** Should be connected to the 5V supply and Pin 9. |
| 2 | **CT:** One end of an external capacitor that is used to tune the receiver. |
| 3 | **LT:** One end of an indicator that is used to tune the receiver. |
| 4 | **MT:** The junction of the capacitor and inductor used for tuning the receiver. |
| 5 | **F2** |
| 6 | **F1** Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier |
| 7 | **F3** harmonics from the data output. |
| 8 | **F4** |
| 9 | **$V_{CC2}$:** Connect to Pin 1 (see Pin 1 function) close to the device. |
| 10 | **Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level. |
| 11 | **Data Output:** Supplies T$^2$L level data that corresponds to the FSK input received. |
| 12 | **Digital Ground:** Should be connected to digital ground. |
| 13, 14 | **Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid. |
| 15 | **Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable. |
| 16 | **Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency. |
| 17 | **Analog Ground:** Connect to analog ground close to the device. |
| 18 | **Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry. |
| 19 | **Input:** The FSK signal from the cable goes to this pin. |
| 20 | **No Connection.** |

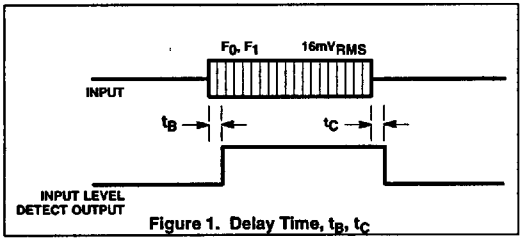



Figure 1. Delay Time, $t_B$, $t_C$

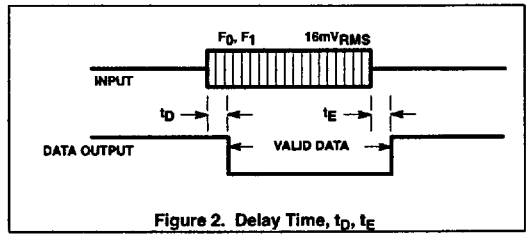



Figure 2. Delay Time, $t_D$, $t_E$