NE5240
Dolby Digital Audio Decoder

Preliminary Specification

DESCRIPTION

The NE5240 is a two channel decoder for the Dolby Digital Audio System. *The IC includes input latches to separate two channels of audio and control data, a precision internal voltage reference, and digital/analog signal processing circuitry for each channel. The IC design is implemented in a bipolar process to achieve low noise, low distortion, and wide dynamic range.

NOTE:

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and applications information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

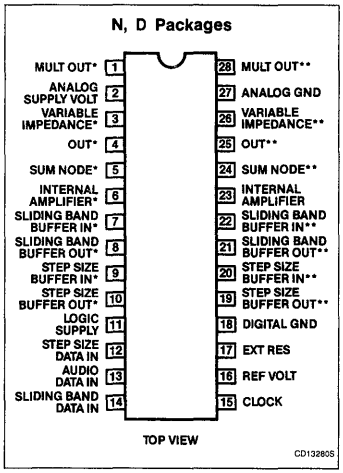
FEATURES

- **Wide dynamic range — 85dB**
- **Low distortion 0.05% @ 1kHz, −10dB**
- **TTL and CMOS compatible logic inputs**
- **Audio bandwidth — 30Hz to 15kHz**

APPLICATIONS

- **High quality digital transmission of audio data**
- **Satellite reception**
- **Cable TV**
- **Microwave distribution systems**

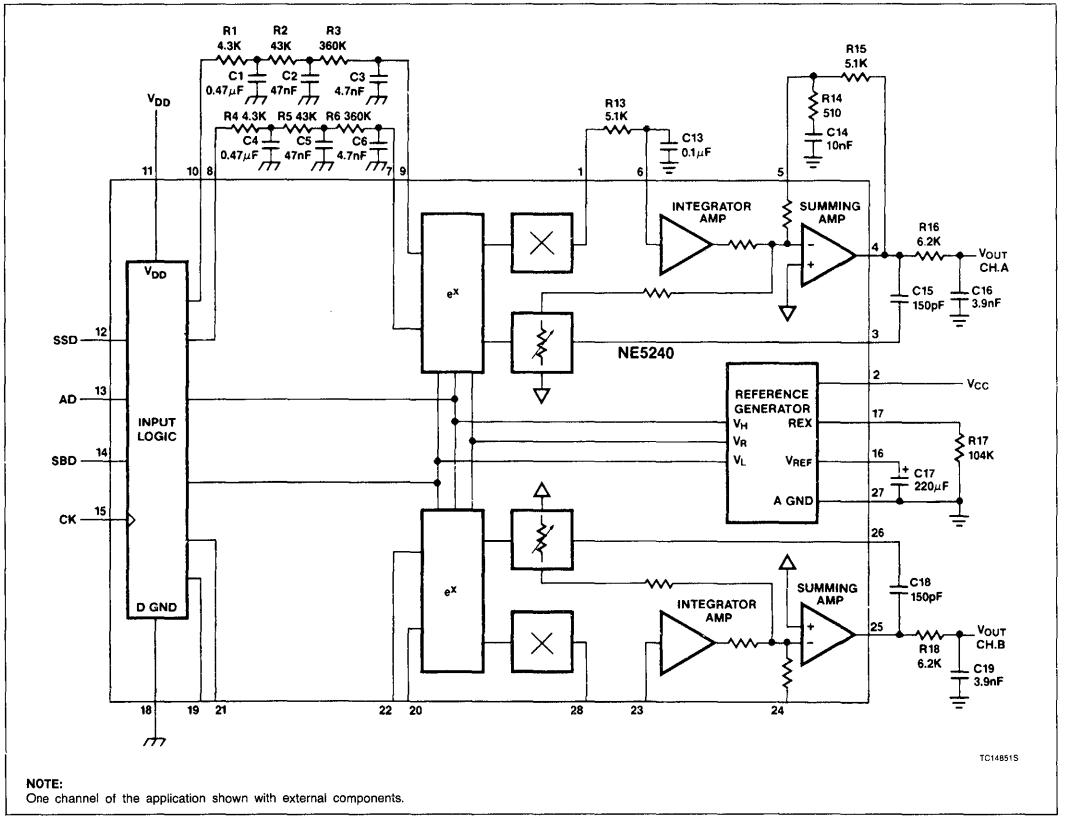
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin SO	0 to +70°C	NE5240D
28-Pin Plastic DIP	0 to +70°C	NE5240N

BLOCK DIAGRAM



NOTE:
One channel of the application shown with external components.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Analog supply voltage	+15	V
V_{DD}	Logic supply voltage	+7	V
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

All specifications are at $T_A = 25°C$, $V_{CC} = 12V$, $V_{DD} = 5V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Analog voltage supply range		10	12	14	V
V_{DD}	Logic voltage supply range		4.5	5	5.5	V
I_{CC}	Supply current	$V_{CC} = 12V$	10	24	35	mA
I_{DD}	Supply current	$V_{DD} = 5V$	5	12	18	mA
V_{IH}	Input voltage high		2		5	V
V_{IL}	Input voltage low		0		0.8	V
I_{IL}	Input current low	$V_{DD} = 4.5V$		10	100	μA
I_{IH}	Input current high			1	100	μA
t_S	Setup time		150			ns
t_H	Hold time		150			ns
I_B	Input buffers, Pins 7, 9, 20, 22	$V_{IN} = 2.0V$			100	nA
R_L	Summing amp output load		5			kΩ
V_{OS}	Output offset voltage			0.1	0.6	V
V_{OS}	Output offset change	10%-SBD-70%		±5	±20	mV
V_{REF}	Reference voltage		5.5	$0.5V_{CC}$	6.5	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS			UNIT
			Min	Typ	Max	
V_O	Full-Scale output, 0dB	f = 100Hz		1.8		V_{RMS}
	Absolute output level	f = 1kHz, SSD = 40%	93	118	150	mV_{RMS}
	Channel balance	f = 1kHz, 20%-SSD-70%	-1.5		1.5	dB
	Step-Size linearity	f = 1kHz, 20%-SSD-70%	-1.5		1.5	dB
	Step-Size linearity	f = 100Hz, SSD = 90%	-2.5		1.0	dB
f_R	Frequency response	f = 2kHz, SBD = 10%	-1.0		1.0	dB
f_R	Frequency response	f = 5kHz, SBD = 20%	-1.0		1.0	dB
f_R	Frequency response	f = 7kHz, SBD = 30%	-1.0		1.0	dB
f_R	Frequency response	f = 8kHz, SBD = 40%	-1.0		1.0	dB
f_R	Frequency response	f = 10kHz, SBD = 50%	-1.0		1.0	dB
f_R	Frequency response (all WRT 100Hz)	f = 12kHz, SBD = 60% f = 14kHz, SBD = 70%	-1.0 -1.5		1.0 1.5	dB dB
S/N	Dynamic range	SSD = 70%, CCIR/ARM	80	85		dB
THD	Harmonic distortion	f = 1kHz, -3dB		0.1	0.5	%
THD	Harmonic distortion Channel separation	f = 1kHz, -10dB f = 1kHz, 0dB	 60	0.05 75	0.2	% dB
PSRR	Power supply rejection ratio[1]	f = 1kHz		60		dB

NOTES:
1. PSRR depends on value of capacitor on Pin 16.
2. The duty cycle of SSD and SBD control data is 10%, unless otherwise noted.