NE580-F,N

DESCRIPTION

The NE580 is a dual bar-graph logic circuit designed to provide all the functions necessary to drive a gas discharge self-scan ™ bar-graph panel. The NE580 is configured to drive a 201 element bar-graph in either 5 or 6 phase operation. Phase number selection is obtained by applying a logic 0 or 1 level to the phase select pin. 3 phase operation for a 101 element device can be attained by a wire-or connection of adjacent cathode phase outputs.

The device inputs accept an analog voltage in the range 0 to 2.5V and performs an A/D conversion with reference to a fixed input voltage at the reference terminal. On-chip functions include a clock generator, linear ramp generator, control logic and ROM decoding. Output functions comprise 2 anode control lines, 2 overrange indication outputs, 6 cathode phase outputs and 1 cathode reset output. Refer to the system block diagram for clarification.

A minimum of external components are required for the whole conversion and display system shown in the typical application. The NE580 can be expanded to handle more analog channels using external comparators. Either LM393A or LM339A type comparators will function well. A few external low-cost logic packages can in addition provide binary or BCD encoded data to interface with a logic control system.

The device is supplied in a 22-pin plastic molded or ceramic dual-in-line package.

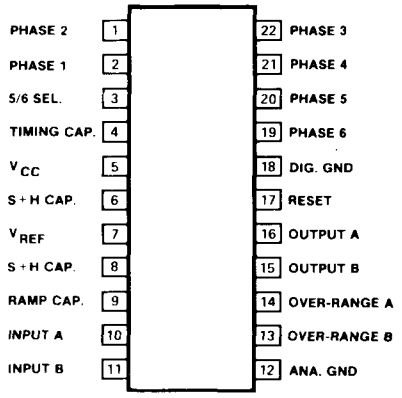
™-self-scan is a trademark of Burroughs Corporation.

FEATURES

- **Dual channel device**
- **Easily expandable to handle more channels.**
- **Single 5 volt supply**
- **3, 5 or 6 phase operation**
- **Can be custom masked for different cathode segment counts, (maximum 240)**
- **Equivalent 8-bit resolution of displayed information.**
- **Overrange indication outputs.**

PIN CONFIGURATION

F,N PACKAGE



ORDERING INFORMATION

Plastic DIL package—NE580N
Cerdip package—NE580F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+7	V
Output voltage (all outputs)	$+V_{CC}$	V
Analog input voltage range	-0.3 to +7	V
Reference voltage input	$+V_{CC}$	V
Phase select input	+5.5	V
Analog/digital ground voltage differential	±0.3	V
Power dissipation		
plastic	500	mW
cerdip*	800	mW
Operating temperature range	0 to +50	°C
Storage temperature range	-65 to +150	°C
Soldering temperature (10sec)	300	°C

*NOTE

The plastic 22 pin package has a thermal impedance θ_{JA} of 120°C/W and the cerdip package, θ_{JA} of 75°C/W. Provided the maximum junction temperature is kept below 150°C then more power may be dissipated to a maximum of 1 watt.

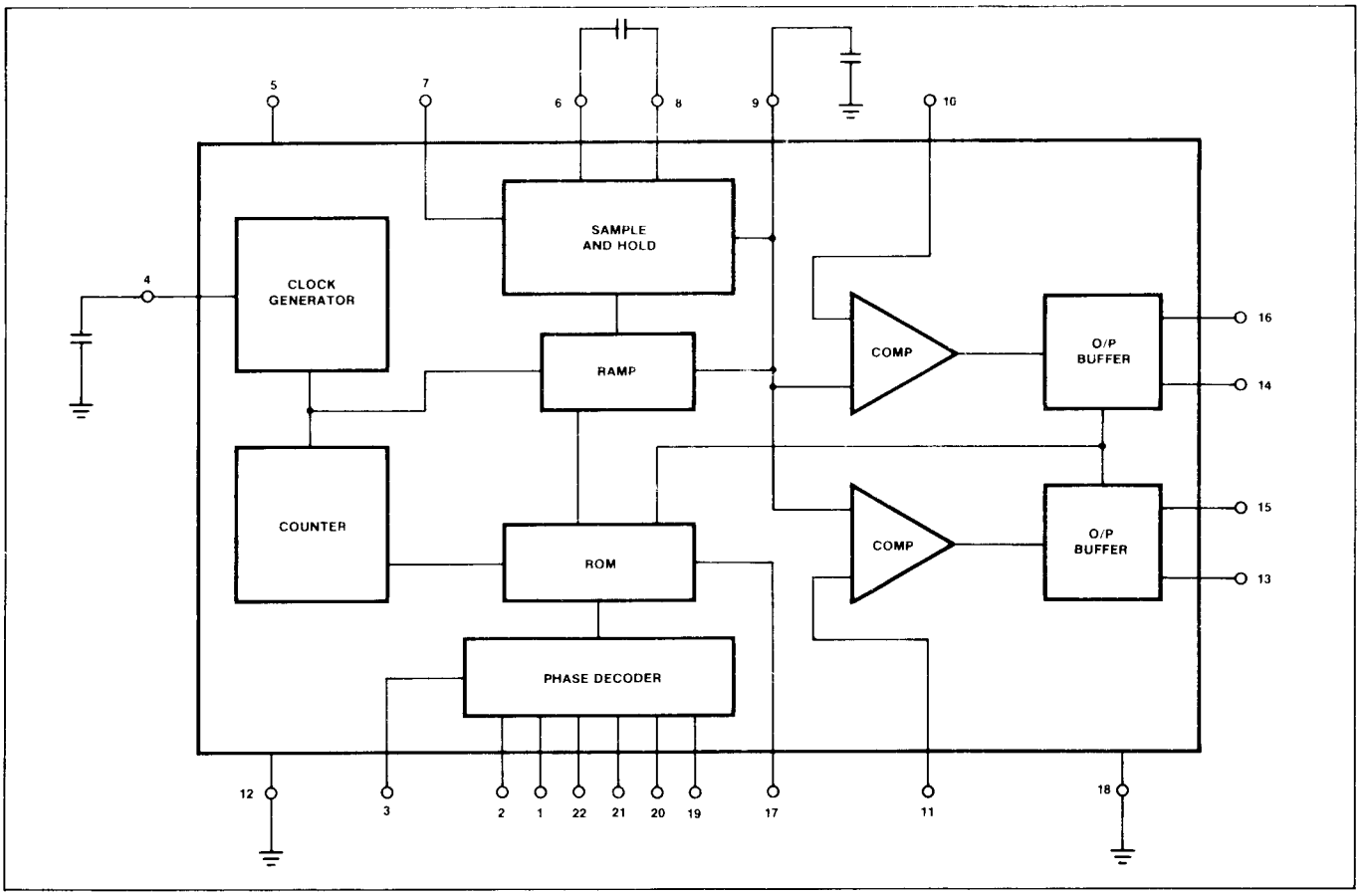
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Operating supply voltage range		4.75	5.0	5.25	V
V_{IN}	Input voltage range		0		2.5	V
V_{REF}	Applied reference voltage[1]		0		2.5	V
I_{BREF}	Bias current at reference voltage input	$V_{REF} = 2.5V$		500		nA
I_{IB}	Bias current at analog input	$V_{REF} = 2.5V$ $V_{IN} = 0V$		500		nA
$V_{OUT\ (1)}$	All outputs[2]	$I_{OUT} = -500\mu A$		3.5		V
$I_{OUT\ (1)}$	All outputs[2]	$V_{OUT} = 1.5V$		-1.0		mA
$I_{OUT\ (sc)}$	All outputs[2]	$V_{OUT} = 0_V$		-1.5		mA
$V_{OUT\ (0)}$	All outputs	$I_{SINK} = 1.6mA$			0.4	V
F_C	Clock generator frequency	Timing capacitor $= .022\mu F$		25		KHz
Accuracy		$2V \leq V_{REF} \leq 2.5V$ $V_{IN} = V_{REF}$		±1		bar
I_{CC}	Supply current			50		mA

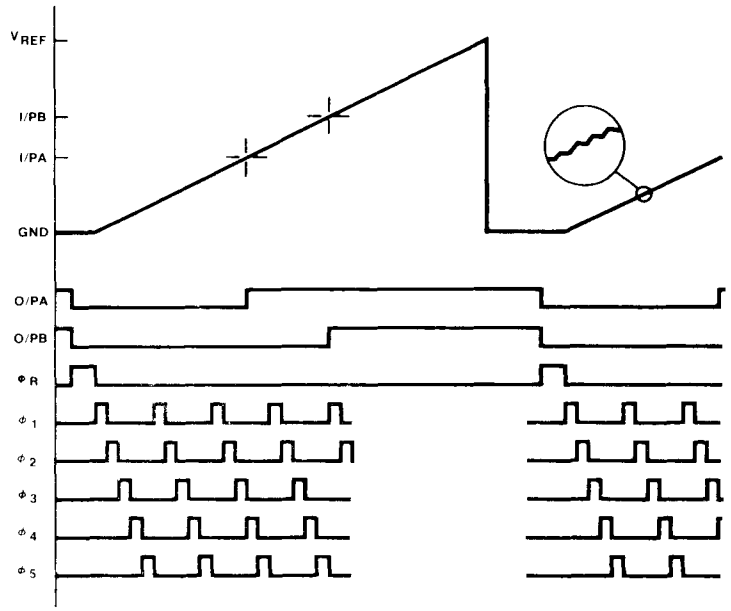
NOTES

1. Displayed accuracy is a function of reference voltage. Values of V_{REF} below 2 volts will impair conversion accuracy.
2. All logic outputs comprise an NPN transistor with 3kΩ pull-up resistor to 5 volts.

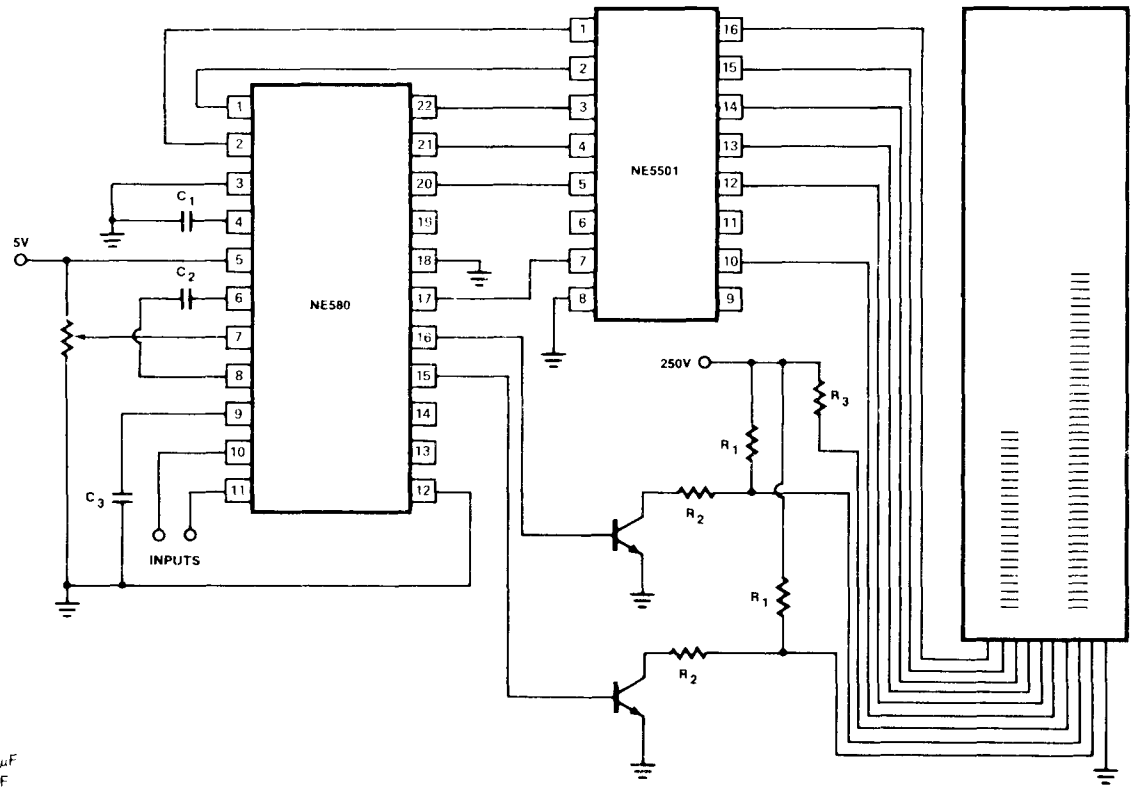
BLOCK DIAGRAM



TIMING DIAGRAM



TYPICAL APPLICATION



NOTES

R_1 = 14KΩ
R_2 = 14KΩ
R_3 = 1MΩ
C_1 = 0.022μF
C_2 = 0.47μF
C_3 = 0.47μF

Schematic shown is for a dual 5 phase 200 element bar-graph.

BAR-GRAPH SYSTEM OPERATION

The bar-graph display is a thick-film planar, gas discharge device. The principal of operation is called self-scan™, in which a neon glow-discharge is propagated from one cathode spot to another under one anode. The bar-graph device appears as a series of cathode bars arranged in a column. A glow discharge is continually propagated along the column from a keep-alive cathode at one end. Provided the scan rate for a whole column is above the eye flicker detection rate, then the glow appears as a continuous column of light.

BAR-GRAPH SIGNAL REQUIREMENTS

The NE580 comprises most of the electronic components necessary to interface an analog voltage level to the bar-graph display. Each column of the display requires an anode control signal and each cathode (usually from 4 to 7 in number) requires an interlaced logic signal of 1/N duty cycle (where N is the number of cathode phases). The pulse width of each cathode signal is of the order of 50 to 100μs. The cathode signals clock continuously throughout the frame period. The anode signal is on only for a proportion of time corresponding to the input voltage.

Thus

$$V_{IN} = V_{REF} \times \frac{T_{AN}}{200}$$

for a 200 element device, where T_{AN} is the number of cathode clock cycles for which the anode is on. Figure 2 illustrates the relative output phasing of the linear ramp cathode and anode lines for 5 phase operation.

CIRCUIT OPERATION

The NE580 provides the circuitry to generate all these signals to the point where they drive the high voltage display elements. An on-chip clock generator drives the master counter and cathode phase generator.

The clock also gates a constant current source which charges the ramp capacitor with a staircase waveform of equal increment steps. These steps correspond to the cathode segments. There are two steps per segment so that the comparison of input voltage with respect to the ramp is made at the mid-point of each segment. The master counter inhibits the current source and discharges the ramp after 200 cathode counts. At the 200th count, the ramp voltage is strobed into a sample-and-hold amplifier. This voltage is compared with the reference voltage and a signal fed back to the ramp constant current source. Hence, the maximum value of the ramp will be adjusted to the same level as the reference voltage.

The anode output goes low at the beginning of each frame and goes high again when the ramp voltage becomes greater than the input voltage. If the ramp reaches full scale before setting the anode output high, then the over-range output goes low and stays low until the end of the next frame if the input signal recovers to an in-range value. A continuing over-range signal will cause the output to go low indefinitely.

Because the ramp is the result of accumulated charge on the integrating capacitor, it is inherently monotonic; thus, each step is greater than the previous one by the expression

$$\Delta V = \frac{\Delta Q}{C}$$

Errors in the ramp can occur due to

1) Starting the ramp from a voltage other than zero. Some capacitors have a time related polarization.
2) Sag in the sampled and hold ramp voltage causing an inconstant charging current.
3) Offset errors in the sample and hold amplifier.
4) Leakage currents into or out of the ramp capacitor.

The zero starting point is achieved by using a very low offset transistor to fully discharge the ramp capacitor to within 1-5mV of ground. The maximum voltage end of the ramp is made stable by using a large value capacitor to overcome the effects of any leakage.

The classical histogram has cells which represent a nominal value plus/minus 1/2 cell width. The NE580 works in the same way. This is realized by having a clock rate which is twice the cathode switching rate, and so the staircase ramp has two steps per cathode dwell time. Each comparison step is made at the nominal cell value plus 1/2 cell, and the anode remains on (anode output low) as long as the ramp voltage is less than the input voltage.