MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NE592
SE592

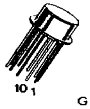
VIDEO AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

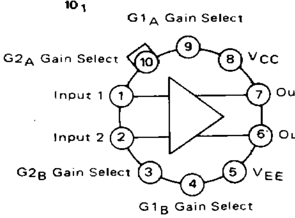
DIFFERENTIAL TWO STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

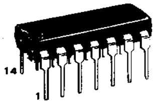
- 90 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required



H SUFFIX
METAL PACKAGE
CASE 603



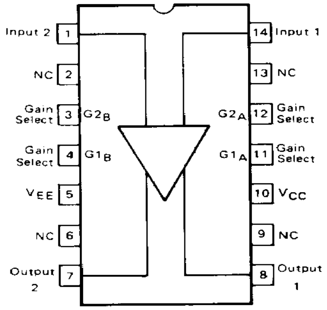
(Top View)
*Pin 5 connected to case



N SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CSE 751A
(SO-14)

PIN CONNECTIONS

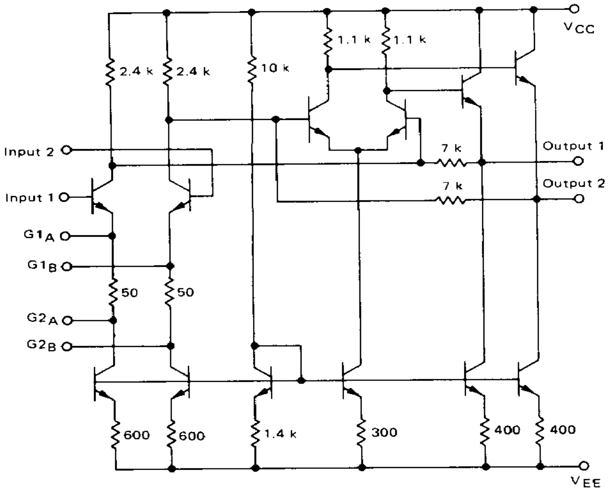


(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
NE592D NE592N NE592H	0 to 70°C	SO-14 Plastic DIP Metal Can
SE592H	−55 to +125°C	Metal Can

CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 −8.0	Volts
Differential Input Voltages	V_{ID}	±5.0	Volts
Common-Mode Input Voltage	V_{IC}	±6.0	Volts
Output Current	I_o	10	mA
Operating Ambient Temperature Range SE592 NE592	T_A	 −55 to +125 0 to +70	°C
Operating Junction Temperature Range Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C
Storage Temperature Range Metal and Ceramic Packagee Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

ELECTRICAL CHARACTERISTICS T_A **= 25°C unless otherwise noted.** (V_{CC} = +6.0 V, V_{EE} = −6.0 V, V_{CM} = 0)

Characteristic	Symbol	SE592			NE592			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain – Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p) (Gain 1, Note 1) (Gain 2, Note 2)	A_{vd}	 300 90	 400 100	 500 110	 250 80	 400 100	 600 120	V/V
Bandwidth – Figure 3 (Gain 1, Note 1) (Gain 1, Note 2)	BW	 – –	 40 90	 – –	 – –	 40 90	 – –	MHz
Rise Time – Figure 3 (Gain 1, e_{out} = 1 Vp-p, Note 1) (Gain 2, e_{out} = 1 Vp-p, Note 2)	 t_{TLH} t_{THL}	 – –	 10.5 4.5	 – 10	 – –	 10.5 4.5	 – 12	ns
Propagation Delay – Figure 3 (Gain 1, e_{out} = 1 Vp-p, Note 1) (Gain 2, e_{out} = 1 Vp-p, Note 2)	 t_{PLH} t_{PHL}	 – –	 7.5 6.0	 – 10	 – –	 7.5 6.0	 – 10	ns
Input Resistance (Gain 1, Note 1) (Gain 2, Note 2)	R_{in}	 – 20	 4.0 30	 – –	 – 10	 4.0 30	 – –	kΩ
Input Capacitance (Gain 2, Note 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current (Gain 3, Note 3) – Fig. 2	I_{IO}	–	0.4	3.0	–	0.4	5.0	μA
Input Bias Current (Gain 3, Note 3) – Fig. 2	I_{IB}	–	9.0	20	–	9.0	30	μA
Input Noise Voltage (Gain 1 and Gain 2) (BW = 1 kHz to 10 MHz) – Figure 1	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range (Gain 2, Note 2) – Fig. 3	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio – Figure 3 (Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz) (Gain 2, V_{CM} = ±1 V, f = 5 MHz)	CMRR	 60 –	 86 60	 – –	 60 –	 86 60	 – –	dB
Supply Voltage Rejection Ratio – Figure 2 (Gain 2, ΔV_s = ±0.5 V)	PSRR	50	70	–	50	70	–	dB
Output Offset Voltage – Figure 2 (Gain 3, R_L = ∞, Note 3)	V_{OO}	–	0.35	0.75	–	0.35	0.75	V
Output Common-Mode Voltage – Figure 2 (R_L = ∞, Gain 3, Note 3)	V_{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing – Figure 3 (R_L = 2k, Gain 2, Note 2)	V_O	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Resistance	r_o	–	20	–	–	20	–	Ω
Power Supply Current – Figure 2 (R_L = ∞, Gain 2, Note 2)	I_D	–	18	24	–	18	24	mA

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.
Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.
Note 3. All gain select pins open.

ELECTRICAL CHARACTERISTICS $T_A = T_{high}$ to T_{low} unless otherwise noted.* (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, V_{CM} = 0)

Characteristic	Symbol	SE592			NE592			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain – Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p)	A_{vd}							V/V
(Gain 1, Note 1)		200	–	600	250	–	600	
(Gain 2, Note 2)		80	–	120	80	–	120	
Input Resistance (Gain 2)	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3) – Figure 2	$\lvert I_{IO} \rvert$	–	–	5.0	–	–	6.0	μA
Input Bias Current (Gain 3) – Figure 2	I_{IB}	–	–	40	–	–	40	μA
Input Voltage Range (Gain 2) – Figure 3	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio – Figure 3 (Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio – Figure 2 (Gain 2, ΔV_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage (Gain 3) – Figure 2	V_{OO}	–	–	1.2	–	–	1.5	V
Output Voltage Swing (Gain 2) – Figure 3	V_O	2.5	–	–	2.5	–	–	Vp-p
Power Supply Current (Gain 2) – Figure 2	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for NE592, -55°C for SE592
T_{high} = +70°C for NE592, +125°C for SE592

GENERAL TEST CIRCUITS

FIGURE 1

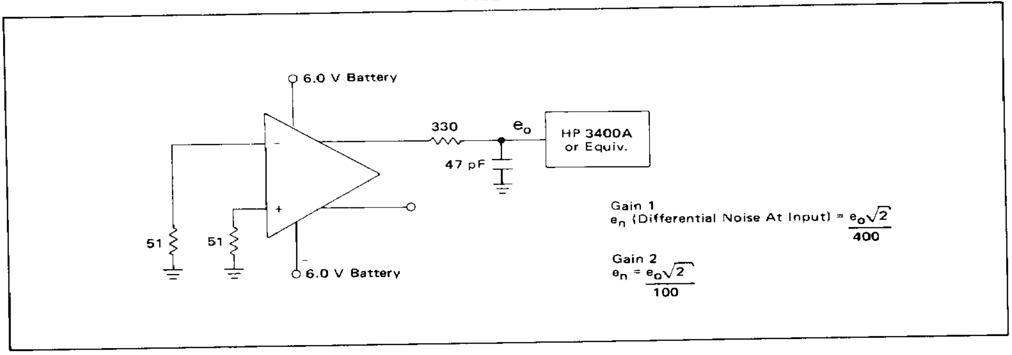


FIGURE 2

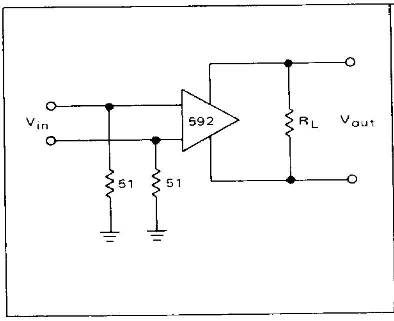


FIGURE 3

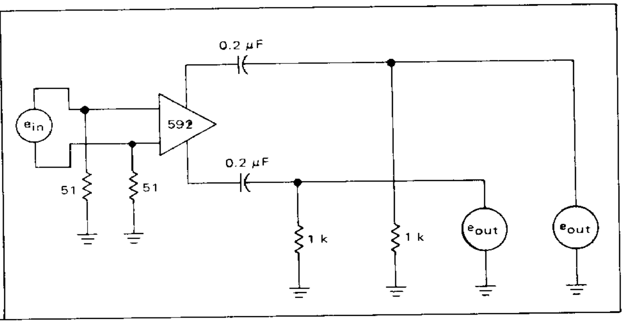


FIGURE 4 — GAIN 1 versus FREQUENCY

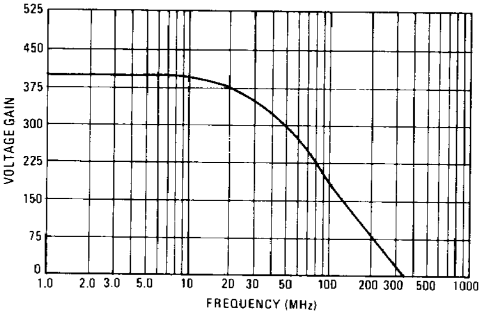


FIGURE 5 — GAIN 2 versus FREQUENCY

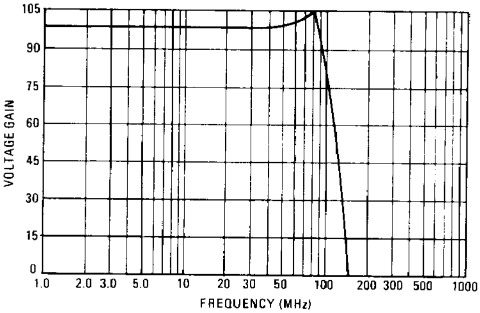


FIGURE 6 — OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

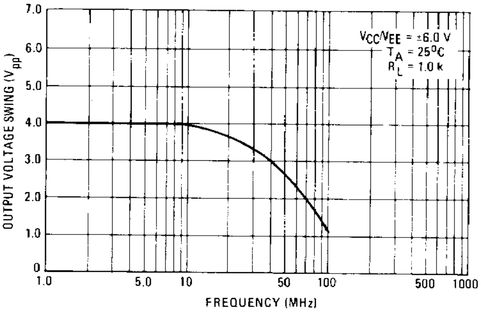


FIGURE 7 — OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

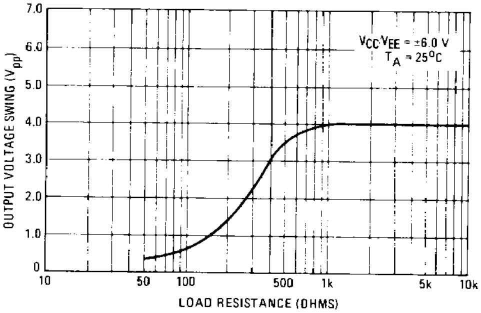


FIGURE 8 — VOLTAGE GAIN AS A FUNCTION OF R_{adj} RESISTANCE

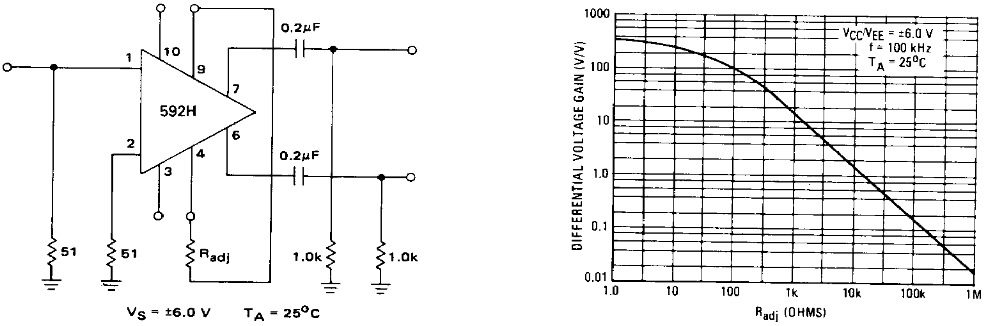


FIGURE 9 – DISK/TAPE PHASE MODULATED READBACK SYSTEMS

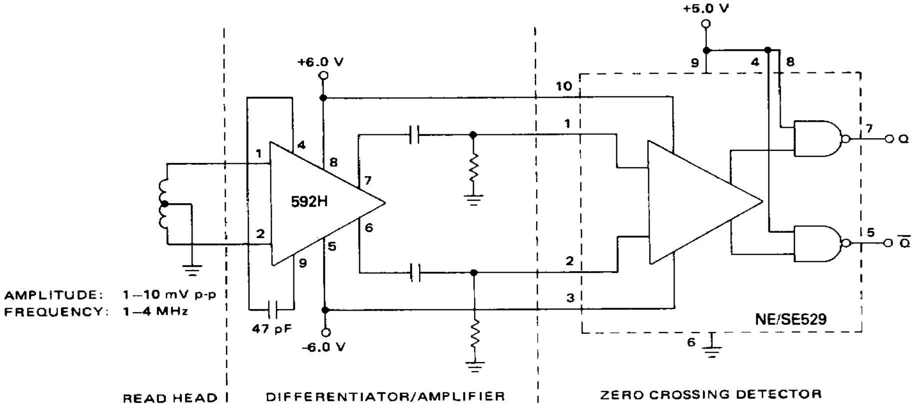
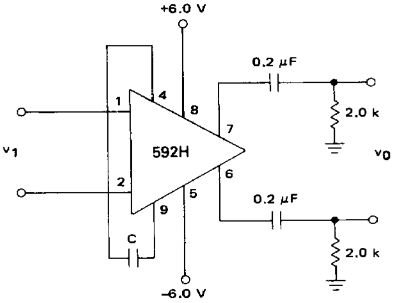


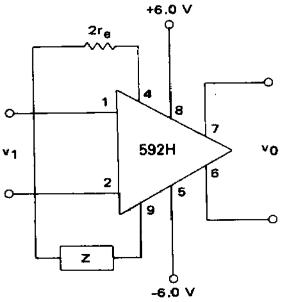
FIGURE 10 – DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $f_1 << 1/2\pi(32)C$

$$v_O \cong 1.4 \times 10^4 C \frac{dv_1}{dt}$$

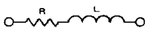
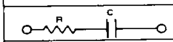
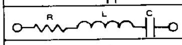
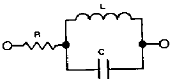
FIGURE 11 – FILTER NETWORKS



$$\frac{v_O(s)}{v_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$\frac{v_O(s)}{v_1(s)}$ TRANSFER FUNCTION
	Low Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	High Pass	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	Band Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
	Band Reject	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 30 Ohms.