Video amplifier — NE592

DESCRIPTION

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

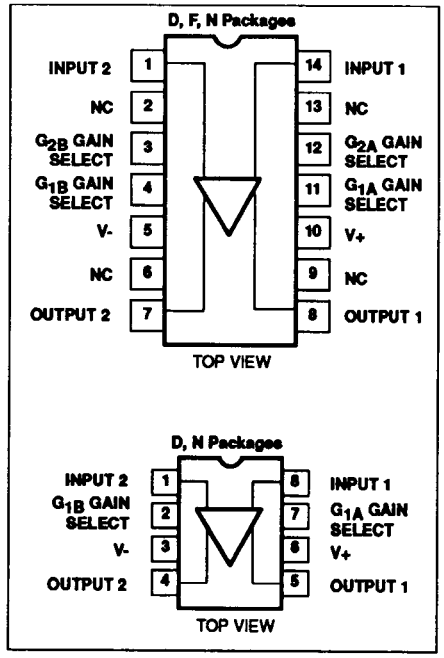
FEATURES

- 120MHz unity gain bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components
- MIL-STD processing available

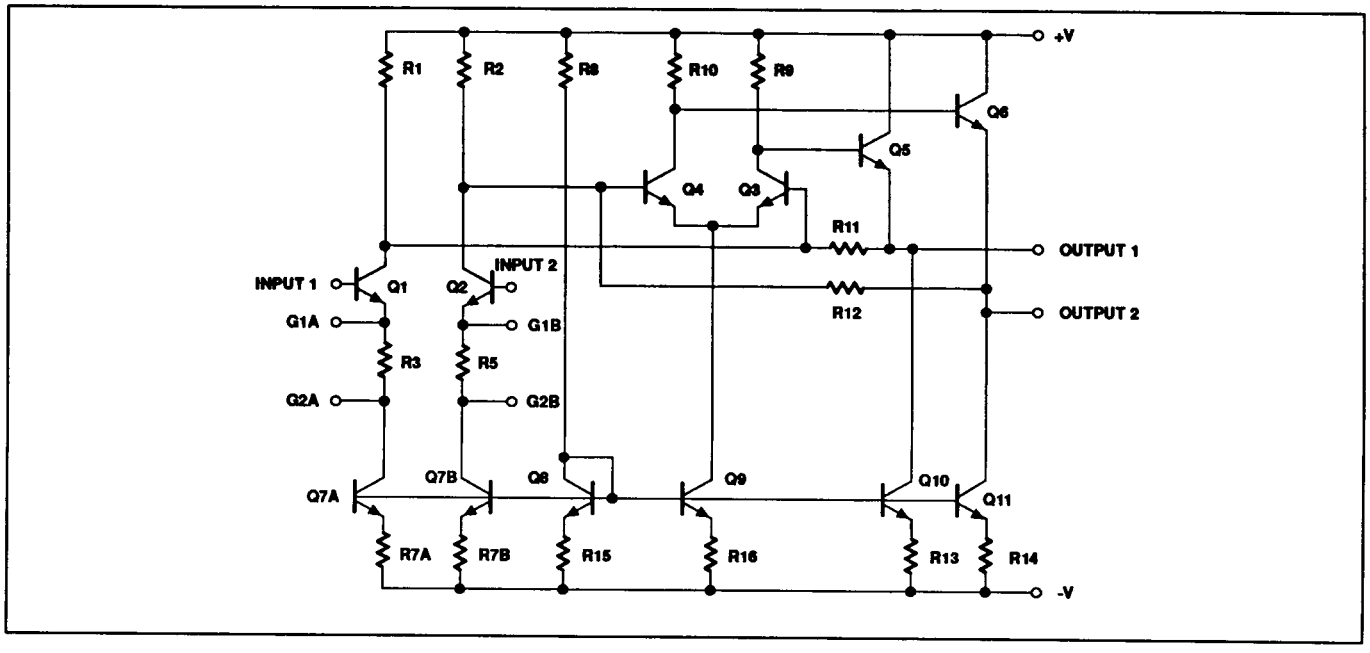
APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic DIP	0 to +70°C	NE592N14	0405
14-Pin Cerdip	0 to +70°C	NE592F14	0581
14-Pin SO	0 to +70°C	NE592D14	0175
8-Pin Plastic DIP	0 to +70°C	NE592N8	0404
8-Pin SO	0 to +70°C	NE592D8	0174

NOTES:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HDB

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\,MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	F-14 package	1.17	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTES:
2. Derate above 25°C at the following rates:
   F-14 package at 9.3mW/°C
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=+6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=+6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250	400	600	V/V
	Gain 2[2,4]		80	100	120	V/V
	High gain part		400	500	600	V/V
R_{IN}	Input resistance					
	Gain 1[1]			4.0		kΩ
	Gain 2[2,4]		10	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0		pF
I_{OS}	Input offset current			0.4	5.0	μA
I_{BIAS}	Input bias current			9.0	30	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	60	86		dB
	Gain 2[4]	V_{CM}±1V, f=5MHz		60		dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50	70		dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]	R_L=∞			1.5	V
	Gain 3[3]	R_L=∞		0.35	0.75	V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current	R_L=∞		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics V_{SS}=±6V, V_{CM}=0, 0°C ≤T_A≤70°C, unless otherwise specified. Recommended operating supply voltages V_S=+6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250		600	V/V
	Gain 2[2,4]		80		120	V/V
	High gain part		400	500	600	V/V
R_{IN}	Input resistance					
	Gain 2[2,4]		8.0			kΩ
I_{OS}	Input offset current				6.0	µA
I_{BIAS}	Input bias current				40	µA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	50			dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV$_S$=±0.5V	50			dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]				1.5	
	Gain 3[3]				1.0	
V_{OUT}	Output voltage swing differential	R_L=2kΩ	2.8			V
I_{CC}	Power supply current	R_L=∞			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

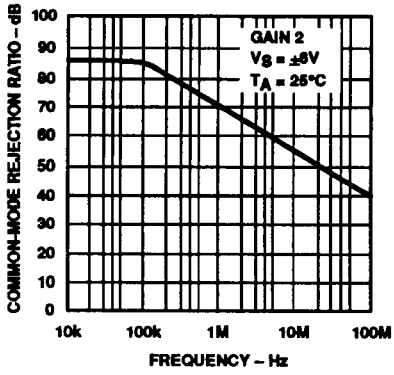
T_A=+25°C V_{SS}=+6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
BW	Bandwidth					
	Gain 1[1]			40		MHz
	Gain 2[2,4]			90		MHz
t_R	Rise time					
	Gain 1[1]	V_{OUT}=1V_{P-P}		10.5	12	ns
	Gain 2[2,4]			4.5		ns
t_{PD}	Propagation delay					
	Gain 1[1]	V_{OUT}=1V_{P-P}		7.5	10	ns
	Gain 2[2,4]			6.0		ns

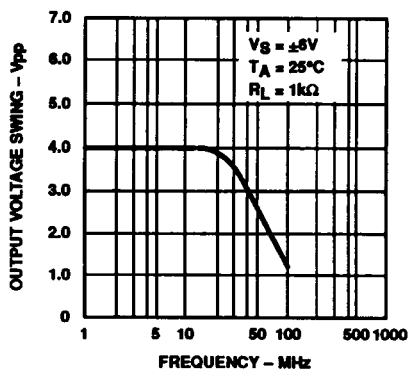
NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

TYPICAL PERFORMANCE CHARACTERISTICS

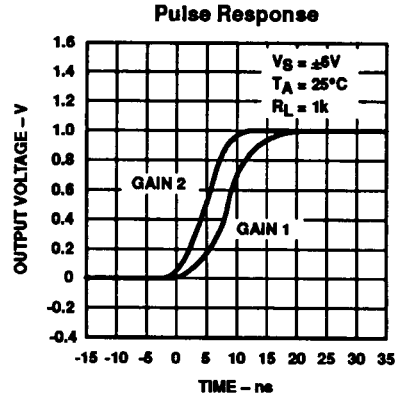
Common-Mode Rejection Ratio as a Function of Frequency



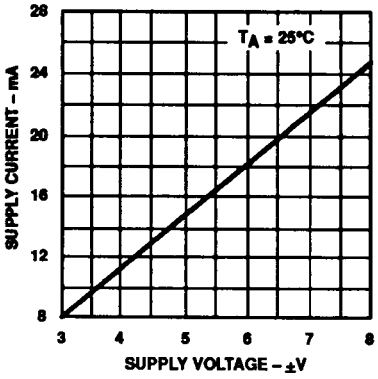
Output Voltage Swing as a Function of Frequency



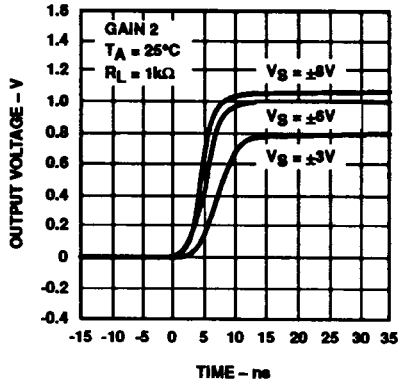
Pulse Response



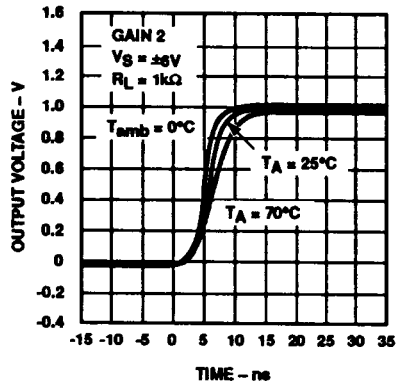
Differential Overdrive Recovery Time



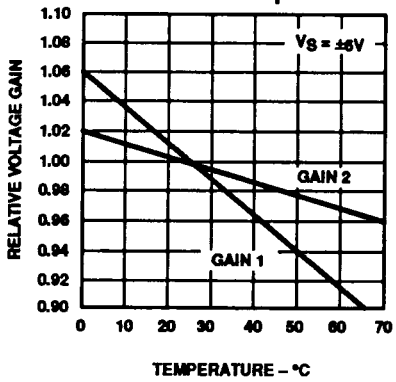
Pulse Response as a Function of Supply Voltage



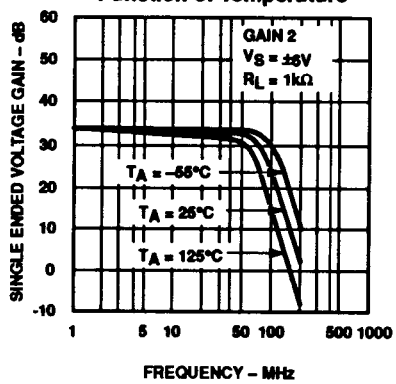
Pulse Response as a Function of Temperature



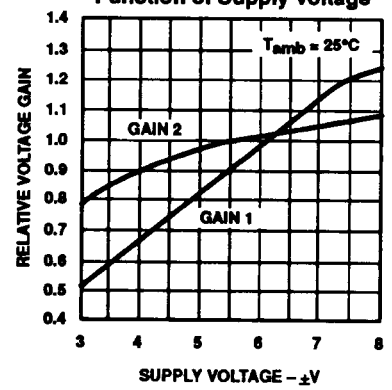
Voltage Gain as a Function of Temperature



Gain vs. Frequency as a Function of Temperature

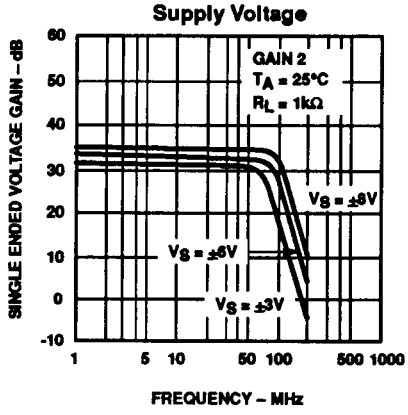


Voltage Gain as a Function of Supply Voltage

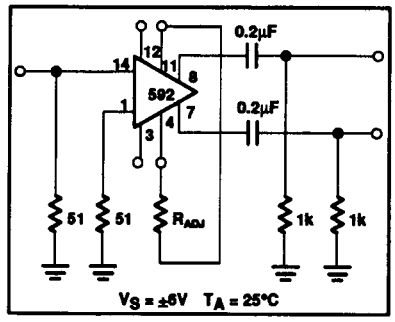


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

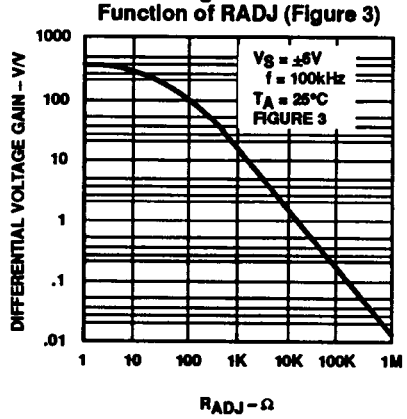
Gain vs. Frequency as a Function of Supply Voltage



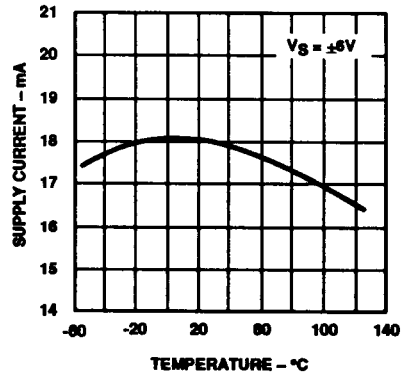
Voltage Gain Adjust Circuit



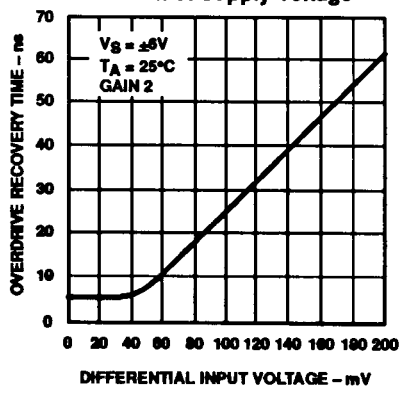
Voltage Gain as a Function of RADJ (Figure 3)



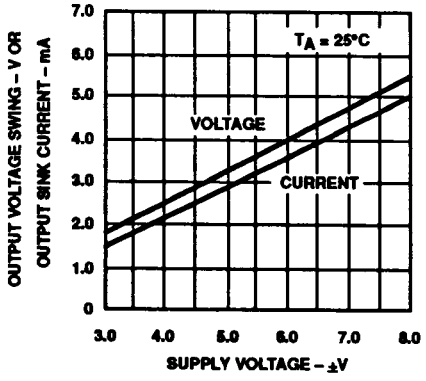
Supply Current as a Function of Temperature



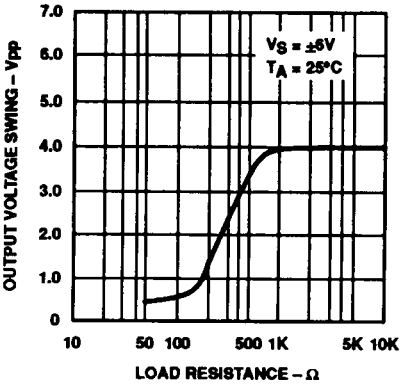
Supply Current as a Function of Supply Voltage



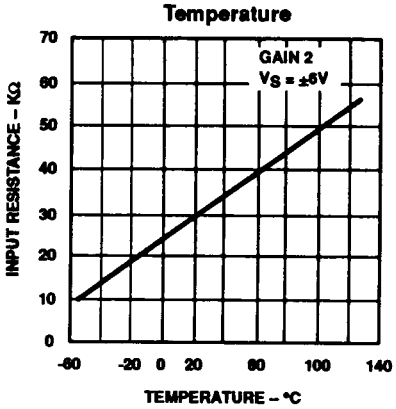
Output Voltage and Current Swing as a Function of Supply Voltage



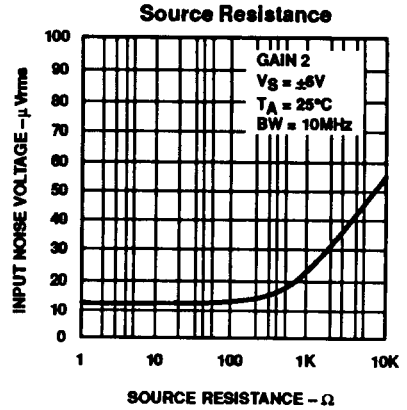
Output Voltage Swing as a Function of Load Resistance

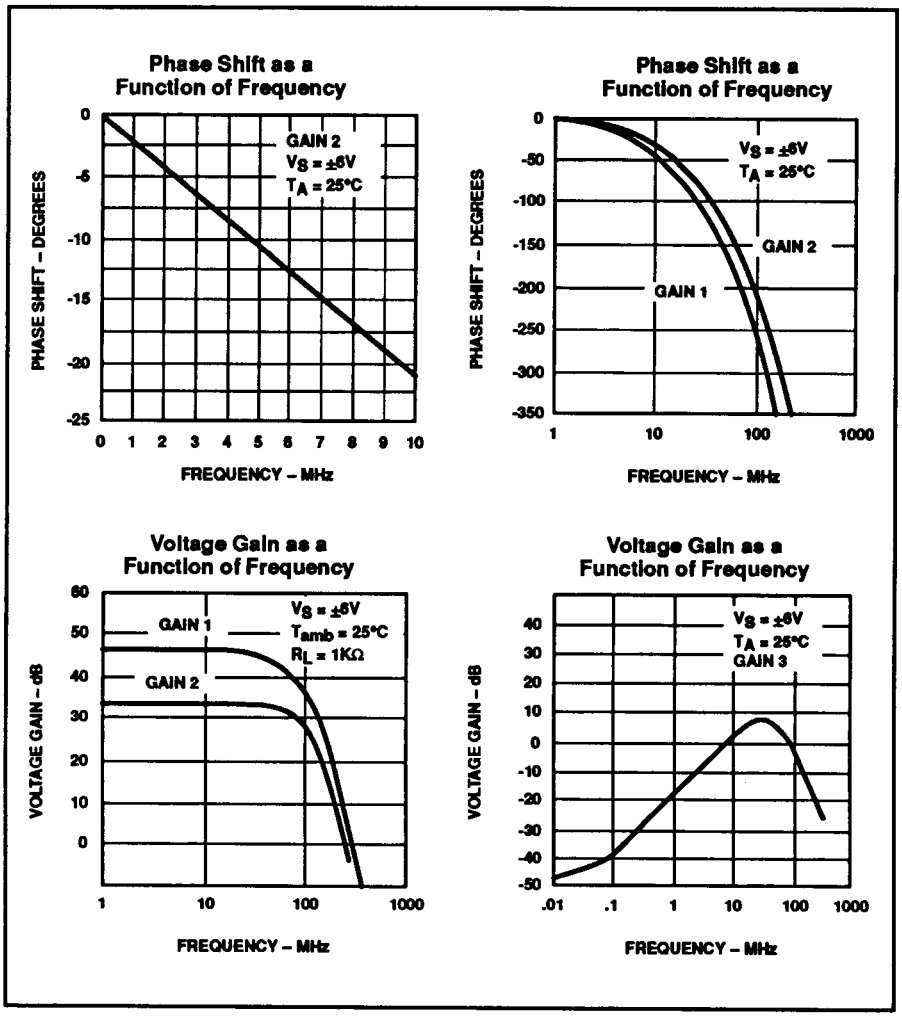


Input Resistance as a Function of Temperature

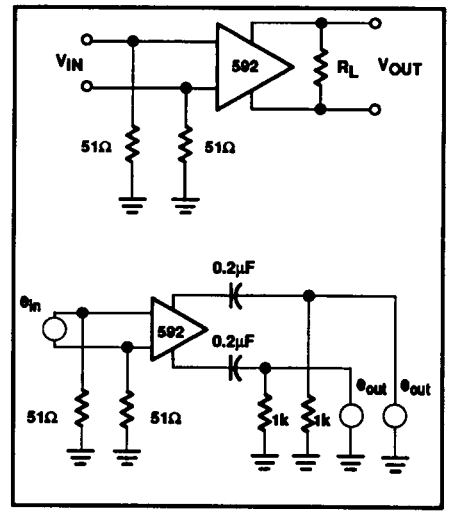


Input Noise Voltage as a Function of Source Resistance





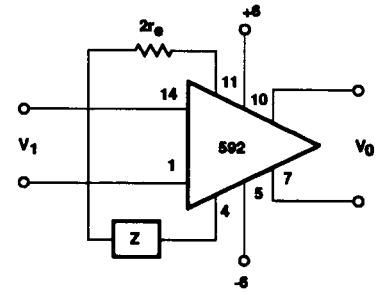
TEST CIRCUITS T_A = 25°C, unless otherwise specified.



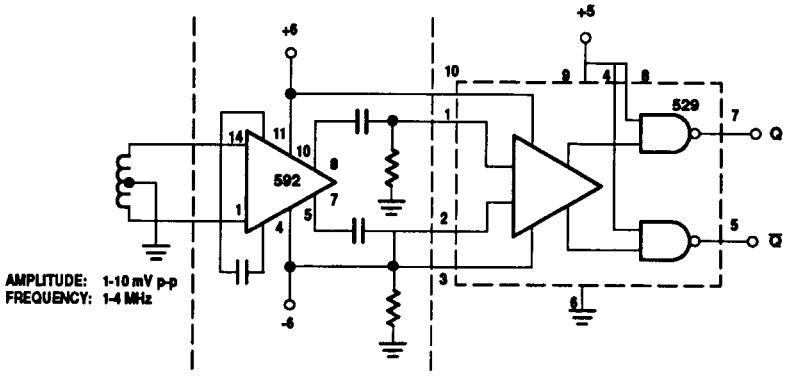
TYPICAL APPLICATIONS

NOTE:

$$\frac{V_O(s)}{v_1(s)} \approx \frac{1.4 \cdot 10^4}{Z(S) + 2r_e} \approx \frac{1.4 \cdot 10^4}{Z(S) + 32}$$

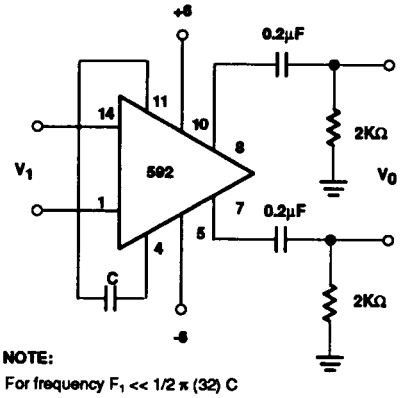


Basic Configuration



READ HEAD | DIFFERENTIATOR/AMPLIFIER | ZERO CROSSING DETECTOR

Disc/Tape Phase-Modulated Readback Systems

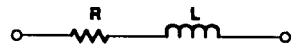
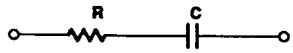
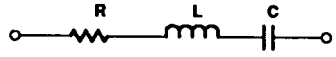
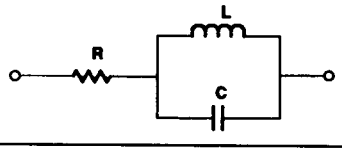


NOTE:
For frequency $F_1 << 1/2\pi$ (32) C

$$V_O = 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_O (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

Signetics

Packaging Information

T-90-20

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

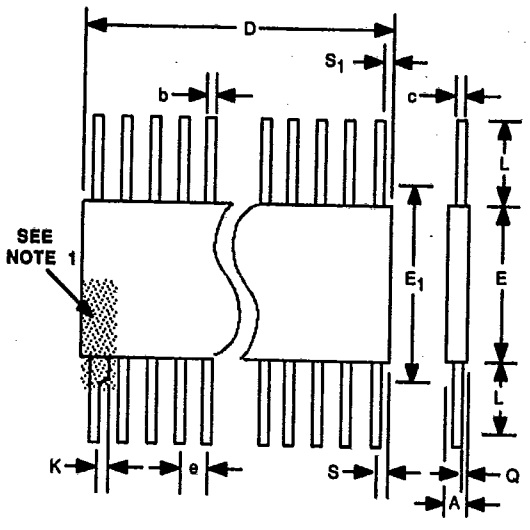
Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

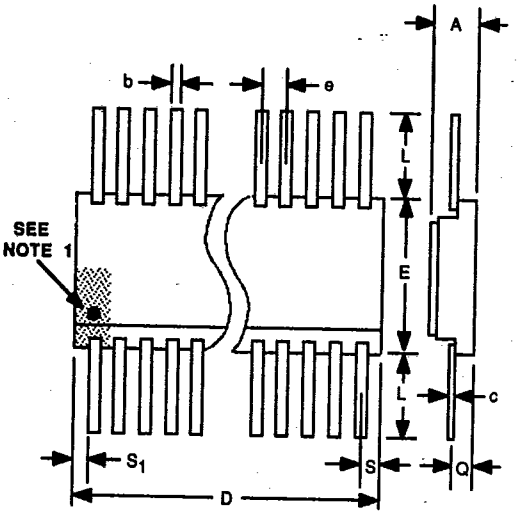
T-90-20

Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

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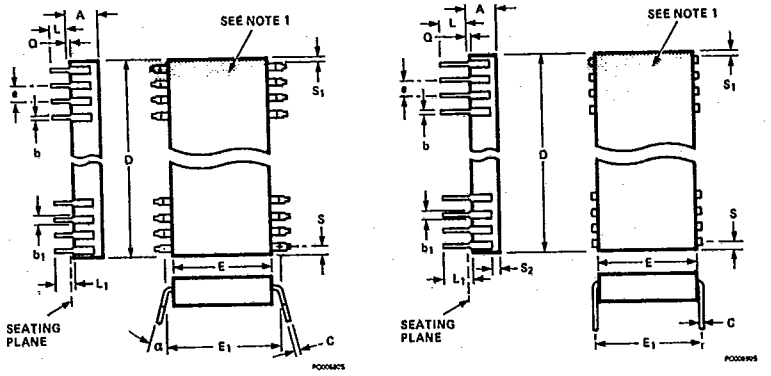
Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1 Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

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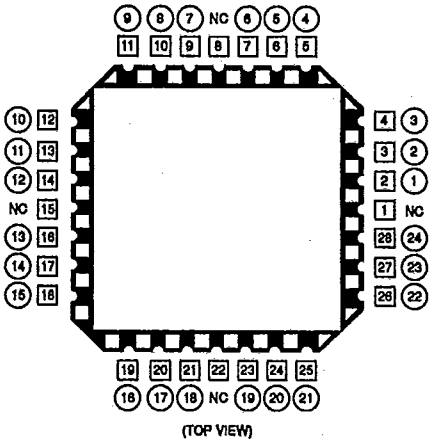
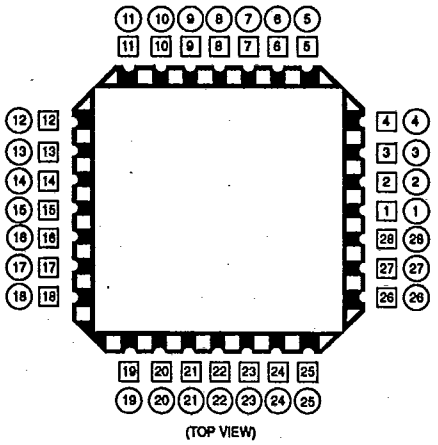
Packaging Information

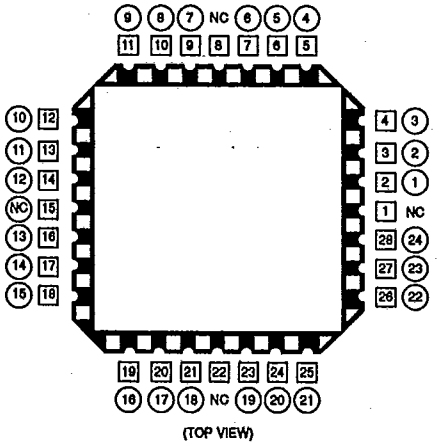
LEADLESS CHIP CARRIER (LLCC) PINOUTS



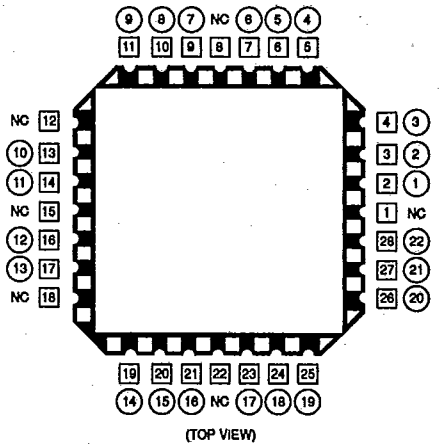
24–Lead Logic Pinout for 28 Terminal Chip Carrier



28–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect