



# NEX13120F-Q100

12-channel automotive linear LED driver

Rev. 1 — 29 May 2025

Preliminary data sheet

## 1. General description

NEX13120F-Q100 is an AEC-Q100 grade 1 qualified 12-channel, 40 V high-side LED driver with up to 100 mA output current per channel, PWM and analog dimming support, and MTP for configurable depending on application requirements in automotive lighting systems.

NEX13120F-Q100 supports 8-bit output current with high accuracy from channel to channel and device to device, channels can be used in parallel to support higher current output than 100 mA. The low dropout of the device helps to eliminate the heat generation of the device itself. The device integrates UART over CAN as the digital interface to enable long distance off-board communication, which is a typical scenario for automotive exterior lighting where different lamp functions are typically located in different PCB boards. NEX13120F-Q100 also supports LED open-circuit, short to ground, and single LED short-circuit diagnostics. Additionally, a configurable watchdog automatically sets the part into Fail-Safe states when the CAN bus connection is lost.

NEX13120F-Q100 can operate at a junction temperature range from -40 °C to +150 °C in a thermally enhanced 24-pin HTSSOP24 package.

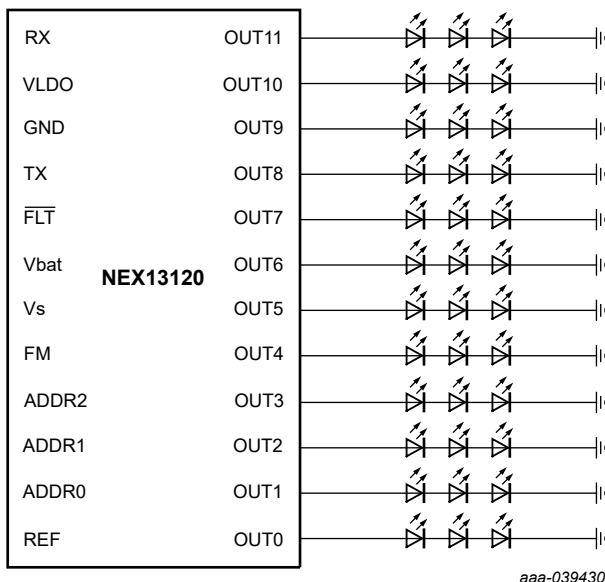


Fig. 1. Typical application

## 2. Features and benefits

- AEC-Q100 qualified for automotive applications
  - Specified from -40 °C to 125 °C
- Compliant with ISO 26262 and meets ASIL B requirements for functional safety
- 12-channel precision high-side current output:
  - $V_{bat}$ : 4.5 V to 36 V and  $V_s$ : 3.8 V to 36 V
  - Up to 100 mA channel current per channel
  - 2-bit global, 6-bit independent current setting
  - Current accuracy within  $\pm 5\%$  from 18 mA to 100 mA
  - Low voltage drops: 600 mV at 100 mA
  - 12-bit independent PWM dimming
  - Programmable PWM frequency: 50 Hz to 23.4 kHz
  - Linear and exponential dimming method
- Integrated UART interface:
  - Data rate up to 2 Mbit/s
  - Support UART data format
  - Support 27 slave address set by resistor
- Diagnostics and protections:
  - Programmable FAIL-SAFE state
  - LED open-circuit detection
  - LED short-circuit detection
  - Single-LED short-circuit diagnostic
  - Programmable low- $V_s$  detection
  - Open-drain FLT pin for fault indication
  - Watchdog and CRC for data line
  - MTP ECC check
  - 8-bit ADC for pin voltage measurement
  - Over-temperature protection
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V

## 3. Applications

- Automotive exterior rear light
- Automotive exterior headlight

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">NEX13120FPC-Q100</a>	-40 °C to +125 °C	HTSSOP24	Thermal enhanced thin shrink small outline package; 24 leads; body size: 7.8 mm x 4.4 mm x 1.2 mm	<a href="#">SOT8083-1</a>

5. Device comparison

Table 2. Device comparison

Type number	Compliant safety standard
NEX13120PC-Q100	Function safety capable Documents are provided to support function safety design.
NEX13120FPC-Q100	Compliant with ISO 26262 and meets ASIL B requirements for functional safety

6. Marking

Table 3. Marking

Type number	Marking code
NEX13120PC-Q100	N13120
NEX13120FPC-Q100	N13120F

7. Application block diagram

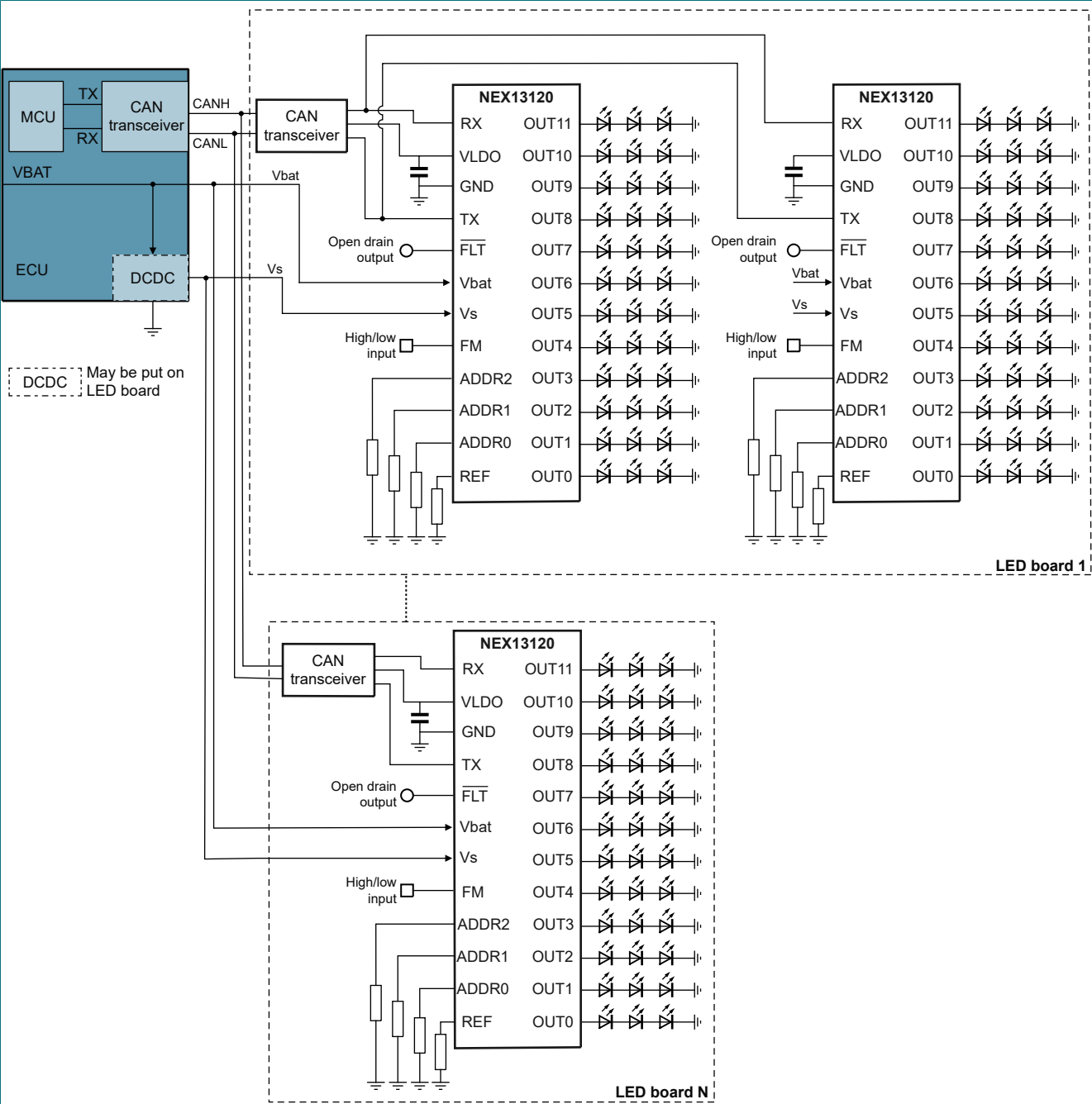


Fig. 2. Application block diagram

8. Pinning information

8.1. Pinning

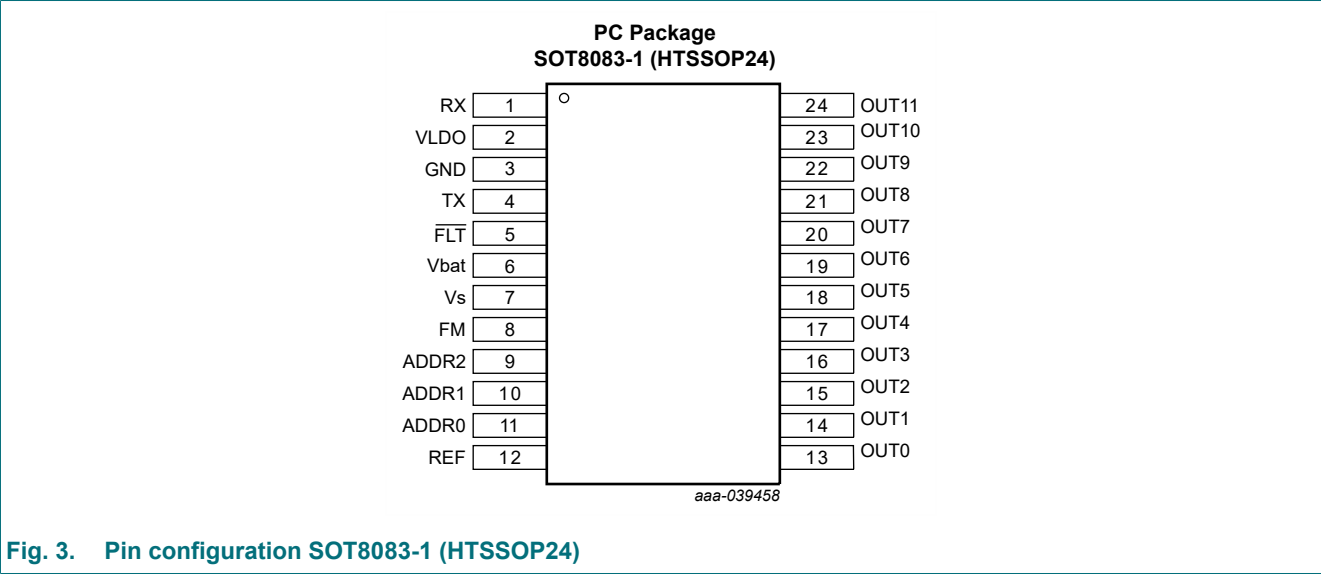


Fig. 3. Pin configuration SOT8083-1 (HTSSOP24)

8.2. Pin description

Table 4. Pin description

Symbol	Pin	I/O	Description
RX	1	I	UART RX over CAN physical layer
VLDO	2	Power	output of internal 5 V LDO
GND	3	GND	device ground
TX	4	O	UART TX over CAN physical layer
FLT	5	I/O	open-drain fault/error output
V <sub>bat</sub>	6	I	power supply for internal circuit
V <sub>s</sub>	7	I	power supply for current output channels
FM	8	I	Fail-Safe state selection <ul style="list-style-type: none"><li>0: Fail-Safe mode 0</li><li>1: Fail-Safe mode 1</li></ul>
ADDR2	9	I	device address 2
ADDR1	10	I	device address 1
ADDR0	11	I	device address 0
REF	12	I/O	device reference current setting, MTP programming chip-selection input
OUT0 to OUT11	13 to 24	O	current output channel 0 to 11

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>I</sub>	input voltage	pins V <sub>bat</sub> , V <sub>s</sub>	- 0.3	45	V
		pin REF, ADDRn	- 0.3	5.5	V
V <sub>O</sub>	output voltage	pins OUTn	- 0.3	V <sub>s</sub> + 0.3	V
		pin VLDO	- 0.3	5.5	V
V <sub>I/O</sub>	I/O voltage	pin FM	- 0.3	V <sub>s</sub> + 0.3	V
		pin FLT	- 0.3	22	V
		pins RX, TX	- 0.3	5.5	V
T <sub>j</sub>	junction temperature		- 40	150	°C
T <sub>amb</sub>	ambient temperature		- 40	125	°C
T <sub>stg</sub>	storage temperature		- 65	150	°C
ESD					
V <sub>ESD</sub>	ESD voltage	Human Body Model (HBD) for all pins, per AEC Q100-002	- 2000	+ 2000	V
		Charged device model (CDM), per AEC Q100-011			
		corner pins (1, 12, 13 and 24)	- 750	+ 750	V
		all pins	- 500	+ 500	V

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>I</sub>	input voltage	pin V <sub>bat</sub> ; device supply voltage	4.5	-	36	V
		pin V <sub>s</sub> ; power supply for output current channel	3.8	-	36	V
I <sub>O</sub>	output current	pins OUTn; channel output current	-	-	100	mA
V <sub>I</sub>	input voltage	pin FM; external Fail-Safe selection input	0	-	V <sub>s</sub>	V
V <sub>I/O</sub>	input/output voltage	pin TX; UART TX output	0	-	5	V
		pin RX; UART RX input	0	-	5	V
V <sub>VLDO</sub>	VLDO voltage	pin VLDO; internal 5 V VLDO output	0	-	5	V
I <sub>VLDO</sub>	VLDO current	pin VLDO; current capability	0	-	80	mA
V <sub>I</sub>	input voltage	pins ADDRn; device address selection	0	-	5	V
V <sub>I/O</sub>	input/output voltage	pin REF; current reference setting	0	-	5	V
		pin FLT; fault/error feedback open-drain output	0	-	20	V
F <sub>CLK</sub>	UART baud rate		0.1	-	2	Mbps
D <sub>sync</sub>	synchronization pulse duty cycle		45	50	55	%
T <sub>j</sub>	junction temperature		-40	-	150	°C
T <sub>amb</sub>	ambient temperature		-40	25	125	°C

## 11. Thermal information

Table 7. Thermal information

Symbol	Parameter	SOT8083-1	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	25.8	°C/W
$R_{\Theta JC(TOP)}$	junction-to-case (top) thermal resistance	29.2	°C/W
$R_{\Theta JB}$	junction-to-board thermal resistance	11.7	°C/W
$\Psi_{JT}$	junction-to-top char parameter	3.6	°C/W

## 12. Electrical characteristics

Table 8. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
Bias						
V <sub>(Vbat)</sub>	operating input voltage range		4.5	12	36	V
I <sub>q(Vbat)</sub>	quiescent current, all-channels ON	V <sub>bat</sub> = 12 V; R <sub>REF</sub> = 8.45 kΩ; all outputs ON; REFRANGE = 11b; PWM duty = 0	-	8	9	mA
	quiescent current, all-channels OFF	V <sub>bat</sub> = 12 V; R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; all outputs OFF	-	8	9	mA
I <sub>q(Vs)</sub>	quiescent current, all-channels ON	V <sub>bat</sub> = 12 V; V <sub>s</sub> = 12 V; R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; PWM Duty = 0; all outputs ON	-	8	-	mA
	quiescent current, all-channels-off	V <sub>bat</sub> = 12 V; V <sub>s</sub> = 12 V; R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; all outputs OFF	-	20	30	μA
I <sub>fault(Vbat)</sub>	quiescent current, Fail-Safe state fault mode	V <sub>s</sub> = 12 V; Fail-Safe state; all outputs OFF; $\overline{\text{FLT}}$ = LOW	-	8	9	mA
I <sub>fault(Vs)</sub>	quiescent current, Fail-Safe state fault mode	V <sub>s</sub> = 12 V; Fail-Safe state; all outputs OFF; $\overline{\text{FLT}}$ = LOW	-	20	30	μA
I <sub>LKG(Vs)</sub>	V <sub>s</sub> leakage current	V <sub>s</sub> = 36 V; V <sub>bat</sub> = 0 V	-	-	85	μA
V <sub>(Vbat_POR_rise)</sub>	V <sub>bat</sub> power-on-reset rising threshold		4	4.2	4.45	V
V <sub>(Vbat_POR_fall)</sub>	V <sub>bat</sub> power-on-reset falling threshold		3.8	4	4.2	V
V <sub>O(VLDO)</sub>	VLDO output voltage	V <sub>bat</sub> > 5.6 V; I <sub>(VLDO)</sub> = 40 mA	4.65	5	5.25	V
I <sub>O(VLDO)</sub>	VLDO output current capability		80	-	-	mA
I <sub>(VLDO_limit)</sub>	VLDO output current limit		110	-	-	mA
V <sub>(VLDO_POR_rise)</sub>	VLDO power-on-reset rising threshold		2.75	3	3.25	V
V <sub>(VLDO_POR_fall)</sub>	VLDO power-on-reset falling threshold		2.45	2.75	3	V
V <sub>(VLDO_OV_rise)</sub>	VLDO overvoltage rising threshold <a href="#">[1]</a>		-	5.7	-	V
V <sub>(VLDO_OV_fall)</sub>	VLDO overvoltage falling threshold <a href="#">[1]</a>		-	5.5	-	V
C <sub>VLDO</sub>	supported VLDO loading capacitance		1	-	10	μF
f <sub>osc</sub>	internal oscillator frequency		-	24	-	MHz

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
FLT						
V <sub>IH(FLT)</sub>	logic high voltage, FLT		2	-	-	V
V <sub>IL(FLT)</sub>	logic low voltage, $\overline{\text{FLT}}$		-	-	0.7	V
I <sub>pd(FLT)</sub>	FLT pull-down current capability	V <sub>(FLT)</sub> = 0.4 V	3	5.5	9	mA
I <sub>LKG(FLT)</sub>	FLT leakage current	V <sub>(FLT)</sub> = 5 V	-	-	1	μA
UART interface						
V <sub>IL(RX)</sub>	input logic low voltage, RX		-	-	0.7	V
V <sub>IH(RX)</sub>	input logic high voltage, RX		2	-	-	V
V <sub>OL(TX)</sub>	low-level output voltage TX,	I <sub>sink</sub> = 5 mA	0	-	0.47	V
V <sub>OH(TX)</sub>	high-level output voltage TX,	I <sub>source</sub> = 5 mA; V <sub>pull-up</sub> = 5 V	4.5	-	5	V
I <sub>LKG(TX-RX)</sub>	TX, RX leakage current	V <sub>RX</sub> = 5 V; V <sub>TX</sub> = 5 V	-1	-	1	μA
ADDRESS, FS						
V <sub>IL(FS)</sub>	input logic low voltage, FS		-	-	0.7	V
V <sub>IH(FS)</sub>	input logic high voltage, FS		2	-	-	V
V <sub>IL(ADDRn)</sub>	logic low voltage ADDR2, ADDR1, ADDR0		-	-	0.7	V
V <sub>IM(ADDRn)</sub>	middle logic voltage ADDR2, ADDR1, ADDR0		0.86	-	1.6	V
V <sub>IH(ADDRn)</sub>	logic high voltage ADDR2, ADDR1, ADDR0		2	-	-	V
R <sub>PD(FS)</sub>	internal pull-down resistance, FS		-	100	-	kΩ
ADC[1]						
DNL	differential non linearity		-1	-	1	LSB
INL	differential non linearity		-2	-	2	LSB
OUTPUT DRIVERS						
f <sub>PWM</sub>	PWM dimming frequency range	CONF_PWMSLOW = 0	0.2	-	25.3	kHz
		CONF_PWMSLOW = 1	0.05	-	5.86	kHz
ΔI <sub>(OUT_d2d)</sub>	device-to-device accuracy ΔI <sub>(OUT_d2d)</sub> = 1-I <sub>avg(OUT)</sub> /I <sub>nom(OUT)</sub>	R <sub>REF</sub> = 6.34 kΩ; REFRANGE = 11b; DC = 63; I <sub>OUT</sub> = 100 mA	-5	0	5	%
		R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; DC = 63; I <sub>OUT</sub> = 75 mA	-5	0	5	%
		R <sub>(REF)</sub> = 8.45 kΩ; REFRANGE = 10b; DC = 63; I <sub>OUT</sub> = 37.5 mA	-5	0	5	%
		R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 01b; DC = 63; I <sub>OUT</sub> = 18.75 mA	-6	0	6	%
ΔI <sub>(OUT_c2c)</sub>	channel-to-channel accuracy ΔI <sub>(OUT_c2c)</sub> = 1- I <sub>(OUTn)</sub> /I <sub>avg(OUT)</sub>	R <sub>REF</sub> = 6.34 kΩ; REFRANGE = 11b; DC = 63; I <sub>OUT</sub> = 100 mA	-5	0	5	%
		R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; DC = 63; I <sub>OUT</sub> = 75 mA	-5	0	5	%
		R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 10b; DC = 63; I <sub>OUT</sub> = 37.5 mA	-5	0	5	%
		R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 01b; DC = 63; I <sub>OUT</sub> = 18.75 mA	-6	0	6	%

Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
V <sub>(OUT_drop)</sub>	output dropout voltage	R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; DC = 38; I <sub>OUT</sub> = 45 mA	300	430	590	mV
		R <sub>REF</sub> = 8.45 kΩ; REFRANGE = 11b; DC = 63; I <sub>OUT</sub> = 75 mA	360	490	730	mV
		R <sub>REF</sub> = 6.34 kΩ; REFRANGE = 11b; DC = 63; I <sub>OUT</sub> = 100 mA	400	600	860	mV
R <sub>REF</sub>			5	-	50	kΩ
C <sub>REF</sub>			0	-	4.7	nF
V <sub>REF</sub>			-	1.235	-	V
K <sub>(REF_11)</sub>		REFRANGE = 11b	-	512	-	-
K <sub>(REF_10)</sub>		REFRANGE = 10b	-	256	-	-
K <sub>(REF_01)</sub>		REFRANGE = 01b	-	128	-	-
K <sub>(REF_00)</sub>		REFRANGE = 00b	-	64	-	-
I <sub>(REF_OPEN_th)</sub>			4	12	20	μA
V <sub>(REF_SHORT_th)</sub>			0.4	0.6	0.8	V
DIAGNOSTICS						
V <sub>(Vs_th_rise)</sub>	V <sub>s</sub> undervoltage rising threshold		2.5	2.75	2.9	V
V <sub>(Vs_th_fall)</sub>	V <sub>s</sub> undervoltage falling threshold		2.3	2.55	2.7	V
V <sub>(Vs_th_hyst)</sub>	V <sub>s</sub> undervoltage hysteresis		-	200	-	mV
V <sub>(OPEN_th_rise)</sub>	LED open rising threshold, AUTOSS = 0	V <sub>(Vs)</sub> - V <sub>(OUTn)</sub>	200	240	325	mV
V <sub>(OPEN_th_rise)</sub>	LED open rising threshold, AUTOSS = 1	V <sub>(Vs)</sub> - V <sub>(OUTn)</sub>	230	300	445	mV
V <sub>(OPEN_th_fall)</sub>	LED open falling threshold	V <sub>(Vs)</sub> - V <sub>(OUTn)</sub>	140	400	450	mV
V <sub>(OPEN_th_hyst)</sub>	LED open hysteresis		-	100	-	mV
V <sub>(SG_th_rise)</sub>	short to GND rising threshold		0.8	0.9	1	V
V <sub>(SG_th_fall)</sub>	short to GND falling threshold		1.05	1.2	1.3	V
V <sub>(SG_th_hyst)</sub>	short to GND hysteresis		-	0.3	-	V
MTP						
N <sub>(MTP)</sub>	number of programming cycles	VLDO = 5 V	1000	-	-	-
Temperature <sup>[1]</sup>						
T <sub>(PRETSD)</sub>	pre-thermal warning threshold		-	135	-	°C
T <sub>(PRETSD_HYS)</sub>	pre-thermal warning hysteresis		-	5	-	°C
T <sub>(TSD1)</sub>	over-temperature protection threshold		-	175	-	°C
T <sub>(TSD2)</sub>	over-temperature shutdown threshold		-	185	-	°C
T <sub>(TSD1_HYS)</sub>	over-temperature protection hysteresis		-	15	-	°C
T <sub>(TSD2_HYS)</sub>	over-temperature shutdown hysteresis		-	15	-	°C

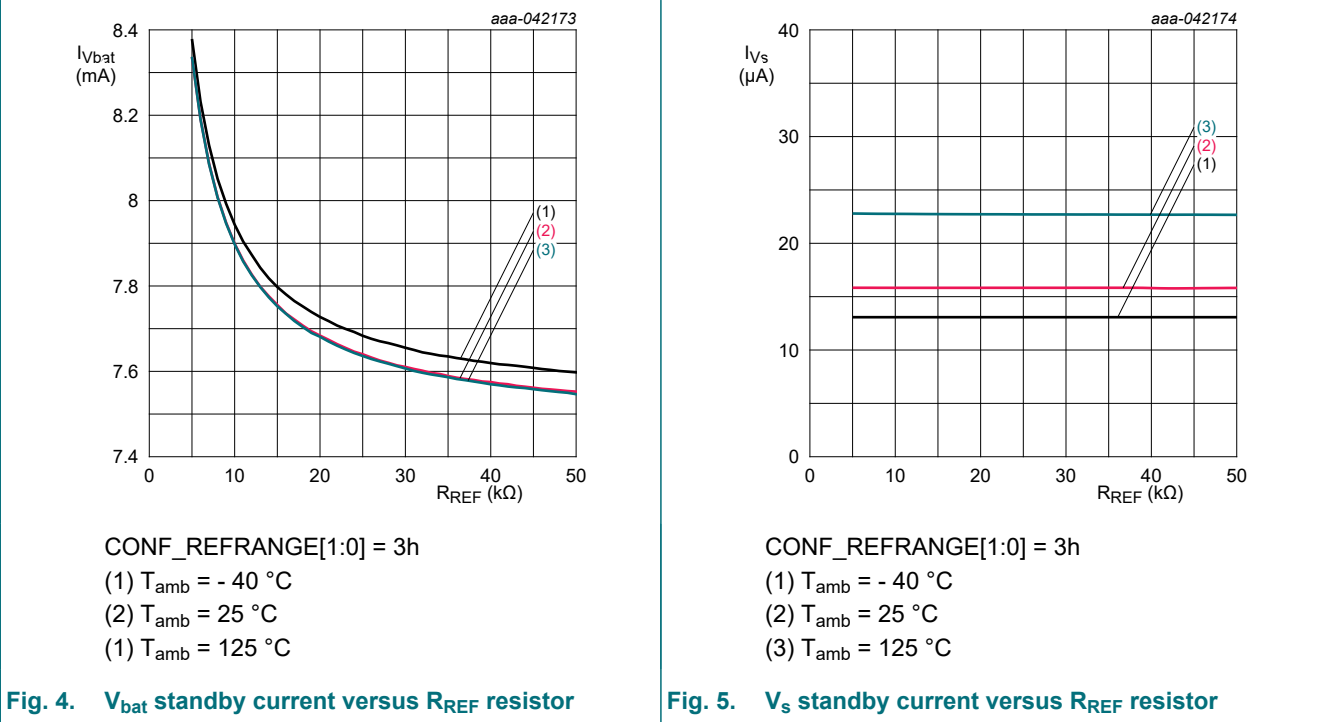
[1] Guaranteed by bench test, not fully tested in production.

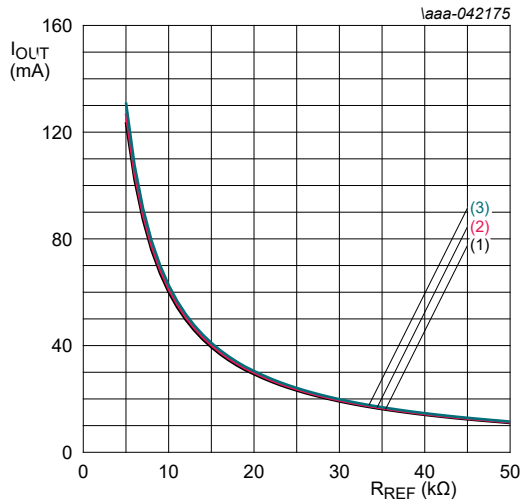


Table 9. Timing requirement

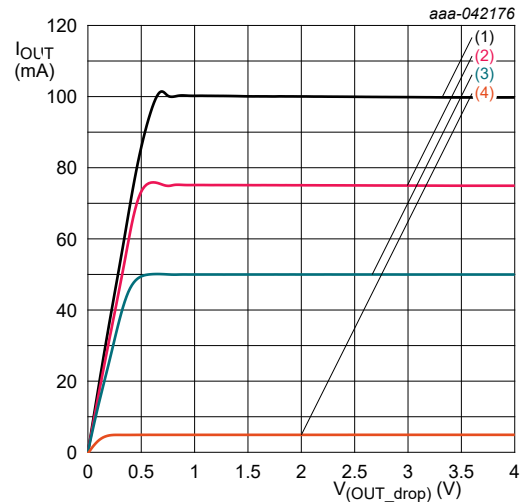
Symbol	Parameter	Conditions	-40 °C to +125 °C			Unit
			Min	Typ	Max	
t <sub>(ODPW)</sub>	diagnostics pulse-width, ODPW = 0h		-	100	-	µs
t <sub>(CONV)</sub>	time needed to complete one AD conversion		-	55	-	µs
t <sub>(retry)</sub>	fault retry timer		-	10	-	ms

13. Typical characteristics



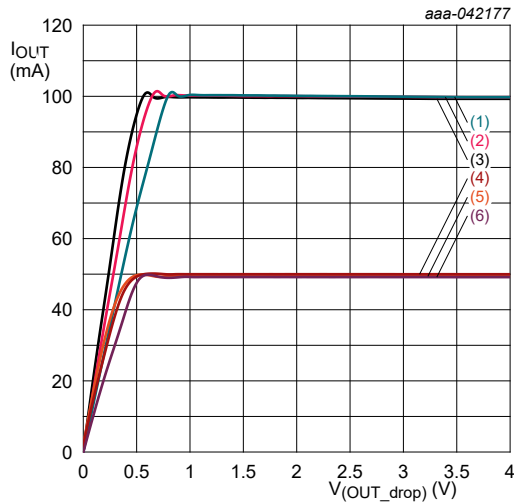


CONF\_IOUTx[5:0] = 3Fh  
 CONF\_REFRANGE[1:0] = 3h  
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 125\text{ °C}$

Fig. 6. Output full-range current versus  $R_{REF}$  resistor

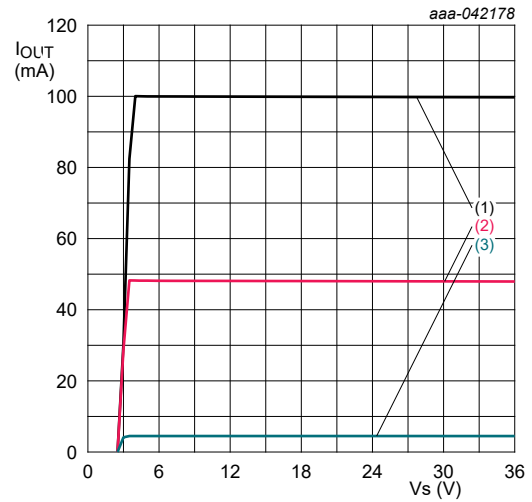
CONF\_REFRANGE[1:0] = 3h  
 (1)  $I_{OUT} = 100\text{ mA}$   
 (2)  $I_{OUT} = 75\text{ mA}$   
 (3)  $I_{OUT} = 50\text{ mA}$   
 (4)  $I_{OUT} = 5\text{ mA}$

Fig. 7. Output current versus dropout voltage



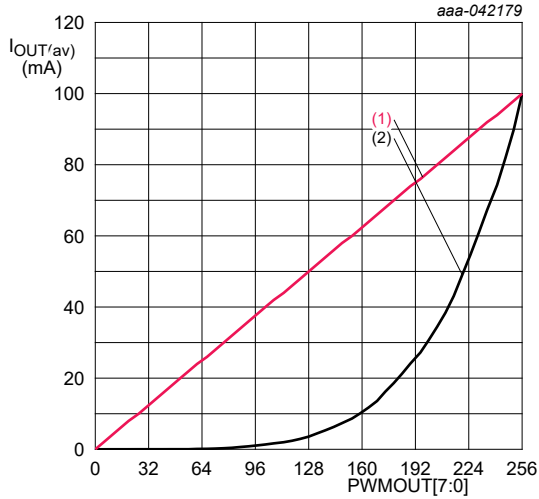
$R_{REF} = 6.34\text{ k}\Omega$  &  $12.6\text{ k}\Omega$   
 CONF\_REFRANGE[1:0] = 3h  
 (1)  $I_{OUT} = 100\text{ mA}$ ;  $T_{amb} = 125\text{ °C}$   
 (2)  $I_{OUT} = 100\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$   
 (3)  $I_{OUT} = 100\text{ mA}$ ;  $T_{amb} = -40\text{ °C}$   
 (4)  $I_{OUT} = 50\text{ mA}$ ;  $T_{amb} = 125\text{ °C}$   
 (5)  $I_{OUT} = 50\text{ mA}$ ;  $T_{amb} = -40\text{ °C}$   
 (6)  $I_{OUT} = 50\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$

Fig. 8. Output current versus dropout voltage



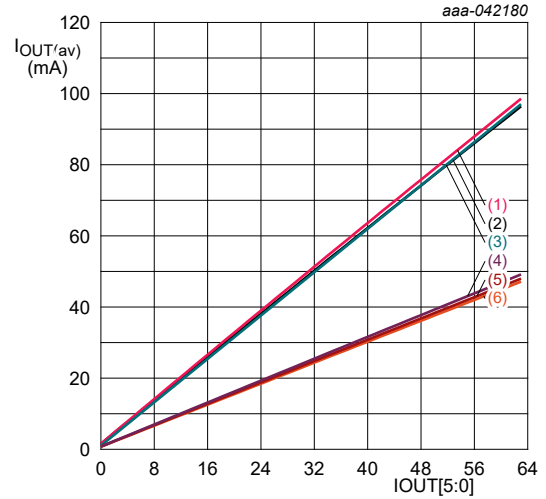
CONF\_REFRANGE[1:0] = 3h  
 (1)  $I_{OUT} = 100\text{ mA}$   
 (2)  $I_{OUT} = 50\text{ mA}$   
 (3)  $I_{OUT} = 5\text{ mA}$

Fig. 9. Output current versus dropout voltage



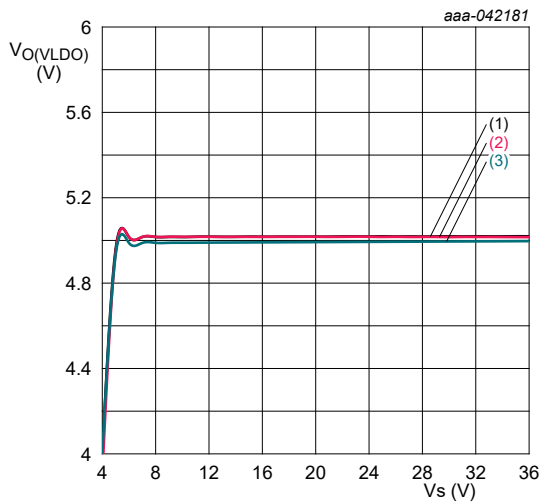
CONF\_EXPEN = 0 & 1  
 CONF\_IOUTx[5:0] = 3Fh  
 (1) CONF\_EXPEN = 0  
 (2) CONF\_EXPEN = 1

Fig. 10. Average current versus PWMOUT[7:0]



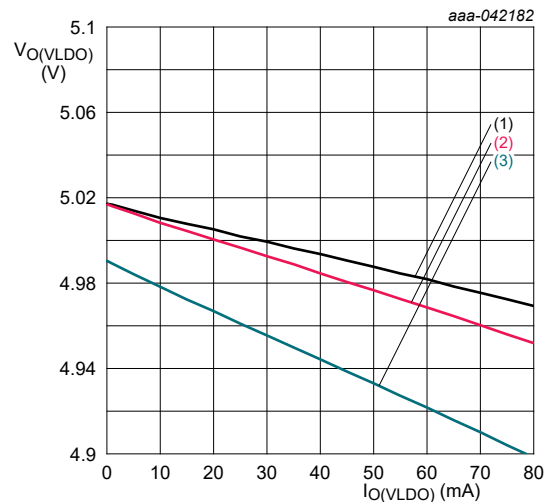
$R_{REF} = 6.34 \text{ k}\Omega$  &  $12.6 \text{ k}\Omega$   
 CONF\_REFRANGE[1:0] = 3h  
 (1)  $I_{OUT} = 100 \text{ mA}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (2)  $I_{OUT} = 100 \text{ mA}$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C}$   
 (3)  $I_{OUT} = 100 \text{ mA}$ ;  $T_{amb} = 125 \text{ }^{\circ}\text{C}$   
 (4)  $I_{OUT} = 50 \text{ mA}$ ;  $T_{amb} = 125 \text{ }^{\circ}\text{C}$   
 (5)  $I_{OUT} = 50 \text{ mA}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (6)  $I_{OUT} = 50 \text{ mA}$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

Fig. 11. Output DC current versus IOUT[5:0]



(1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 125 \text{ }^{\circ}\text{C}$

Fig. 12. LDO output line regulation



(1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 125 \text{ }^{\circ}\text{C}$

Fig. 13. LDO output load regulation

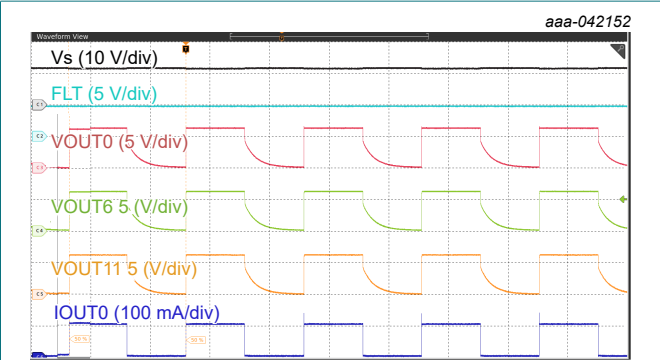


Fig. 14. PWM dimming at 50 Hz

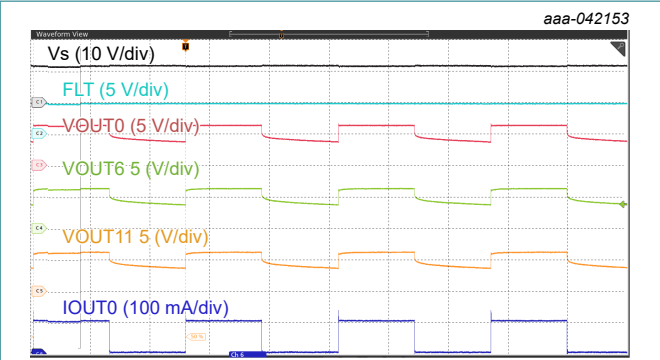


Fig. 15. PWM dimming at 2000 Hz

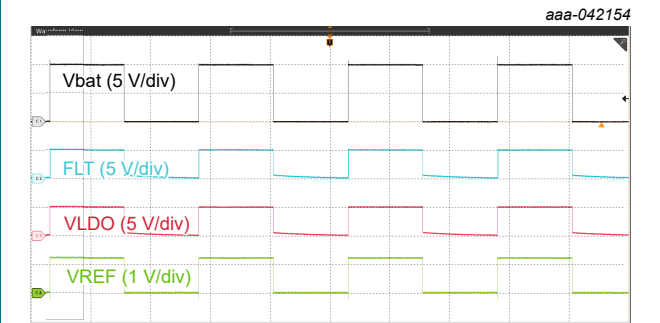


Fig. 16. V<sub>bat</sub> start-up and shutdown

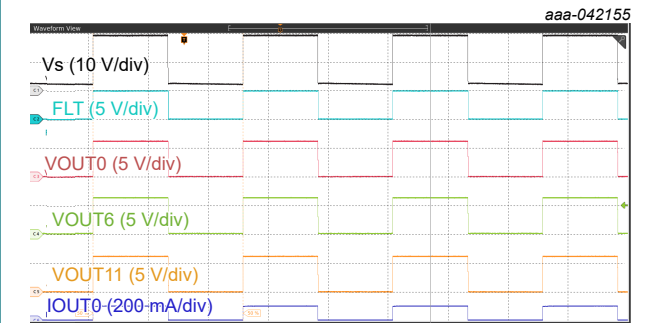


Fig. 17. V<sub>s</sub> start-up and shutdown

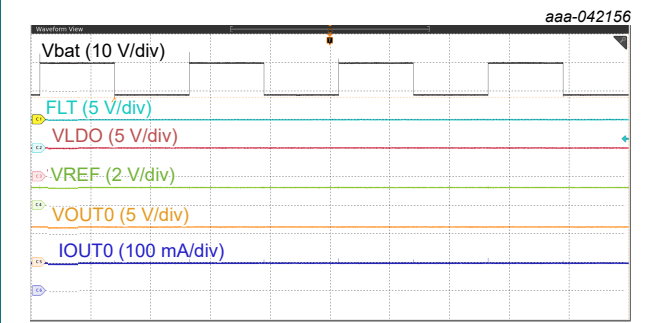


Fig. 18. V<sub>bat</sub> transient

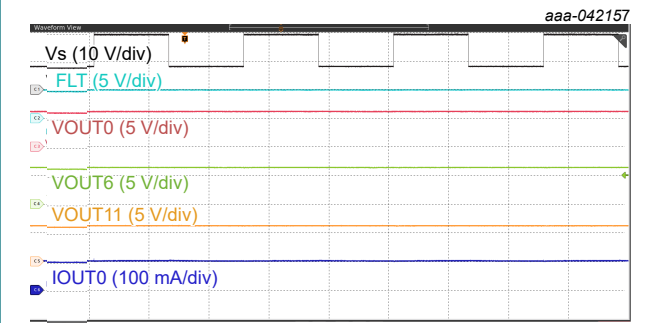


Fig. 19. V<sub>s</sub> transient

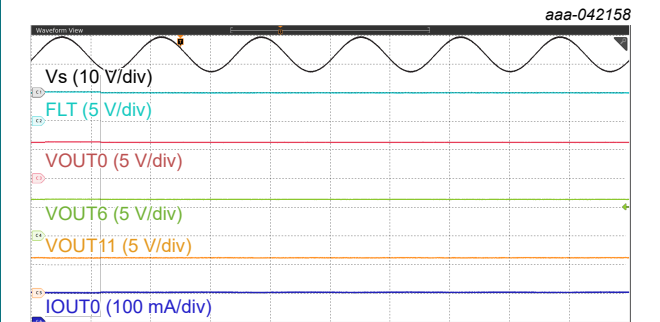


Fig. 20. Superimposed alternating voltage 15 Hz

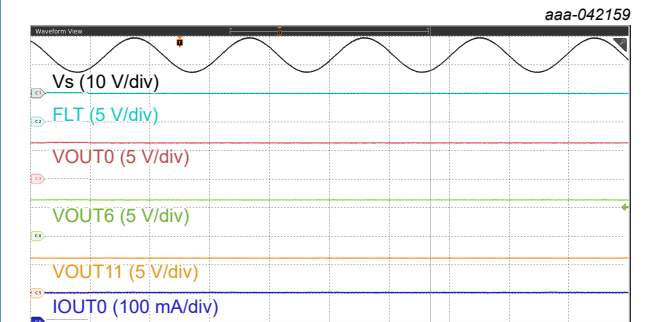


Fig. 21. Superimposed alternating voltage 1 kHz

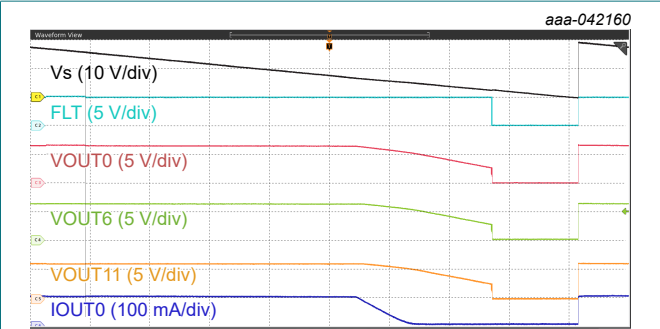


Fig. 22. Slow decrease and quick increase of supply voltage

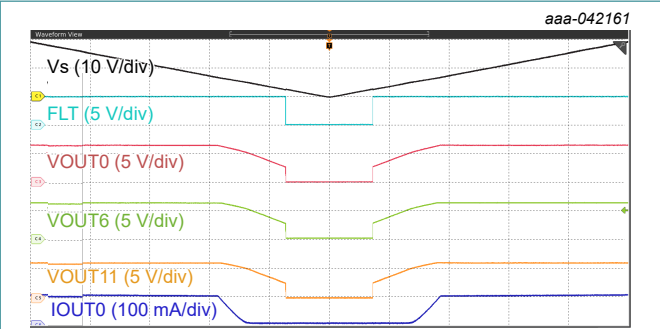


Fig. 23. Slow decrease and slow increase of supply voltage

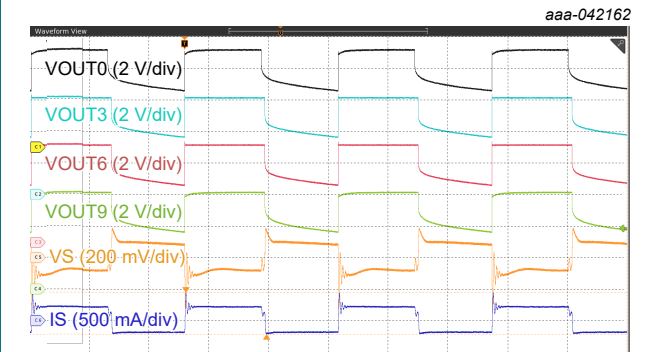


Fig. 24. Phase shift disable

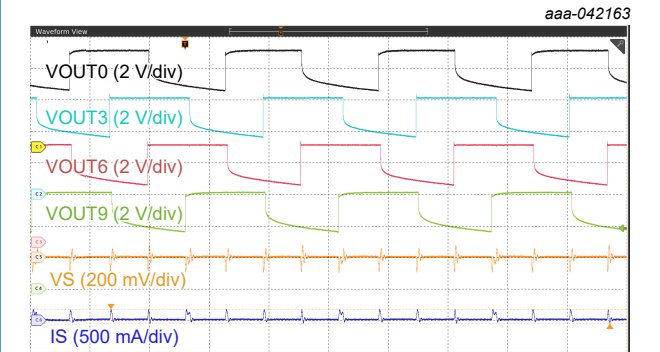


Fig. 25. Phase shift enable

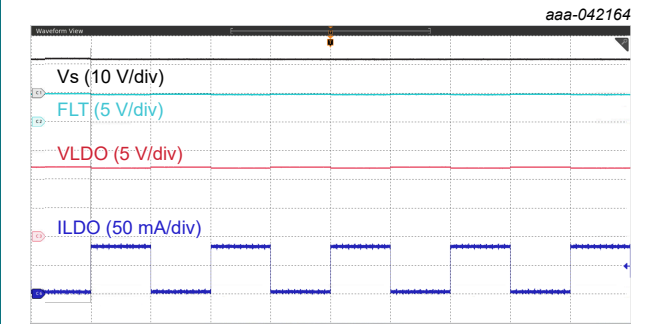


Fig. 26. LDO output load transient

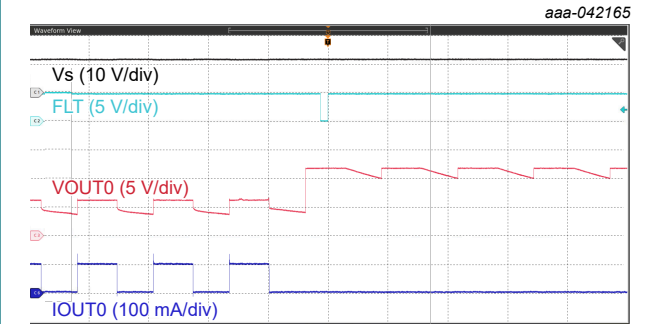


Fig. 27. LED open-circuit detection in normal mode

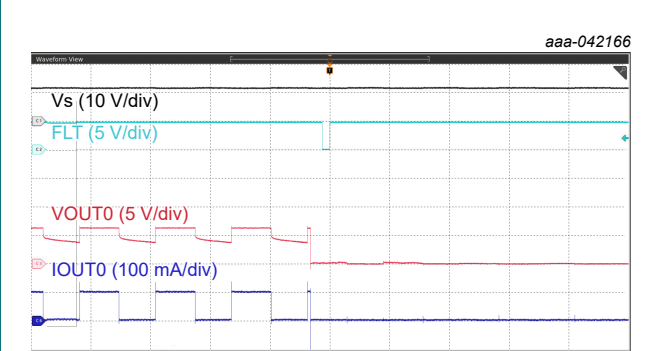


Fig. 28. LED short-circuit detection in normal mode

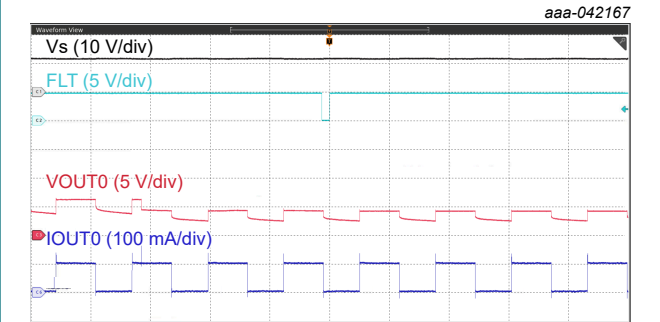


Fig. 29. Single-LED short circuit detection in normal mode

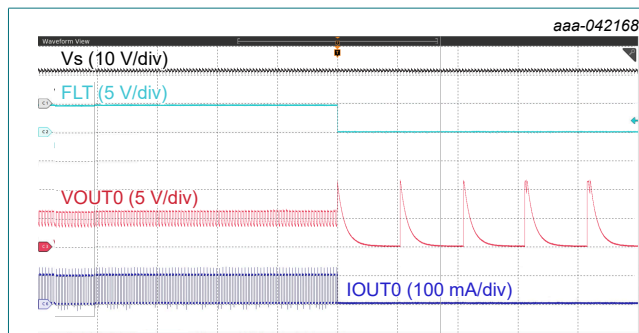


Fig. 30. LED open-circuit detection in FS mode

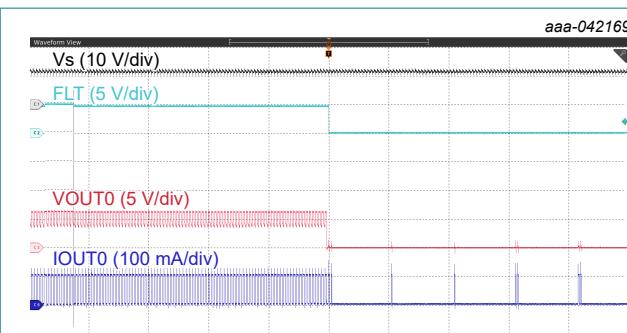


Fig. 31. LED short-circuit detection in FS mode

## 14. Detailed description

### 14.1. Overview

The NEX13120F-Q100 is an automotive 12-channel LED driver equipped with a UART interface to meet the growing demand for individual control of each LED string. Each channel supports both analog dimming and PWM dimming, configurable via the UART. The internal MTP memory enables users to set configurations in the event of communication loss, ensuring compliance with system-level safety requirements.

The integrated UART interface is compliant with physical layer transceiver such as CAN or LIN transceivers. It can support off-board communication with the transition of CAN or LIN transceivers.

Each output channel serves as a constant current source, allowing for individually programmable current outputs and PWM duty cycles. The device includes various diagnostic features, such as LED open-circuit, short-circuit, and single-LED short-circuit detection. Additionally, the on-chip ADC enables real-time monitoring of output conditions.

To enhance robustness, NEX13120F-Q100 integrates Fail-Safe state machine that automatically switches to Fail-Safe states in case of communication loss, such as MCU failure. Users can program Fail-Safe settings using the MTP, allowing for different configurations in the event of output failure, such as one-fails-all-fail or one-fails-others-on. Each channel can be independently programmed to either remain on or off during Fail-Safe states.

The Fail-Safe state machine also permits the system to operate with pre-programmed MTP settings without the presence of a controller, enabling stand-alone operation. The micro-controller can access each device through the UART interface, allowing full control over the device and LEDs by setting and reading back registers. All MTPs are pre-programmed with default values, and it is recommended for the users to program the MTP at the end of the production line for application-specific settings and Fail-Safe configurations.

## 14.2. Function block diagram

The NEX13120F-Q100 function block diagram is shown below:

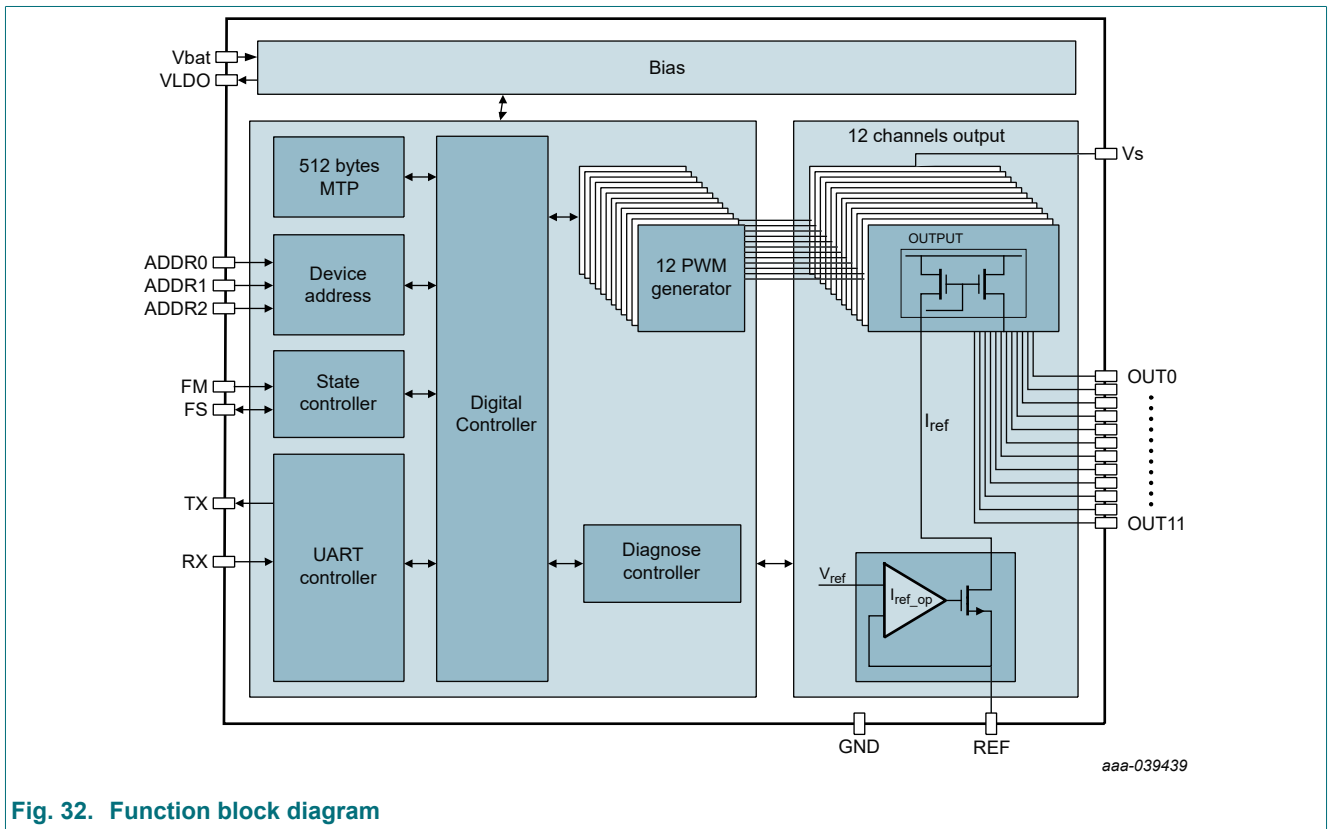


Fig. 32. Function block diagram

## 14.3. Feature description

### 14.3.1. Device bias and power

#### Power supply ( $V_{bat}$ )

The NEX13120F-Q100 is AEC Q-100 qualified for automotive applications. The power input to the device through  $V_{bat}$  pin can be low to 4.5 V and up to 36 V for automotive battery directly powered systems. All the internal analog and digital circuits except for the current output channels are powered by  $V_{bat}$ .

#### 5 V low drop-out linear regulator (VLDO)

NEX13120F-Q100 has an integrated low-drop-out linear regulator to provide power supply to external CAN transceivers. The internal LDO powered by input voltage  $V_{(V_{bat})}$  provides a stable 5 V output with up to 80 mA constant current capability. It is recommended to use a ceramic capacitor from 1  $\mu$ F to 10  $\mu$ F on the VLDO pin. The LDO has an internal current limit  $I_{(VLDO\_limit)}$  for protection and soft start. The capacitor charging time must be considered to total start-up time because the device is held in POR state if the capacitor voltage is not charged to above UVLO threshold.

#### Under-voltage lockout (UVLO) and power-on-reset (POR)

NEX13120F-Q100 uses UVLO and POR circuitry to clear its internal registers upon power-up and to reset registers with its default values. NEX13120F-Q100 has internal UVLO circuits so that when either input voltage  $V_{(V_{bat})}$  or LDO output voltage  $V_{(VLDO)}$  is lower than its UVLO threshold, POR is triggered. In POR state, the device resets digital core and all registers to default value. FLAG\_POR and FLAG\_ERR register are set to 1 for each POR cycle to indicate the POR history. Before both powers are above UVLO thresholds, NEX13120F-Q100 stays in POR state with all outputs off and FLT pin pulled down.

Once both power supplies are above UVLO threshold, the device enters INIT mode for initialization releasing FLT pin pull-down. A programmable timer starts counting in INIT state, the timer length can be set by MTP register NV\_INITTIMER. When the timer has expired, the device switches to NORMAL state. In INIT state, setting CLR\_POR to 1 clears FLAG\_POR, disables the timer, and sets the device to NORMAL state. Upon powering up, NEX13120F-Q100 automatically loads all the settings stored in MTP to correlated registers and sets the other registers to default value which do not have correlated MTP. All channels are powered up off-state by default to avoid unwanted blinking. Writing 1 to CLR\_REG manually loads MTP setting to the correlated registers and set the other registers to default value. After CLR\_REG is set, the FLAG\_POR is cleared to 0.

Writing 1 to CLR\_POR also resets the FLAG\_POR register to 0. It is recommended to set CLR\_REG to 1 to clear the internal registers every time after POR. The CLR\_REG automatically resets to 0.

### Power supply ( $V_s$ )

NEX13120F-Q100 has additional  $V_s$  input pins for powering all 12 high-side current output channels. The  $V_s$  voltage can be low to 3.8 V and up to 36 V for either automotive battery directly powered systems or an external DC-to-DC converter output. An external DC-to-DC converter can provide a regulated voltage for required LED output forward voltage from wide automotive battery voltage range.

NEX13120F-Q100 has an internal under-voltage detection circuit for  $V_s$  input. When the  $V_s$  input voltage is lower than under-voltage threshold,  $V_{(V_s\text{th\_fall})}$ , all 12 current output channels are disabled with FLT pin constantly pulled low and register flags set to 1 including FLAG\_ERR bit and FLAG\_VSUV bit. [Table 17](#) shows the detailed fault behavior in NORMAL state.

### Programmable low $V_s$ supply warning

NEX13120F-Q100 uses its internal ADC to monitor supply voltage  $V_s$ . If the  $V_s$  is below allowable working threshold, the output voltage can be insufficient to keep the LED operating with the desired brightness output as expected. The  $V_s$  voltage is automatically compared with the threshold set by register CONF\_ADCLOWVSTH. When the  $V_s$  voltage is below the threshold, the device sets the warning flag register FLAG\_LOWVS and FLAG\_ERR to 1 in the status register. CLR\_ERR can clear the FLAG\_LOWVS as well as other fault registers. Low- $V_s$  warning clears LED open and single-LED short faults. In addition, the LED open-circuit and single LED short-circuit detection is disabled if the  $V_s$  voltage is below threshold to avoid the LED open circuit and to prevent the single LED short-circuit fault from being mis-triggered. The 4-bit register CONF\_ADCLOWVSTH has 16 options covering from 4 V to 19 V as shown below.

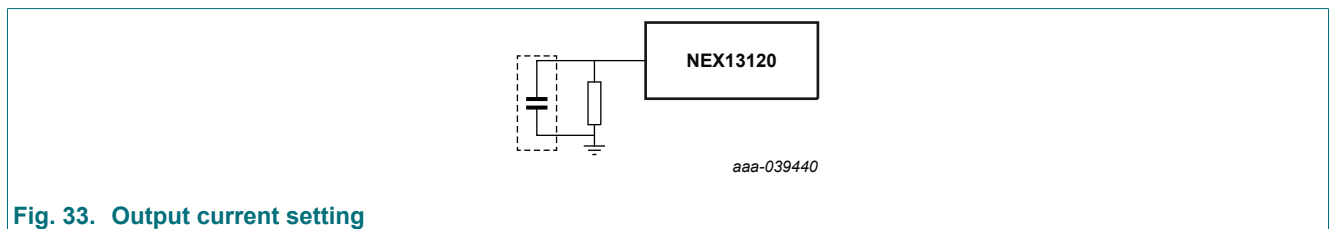
**Table 10. Low supply warning threshold setting**

CONF_ADCLOWVSTH	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
Voltage (V)	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	4

## 14.3.2. Constant current output

### Constant current output reference current with external resistor ( $R_{REF}$ )

The NEX13120F-Q100 must have an external resistor  $R_{REF}$  to set the internal current reference  $I_{REF}$  as shown in [Fig. 33](#).



**Fig. 33. Output current setting**

The internal current reference,  $I_{(FULL\_RANGE)}$ , is generated based on the  $I_{REF}$  multiplied by factor  $K_{(REF)}$  to provide the full range current reference for each OUTx channel. The  $K_{REF}$  is programmable by 2-bit register CONF\_REFRANGE with four different options. Use the following equation to calculate the  $I_{(full\_range)}$ :

$$I_{full\_range} = \frac{V_{REF}}{R_{REF}} \cdot K_{REF} \quad (1)$$



Where  $V_{REF} = 1.235\text{ V}$ ,  $K_{REF} = 64, 128, 256$  or  $512$  (default)

**Table 11. Reference current range setting**

Reference	$K_{REF}$	Full range current (mA)			
		$R_{REF} = 6.34\text{ k}\Omega$	$R_{REF} = 8.45\text{ k}\Omega$	$R_{REF} = 12.7\text{ k}\Omega$	$R_{REF} = 31.6\text{ k}\Omega$
11b	512	100	75	50	20
10b	256	50	37.5	25	10
01b	128	25	18.75	12.5	5
00b	64	12.5	9.375	6.25	2.5

It is recommended to place the  $R_{REF}$  resistor as close as possible to the REF pin with a ceramic capacitor (up to  $2.2\text{ nF}$ ) in parallel to improve the noise immunity. It is also recommended to use a  $1\text{ nF}$  ceramic capacitor in parallel with  $R_{REF}$ .

### 64-step programmable high-side constant-current output

NEX13120F-Q100 has 12 channels of high-side current sources. Each channel has its own enable configuration register  $CONF\_ENCHn$ . Setting  $CONF\_ENCHn$  to 1 enables the channel output, clearing the register to 0 disables the channel output. To completely turn off the channel current, user can clear channel enable bit  $CONF\_ENCHn$  to 0. Upon powering up,  $CONF\_ENCHn$  is automatically reset to 0 to avoid unwanted blinking.

Each  $OUTn$  channel supports individual 64-step programmable current setting, also known as Dot Correction (DC). The DC feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on external visual system to further save binning cost. The 6-bit register  $CONF\_IOUTn$  sets the current independently, where  $n$  is the channel number from 0 to 11. The  $OUTn$  current can be calculated with the equation below:

$$I_{(OUTn)} = \frac{(CONF\_IOUTn+1)}{64} \times I_{(full\_range)} \quad (2)$$

Where:

- $CONF\_IOUTn$  is programmable from 0 to 63
- $n$  is from 0 to 11 for different output channel
- $I_{(full\_range)}$  can be calculated with equation (1)

14.3.3. PWM dimming

NEX13120F-Q100 integrates independent 12-bit PWM generators for each OUTn channel. The integrated PWM generator turns the current output for each OUTn channel on and off. The average current of each OUTn can be adjusted by PWM duty cycle independently, therefore, to control the brightness for LEDs in each channel.

PWM dimming frequency

The frequency for PWM dimming is programmable by 4-bit register CONF\_PWMFREQ and register CONF\_PWMSLOW with 32 options covering from 50 Hz to 23.4 kHz. CONF\_PWMSLOW default value is 0, it supports 200 Hz to 23.4 kHz; when set CONF\_PWMSLOW to 1, it supports lower PWM frequency, the range is 50 Hz to 5.86 kHz. Select the frequency for PWM dimming based on the minimum brightness requirement in application. NEX13120F-Q100 supports down to 1 μs minimum pulse current for all 12 channel outputs.

Below is the frequency table:

Table 12. PWM frequency setting

PWM frequency setting CONF_PWMFREQ	PWM cycle frequency	
	CONF_PWMSLOW = 0	CONF_PWMSLOW = 1
0	200	50
1	250	60
2	300	75
3	350	90
4	400	100
5	500	125
6	600	150
7	800	200
8	1000	250
9	1200	300
10	2000	500
11	4000	1000
12	5800	1500
13	7800	2000
14	9400	2300
15	23400	5800

### ODPW time

As NEX13120F-Q100 supports PWM control for adjusting LED brightness, the voltage on OUTn is like a pulse waveform. The output voltage and current ramp up to the target value in a certain period of time after the channel is turned on, depending on the value of capacitor on the OUTn pin. The ramping up period is proportional to the capacitance value of the capacitor. To avoid the output voltage of each OUTn is measured in the ramping up transient period, NEX13120F-Q100 integrates a  $t_{(ODPW)}$  timer which is programmable by a 4-bit register CONF\_ODPW to setup the ODPW time for all OUTn. The device does not start the OUTn diagnostics and ADC measurement until the  $t_{(ODPW)}$  timer is overflow. The  $t_{(ODPW)}$  timer is programmable from 20  $\mu$ s to 5 ms as described in Table 13. It is recommended to set  $t_{(ODPW)}$  less than the PWM dimming period which is programmable by CONF\_PWMFREQ register, otherwise the OUTn diagnostics and ADC measurement only operates properly when PWM duty cycle is set to 100 %.

Table 13. ODPW time setting

	ODPW time															
Binary code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
$T_{(ODPW)}$ ( $\mu$ s)	100	20	30	50	80	150	200	300	500	800	1000	1200	1500	2000	3000	5000

### Phase shift PWM dimming

If all 12 output channels start PWM period at the same time, the peak output current of the chip is high. To reduce the peak current of the chip, the user can configure a phase shift. In phase shift PWM dimming mode, every three current output channels are formed as one group, one group phase is same and its phase is controlled by NV\_PS0[1:0]. In case the phase shift is enabled, Group[x] turns on with a delay of  $T\theta = X \times \theta \times 1/FPWM$ , where  $X = 0$  to 4. In case the phase shift is disabled, Group[x] turns on simultaneously with Group[x-1]. Both cases are shown in Fig. 34. When CONF\_PSENx is set to 1, Group[x] phase shift is enabled. Setting CONF\_PSENx to 0 can disable phase shift for Group[x].  $\theta$  is configurable by register CONF\_PS0[1:0],  $\theta$  is a ratio parameter of  $1/FPWM$ , FPWM is configured by CONF\_PWMFREQ.

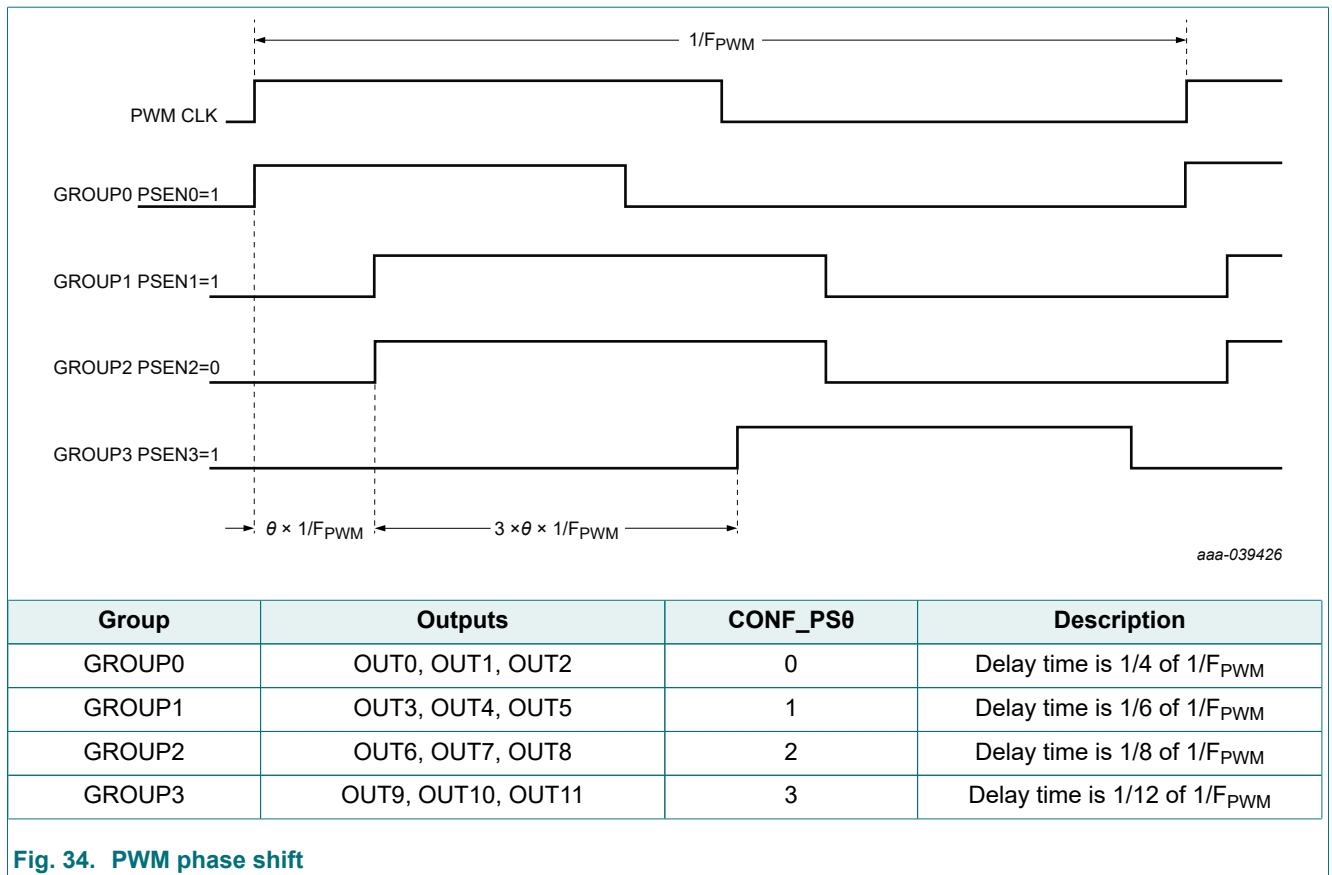


Fig. 34. PWM phase shift

### Linear brightness control

When register CONF\_EXPEN is set to 0, the MSB 8 bits of 12-bit binary input to PWM generator are directly copied from 8-bit register CONF\_PWMOUTn, and the LSB 4 bits are directly copied from 4-bit register CONF\_PWMLOWOUTn. The PWM output duty cycle can be calculated with the following equation:

$$D_{OUTn} = \frac{(16 \times PWMOUTn + PWMLOWOUTn + 1)}{4096} \times 100\% \quad (3)$$

Where:

PWMOUTn is decimal number from 0 to 255

PWMLOWOUTn is decimal number from 0 to 15

n is from 0 to 11

The PWM output duty cycle is linearly controlled by the register CONF\_PWMOUTn and CONF\_PWMLOWOUTn, which provides linear brightness control to each channel output. When CONF\_PWMOUTn is 00h, and CONF\_PWMLOWOUTn is 0h, the channel turns off.

As 12-bit PWM duty cycles require 2 bytes of write operation to update the completed data, the output PWM duty cycle is not changed in between of the two bytes data transmission. NEX13120F-Q100 only updates the PWM duty cycle of any output when its high 8-bit CONF\_PWMOUTn is written. When very fast brightness change is needed, such as fade-in and fade-out effects, it is essential to change the PWM duty cycles of all channels simultaneously. Setting CONF\_SHAREPWM to 1 enables all channels using the PWM duty cycle setting of channels 0 to save communication latency.

### Exponential brightness control

The NEX13120F-Q100 can generate PWM duty-cycle outputs that follow an exponential curve. When the CONF\_EXPEN register is set to 1, the integrated conversion circuit provides a one-to-one conversion from the 8-bit register CONF\_PWMOUTn to a 12-bit binary code that follows an exponential increment, as illustrated in Fig. 35. In exponential mode, the upper 8 bits (MSB) of the PWM configuration register serve as the input to the exponential conversion circuit. The output from this circuit is a 12-bit value, which is used as the duty cycle of the PWM engine.

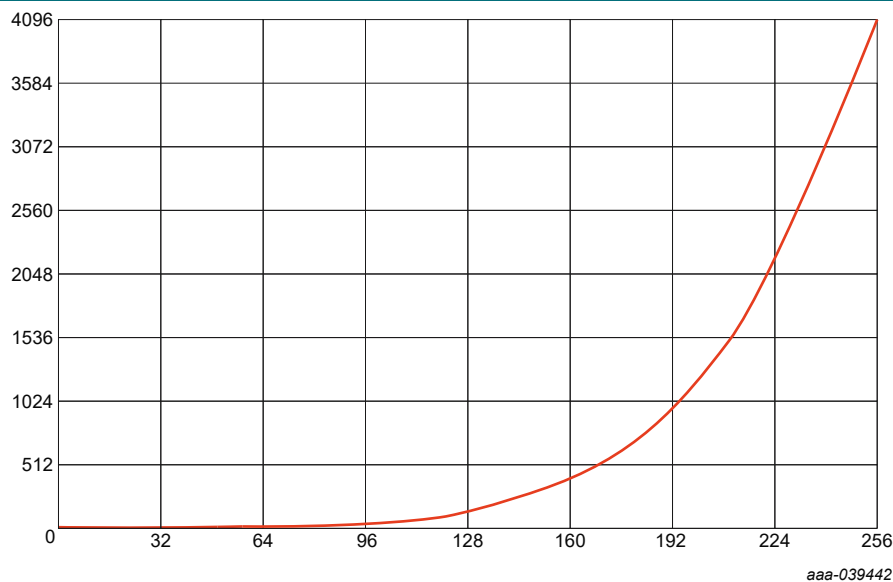


Fig. 35. PWM duty cycle versus 8 bit code for exponential dimming

CONF\_EXPEN bit selects the dimming method between linear or exponential. Setting the bit CONF\_EXPEN to 1 enables the conversion circuit for exponential dimming curve. In exponential PWM dimming mode, 8-bit register CONF\_PWMOUTn is converted to 12-bit PWM duty cycle by conversion circuit automatically. Clearing the bit CONF\_EXPEN to 0 disables the conversion. In this case, users must provide 12-bit PWM duty cycle. CONF\_PWMOUTn stores the high 8-bit of 12-bit PWM duty-cycle information. CONF\_PWMLOWOUTn stores the low 4-bit.

To avoid visible brightness flicker for exponential dimming, choose PWM frequency higher than 2 kHz through setting register CONF\_PWMFREQ. Higher PWM frequency can also avoid the visible LED flash in video display due to the low beat frequency between digital camera shutter frequency and PWM frequency for LED dimming.

During power-up or in Fail-Safe state, the registers CONF\_EXPEN, CONF\_PWMOUTn, CONF\_PWMFREQ are automatically reset to their default values stored in MTP register NV\_EXPEN, NV\_PWMOUTn, NV\_PWMFREQ. CONF\_PWMLOWOUTn is reset to Fh as default value.

In Fail-Safe state, PWM generator only uses 8-bit MTP data from NV\_PWMOUTn to build PWM duty cycle output and ignores the low 4-bits. The PWM duty-cycle calculation is shown in the equation below. When NV\_PWMOUTn is 00h, the channel turns off.

$$D_{OUTn} = \frac{NV\_PWMOUTn + 1}{256} \times 100\% \quad (4)$$

Where:

NV\_PWMOUTn is decimal number from 0 to 255

n is from 0 to 11 for different output channel

#### 14.3.4. Fail-Safe state operation

The NEX13120F-Q100 supports independent channel brightness control through the UART interface. The brightness of each channel is adjustable according to its DC current register I<sub>OUTn</sub>, PWM duty cycle register CONF\_PWMOUTn, CONF\_PWMLOWOUTn and channel enable register CONF\_ENOUTn setting. The brightness of each channel reflects its register setting value immediately after register is successfully updated through the UART interface by master unit.

However, the master unit loses control for all current channels if the UART communication fails between the master unit and the NEX13120F-Q100. For example, the interface cable is broke, by accident. Therefore, the brightness for all output channels of the NEX13120F-Q100 is stuck and the ON and OFF control for all output channels are missing too. To keep the basic ON and OFF control for each output channel, the NEX13120F-Q100 provides a FAIL-SAFE state when the communication to master is lost. For detailed description for FAIL-SAFE state entering and quitting criteria, refer to [Section 14.4](#). When the NEX13120F-Q100 is entering FAIL-SAFE state, all the registers are set to default value or reloaded from MTP, including CONF\_IOUTn, CONF\_PWMOUTn and CONF\_ENOUTn. The pre-programmed settings in the MTP are loaded and the corresponding registers are reset to the default values. During the MTP loading process, all the PWM output channels are disabled, and the channels' faults detected in the NORMAL state are cleared. The NEX13120F-Q100 provides one hardware input pin, FM to turn on or off corresponding current output channels in FAIL-SAFE state. Each current output channel has its own register. The FAIL-SAFE state also allows the NEX13120F-Q100 to operate as a standalone device without master controlling in the system. The FLT pin is used as a fault indicator to achieve one-fails-all-fail or one-fails-others-on diagnostics requirement. When low quiescent current in fault mode is required, the device must be set as one-fails-all-fail. In this case, if a fault is triggered, the device goes into low current fault mode.

#### 14.3.5. 8-bit ADC

NEX13120F-Q100 has integrated a successive-approximation-register (SAR) ADC for diagnostics. It routinely monitors supply voltage if the ADC is idle and stores V<sub>s</sub> conversion results into ADC\_Vs. To manually read the voltage of an ADC channel as listed in [Table 14](#), user must write the 5-bit register CONF\_ADCCH to select channel. Once CONF\_ADCCH register is written, the one-time ADC conversion starts and clears FLAG\_ADCDONE register. If the ADC conversion is completed, the ADC result is available in 8-bit register ADC\_OUT and sets FLAG\_ADCDONE to 1. Reading the ADC\_OUT register also clears FLAG\_ADCDONE, and the FLAG\_ADCDONE is set to 0 after reading completes. Because NEX13120F-Q100 supports PWM control for adjusting LED brightness, the voltage on OUT0 to OUT11 is like a pulse waveform. When the current output is enabled by setting CONF\_ENCHn to 1, the ADC measures the voltage on assigned OUTn after the channel is turned on with t<sub>(diag\_pulse)</sub> delay time, which is programmable by 4-bit register CONF\_ODPW. When the channel is disabled by setting CONF\_ENCHn to 0, the ADC samples the voltage on assigned OUTn at off state. The analog value can be calculated based on the read back binary code with Equation 5 and [Table 14](#). Auto scan for below values

$$\text{AnalogValue} = a + k \times (\text{ADC\_OUT}) \quad (5)$$

Where ADC\_OUT is decimal number from 0 to 255

The NEX13120F-Q100 also provides ADC auto-scan mode for single-LED short-circuit diagnostics. The detailed description for auto-scan mode can be found in [On-demand OFF-state single-LED short-circuit \(SS\) diagnostics](#).

In ADC auto-scan mode, If MAXOUT channel is selected by writing 05h to CONF\_ADCCH, the maximum voltage of OUT0 to OUT11 is recorded into ADC\_OUT register. The maximum channel output voltage is available after at least one output PWM cycle is completed. Based on the measured maximum output voltage and supply voltage, microcontroller is able to regulate supply voltage from previous power stage to minimize the power consumption on the NEX13120F-Q100. To refresh the MAXOUT result, it is recommended to set CONF\_ADCCH to a different value before setting CONF\_ADCCH to 05 each time; MAXOUT value does not refresh, if CONF\_ADCCH remains at 05h. Basically, microcontroller needs to program the output voltage of previous power stage to be just higher than the measured maximum channel output voltage plus the required dropout voltage  $V_{(OUT\_drop)}$  of the NEX13120F-Q100. In this way, the NEX13120F-Q100 can achieve minimum power consumption, and overall power efficiency is optimized.

Table 14. ADC channel definition

CHANNEL	CONF_ADCCH	NAME	ADC CALCULATION PARAMETER (a)	ADC CALCULATION PARAMETER (k)	Comment
0	00h	REF	0.007 V	0.0101 V/LSB	Reference voltage
1	01h	VS	0.0673 V	0.0804 V/LSB	Supply voltage
2	02h	VLDO	0.0465V	0.022 V/LSB	5 V VLDO output voltage
3	03h	TEMPSNS	-242.35 °C	2.152 °C/LSB	Internal temperature sensor
4	04h	IREF	0.9969 µA	0.9969 µA/LSB	Reference current
5	05h	MAXOUT	0.0673 V	0.0804 V/LSB	Maximum channel output voltage
6	06h	VBAT	0.1346 V	0.1608 V/LSB	Vbat pin voltage
8-15	08h- 0Fh	Reserved	Reserved	Reserved	Reserved
16	10h	OUT0	0.0673 V	0.0804 V/LSB	Output voltage channel 0
17	11h	OUT1			Output voltage channel 1
18	12h	OUT2			Output voltage channel 2
19	13h	OUT3			Output voltage channel 3
20	14h	OUT4			Output voltage channel 4
21	15h	OUT5			Output voltage channel 5
22	16h	OUT6			Output voltage channel 6
23	17h	OUT7			Output voltage channel 7
24	18h	OUT8			Output voltage channel 8
25	19h	OUT9			Output voltage channel 9
26	1Ah	OUT10			Output voltage channel 10
27	1Bh	OUT11			Output voltage channel 11
28	1Ch	Reserved	Reserved	Reserved	Reserved
29	1Dh	Reserved	Reserved	Reserved	Reserved
30	1Eh	Reserved	Reserved	Reserved	Reserved
31	1Fh	Reserved	Reserved	Reserved	Reserved

#### 14.3.6. Diagnostic and protection in NORMAL state

The NEX13120F-Q100 has full-diagnostics coverage for supply voltage, current output, and junction temperature. In NORMAL state, the device detects all failures and reports the status out through the FLT pin or FLAG registers, without any actions taken by the device except  $V_{BAT}$  UVLO,  $V_s$  under-voltage, and over-temperature protection. The master controller must handle all fault actions, for example, retry several times and shut down the outputs if the error still exists. The fault behavior in NORMAL state can be found in [Table 17](#).

#### $V_{BAT}$ and VLDO under-voltage lockout diagnostics in NORMAL state

When  $V_{BAT}$  or VLDO voltage drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG\_POR and FLAG\_ERR set to 1. The master controller can write 1 to

register CLR\_POR to clear the FLAG\_POR, write 1 to CLR\_ERR to clear FLAG\_ERR, and the CLR\_POR, CLR\_ERR bit automatically returns to 0.

### Low $V_s$ -supply warning diagnostics in NORMAL state

The NEX13120F-Q100 continuously monitors the  $V_s$  voltage and compares the results with internal threshold  $V_{(LOWVSTH)}$  set by CONF\_ADCLOWVSTH for low- $V_s$  voltage warning. If the  $V_s$  voltage is lower than threshold, the device pulls  $\overline{FLT}$  pin down with one pulsed current sink for 50  $\mu$ s to report the fault and set flag registers including FLAG\_LOWVS and FLAG\_ERR to 1. The fault is latched in flag registers. When the  $V_s$  voltage rises above low- $V_s$  warning threshold, the master controller must write 1 to register CLR\_ERR to clear FLAG\_LOWVS and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0. The low- $V_s$  warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection. When the voltage applied on  $V_s$  pin is higher than the threshold  $V_{(LOWVSTH)}$ , the NEX13120F-Q100 enables LED open-circuit and single-LED short-circuit diagnosis. When  $V_s$  is lower than the threshold  $V_{(LOWVSTH)}$ , the device disables LED-open-circuit detection and single-LED short-circuit diagnosis. Because when  $V_s$  drops below the maximum total LED forward voltage plus required  $V_{(OUT\_drop)}$  at required current, the NEX13120F-Q100 is not able to deliver sufficient current output. The device pulls the voltage of each output channel as close as possible to the  $V_s$ . In this condition, the LED open-circuit fault or single-LED short-circuit fault can be detected and reported by mistake. Setting the low- $V_s$  warning threshold high enough can avoid the LED open-circuit and single LED short-circuit fault being detected when  $V_s$  drops to low. The  $V_{(LOWVSTH)}$  is programmable from 4 V to 19 V.

### $V_s$ -supply under-voltage diagnostics in NORMAL state

The NEX13120F-Q100 provides an internal analog comparator to monitor the  $V_s$  voltage for under-voltage protection. If the  $V_s$  voltage falls below the internal threshold,  $V_{(Vs\_th\_fall)}$ , the device pulls the  $\overline{FLT}$  pin low with constant current sink to report the fault and set flag registers including FLAG\_VSUV and FLAG\_ERR to 1. The supply under-voltage detection is used to disable all current output. When the voltage applied on the  $V_s$  pin is higher than the threshold  $V_{(Vs\_th\_rise)}$ , the NEX13120F-Q100 enables all current outputs. When  $V_s$  is lower than the threshold  $V_{(Vs\_th\_fall)}$ , the device disables every output to avoid the unwanted LED flickering or output fault triggered improperly.

The fault is latched in flag registers. When the supply voltage rises above  $V_{(Vs\_th\_rise)}$ , the master controller must write register CLR\_ERR to 1 to clear FLAG\_VSUV and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### Reference diagnostics in NORMAL state

NEX13120F-Q100 integrates diagnostics for REF resistor open and short fault in NORMAL state. The device monitors the reference current  $I_{(REF)}$  set by external resistor  $R_{(REF)}$ . Use Equation 6 to calculate the  $I_{(REF)}$ . If the current output from REF pin  $I_{(REF)}$  is lower than  $I_{(REF\_OPEN\_th)}$ , the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin  $V_{(REF)}$  is lower than  $V_{(REF\_SHORT\_th)}$ . The device pulls the  $\overline{FLT}$  pin down with constant current sink and sets flag registers including FLAG\_REF and FLAG\_ERR to 1. The fault is latched in flag registers.

After the REF pin  $I_{(REF)}$  and  $V_{(REF\_SHORT\_th)}$  recover to normal, the device releases  $\overline{FLT}$  pin pull-down automatically and the master controller must send CLR\_ERR to clear FLAG\_REF and FLAG\_ERR. CLR\_ERR automatically returns to 0.

In NORMAL state, the device does not perform any actions automatically when reference resistor fault is detected. However, the output may not work properly, and the output current may be operating at high current level when REF short. It is recommended for master controller to shut down the device outputs and report error to upper level control system such as body control module (BCM).

The reference current  $I_{(REF)}$  is set by external resistor  $R_{(REF)}$ . The  $I_{(REF)}$  can be calculated with Equation 6.  $V_{(REF)}$  typically is 1.235V.

$$I_{(REF)} = \frac{V_{(REF)}}{R_{(REF)}} \quad (6)$$

### Pre-thermal warning in NORMAL state

The NEX13120F-Q100 has pre-thermal warning at typical 135°C. When the junction temperature,  $T_j$ , of NEX13120F-Q100 rises above pre-thermal warning threshold, the device reports pre-thermal warning, pull  $\overline{FLT}$  pin with pulsed current sink for 50  $\mu$ s and sets the flag registers including FLAG\_PRETSD and FLAG\_ERR to 1. The fault is latched in flag registers. When the junction temperature of NEX13120F-Q100 falls below pre-thermal warning threshold, the master controller must write 1



to CLR\_ERR register to clear FLAG\_PRETSD and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0. When more accurate thermal measurement on LED unit is required, one current output channel can be sacrificed to provide current bias to external thermal resistor, such as PTC or NTC. The voltage of external thermal resistor can be measured by integrated ADC to acquire the temperature information of the thermal resistor located area. The master controller can determine actions based on the acquired temperature information to turn off or reduce current output.

### Over-temperature protection in NORMAL state

The NEX13120F-Q100 has over-temperature protection at  $T_{(TSD1)}$ , typical 175 °C. When device junction temperature  $T_j$  further rises above over-temperature protection threshold, the device turns off all output drivers, pulls the  $\overline{FLT}$  pin low with constant current sink to report fault, and sets the flag registers including FLAG\_TSD and FLAG\_ERR to 1. The fault is latched in flag registers. When the junction temperature falls below  $T_{(TSD1)} - T_{(TSD1\_HYS)}$ , the device resumes all outputs and releases  $\overline{FLT}$  pin pull-down. The master controller must write 1 to CLR\_ERR to clear FLAG\_TSD and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### Over-temperature shutdown in NORMAL state

When the  $T_j$  rises too high above  $T_{(TSD2)}$ , 180 °C typically, the NEX13120F-Q100 turns off the internal linear regulator, VLDO output to shut down all the analog and digital circuit. The  $\overline{FLT}$  pin is pulled down by constant current sink to report the fault, and the FLAG\_POR and FLAG\_ERR are all set to 1. When the  $T_j$  drops below  $T_{(TSD2)} - T_{(TSD2\_HYS)}$ , the NEX13120F-Q100 restarts from POR state with all the registers cleared to default value and  $\overline{FLT}$  pin released. The master controller must write 1 to CLR\_POR to clear both FLAG\_POR and FLAG\_ERR after fault removal. The CLR\_POR bit automatically returns to 0.

### Communication loss diagnostic in NORMAL State

The NEX13120F-Q100 monitors the UART interface for communication with an internal watchdog timer. Any successful non-broadcast communication with correct CRC and address matching target device automatically resets the timer. If the watchdog timer overflows, the device automatically switches to Fail-Safe state as indicated by external FM input.

- If FM = 0, the device switches to Fail-Safe state 0
- If FM = 1, the device switches to Fail-Safe state 1

The watchdog timer is programmable by 4-bit register CONF\_WDTIMER. The NEX13120F-Q100 can directly enter Fail-Safe states from normal mode by burning NV\_WDTIMER to 0xFh. Disabling the watchdog timer by setting CONF\_WDTIMER to 0x0h prevents the device from getting into Fail-Safe state.

### LED open-circuit diagnostics in NORMAL State

The NEX13120F-Q100 integrates LED open-circuit diagnostics to allow users to monitor LED status in real time. The device monitors voltage difference between  $V_s$  and  $OUT_n$  to judge if there is any open-circuit failure. The  $V_s$  voltage is also monitored in parallel with programmable threshold to determine if  $V_s$  is high enough for open-circuit diagnostics.

The open-circuit monitor is only effective during PWM-ON state with programmable minimal pulse width greater than  $t_{(ODPW)}$ . The  $t_{(ODPW)}$  is programmed by register ODPW. If PWM on-time is less than  $t_{(ODPW)}$ , the device does not report any open-circuit fault. When the device supply voltage  $V_s$  is below the threshold  $V_{(LOWVSTH)}$  set by register CONF\_ADCLOWVSTH, the LED open-circuit is not detected nor reported. When the voltage difference  $V_s - V_{(OUT_n)}$  is below threshold  $V_{(OPEN\_th\_rise)}$  with duration longer than  $t_{(ODPW)}$ , and the device supply voltage  $V_s$  is above the threshold  $V_{(LOWVSTH)}$  set by register CONF\_LOWVSTH, the NEX13120F-Q100 pulls the  $\overline{FLT}$  pin down with one pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_OPENCH<sub>n</sub>, FLAG\_OUT and FLAG\_ERR to 1. In NORMAL state, the device does not take any actions in response to the LED open-circuit fault and waits for the master controller to determine the protection behavior. The fault is latched in flag registers. When the voltage difference  $V_s - V_{(OUT_n)}$  rises above threshold  $V_{(OPEN\_th\_rise)}$  with duration longer than  $t_{(ODPW)}$ , or the device supply voltage  $V_s$  is below the threshold  $V_{(LOWVSTH)}$ , the master controller must write 1 to CLR\_ERR to clear FLAG\_OPENCH<sub>n</sub>, FLAG\_OUT and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### LED short-circuit diagnostics in NORMAL state

The NEX13120F-Q100 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold for reporting  $OUT_n$  short to GND fault. The short-circuit detection is only effective during PWM-ON state with programmable



minimal pulse width of  $t_{(ODPW)}$ . The  $t_{(ODPW)}$  is programmable by register ODPW. If PWM on-time is less than  $t_{(ODPW)}$  the device can not report any short-circuit fault. When the voltage  $V_{(OUTn)}$  is below threshold  $V_{(SG\_th\_fall)}$  with duration longer than deglitch timer length of  $t_{(ODPW)}$ , the device pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_SHORTCHn, FLAG\_OUT and FLAG\_ERR. In NORMAL state, the device does not take any actions in response to the LED short-circuit fault and waits for the master controller to determine the protection behavior. The fault is latched in flag registers. When the voltage  $V_{(OUTn)}$  rises above threshold  $V_{(SG\_th\_rise)}$  with duration longer than deglitch timer length of  $t_{(ODPW)}$ , the master controller must write 1 to CLR\_ERR to clear FLAG\_SHORTCHn, FLAG\_OUT and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### On-demand OFF-state invisible diagnostics

It is commonly required to ensure there is no fault on each LED load before lighting them up, especially for LED animation. Otherwise, the LED fault is detected in the middle of the admiration pattern, which results in a random and uncertain failure animation pattern. NEX13120F-Q100 provides a solution to diagnose the LED open-circuit or LED short-circuit fault without lighting up the LEDs. With this feature, the master controller can initiate the on-demand invisible diagnostics before commencing the animation sequence. If one of the channels fails, the device is able to detect it immediately instead of only when the fault channel is turned on in traditional diagnostics mode. To initiate the on-demand invisible diagnostics, the master controller writes register CONF\_INVDIAGSTART to 1. The register CONF\_INVDIAGSTART returns to 0 automatically in the next clock cycle. Once the diagnostics started, the on-demand diagnostics ready flag FLAG\_ODREADY is cleared to 0. Once the diagnostics finished, the FLAG\_ODREADY is set to 1. If any channel has output failures, its on-demand diagnostic flag FLAG\_ODDIAGCHn is set to 1. To ensure the invisibility of the diagnostics, the NEX13120F-Q100 outputs only a small DC current in short period to each output channel and detects if there is any LED open-circuit or LED short-circuit failures. The output DC current  $I_{(ODIOUT)}$  can be adjusted to a proper value by setting the DC current CONF\_ODIOUT and ignoring the DC current setup by register CONF\_IOUTn. The pulse-width  $t_{(ODPW)}$  of output DC current can be programmable by CONF\_ODPW and neglecting duty cycle configuration by register CONF\_PWMOUTn. At the end of the current output pulse, if there is any LED open-circuit fault, the NEX13120F-Q100 pulls the FLT pin down with one pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_OPENCHn, FLAG\_OUT and FLAG\_ERR to 1. If there is any LED short-circuit fault, the NEX13120F-Q100 pulls the FLT pin down with one pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_SHORTCHn, FLAG\_OUT and FLAG\_ERR to 1. The master controller must write 1 to CLR\_ERR register to clear fault flags after the fault removal is verified by another on-demand off-state invisible diagnostics. It is recommended to turn off all output channels by setting CONF\_ENCHn to 0 before invisible diagnostics. For invisible diagnostics mode, it is required to have a short-pulse and low output current to avoid lighting up LEDs. However, the diagnostics are strongly affected by large loading capacitance. If the invisible diagnostics pulse fails to charge output capacitance above short-circuit threshold, the device reports a false short-circuit failure. If pulse failed to charge output above open-circuit threshold at maximum supply voltage, the device does not report open-circuit fault correctly. Thus, the DC current and period of the detection pulse must be carefully selected based on the capacitance value at output in real applications.

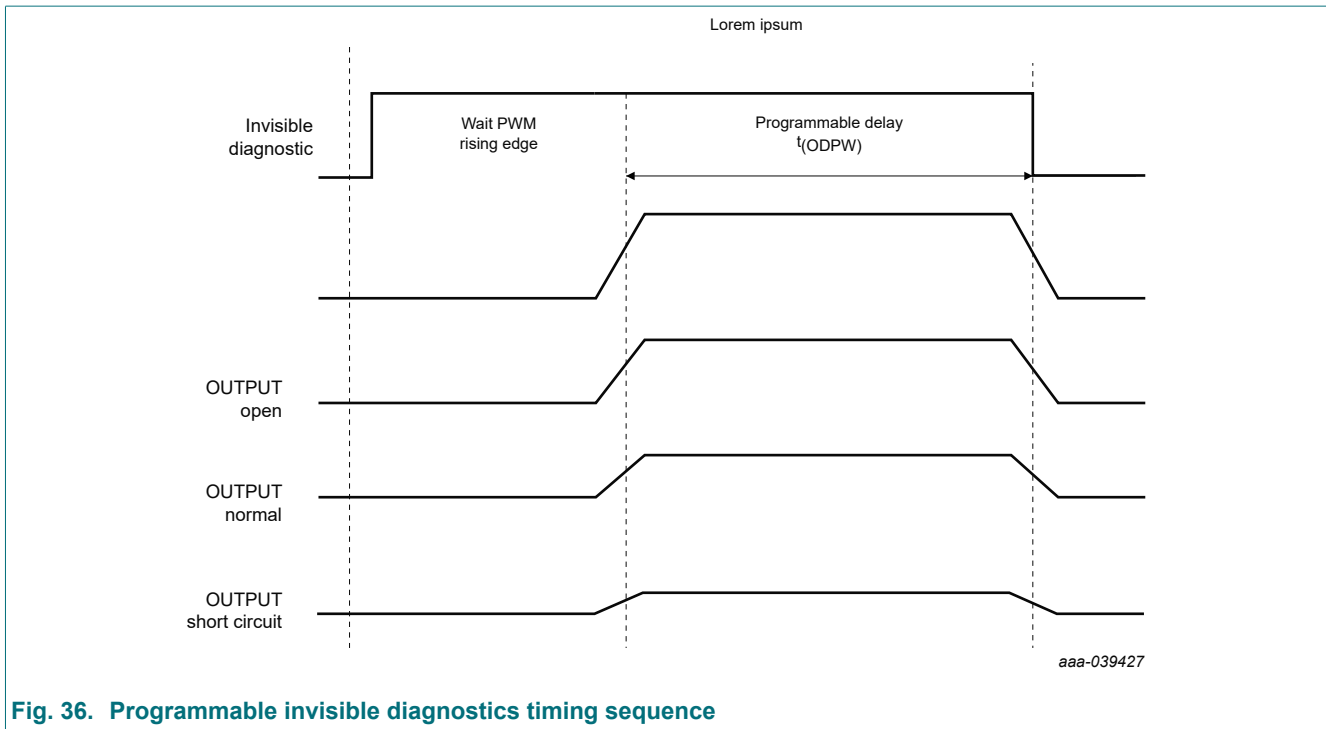


Fig. 36. Programmable invisible diagnostics timing sequence

### On-demand OFF-state single-LED short-circuit (SS) diagnostics

To provide single-LED short-circuit diagnostics, the NEX13120F-Q100 uses internal ADC to compare the output channel voltage with respect to pre-set threshold  $V_{(ADCSHORTTH)}$ . Setting the register CONF\_SSSTART to 1 starts the diagnostics immediately. The CONF\_SSSTART returns to 0 in the next clock cycle. Once the diagnostics starts, the on-demand diagnostics ready flag FLAG\_ODREADY are cleared to 0. Once the diagnostics finishes, the FLAG\_ODREADY are set to 1 in off-state single-LED short-circuit diagnostics, once the master controller initiates single-LED short-circuit diagnostics by setting the register CONF\_SSSTART, the device sequentially turns on all outputs starting from OUT0 with DC current  $I_{(ODIOUT)}$  programmed by register CONF\_ODIOUT and pulse width  $t_{(ODPW)}$  programmable by CONF\_ODPW. At the end of pulse, the device initiates an AD conversion. As long as the completion of ADC conversion, the result is compared with pre-set threshold  $V_{(ADCSHORTTHn)}$  and starts the diagnostics for the next channel. After all channels have been checked, the NEX13120F-Q100 also checks if the supply voltage is over  $V_{(ADCLOWVSTH)}$  to make sure the device is not in low-dropout conditions. If the supply voltage is truly lower than  $V_{(ADCLOWVSTH)}$ , the single-LED short-circuit fault cannot be detected and reported. If the supply voltage is high enough, and any one channel output voltage is less than pre-set threshold  $V_{(ADCSHORTTHn)}$ , the NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set the flag register including FLAG\_ODDIAGCHn, FLAG\_OUT and FLAG\_ERR to 1. The master controller must write 1 to CLR\_ERR register to clear the fault flags after fault removal is verified by another on-demand off-state single-LED short-circuit diagnostic. The configurable DC current  $I_{(ODIOUT)}$  and pulse width  $T_{(ODPW)}$  can be used to minimize the optical impact during on-demand diagnostics. It is recommended to use the normal current setting and short pulse-width to avoid visible pulse; however, the parasitic capacitance impact at each output must be taken care of to leave enough charging time and avoid false alarm. Low DC current setting also reduces LED forward voltage, which also affects the integrity of the detection. Thus, the threshold set by CONF\_ADCSHORTTHn must be selected carefully. Setting CONF\_ODIOUT to 0xFh uses the channel current setting by registering CONF\_IOUTn as on-demand pulse current. The NEX13120F-Q100 provides two alternative threshold  $V_{(ADCSHORTTH0)}$  and  $V_{(ADCSHORTTH1)}$  for single-LED short-circuit detection selected by ADCSHORTTHCHn independently for each current output. The  $V_{(ADCSHORTTH0)}$  is selected for current OUTn when ADCSHORTTHCHn is set to 0, however  $V_{(ADCSHORTTH1)}$  is selected when ADCSHORTTHCHn is set to 1. The actual voltage value for  $V_{(ADCSHORTTH0)}$  and  $V_{(ADCSHORTTH1)}$  is programmable by two 8-bit registers CONF\_ADCSHORTTH0 and CONF\_ADCSHORTTH1 from 0 V to 20.56 V at 80 mV interval. The  $V_{(ADCSHORTTHn)}$  can be calculated with below equation:

$$V_{(ADCSHORTTHn)} = a + K \times (\text{CONF\_ADCSHORTTHn}) \quad (7)$$

Where:

$$a = 0.0673 \text{ V}$$

$K = 0.0804 \text{ V/LSB}$

CONF\_ADCSHORTTHn is decimal number from 0 to 255

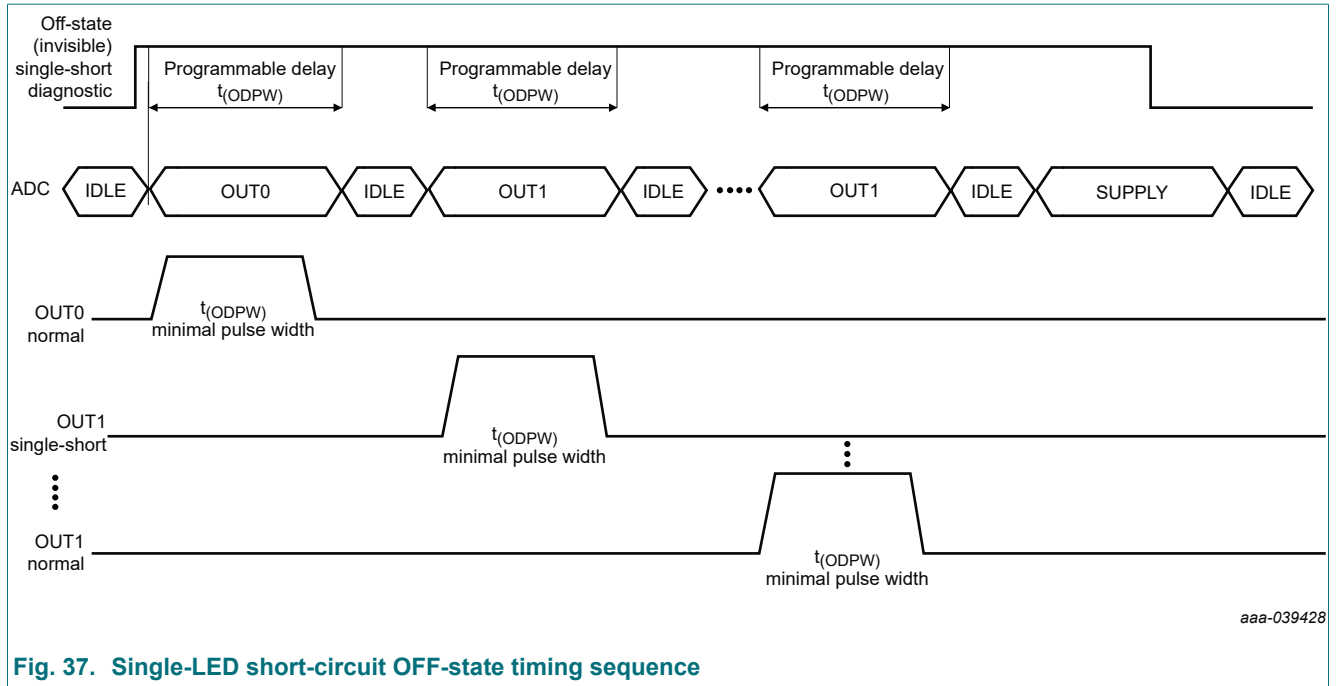


Fig. 37. Single-LED short-circuit OFF-state timing sequence

### Single-LED short-circuit detection in NORMAL state (auto scan)

In order to check LED single-LED short-circuit issue during lighting up, the NEX13120F-Q100 also provides automatically single-LED short-circuit (AutoSS) diagnostic. Setting the register CONF\_AUTOSS to 1 enables the scanning of each current out channel at the beginning of every PWM cycle. The AutoSS detection takes 4 PWM cycles to complete scanning 12 output channels. One group takes one PWM cycle. After sampling 12 output channel voltages, ADC automatically scans other values, includes  $V_{REF}$ ,  $V_{LDO}$ ,  $TEMP_{SNS}$ ,  $I_{REF}$ ,  $V_{BAT}$ ,  $V_{BG1}$ . Fig. 38 shows the details.

For function safety considerations, if CONF\_AUTOSS is set to 1, NEX13120F-Q100 compares all ADC out value with related threshold. Find the threshold in Table 17. On PWM rise edge, the device waits for a programmable delay  $T_{(ODPW)}$  programmable by CONF\_ODPW to allow output voltage settle and starts AD conversion. The minimal pulse width of PWM must be longer than programmable delay  $T_{(ODPW)}$  plus 3 times AD conversion time  $T_{(CONV)}$  to make sure 3 output channels can be scanned in one PWM cycle. The NEX13120F-Q100 checks low- $V_s$  warning to avoid reporting the single-LED short-circuit fault by mistake in low-dropout mode. If the supply voltage is truly lower than  $V_{(ADCLOWVSTH)}$ , the single-LED short-circuit fault cannot be detected and reported. If the supply voltage is high enough, and any one channel output voltage is less than pre-set threshold  $V_{(ADCSHORTTH)}$ , the NEX13120F-Q100 pulls FLT pin down with pulsed current sink for 50  $\mu s$  to report fault and set the flag register including FLAG\_ODDIAGCHn, FLAG\_OUT and FLAG\_ERR to 1. The master controller must write 1 to CLR\_ERR register to clear the fault flags. The NEX13120F-Q100 provides two alternative threshold  $V_{(ADCSHORTTH0)}$  and  $V_{(ADCSHORTTH1)}$  for single-LED short-circuit detection selected by ADCSHORTTHCHn independently for each current output. The  $V_{(ADCSHORTTH0)}$  is selected for current OUTn when ADCSHORTTHCHn is set to 0, however,  $V_{(ADCSHORTTH1)}$  is selected when ADCSHORTTHCHn is set to 1. The actual voltage value for  $V_{(ADCSHORTTH0)}$  and  $V_{(ADCSHORTTH1)}$  is programmable by two 8-bit registers CONF\_ADCSHORTTH0 and CONF\_ADCSHORTTH1 from 0 V to 20.56 V at 80 mV interval. If any channel is disabled by CONF\_ENCHn to 0, the AutoSS diagnostics skips the channel. During the single-LED short-circuit diagnostics, the ADC keeps the on-demand ADC conversion request pending until single-LED short-circuit diagnostics finishes. When CONF\_AUTOSS is set to 1, selecting MAXOUT by writing 05h to CONF\_ADCCH automatically outputs the ADC conversion result to register ADC\_OUT for the output channel with the highest voltage in all scanned channels. The master controller can adjust the previous power stage output voltage based on the voltage difference read back from register ADC\_Vs and ADC\_OUT to minimize the voltage drop on the NEX13120F-Q100 as well as temperature rising if the output voltage of previous power stage is programmable by digital interface.

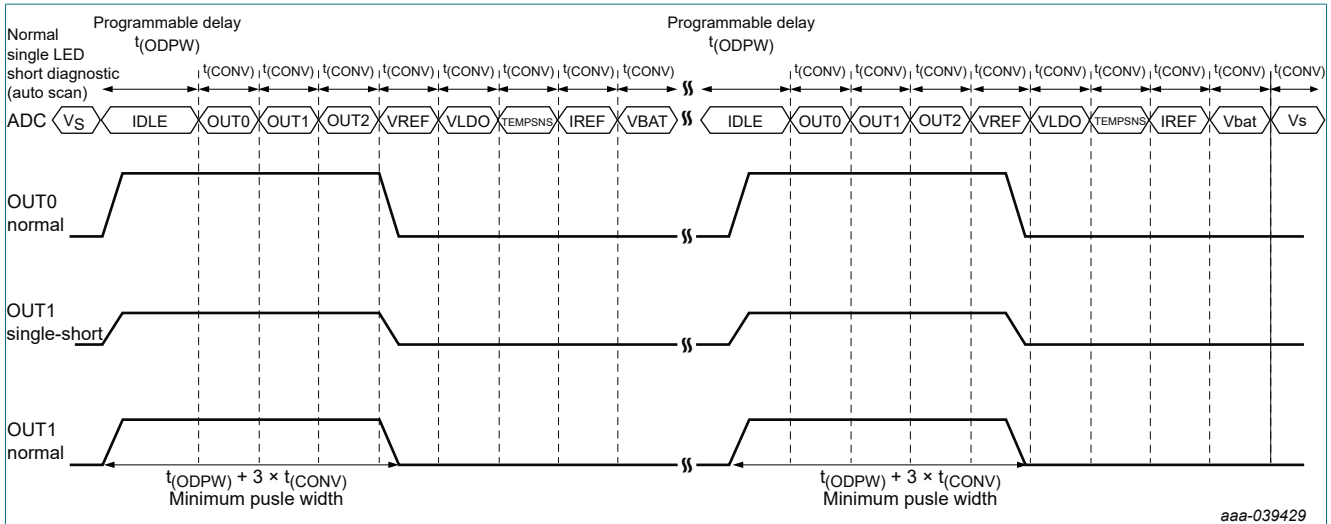


Fig. 38. Single-LED short-circuit on-state diagnostics timing sequence

### MTP CRC error and CONF\_CRC in NORMAL state

The NEX13120F-Q100 implements MTP CRC check after loading the MTP code to configuration register in NORMAL state. The calculated CRC result is sent to register CALC\_MTPCRC and compared to the data in register MTPCRC, which stores the CRC code for all MTP registers. If the code in register CALC\_MTPCRC is not matched to the code in register MTPCRC, the NEX13120F-Q100 pulls the  $\overline{FLT}$  pin down with pulsed current sink for 50  $\mu$ s to report the fault and set the registers including FLAG\_MTPCRC and FLAG\_ERR to 1. The NEX13120F-Q100 only loads MTP to corresponding registers one time during initialization state. Reloading the MTP triggers the MTP CRC check. The master controller must write CLR\_ERR to 1 to clear the fault flags, and the CLR\_ERR bit automatically returns to 0. The CRC code algorithm for multiple bytes of binary data is based on the polynomial,  $X^8 + X^5 + X^4 + 1$ . The CRC code contains 8 bits binary code, and the initial value is FFh. All bits code shift to MSB direction for 1 bit with three exclusive-OR calculation. A new CRC code for one byte input can be generated after repeating the 1-bit shift and three exclusive-OR calculation for 8 times. Based on this logic, the CRC code can be calculated for all the EEPROM register byte and configured register byte. To be compliant with the popular part in the market, users can configure CRC calculation range, when NV\_CRC\_SEL is set to 0, the MTPCRC calculation ignores register BCh to BFh, CONF\_CRC calculation ignores register 66h to 6Bh. CRC calculation range is shown in [Table 15](#):

Table 15. CRC calculation definition

Register setting		CRC calculation range
CONF_CRC_SEL = 0	CALC_NVCRC	80h to 8Bh, A0h to ABh, C0h to CEh
	CALC_CONF_CRC	00h to 0Bh, 20h to 2Bh, 40h to 4Bh, 50h to 51h, 54h to 5Bh, 61h to 64h + 0x00
CONF_CRC_SEL = 1	CALC_NVCRC	80h to 8Bh, A0h to ABh, BCh to BFh, C0h to CEh
	CALC_CONF_CRC	00h to 0Bh, 20h to 2Bh, 3Ch to 3Fh, 40h to 4Bh, 50h to 51h, 54h to 5Bh, 5Ch-5Eh, 61h to 64h + 0x00

### Communication loss diagnostic in NORMAL state

The NEX13120F-Q100 monitors the UART interface for communication with an internal watchdog timer. Any successful non-broadcast communication with correct CRC and address matching target device automatically resets the timer. If the watchdog timer overflows, device automatically switches to FAIL-SAFE state and sets the FLAG\_FS to 1. The master controller can access the NEX13120F-Q100 and write 1 to CLR\_FS to set the device to NORMAL state again when the communication recovers. The watchdog timer is programmable by 4-bit register CONF\_WDTIMER. The NEX13120F-Q100 can directly enter FAIL-SAFE state from NORMAL state by burning MTP of NV\_WDTIMER to Fh. Disabling the watchdog timer by setting CONF\_WDTIMER to 0h prevents the device from getting into FAIL-SAFE state.

## ECC protection

For protecting possible single-bit memory content error. Each byte to be stored in the MTP is encoded with 6-bit ECC parity bits. These 6 bits together with the original 8 data bits occupy two bytes in the MTP memory at 2 consecutive addresses. The ECC decoder can correct any single-bit error in the 14 bits (data and parity) read value. The corrected data is then sent to the MTP. When memory content error occurs, NEX13120F-Q100 pulls the  $\overline{\text{FLT}}$  pin down with pulsed current sink for 50  $\mu\text{s}$  to report the fault and set the registers including FLAG\_ECC and FLAG\_ERR to 1. Writing 1 to CLR\_ERR can clear FLAG\_ECC and FLAG\_ERR. Reloading the MTP triggers the ECC fault reporting.

## Initial competitor self-test

In order to ensue the diagnostic competitor is normal, NEX13120F-Q100 integrates self-test function during power-up, if competitor is abnormal, NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu\text{s}$  to report the fault and set registers including FLAG\_CMP and FLAG\_ERR to 1. Writing 1 to CLR\_ERR can clear FLAG\_CMP and FLAG\_ERR.

## Fault masking

NEX13120F-Q100 provides fault masking function using masking registers. The device is capable of masking faults by channels or by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG\_OUT register, FLAG\_ERR register, and  $\overline{\text{FLT}}$  pin output. [Table 16](#) lists the detailed description for each fault mask register in NORMAL state. To disable diagnostics on a single channel, setting CONF\_DIAGENCHn registers to 0 disables open-circuit, LED short-circuit and single-LED short circuit diagnostics of channel n and thus no fault of this channel is reported to FLAG\_OPENCHn, FLAG\_SHORTCHn, FLAG\_ODDIAGCHn, FLAG\_OUT or FLAG\_ERR registers, or to the  $\overline{\text{FLT}}$  pin output.

**Table 16. Fault masking in NORMAL state**

Fault detected	Mask register	FLAG name	FLT pin
$V_s$ low warning	CONF_MASKLOWVS=1	FLAG_LOWVS=1	No action
	CONF_MASKLOWVS=0	FLAG_LOWVS=1 FLAG_ERR=1	One pulse pulled down for 50 $\mu\text{s}$
$V_s$ under-voltage	CONF_MASKVSUV=1	FLAG_VSUV=1	No action
	CONF_MASKVSUV=0	FLAG_VSUV=1 FLAG_ERR=1	Constant pulled down
Reference fault	CONF_MASKREF=1	FLAG_REF=1	No action
	CONF_MASKREF=0	FLAG_REF=1 FLAG_ERR=1	Constant pulled down
Pre-thermal warning	CONF_MASKPRETSD=1	FLAG_PRETSD=1	No action
	CONF_MASKPRETSD=0	FLAG_PRETSD=1 FLAG_ERR=1	One pulse pulled down for 50 $\mu\text{s}$
Over-temperature protection	CONF_MASKTSD=1	FLAG_TSD=1	No action
	CONF_MASKTSD=0	FLAG_TSD=1 FLAG_ERR=1	Constant pulled down
MTPROMCRC error	CONF_MASKMTPCRC=1	FLAG_MTPCRC=1	No action
	CONF_MASKMTPCRC=0	FLAG_MTPCRC=1 FLAG_ERR=1	One pulse pulled down for 50 $\mu\text{s}$
LED open-circuit fault	CONF_MASKOPEN=1	FLAG_OPENCHn=1	No action
	CONF_MASKOPEN=0	FLAG_OPENCHn=1 FLAG_OUT=1 FLAG_ERR=1	One pulse pulled down for 50 $\mu\text{s}$
LED short-circuit fault	CONF_MASKSHORT= 1	FLAG_SHORTCHn= 1	No action

Fault detected	Mask register	FLAG name	FLT pin
	CONF_MASKSHORT= 0	FLAG_SHORTCHn= 1 FLAG_OUT=1 FLAG_ERR=1	One pulse pulled down for 50 $\mu$ s
Auto single LED short-circuit fault	CONF_MASKSLS=1	FLAG_ODDIAGCHn=1	No action
	CONF_MASKSLS=0	FLAG_ODDIAGCHn=1 FLAG_OUT=1 FLAG_ERR=1	One pulse pulled down for 50 $\mu$ s

### 14.3.7. Additional fault detection for function safety

The NEX13120F-Q100 is developed according to ISO 26262 with process complying with ASIL B. NEX13120F-Q100 integrates many fault detection functions based on the need for functional safety. The detection criteria are listed in [Table 17](#).

#### Address pin failure detection

See [Address check function](#) for detailed description.

#### CONF register value abnormal detection

When CONF\_CONFCRC\_FD = 1, NEX13120F-Q100 calculates configured CRC when receiving new message.

If the CRC calculation is not finished, the new message interrupts the current CRC calculation and restarts the calculation.

- If the CONF register is changed by new message, NEX13120F-Q100 updates the CRC result to register CALC\_CONFCRC. See [Table 15](#) for the calculation range of CONFCRC register. When CONF\_CONFCRC\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.
- If the new message does not change CONF register, NEX13120F-Q100 compares the calculation result with CALC\_CONFCRC value, if the two results do not match, the device pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_CONFCRC, FLAG\_ERR. When CONF\_CONFCRC\_FD = 0, the device does not report this fault.

#### PWM output mismatch detection

When CONF\_PWM\_FD = 1 and channel is ON, the internal PWM engine detects the output duty to see whether the duty matches the setting in register. If not matched, NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_CONFCRC and FLAG\_ERR. When CONF\_PWM\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.

#### State switch error detection

When CONF\_STA\_FD = 1, NEX13120F-Q100 compares double state machine output results. If the results are not the same, NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_STA and FLAG\_ERR. When CONF\_STA\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.

#### OSC warning detection

When CONF\_OSC\_FD = 1, NEX13120F-Q100 uses ring oscillator to counter OSC clock. If the counter overflows, NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report the warning and set flag registers including FLAG\_OSC and FLAG\_ERR. When the warning is triggered, NEX13120F-Q100 can still work with slightly shifted frequency.

If the internal OSC is completely chaotic, it triggers communication loss. When CONF\_OSC\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.

### I<sub>REF</sub> out of range

Internal ADC samples I<sub>REF</sub> value

- after initialization delay counter is reached
- initialization delay counter is in the count but CLR\_POR is set to 1

The initial sample value is stored in ADC\_IREF register.

When Auto Scan is enabled (CONF\_AUTOSS=1) and CONF\_IREF\_FD is set to 1, NEX13120F-Q100 compares the sample value with the initial value in ADC\_IREF, if the deviation between the original values exceeds the limit value, NEX13120F-Q100 sets FLAG\_ERR and FLAG\_IREF to 1 and pulls down FLT output with a pulse of 50  $\mu$ s accordingly. When CONF\_IREF\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.

### V<sub>BG</sub> abnormal detection

When CONF\_AUTOSS=1 and CONF\_VBG\_FD = 1, NEX13120F-Q100 compares ADC sample V<sub>BG</sub> value with V<sub>BG</sub> abnormal threshold. If the sampled VBG value is out of range, NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_VBG and FLAG\_ERR. When CONF\_VBG\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.

### Low V<sub>bat</sub> warning detection

When CONF\_AUTOSS=1 and CONF\_LOWVBAT\_FD= 1, NEX13120F-Q100 compares ADC sampled VBAT value with VBAT threshold, the threshold is set by register CONF\_LOWVBATTH (range is from 4 V to 35 V, CONF\_LOWVBATTH \* 1 V + 4 V). When sampled V<sub>BAT</sub> < V<sub>bat</sub> threshold, NEX13120F-Q100 pulls the FLT pin down with pulsed current sink for 50  $\mu$ s to report fault and set flag registers including FLAG\_LOWVBAT and FLAG\_ERR. When CONF\_LOWVBAT\_FD = 0, NEX13120F-Q100 does not report FLAG\_ERR when this fault is triggered.



Table 17. Diagnostics in NORMAL state

Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	Fault pin	Recovery
VBAT UVLO Base on comparator	$V_{(Vbat)} < V_{(POR\_fall)}$	Comparator	Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR
VLDO UVLO Base on comparator	$V_{(VLDO)} < V_{(VLDO\_POR\_fall)}$	Comparator	Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR
VLDO OV	$V_{(VLDO)} > V_{(VLDO\_OV\_rise)}$	Comparator	No action	FLAG_LDOOV FLAG_ERR	Constant pulled down	Automatically recovery upon fault removal Clear fault flag with CLR_ERR
Low Vbat warning	$V_{(Vbat)} < V_{(LOWVBATTH)}$	ADC (CONF_AUTOSS=1) and CONF_LOWVBAT_FD=1	No action	FLAG_LOWVBAT FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR
Low Vs warning	$V_s < V_{(ADCLOWVSTH)}$	ADC	Disable fault type *	FLAG_LOWVS FLAG_ERR (maskable)	One pulse pulled down for 50 $\mu$ s (maskable)	Clear fault flag with CLR_ERR
Vs undervoltage	$V_s < V_{(Vs\_th\_fall)}$	Comparator or ADC(CONF_AUTOSS = 1)	Turn off all outputs	FLAG_VSUUV FLAG_LOWVS FLAG_ERR (maskable)	Constant pulled down(maskable)	Automatically recovery and release FLT pin upon fault removal Clear fault flag with CLR_ERR
Reference fault	$V_{(REF)} < V_{(REF\_SHORT\_th)}$ or $I_{(REF)} < I_{(REF\_OPEN\_th)}$	Comparator or ADC(CONF_AUTOSS = 1)	No action	FLAG_REF FLAG_ERR (maskable)	Constant pulled down(maskable)	Automatically release FLT pin upon fault removal Clear fault flag with CLR_ERR
Pre-thermal warning	$T_j > T_{(PRETSD)}$	Comparator or ADC(CONF_AUTOSS = 1)	No action	FLAG_PRETSD	One pulse pulled down for 50 $\mu$ s (maskable)	Clear fault flag with CLR_ERR
Overtemperature protection	$T_j > T_{(TSD1)}$	Comparator or ADC(CONF_AUTOSS = 1)	Turn off all outputs	FLAG_PRETSD FLAG_TSD FLAG_ERR (maskable)	Constant pulled down(maskable)	Automatically recover upon fault removal Clear fault flag with CLR_ERR
Overtemperature shutdown	$T_j > T_{(TSD2)}$	Comparator	Turn off LDO	FLAG_PORFLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good Clear fault flag with CLR_POR



Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	Fault pin	Recovery
LED open-circuit fault *	$V_s - V_{(OUTn)} < V_{(OPEN\_th\_rise)}$ and $V_s > V_{(LOWVSTH)}$	PWM pulse width greater than $t_{(ODPW)}$ $CONF\_ENCHn = 1$ $CONF\_DIAGENCHn = 1$ Comparator or ADC( $CONF\_AUTOSS = 1$ )	No action	FLAG_OPENCHn FLAG_OUT (maskable) FLAG_ERR (maskable)	Onepulse pulled down for 50 $\mu$ s (maskable)	Clear fault flag with CLR_ERR
LED short-circuit fault	$V_{(OUTn)} < V_{(SG\_th\_rise)}$	PWM pulse width greater than $t_{(ODPW)}$ $CONF\_ENCHn = 1$ $CONF\_DIAGENCHn = 1$ Comparator or ADC( $CONF\_AUTOSS = 1$ )	No action	FLAG_SHORTCHn FLAG_OUT (maskable) FLAG_ERR (maskable)	One pulse pulled down for 50 $\mu$ s (maskable)	Clear fault flag with CLR_ERR
On-demand off-state invisible diagnostic	LED Open-circuit or LED Short-circuit fault	Pulse width: $T_{(ODPW)}$ Current: $I_{(ODIOUT)}$ $CONF\_ENCHn = 0$ $CONF\_DIAGENCHn = 1$ $CONF\_INVDIAGSTART = 1$	No action	FLAG_ODREADY FLAG_ODDIAGCHn FLAG_OUT FLAG_ERR FLAG_OPENCHn or FLAG_SHORTCHn	One pulse pulled down for 50 $\mu$ s	Clear fault flag with CLR_ERR
On-demand off-state single-LED Short-circuit *	$V_{(OUTn)} < V_{(ADCSHORTTH)}$ and $V_s > V_{(ADCLOWVSTH)}$	Pulse width: $T_{(ODPW)}$ Current: $I_{(ODIOUT)}$ $CONF\_ENCHn = 0$ $CONF\_DIAGENCHn = 1$ $CONF\_SSSTART = 1$ ADC	No action	FLAG_ODREADY FLAG_ODDIAGCHn FLAG_OUT FLAG_ERR	One pulse pulled down for 50 $\mu$ s	Clear fault flag with CLR_ERR
Auto single-LED short circuit *	$V_{(OUTn)} < V_{(ADCSHORTTH)}$ and $V_{(SUPPLY)} > V_{(ADCLOWVSTH)}$	PWM pulse width greater than $T_{(ODPW)} + 3 \times T_{(CONV)}$ $CONF\_ENCHn = 1$ $CONF\_DIAGENCHn = 1$ ADC( $CONF\_AUTOSS = 1$ )	No action	FLAG_ODDIAGCHn FLAG_OUT (maskable) FLAG_ERR (maskable)	One pulse pulled down for 50 $\mu$ s (maskable)	Clear fault flag with CLR_ERR
MTPROMCRC error	CALC_MTPCRC is different MTPCRC		No action	FLAG_MTPCRC FLAG_ERR (maskable)	One pulse pulled down for 50 $\mu$ s (maskable)	Clear fault flag with CLR_ERR
Communication loss fault	$T_{(WDTIMER)}$ overflows		Enter Fail-Safe states	FLAG_FS	No action	Set CLRFS to 1 to set the device to NORMAL state
ECC	ECC_ECNT $\neq$ 0		No action	FLAG_ECC FLAG_ERR	One pulse pulled down for 50 $\mu$ s	Clear fault flag with CLR_ERR
Initial self-test	After CLR_POR, Comparator abnormal		No action	FLAG_CMP FLAG_ERR	One pulse pulled down for 50 $\mu$ s	Clear fault flag with CLR_ERR

Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	Fault pin	Recovery
ADDR Pin failure	Address Check	CONF_ADDR_FD = 1	No action	FLAG_ADDR (optional disable) FLAG_ERR (optional disable)	ADDR Pin failure	Address Check
Config register value abnormal	Cyclical Config Checker Calculate result is different with CALC_CONFCRC	CONF_CONFCRC_FD = 1	No action	FLAG_CONFCRC FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR
PWM output mismatch	CONF_ENCHn=1 & Channel pulse width mismatch CONF_PWMOUTn	CONF_PWM_FD = 1	No action	FLAG_PWM FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR
State switch error	State controller output doesn't match detector output	CONF_STA_FD = 1	No action	FLAG_STA FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR
OSC warning	Clock check counter overflow	CONF_OSC_FD = 1	No action	FLAG_OSC FLAG_ERR (optional disable)	Constant pulled down (optional disable)	Automatically recover upon fault removal. Clear fault flag with CLR_ERR
I <sub>REF</sub> out of range	After CLR_POR and CLR_REG, Deviation between the original values exceeds limit value	CONF_AUTOSS = 1 CONF_IREF_FD = 1	No action	FLAG_IREF FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR
VBG abnormal	VBG out of range	CONF_AUTOSS = 1 CONF_VBG_FD = 1	No action	FLAG_VBG FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR
Unexpected V <sub>out</sub> during channel disable	During channel disable time, $V_{(OUTn)} > V_{(SG\_th\_rise)}$	CONF_OFFOUT_FD = 1 ADC(CONF_AUTOSS = 1)	No action	FLAG_OFFOUT (optional disable) FLAG_ERR (optional disable)	One pulse pulled down for 50 $\mu$ s (optional disable)	Clear fault flag with CLR_ERR

### 14.3.8. Diagnostic and protection in FAIL-SAFE state

In FAIL-SAFE state, the NEX13120F-Q100 also detects failures and reports the status out by  $\overline{\text{FLT}}$  pin or FLAG registers. [Table 19](#) lists the summary of the fault detection criteria and the device behavior after the fault is detected. Basically, the NEX13120F-Q100 actively takes the action to turn off the failed output channels, retry on the failed channels, or restart the device to keep the device operating without controlled by master. The MTP register NV\_OFAF can be used to set the fault behavior for LED open-circuit, LED short-circuit, and single-LED short-circuit faults. The one-fails-all-fail behavior is selected when the register NV\_OFAF is burnt to 1; otherwise, the one-fails-others-on behavior is chosen. The NEX13120F-Q100 turns off all output channels when any type of LED fault is detected on any one of output channels for one-fails-all-fail behavior. On the other hand, the NEX13120F-Q100 only turns off the failed channel and keeps all other normal channels on. In FAIL-SAFE state, the fault flag registers of NEX13120F-Q100 still can be accessed again through UART interface in case the communication is rebuilt.

### $V_{\text{bat}}$ and VLDO under-voltage lockout diagnostics in FAIL-SAFE state

When  $V_{\text{bat}}$  or VLDO voltage drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG\_POR and FLAG\_ERR set to 1.

### Low $V_{\text{s}}$ -supply warning diagnostics in FAIL-SAFE state

The NEX13120F-Q100 continuously monitors the  $V_{\text{s}}$  voltage and compares the results with internal threshold  $V_{(\text{LOWVSTH})}$  set by CONF\_LOWVSTH for low- $V_{\text{s}}$  voltage warning. If the supply voltage is lower than threshold, the device sets flag registers including FLAG\_LOWVVS and FLAG\_ERR to 1. The fault is latched in flag registers. When the supply voltage rises above low- $V_{\text{s}}$  warning threshold, the master controller must write register CLR\_ERR to 1 to reset FLAG\_LOWVVS and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0. The low- $V_{\text{s}}$  warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection. When the voltage applied on  $V_{\text{s}}$  pin is higher than the threshold  $V_{(\text{LOWVSTH})}$ , the NEX13120F-Q100 enables LED open-circuit and single-LED short-circuit diagnosis. When  $V_{\text{s}}$  is lower than the threshold  $V_{(\text{LOWVSTH})}$ , the device disables LED-open-circuit detection and single-LED short-circuit diagnosis. Because when  $V_{\text{s}}$  drops below the maximum total LED forward voltage plus required  $V_{(\text{OUT\_drop})}$  at required current, the NEX13120F-Q100 is not able to deliver sufficient current output to pull the voltage of each output channel as close as possible to the  $V_{\text{s}}$ . In this case, the LED open-circuit fault or single-LED short circuit fault may be detected and reported by mistake. Setting the low- $V_{\text{s}}$  warning threshold high enough can avoid the LED open-circuit and single-LED short-circuit fault being detected when  $V_{\text{s}}$  drops too low. The  $V_{(\text{LOWVSTH})}$  is programmable from 4 V to 19 V.

### $V_{\text{s}}$ under-voltage diagnostics in FAIL-SAFE state

The NEX13120F-Q100 provides internal analog comparator to monitor the supply voltage for undervoltage protection in FAIL-SAFE state. If the supply voltage falls below the internal threshold,  $V_{(\text{Vs\_th\_fall})}$ , the device pulls the  $\overline{\text{FLT}}$  pin low with constant current sink to report the fault and set flag registers including FLAG\_VSUV and FLAG\_ERR to 1. The supply under-voltage detection is used to disable all current output. When  $V_{\text{s}}$  is lower than the threshold  $V_{(\text{Vs\_th\_fall})}$ , the device disables every output to avoid the unwanted LED flickering or output fault triggered improperly. When the voltage applied on  $V_{\text{s}}$  pin rises above the threshold  $V_{(\text{Vs\_th\_rise})}$ , the NEX13120F-Q100 enables all current outputs automatically. The fault is latched in flag registers. When the supply voltage rises above  $V_{(\text{Vs\_th\_rise})}$ , the NEX13120F-Q100 releases  $\overline{\text{FLT}}$  pin and the master controller must write register CLR\_ERR to 1 to clear FLAG\_VSUV and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### Reference diagnostics in FAIL-SAFE state

NEX13120F-Q100 integrates diagnostics for REF resistor open and short fault in FAIL-SAFE state. The device monitors the reference current  $I_{(\text{REF})}$  set by external resistor  $R_{(\text{REF})}$ . Use [Equation 6](#) to calculate the  $I_{(\text{REF})}$ . If the current output from REF pin  $I_{(\text{REF})}$  is lower than  $I_{(\text{REF\_OPEN\_th})}$ , the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin  $V_{(\text{REF})}$  is lower than  $V_{(\text{REF\_SHORT\_th})}$ . The device pulls the  $\overline{\text{FLT}}$  pin down with constant current sink and sets flag registers including FLAG\_REF and FLAG\_ERR to 1. The fault is latched in flag registers.

After the REF pin  $I_{(\text{REF})}$  and  $V_{(\text{REF\_SHORT\_th})}$  recover to normal, the device releases  $\overline{\text{FLT}}$  pin pull-down automatically and the master controller must send CLR\_ERR to clear FLAG\_REF and FLAG\_ERR. The CLR\_ERR automatically returns to 0. In FAIL-SAFE state, the device turns off all output channels when reference fault is detected. The device automatically recovers and turns on all enabled channels after fault removal.

### Pre-thermal warning in FAIL-SAFE state

The NEX13120F-Q100 has pre-thermal warning at typical 135 °C in FAIL-SAFE state. When the junction temperature  $T_j$  of NEX13120F-Q100 rises above pre-thermal warning threshold, the device reports pre-thermal warning and sets the flag registers including FLAG\_PRETSD and FLAG\_ERR to 1. The fault is latched in flag registers. When the junction temperature of NEX13120F-Q100 falls below pre-thermal warning threshold, the master controller must write 1 to CLR\_ERR register to clear FLAG\_PRETSD and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### Over-temperature protection in FAIL-SAFE state

The NEX13120F-Q100 has over-temperature protection at  $T_{(TSD1)}$ , typical 175 °C in FAIL-SAFE state. When device junction temperature  $T_j$  further rises above over-temperature protection threshold, the device turns off all output drivers, pulls the FLT pin low with constant current sink to report fault, and sets the flag registers including FLAG\_TSD and FLAG\_ERR to 1. The fault is latched in flag registers. When the junction temperature falls below  $T_{(TSD1)} - T_{(TSD1\_HYS)}$ , the device resumes all outputs and releases FLT pin pull-down. The master controller must write 1 to CLR\_ERR to clear FLAG\_TSD and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### Over-temperature shutdown in FAIL-SAFE state

When the  $T_j$  rises too high above  $T_{(TSD2)}$ , typically 180 °C, the NEX13120F-Q100 turns off the internal linear regulator, VLDO output to shut down all the analog and digital circuits. The FLT pin is pulled down by constant current sink to report the fault, and the FLAG\_POR and FLAG\_ERR are all set to 1. When the  $T_j$  drops below  $T_{(TSD2)} - T_{(TSD2\_HYS)}$ , the NEX13120F-Q100 restarts from POR state with all the registers cleared to default value and FLT pin released. The master controller must write 1 to CLR\_POR to clear both FLAG\_POR and FLAG\_ERR after fault removal. The CLR\_POR bit automatically returns to 0.

### LED open-circuit diagnostics in FAIL-SAFE state

The NEX13120F-Q100 integrates LED open-circuit diagnostics to allow users to monitor LED status in real-time in FAIL-SAFE state. The device monitors voltage difference between  $V_s$  and  $OUT_n$  to judge if there is any open-circuit failure. The  $V_s$  voltage is also monitored in parallel with programmable threshold to determine if supply voltage is high enough for open-circuit diagnostics. The open-circuit monitor is only effective during PWM-ON state with programmable minimal pulse width greater than  $t_{(ODPW)}$ . The  $t_{(ODPW)}$  is programmed by register ODPW. If PWM on-time is less than  $t_{(ODPW)}$ , the device does not report any open-circuit fault. When the device supply voltage  $V_s$  is below the threshold  $V_{(LOWVSTH)}$  set by register CONF\_ADCLOWVSTH, the LED open-circuit fault is not detected nor reported. When the voltage difference  $V_s - V_{(OUT_n)}$  is below threshold  $V_{(OPEN\_th\_rise)}$  with duration longer than  $t_{(ODPW)}$ , and the device supply voltage  $V_s$  is above the threshold  $V_{(LOWVSTH)}$ , the NEX13120F-Q100 pulls the FLT pin down with constant current sink to report fault and set flag registers including FLAG\_OPENCH<sub>n</sub>, FLAG\_OUT and FLAG\_ERR to 1. In FAIL-SAFE state, the NEX13120F-Q100 shuts down the normal current regulation and PWM duty cycle for the error output, then the device sources a current  $I_{(RETRY)}$  to faulty output every  $t_{(retry)}$ , typically 10 ms for retrying.  $I_{(RETRY)}$  is programmed by CONF\_IOUT register. The current  $I_{(RETRY)}$  can be calculated with the below equation. When the voltage difference  $V_s - V_{(OUT_n)}$  of error output rises above threshold  $V_{(OPEN\_th\_rise)}$  with duration longer than  $t_{(ODPW)}$ , or the supply voltage  $V_s$  is above the threshold  $V_{(LOWVSTH)}$ , the device automatically resumes the normal current and PWM duty cycle setup and releases the FLT pin.

The fault is latched in flag registers. When the open-circuit failure is removed, the master controller must write 1 to CLR\_ERR to clear FLAG\_OPENCH<sub>n</sub>, FLAG\_OUT and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### LED short-circuit diagnostics in FAIL-SAFE state

The NEX13120F-Q100 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold for reporting  $OUT_n$  short to GND fault in FAIL-SAFE state. The short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of  $t_{(ODPW)}$ . The  $t_{(ODPW)}$  is programmable by register ODPW. If PWM on-time is less than  $t_{(ODPW)}$ , the device cannot report any short-circuit fault. When the voltage  $V_{(OUT_n)}$  is below threshold  $V_{(SG\_th\_fall)}$  with duration longer than deglitch timer length of  $t_{(ODPW)}$ , the device pulls FLT pin down with constant current sink to report fault and set flag registers including FLAG\_SHORTCH<sub>n</sub>, FLAG\_OUT and FLAG\_ERR. In FAIL-SAFE state, the NEX13120F-Q100 shuts down the normal current regulation and PWM duty cycle for the faulty output, then the device sources a pulse current to faulty output every  $t_{(retry)}$ , 10 ms for retrying.  $I_{(RETRY)}$  is programmed by CONF\_ODIOUT register. Use Equation 8 to calculate the current,  $I_{(RETRY)}$ . When the voltage  $V_{(OUT_n)}$  of error output rises above threshold  $V_{(SG\_th\_rise)}$  with duration longer than  $t_{(ODPW)}$ , the device automatically resumes the normal current and PWM duty cycle setup and releases the FLT pin. The fault is latched in flag registers. When the short-circuit failure is removed, the master controller

must write 1 to CLR\_ERR to clear FLAG\_SHORTCHn, FLAG\_OUT and FLAG\_ERR. The CLR\_ERR bit automatically returns to 0.

### Single-LED short-circuit detection in FAIL-SAFE state

The NEX13120F-Q100 also integrates analog comparators to monitor all outputs with respect to two alternative threshold for single-LED short-circuit diagnostic in FAIL-SAFE state. Setting the register CONF\_AUTOSS to 1 enables the single-LED short-circuit detection. The single-LED short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of  $t_{(ODPW)}$ . The  $t_{(ODPW)}$  is programmable by register ODPW. If PWM on-time is less than  $t_{(ODPW)}$ , the device cannot report any single-LED short-circuit fault. When the device supply voltage  $V_s$  is below the threshold  $V_{(LOWVSTH)}$  set by register CONF\_ADCLOWVSTH, the single-LED short-circuit is not detected nor reported. When the voltage  $V_{(OUTn)}$  is below threshold  $V_{(ADCSHORTTHn)}$  with duration longer than deglitch timer length of  $t_{(ODPW)}$ , and the device supply voltage  $V_s$  is above the threshold  $V_{(LOWVSTH)}$ , the device pulls the FLT pin down with constant current sink to report fault and set flag registers including FLAG\_ODDIAGCHn, FLAG\_OUT and FLAG\_ERR. The NEX13120F-Q100 provides two alternative threshold  $V_{(ADCSHORTTH0)}$  and  $V_{(ADCSHORTTH1)}$  for single-LED short-circuit detection selected by ADCSHORTTHCHn independently for each current output. The  $V_{(ADCSHORTTH0)}$  is selected for current OUTn when ADCSHORTTHCHn is set to 0, however,  $V_{(ADCSHORTTH1)}$  is selected when ADCSHORTTHCHn is set to 1. The actual voltage value for  $V_{(ADCSHORTTH0)}$  and  $V_{(ADCSHORTTH1)}$  is programmable by two 8-bit registers CONF\_ADCSHORTTH0 and CONF\_ADCSHORTTH1 from 0 V to 20.56 V at 80 mV interval. In FAIL-SAFE state, the NEX13120F-Q100 shuts down the normal current regulation and PWM duty cycle for the faulty output, then the device sources a pulse current,  $I_{(OUTn)}$  programed by  $I_{(OUTn)}$  register to the faulty output every  $t_{(retry)}$ , 10 ms for retrying. When the voltage  $V_{(OUTn)}$  of error output rises above threshold  $V_{(ADCSHORTTHn)}$  + 125 mV with duration longer than  $t_{(ODPW)}$  during retrying, or the supply voltage  $V_s$  is below the threshold  $V_{(LOWVSTH)}$ , the device automatically resumes the normal current and PWM duty cycle setup and releases the FLT pin. The fault is latched in flag registers. When the single-LED short-circuit fault is removed, the master controller must write 1 to register CLR\_ERR to clear FLAG\_ODDIAGCHn, FLAG\_OUT and FLAG\_ERR. The CLR\_ERR automatically returns to 0.

### MTP CRC error in FAIL-SAFE state

The NEX13120F-Q100 automatically reloads all MTP code into the corresponding configuration registers every time after entering the FAIL-SAFE state. The NEX13120F-Q100 implements a MTP CRC check after loading the MTP code to configuration register in FAIL-SAFE state. The calculated CRC results are sent to register CALC\_MTPCRC and compared to the data in MTP register NV\_CRC, which stores the CRC code for all MTP registers. If the code in register CALC\_MTPCRC is not matched to that in register NV\_CRC, the NEX13120F-Q100 turns off all channels output, pulls the FLT pin down with constant current sink to report the fault, and sets the registers including FLAG\_MTPCRC and FLAG\_ERR to 1. The CRC code for all the MTP registers must be burnt into MTP register MTPCRC in the end of production line. The CRC code algorithm is described in MTP CRC Error in NORMAL state.

### Fault masking in FAIL-SAFE state

The NEX13120F-Q100 provides fault masking function using masking registers. The device is capable of masking faults by channels or by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG\_OUT register, FLAG\_ERR register, and FLT pin output. Table 18 gives the detailed description for each fault mask register in NORMAL state.

To disable diagnostics on a single channel in FAIL-SAFE state, burning MTP of NV\_DIAGENCHn registers to 0 disables open-circuit, LED short-circuit diagnostics of channel n, and thus no fault of this channel is reported to FLAG\_OPENCHn, FLAG\_SHORTCHn, FLAG\_OUT or FLAG\_ERR registers, or to the FLT pin output.

**Table 18. Fault masking register in NORMAL state**

Fault detected	Mask register	FLAG name	FLT pin
$V_s$ low warning	CONF_MASKLOWVS = 1	FLAG_LOWVS = 1	No action
	CONF_MASKLOWVS = 0	FLAG_LOWVS = 1 FLAG_ERR = 1	Constant pulled down
$V_s$ under-voltage	CONF_MASKVSUV = 1	FLAG_VSUV = 1	No action
	CONF_MASKVSUV = 0	FLAG_VSUV = 1 FLAG_ERR = 1	Constant pulled down

Fault detected	Mask register	FLAG name	FLT pin
Reference fault	CONF_MASKREF = 1	FLAG_REF = 1	No action
	CONF_MASKREF = 0	FLAG_REF = 1 FLAG_ERR = 1	Constant pulled down
MTPROMCRC error	CONF_MASKMTPCRC = 1	FLAG_MTPCRC = 1	No action
	CONF_MASKMTPCRC = 0	FLAG_MTPCRC = 1 FLAG_ERR = 1	Constant pulled down
LED open-circuit fault	CONF_MASKOPEN = 1	FLAG_OPENCHn = 1	No action
	CONF_MASKOPEN = 0	FLAG_OPENCHn = 1 FLAG_OUT = 1 FLAG_ERR = 1	Constant pulled down
LED short-circuit fault	CONF_MASKSHORT= 1	FLAG_SHORTCHn = 1	No action
	CONF_MASKSHORT= 0	FLAG_SHORTCHn = 1 FLAG_OUT = 1 FLAG_ERR = 1	Constant pulled down
Over-temperature protection	CONF_MASKTSD = 1	FLAG_TSD=1	No action
	CONF_MASKTSD = 0	FLAG_TSD = 1 FLAG_ERR = 1	Constant pulled down



Table 19. Diagnostics table in FAIL-SAFE state

Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	FLT pin	Recovery
VBAT UVLO Base on comparator	$V_{(Vbat)} < V_{(POR\_fall)}$	Comparator	Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR.
VLDO UVLO Base on comparator	$V_{(VLDO)} < V_{(VLDO\_POR\_fall)}$	Comparator	Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR.
Low- $V_s$ warning	$V_s < V_{(LOWVSTH)}$	ADC	Disable fault type*	FLAG_LOWVS FLAG_ERR (maskable)	No action	Clear fault flag with CLR_ERR.
$V_s$ under-voltage	$V_s < V_{(Vs\_th\_fall)}$	Comparator	Turn off all outputs	FLAG_VSUUV FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recovery and release FLT pin upon fault removal. Clear fault flag with CLR_ERR.
Reference fault	$V_{(REF)} < V_{(REF\_SHORT\_th)}$ or $I_{(REF)} < I_{(REF\_OPEN\_th)}$	Comparator	Turn off all outputs	FLAG_REF FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release FLT pin upon fault removal. Clear fault flags with CLR_ERR.
Over-temperature protection	$T_j > T_{(TSD1)}$	Comparator	Turn off all outputs	FLAG_TSD FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release FLT pin upon fault removal. Clear fault flags with CLR_ERR.
Over-temperature shutdown	$T_j > T_{(TSD2)}$	Comparator	Turn off VLDO	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR.
LED open-circuit fault *	$V_s - V_{(OUTn)} < V_{(OPEN\_th\_rise)}$ and $V_s > V_{(LOWVSTH)}$	PWM pulse width greater than $t_{(ODPW)}$ CONF_ENCHn = 1 CONF_DIAGENCHn = 1	Turn off the failed outputs and retry every 10 ms	FLAG_OPENCHn FLAG_OUT (maskable) FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release FLT pin upon fault removal. Clear fault flags with CLR_ERR.
LED short-circuit fault	$V_{(OUTn)} < V_{(SG\_th\_rise)}$	PWM pulse width greater than $t_{(ODPW)}$ CONF_ENCHn = 1 CONF_DIAGENCHn = 1	Turn off the failed outputs and retry every 10 ms	FLAG_SHORTCHn FLAG_OUT (maskable) FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release FLT pin upon fault removal. Clear fault flags with CLR_ERR.
MTP CRC error	CALC_MTPCRC is different MTPCRC		Turn off all outputs	FLAG_MTPCRC FLAG_ERR (maskable)	Constant pulled down (maskable)	Clear fault flags with CLR_ERR.

14.3.9. OFAF setup in FAIL-SAFE state

The NEX13120F-Q100 has a unique setup for failure behavior in FAIL-SAFE state. If there is a failure detected in FAIL-SAFE state, the NEX13120F-Q100 automatically reacts to the failure. The register OFAF determines whether the result behavior of output failure is one-fails-all-fail or one-fails-others-on.

In FAIL-SAFE state, the NEX13120F-Q100 shuts down all enabled current outputs except the faulty output when OFAF is set to 1. Otherwise, the NEX13120F-Q100 keeps regulation for all enable current outputs except the faulty output when OFAF is set to 0. [Table 20](#) provides details.

14.3.10.  $\overline{\text{FLT}}$  Output

The  $\overline{\text{FLT}}$  pin is a programmable fault indicator pin. This pin can be used as an interrupt output to master controller in case there is any fault in NORMAL state. In FAIL-SAFE states, the  $\overline{\text{FLT}}$  pin can be used as an output to other  $\overline{\text{FLT}}$  pin of other NEX13120F-Q100 to achieve one-fails-all-fail at system level. The  $\overline{\text{FLT}}$  pin is an open-drain output with current limit up to  $I_{\text{PD(ERR)}}$ . Nexperia recommends a  $< 10\text{ k}\Omega$  external pull-up resistor from the  $\overline{\text{FLT}}$  pin to the same IO voltage of the master controller.

In NORMAL state, when a fault is triggered, depending on the fault type, the  $\overline{\text{FLT}}$  pin is either pulled down constantly or pulled down for a single pulse. After an  $\overline{\text{FLT}}$  output is triggered, the master controller must take action to deal with the failure and reset the fault flag. For non-critical faults, the NEX13120F-Q100 pulls down the  $\overline{\text{FLT}}$  pin with a duration of 50  $\mu\text{s}$  and release; for critical faults, device constantly pulls down  $\overline{\text{FLT}}$  as described in [Table 17](#). In NORMAL state, basically, the NEX13120F-Q100 only reports the faults to the master controller for most of the failure and takes no action except supply or LDO UVLO, reference fault, and over-temperature. The master controller determines what action to take according to the type of the failure.

The NEX13120F-Q100 provides a forced-error feature to validate the error feedback-loop integrity in NORMAL state. In NORMAL state, if the micro-controller sets FORCEERR to 1, the FLAG\_ERR is set 1 and pulls down  $\overline{\text{FLT}}$  output with a pulse of 50  $\mu\text{s}$  accordingly. The FORCEERR automatically returns to 0.

In FAIL-SAFE states, the  $\overline{\text{FLT}}$  pin is used as fault bus. When there is any output failure reported, the  $\overline{\text{FLT}}$  is pulled down by internal current sink  $I_{\text{PD(ERR)}}$ . The NEX13120F-Q100 monitors the voltage of the  $\overline{\text{FLT}}$  pin. If the one-fails-all-fail diagnostics is enabled by setting register OFAF to 1, all current output channels are turned off, as well as diagnostics, when the  $\overline{\text{FLT}}$  pin voltage is low. If register OFAF is 0, the device only turns off the failed channel with active channels diagnostics enabled.

Table 20. One-Fails-All-Fail feature in FAIL-SAFE state

FLT pin	OFAF = 1	OFAF = 0
FLT pulled low internally	All OUT channel OFF except failure detected OUT retries every 10 ms	Only failure detected OUT OFF
FLT pulled low externally	All OUT channel OFF	All OUT channel ON

If multiple NEX13120F-Q100 devices are used in one application, tying the  $\overline{\text{FLT}}$  pins together achieves the one-fails-all-fail behavior in FAIL-SAFE states without master controlling. Any one of NEX13120F-Q100 reports fault by pulling the  $\overline{\text{FLT}}$  pin to low, and the low voltage on ERR bus is detected by other NEX13120F-Q100 as [Fig. 39](#) illustrated. If the register OFAF is set to 1 for all NEX13120F-Q100 devices having the  $\overline{\text{FLT}}$  pins tied together, all NEX13120F-Q100 devices turn off current for all output channels.



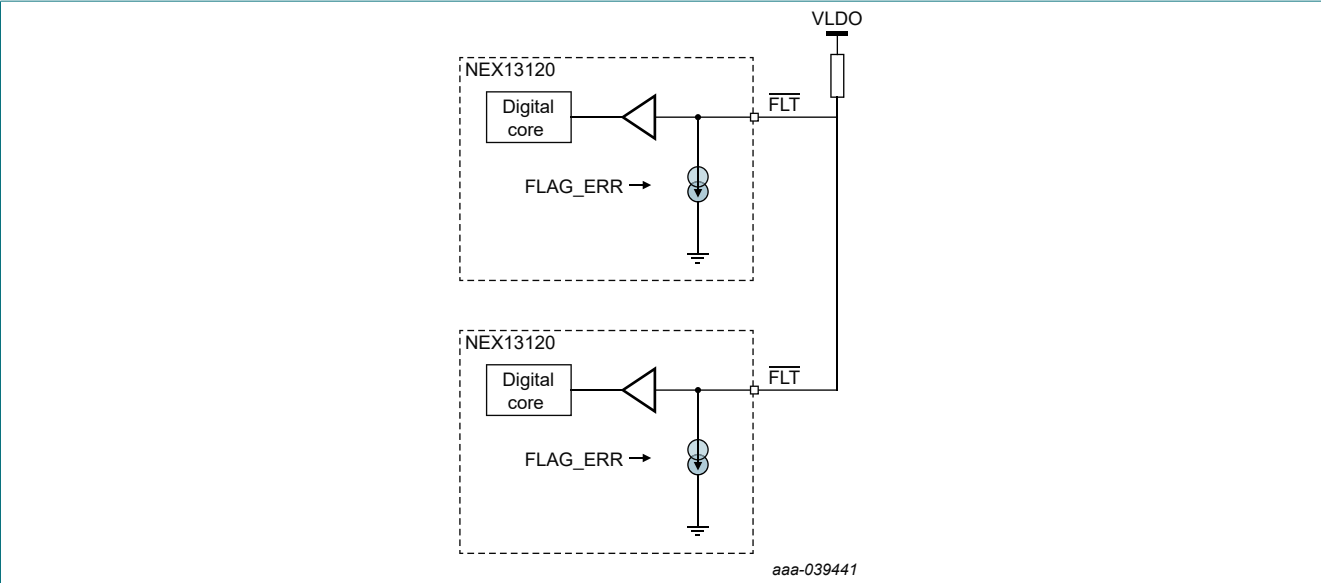


Fig. 39. Fault pin internal diagram

14.4. Device functional modes

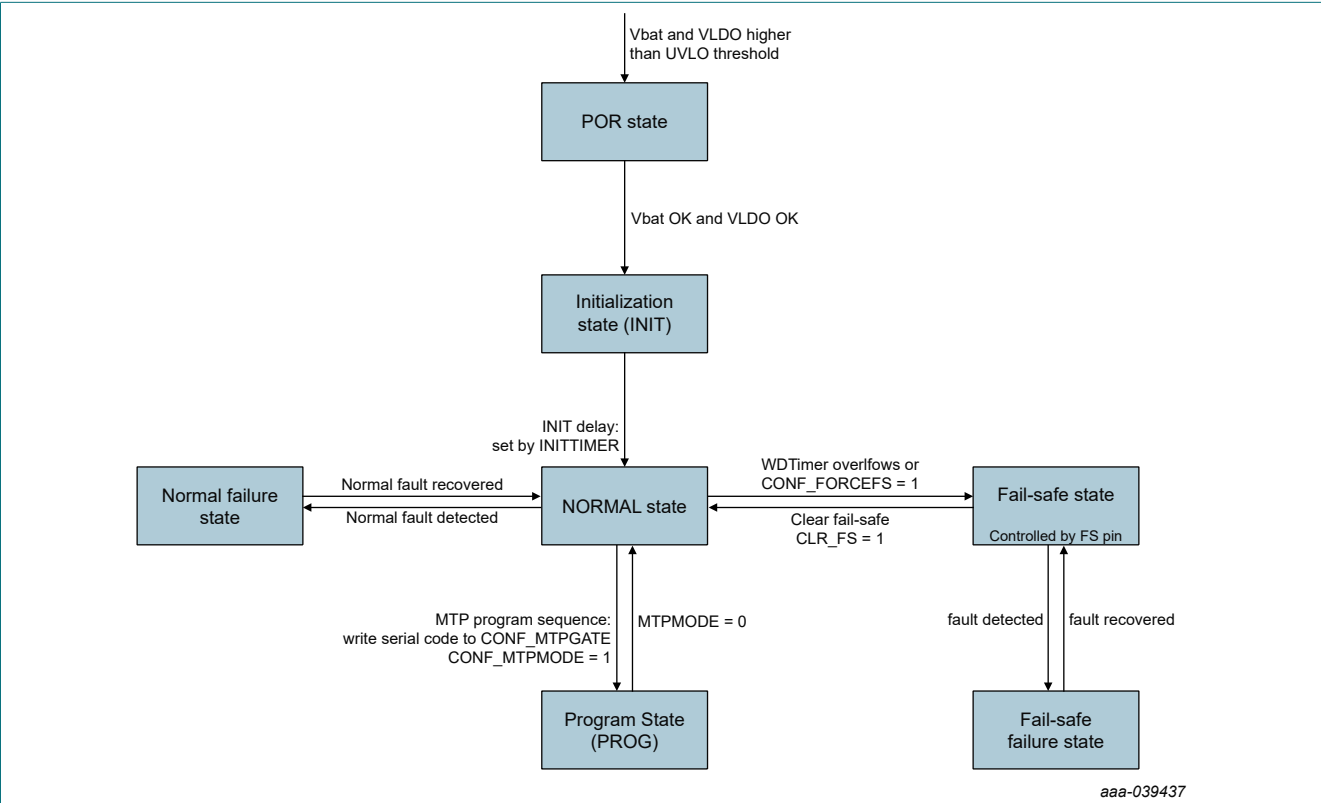


Fig. 40. Device functional mode state machine

14.4.1. POR state

Upon power-up, the NEX13120F-Q100 enters POR state. In this state, registers are cleared to default value, outputs are disabled, and the device cannot be accessed through the UART interface.

After both the  $V_{bat}$  input and the VLDO output are above their UVLO threshold, the device switches to INITIALIZATION state (INIT). If any of the supply fails below UVLO threshold in other states, the device immediately switches to POR state.

#### 14.4.2. INITIALIZATION state

The INITIALIZATION state is designed to allow master controller to have enough time to power up before the device automatically gets into FAIL-SAFE states.

INIT mode has a configurable delay programmed by 4-bit register NV\_INITTIMER. After the delay counter is reached, the device changes to NORMAL state. In INIT state, the communication between master controller and the NEX13120F-Q100 is enabled through UART interface. In INITIALIZATION state, device automatically load register map default values, which can be programmed in corresponding MTP. The master controller sets CLR\_POR to 1 in INITIALIZATION state, the device immediately switches to NORMAL state. Only write CLR\_POR to NEX13120F-Q100 in INITIALIZATION state.

#### 14.4.3. NORMAL state

After the NEX13120F-Q100 is in NORMAL state, the device operates under master control for LED animation and diagnostics using UART interface.

The NEX13120F-Q100 integrates a watchdog timer to monitor the communication on UART interface. The watchdog timer is programmable by a 4-bit register CONF\_WDTIMER for 13 options. The timer in NEX13120F-Q100 starts to count when there is no instruction received from the master controller.

The NEX13120F-Q100 enters FAIL-SAFE state when the timer overflows. The device can be also forced into FAIL-SAFE states anytime in NORMAL state by setting FORCEFS to 1. The FORCEFS register automatically returns to 0.

#### 14.4.4. FAIL-SAFE state

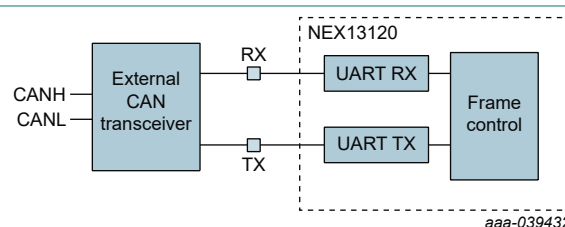
When the NEX13120F-Q100 is entering FAIL-SAFE state from NORMAL state, all the registers are set to default value or reloaded from MTP. The UART interface keeps alive in FAIL-SAFE state. Setting CONF\_FORCEFS to 1 forces the device into FAIL-SAFE state from NORMAL state. The NEX13120F-Q100 can quit from FAIL-SAFE state to NORMAL state by setting CLR\_FS to 1 with FLAG\_FS register cleared.

#### 14.4.5. PROGRAM state

The NEX13120F-Q100 can enter MTP PROGRAM state by writing multiple configuration registers to CONF\_NVGATE and setting 1 to CONF\_NVMODE. For details of getting into PROGRAM state, refer to [Section 14.4.5.2](#).

##### 14.4.5.1. UART over CAN protocol

NEX13120F-Q100 integrates UART-compliant controller, the structure is shown in [Fig. 41](#). NEX13120F-Q100 is compliant with the UART, the data format is similar to UART. The signal input to NEX13120F-Q100 is usually transferred from external CAN transceiver.



**Fig. 41. Interface structure**

The internal frame controller is a UART-based protocol supported by most MCUs. Each frame contains multiple bytes started with a synchronization byte. The synchronization byte allows LED drivers to synchronize with master MCU frequency, therefore saving the extra cost on high precision oscillators that are commonly used in UART/CAN interfaces. Each byte has 1 start bit, 8 data bits, 1 stop bit, no parity check. The interface supports adaptive communication frequency ranging from 50 kHz to 1 MHz. The protocol supports master-slave with star-connected topology.

## UART interface slave address setting

NEX13120F-Q100 supports up to 27 slave devices. NEX13120F-Q100 has three pin outs including ADDR2, ADDR1, and ADDR0 for slave address configuration. Different configurations allow NEX13120F-Q100 to support different slaves as below:

- If NV\_EXTADDR = 0, the device uses NV\_DEVADDR [3] code together with external inputs on ADDR2, ADDR1 and ADDR0 to support 16 slaves as [Table 22](#).
- If NV\_EXTADDR = 1, ADDR2, ADDR1 and ADDR0 can support three statuses, include M status as listed in [Table 21](#). The device uses external inputs on ADDR2, ADDR1 and ADDR0 to set 27 slaves as shown in [Table 23](#), in this mode.

**Table 21. Address pin status assessment**

Status	Settings
0	Tie directly (0 $\Omega$ ) to GND
M	Tie 30 k $\Omega$ to GND
1	Option 1: Tie 90 k $\Omega$ to GND Option 2: Tie directly to V <sub>CC</sub>

**Table 22. Address setting (NV\_EXTADDR = 0)**

Address(Decimal)	Bit 3	Bit 2	Bit 1	Bit 0
	NV_DEVADDR [3]	ADDR2	ADDR1	ADDR0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

**Table 23. Address setting (NV\_EXTADDR = 1)**

Address (Decimal)	ADDR2	ADDR1	ADDR0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	M
9	0	1	M

Address (Decimal)	ADDR2	ADDR1	ADDR0
10	1	0	M
11	1	1	M
12	0	M	0
13	0	M	1
14	1	M	0
15	1	M	1
16	M	0	0
17	M	0	1
18	M	1	0
19	M	1	1
20	0	M	M
21	1	M	M
22	M	0	M
23	M	1	M
24	M	M	0
25	M	M	1
26	M	M	M

Address check function

NEX13120F-Q100 automatically checks the address setting by ADDR pin with internal MTP address register value. User needs to write the address into the MTP register. This function can be disabled by setting CONF\_ADDR\_FD to 0.

- If NV\_EXTADDR = 0, NEX13120F-Q100 compares ADDR0 to ADDR2 value with NV\_DEVADDR [0-2]. If the addresses don't match, NEX13120F-Q100 constantly pulls low FLT pin, and set FLAG\_ERR and FLAG\_ADDR to 1. The master controller must write 1 to CLR\_ERR register to clear the fault flags.
- If NV\_EXTADDR = 1, NEX13120F-Q100 compares ADDR0 to ADDR2 value with NV\_DEVADDR [4] x16 + NV\_DEVADDR [0-3]. If the addresses don't match, NEX13120F-Q100 constantly pulls low FLT pin, and set FLAG\_ERR and FLAG\_ADDR to 1. The master controller must write 1 to CLR\_ERR register to clear the fault flags.

Burst mode and 27 slave configurations

NEX13120F-Q100 supports unique burst mode by setting CONF\_LENEXT to 0 or 1, and user can select different burst mode.

- When CONF\_LENEXT=0, burst mode supports 1 byte, 2 bytes, 4 bytes and 8 bytes.
- When CONF\_LENEXT=1, burst mode supports 1 byte, 4 bytes, 16 bytes and 24 bytes.

To support burst mode and 27 slaves, user need to configure DEV\_ADDR byte. The device address byte, DEV\_ADDR frame follows the SYNC frame. There are totally 8 bits binary code in device address byte. The detail definition for each bit function is described in [Table 24](#).

The DEV\_ADDR register is required to set to 0000b for broadcast mode, otherwise the broadcast mode cannot be enabled. If burst mode is set to 16 or 24 bytes, NEX13120F-Q100 only receives first 12 bytes and CRC bytes, and ignores other data. For reading, it still reads 16 or 24 bytes.

Table 24. DEV\_ADDR byte

Bit	Field	Description
3-0	DEVICE_ADDR	Target device address.

Bit	Field	Description
5-4	DATA_LENGTH	CONF_LENEXT = 0 00b: Single-byte mode with 1 byte of data; 01b: Bust mode with 2 bytes of data. 10b: Burst mode with 4 bytes of data; 11b: Burst mode with 8 bytes of data CONF_LENEXT =1 00b: Single-byte mode with 1 byte of data; 01b: Bust mode with 4 bytes of data. 10b: Burst mode with 16 bytes of data; 11b: Burst mode with 24 bytes of data
6	BROADCAST	Broadcast mode. 1: Broadcast (DEVICE_ADDR =0000b); 0: Single-device only
7	READ/WRITE	Read/Write mode. 1: Write mode; 0: Read mode

To support more than 16 slaves, broadcast bit is used as address bit when slave address is higher than 15, the details of DEV\_ADDR byte for different slaves is listed in [Table 25](#).

Table 25. DEV\_ADDR byte

DEV_ADDR byte				
Read/Write[7]	Broadcast[6]	Data_length [5:4]	Device_ADDR[3:0]	Read/Write slave
Write: 1 Read: 0	0	CONF_LENEXT = 0	1	slave 1
	0	00: 1 byte	2	slave 2
	0	01: 2 byte	3	slave 3
	0	10: 4 byte	4	slave 4
	0	11: 8 byte	5	slave 5
	0	CONF_LENEXT = 1	6	slave 6
	0	00: 1 byte	7	slave 7
	0	01: 4 byte	8	slave 8
	0	10: 16 byte	9	slave 9
	0	11: 24 byte	A	slave 10
	0		B	slave 11
	0		C	slave 12
	0		D	slave 13
	0		E	slave 14
	0		F	slave 15
	1		0	broadcast mode
	1		1	slave 16
	1		2	slave 17
	1		3	slave 18
	1		4	slave 19
	1		5	slave 20
	1		6	slave 21
	1		7	slave 22
	1		8	slave 23
	1		9	slave 24
	1		A	slave 25
	1		B	slave 26

#### 14.4.5.2. MTP Programming

The NEX13120F-Q100 has a user-programmable MTP with high reliability for automotive applications. All the MTP registers can be burnt through writing the target data into its corresponding register. The NEX13120F-Q100 supports two solutions for individual chip selection through pulling the REF pin high or through device address configuration by address pin.

##### Chip selection by pulling REF pin high

The NEX13120F-Q100 supports using REF pin as chip-select during MTP programming. Considering multiple NEX13120F-Q100 devices connected to one UART bus before burning MTP, the slave address for all NEX13120F-Q100 is all the same before programming in case internal MTP register DEVADDR is used for slave address setup. The MTP burning instruction can be sent to target NEX13120F-Q100 by pulling the REF pin of the target NEX13120F-Q100 to 5 V. After the REF pin is pulled up to 5 V, the NEX13120F-Q100 ignores the device address setup by ADDR2/ADDR1/ADDR0 pins or MTP programmed device address in DEVADDR.

The master controller must send out data to target NEX13120F-Q100 with device address as 0h and not in broadcast mode.

##### Chip selection by ADDR pins configuration

The NEX13120F-Q100 also supports using configuration on ADDR2/ADDR1/ADDR0 pins to determine the slave address for NEX13120F-Q100 if multiple NEX13120F-Q100 devices are connected on the same differential data bus.

It is recommended to use this approach for applications of multiple NEX13120F-Q100 in the same differential data bus. The master controller can send out register data to target NEX13120F-Q100 with device address matched to the ADDR2/ADDR1/ADDR0 pins configuration and not in broadcast mode.

##### MTP register access and burn

After selecting the target NEX13120F-Q100 for MTP burning, the master controller must send a serial data byte to register CONF\_MTPGATE, set 1 to CONF\_MTPMODE and set 1 to register CONF\_STAYINMTP one by one to finally enable the MTP register access.

For the detailed program sequence, please refer to file: ***NEX13120F-Q100 configuration guide and register map***.

##### Quit MTP program state

The REF pin can be released after MTP burning if it is pulled high to 5 V for chip selection. The REF pin must be kept high during the whole MTP programming state. The NEX13120F-Q100 can quit the MTP program state to normal state after burning by writing 0 to register CONF\_STAYINMTP. It is recommended to reload the MTP data to the registers after MTP burning by set 1 to CLR\_REG.

##### Read back MTP

The NEX13120F-Q100 supports MTP data reading back for both shadow registers and MTP cells.

- When the register CONF\_READSHADOW is set to 1, reading back for certain MTP registers address returns shadow registers content.
- When the register CONF\_READSHADOW is set to 0, reading back for certain MTP registers address returns content in MTP cell.

## 14.5. Normal register map and MTP register map

### Normal register map

Table 26. Normal register map

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
00h	IOUT0	Reserved	Reserved	CONF_IOUT0						NVI0
01h	IOUT1	Reserved	Reserved	CONF_IOUT1						NVI1
02h	IOUT2	Reserved	Reserved	CONF_IOUT2						NVI2
03h	IOUT3	Reserved	Reserved	CONF_IOUT3						NVI3
04h	IOUT4	Reserved	Reserved	CONF_IOUT4						NVI4
05h	IOUT5	Reserved	Reserved	CONF_IOUT5						NVI5
06h	IOUT6	Reserved	Reserved	CONF_IOUT6						NVI6
07h	IOUT7	Reserved	Reserved	CONF_IOUT7						NVI7
08h	IOUT8	Reserved	Reserved	CONF_IOUT8						NVI8
09h	IOUT9	Reserved	Reserved	CONF_IOUT9						NVI9
0Ah	IOUT10	Reserved	Reserved	CONF_IOUT10						NVI10
0Bh	IOUT11	Reserved	Reserved	CONF_IOUT11						NVI11
20h	PWM0	CONF_PWMOUT0								NVP0
21h	PWM1	CONF_PWMOUT1								NVP1
22h	PWM2	CONF_PWMOUT2								NVP2
23h	PWM3	CONF_PWMOUT3								NVP3
24h	PWM4	CONF_PWMOUT4								NVP4
25h	PWM5	CONF_PWMOUT5								NVP5
26h	PWM6	CONF_PWMOUT6								NVP6
27h	PWM7	CONF_PWMOUT7								NVP7
28h	PWM8	CONF_PWMOUT8								NVP8



ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
29h	PWM9	CONF_PWMOUT9								NVP9
2Ah	PWM10	CONF_PWMOUT10								NVP10
2Bh	PWM11	CONF_PWMOUT11								NVP11
3Ch	CONF_MISC13	CONF_ADCSHORTTH1[7:0]								NV16
3Dh	CONF_MISC14	CONF_ADCS HORTTHCH7	CONF_ADCS HORTTHCH6	CONF_ADCS HORTTHCH5	CONF_ADCS HORTTHCH4	CONF_ADCS HORTTHCH3	CONF_ADCS HORTTHCH2	CONF_ADCS HORTTHCH1	CONF_ADCS HORTTHCH0	NV17
3Eh	CONF_MISC15	Reserved	Reserved	Reserved	Reserved	CONF_ADCS HORTTHCH11	CONF_ADCS HORTTHCH10	CONF_ADCS HORTTHCH9	CONF_ADCS HORTTHCH8	NV18
3Fh	CONF_MISC16	CONF_O FFDelay	CONF_PS0[1:0]		CONF_LOWVBATTH					NV19
40h	PWML0	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT0				0Fh
41h	PWML1	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT1				0Fh
42h	PWML2	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT2				0Fh
43h	PWML3	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT3				0Fh
44h	PWML4	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT4				0Fh
45h	PWML5	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT5				0Fh
46h	PWML6	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT6				0Fh
47h	PWML7	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT7				0Fh
48h	PWML8	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT8				0Fh
49h	PWML9	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT9				0Fh
4Ah	PWML10	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT10				0Fh
4Bh	PWML11	Reserved	Reserved	Reserved	Reserved	CONF_PWMLOWOUT11				0Fh
50h	CONF_EN0	CONF_ENCH7	CONF_ENCH6	CONF_ENCH5	CONF_ENCH4	CONF_ENCH3	CONF_ENCH2	CONF_ENCH1	CONF_ENCH0	00h
51h	CONF_EN1	Reserved	Reserved	Reserved	Reserved	CONF_ENCH11	CONF_ENCH10	CONF_ENCH9	CONF_ENCH8	00h

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
54h	CONF_D IAGEN0	CONF_DIAGEN CH7	CONF_DIAGEN CH6	CONF_DIAGEN CH5	CONF_DIAGEN CH4	CONF_DIAGEN CH3	CONF_DIAGEN CH2	CONF_DIAGEN CH1	CONF_DIAGEN CH0	NV4
55h	CONF_D IAGEN1	Reserved	Reserved	Reserved	Reserved	CONF_DIAGEN CH11	CONF_DIAGEN CH10	CONF_DIAGEN CH9	CONF_DIAGEN CH8	NV5
56h	CONF_MISC0	CONF_AUTOSS	Reserved(R/W)	Reserved(R)	CONF_EXPEN	Reserved(R/W)				NV6
57h	CONF_MISC1	CONF_PWMFREQ				Reserved		CONF_REFRANGE		NV7
58h	CONF_MISC2	Reserved	CONF_FLTIMEOUT			CONF_ADCLOWVSTH				NV8
59h	CONF_MISC3	CONF_ODIOUT				CONF_ODPW				NV9
5Ah	CONF_MISC4	CONF_WDTIMER				Reserved				NV10
5Bh	CONF_MISC5	CONF_ADCSHORTTH0								NV11
5Ch	CONF_MISC17	CONF_LO WVBAT_FD	CONF_A DDR_FD	CONF_CO NFCRC_FD	CONF_PWM_FD	CONF_STA_FD	CONF_OSC_FD	CONF_IREF_FD	CONF_VBG_FD	NV12
5Dh	CONF_MISC18	CONF_C RC_SEL	Reserved	CONF_P WMSLOW	CONF_LENEXT	CONF_PSEN3	CONF_PSEN2	CONF_PSEN1	CONF_PSEN0	NV13
5Eh	CONF_MISC19	Reserved	Reserved	Reserved	CONF_OF FOUT_FD	CONF_MA SKPRETSD	CONF_M ASKVSUV	CONF_MA SKLOWVS	CONF_M ASKSLS	NV14
60h	CLR	Reserved	Reserved	CONF_FORCEF S	CLR_REG	CONF_FORCEE RR	CLR_FS	CLR_ERR	CLR_POR	00h
61h	CONF_LOCK	Reserved	Reserved	Reserved	Reserved	CONF_CLRLOC K	CONF_CONFLO CK	CONF_IOUTLO CK	CONF_PWMLO CK	0Fh
62h	CONF_MISC9	CONF_STAYINE EP	CONF_NVREA DBACK	Reserved	CONF_ADCCH					00h
63h	CONF_MISC10				CONF_SHAREP WM			CONF_READSH ADOW	CONF_NVMODE	00h
64h	CONF_MISC11	CONF_MASKRE F	CONF_MAS KMTPCRC	CONF_MASKOP EN	CONF_MASKSH ORT	CONF_MASKTS D	CONF_NVPRO G	CONF_SSSTAR T	CONF_INVDIAG START	00h
65h	CONF_MISC12	CONF_NVGATE								00h

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
66h	ADC_IREF	ADC_IREF								X
6Eh	ECC0	ECC_WCNT								X
6Fh	ECC1	ECC_ECNT								X
70h	FLAG0	FLAG_ECC	FLAG_REF	FLAG_FS	FLAG_OUT	FLAG_PRETSD	FLAG_TSD	FLAG_POR	FLAG_ERR	03h
71h	FLAG1	FLAG_CMP	FLAG_VSUV	FLAG_EXTFS	FLAG_PROGRE ADY	FLAG_ADCLOW VS	FLAG_ADCDON E	FLAG_ODREAD Y	FLAG_NVCRC	X
72h	FLAG2	ADC_VS								X
73h	FLAG3	ADC_OUT								00h
74h	FLAG4	FLAG_ODDIAG CH7	FLAG_ODDIAG CH6	FLAG_ODDIAG CH5	FLAG_ODDIAG CH4	FLAG_ODDIAG CH3	FLAG_ODDIAG CH2	FLAG_ODDIAG CH1	FLAG_ODDIAG CH0	00h
75h	FLAG5	Reserved	Reserved	Reserved	Reserved	FLAG_ODDIAG CH11	FLAG_ODDIAG CH10	FLAG_ODDIAG CH9	FLAG_ODDIAG CH8	00h
76h	FLAG6	FLAG_L OWVBAT	FLAG_ADDR	FLAG_C ONFCRC	FLAG_PWM	FLAG_STA	FLAG_OSC	FLAG_IREF	FLAG_VBG	00h
77h	FLAG7	CALC_NVCRC								95h
78h	FLAG8	CALC_CONFRC								X
7Bh	FLAG11	FLAG_OPENCH 7	FLAG_OPENCH 6	FLAG_OPENCH 5	FLAG_OPENCH 4	FLAG_OPENCH 3	FLAG_OPENCH 2	FLAG_OPENCH 1	FLAG_OPENCH 0	00h
7Ch	FLAG12	Reserved	Reserved	Reserved	Reserved	FLAG_OPENCH 11	FLAG_OPENCH 10	FLAG_OPENCH 9	FLAG_OPENCH 8	00h
7Dh	FLAG13	FLAG_SHORTC H7	FLAG_SHORTC H6	FLAG_SHORTC H5	FLAG_SHORTC H4	FLAG_SHORTC H3	FLAG_SHORTC H2	FLAG_SHORTC H1	FLAG_SHORTC H0	00h
7Eh	FLAG14	Reserved	Reserved	Reserved	Reserved	FLAG_SHORTC H11	FLAG_SHORTC H10	FLAG_SHORTC H9	FLAG_SHORTC H8	00h
7Fh	FLAG15							FLAG_OFFOUT	FLAG_LDOOV	00h

## MTP register map

Table 27. MTP register map

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
80h	NVI0	Reserved	Reserved				NV_IOUT0			3Fh
81h	NVI1	Reserved	Reserved				NV_IOUT1			3Fh
82h	NVI2	Reserved	Reserved				NV_IOUT2			3Fh
83h	NVI3	Reserved	Reserved				NV_IOUT3			3Fh
84h	NVI4	Reserved	Reserved				NV_IOUT4			3Fh
85h	NVI5	Reserved	Reserved				NV_IOUT5			3Fh
86h	NVI6	Reserved	Reserved				NV_IOUT6			3Fh
87h	NVI7	Reserved	Reserved				NV_IOUT7			3Fh
88h	NVI8	Reserved	Reserved				NV_IOUT8			3Fh
89h	NVI9	Reserved	Reserved				NV_IOUT9			3Fh
8Ah	NVI10	Reserved	Reserved				NV_IOUT10			3Fh
8Bh	NVI11	Reserved	Reserved				NV_IOUT11			3Fh
A0h	NVP0						NV_PWMOUT0			FFh
A1h	NVP1						NV_PWMOUT1			FFh
A2h	NVP2						NV_PWMOUT2			FFh
A3h	NVP3						NV_PWMOUT3			FFh
A4h	NVP4						NV_PWMOUT4			FFh
A5h	NVP5						NV_PWMOUT5			FFh
A6h	NVP6						NV_PWMOUT6			FFh
A7h	NVP7						NV_PWMOUT7			FFh
A8h	NVP8						NV_PWMOUT8			FFh
A9h	NVP9						NV_PWMOUT9			FFh
AAh	NVP10						NV_PWMOUT10			FFh

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
ABh	NVP11	NV_PWMOUT11								FFh
BCh	NV16	NV_ADCSHORTTH1[7:0]								00h
BDh	NV17	NV_ADCSH ORTTHCH7	NV_ADCSH ORTTHCH6	NV_ADCSH ORTTHCH5	NV_ADCSH ORTTHCH4	NV_ADCSH ORTTHCH3	NV_ADCSH ORTTHCH2	NV_ADCSH ORTTHCH1	NV_ADCSH ORTTHCH0	00h
BEh	NV18	Reserved	Reserved	Reserved	Reserved	NV_ADCSH ORTTHCH11	NV_ADCSH ORTTHCH10	NV_ADCSH ORTTHCH9	NV_ADCSH ORTTHCH8	00h
BFh	NV19	NV_OFFDelay	NV_PS0[1:0]		NV_LOWVBATTH [4:0]					00h
C0h	NV0	NV_FS0CH7	NV_FS0CH6	NV_FS0CH5	NV_FS0CH4	NV_FS0CH3	NV_FS0CH2	NV_FS0CH1	NV_FS0CH0	00h
C1h	NV1	Reserved	Reserved	Reserved	Reserved	NV_FS0CH11	NV_FS0CH10	NV_FS0CH9	NV_FS0CH8	00h
C2h	NV2	NV_FS1CH7	NV_FS1CH6	NV_FS1CH5	NV_FS1CH4	NV_FS1CH3	NV_FS1CH2	NV_FS1CH1	NV_FS1CH0	FFh
C3h	NV3	Reserved	Reserved	Reserved	Reserved	NV_FS1CH11	NV_FS1CH10	NV_FS1CH9	NV_FS1CH8	0Fh
C4h	NV4	NV_DIAGENC H7	NV_DIAGENC H6	NV_DIAGENC H5	NV_DIAGENC H4	NV_DIAGENC H3	NV_DIAGENC H2	NV_DIAGENC H1	NV_DIAGENC H0	FFh
C5h	NV5	Reserved	Reserved	Reserved	Reserved	NV_DIAGENC H11	NV_DIAGENC H10	NV_DIAGENC H9	NV_DIAGENC H8	0Fh
C6h	NV6	NV_AUTOSS	Reserved	NV_DEVADDR [4]	NV_EXPEN	NV_DEVADDR [3:0]				80h
C7h	NV7	NV_PWMFREQ				NV_EXTADDR	NV_OFAF	NV_REFRANGE		AFh
C8h	NV8	Reserved	NV_FLTIMEOUT			NV_ADCLOWVSTH				03h
C9h	NV9	NV_ODIOUT				NV_ODPW				00h
CAh	NV10	NV_WDTIMER				NV_INITTIMER				00h
CBh	NV11	NV_ADCSHORTTH0								00h
CCh	NV12	NV_LOW VBAT_FD	NV_ADDR_FD	NV_CON FCRC_FD	NV_PWM_FD	NV_STA_FD	NV_OSC_FD	NV_IREF_FD	NV_VBG_FD	00h
CDh	NV13	NV_CRC_SEL	Reserved	NV_PWMSLOW	NV_LENEXT	NV_PSEN3	NV_PSEN2	NV_PSEN1	NV_PSEN0	00h
CEh	NV14	Reserved	Reserved	Reserved	NV_OFFOUT_FD	NV_MAS KPRETSD	NV_MASKVSUV	NV_MAS KLOWVS	NV_MASKSLS	00h
CFh	NV15	NV_CRC								95h

## 14.6. Layout guide

A good PCB layout can minimize EMI, improve thermal performance, and achieve a good constant current output.

For NEX13120F-Q100, the following PCB layout guidelines are recommended:

- Use a continuous ground plane layer beneath the device and associated circuitry, incorporating multiple vias for enhanced grounding.
- Place the VLDO capacitor as close as possible to both the VLDO pin and the ground pin. This practice minimizes stray inductance and reduces the current loop area, helping to prevent EMI.
- Maximize the number of vias on the thermal pad to improve thermal performance.

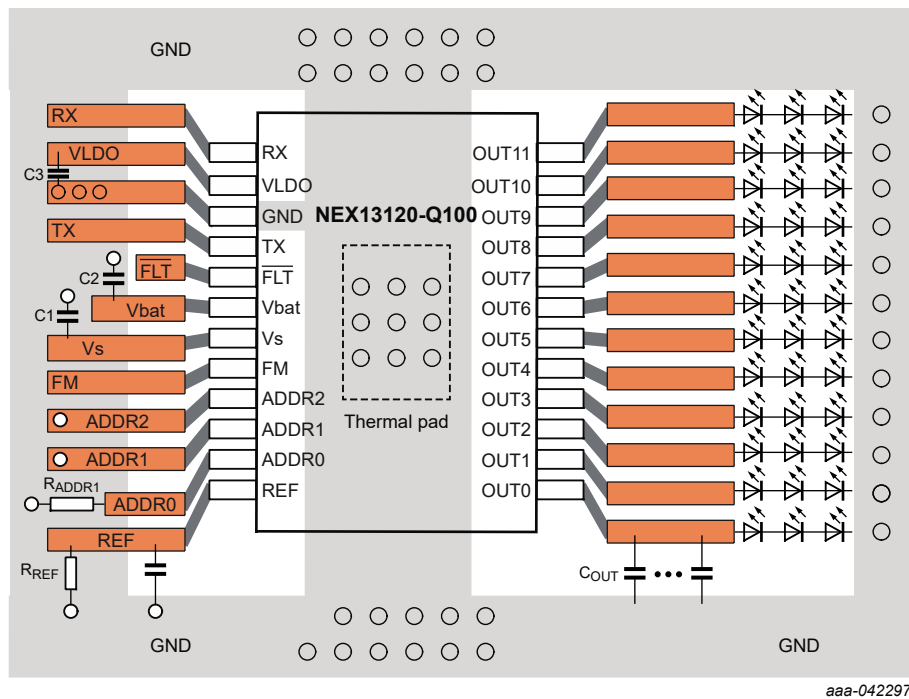


Fig. 42. Layout example

15. Package outline

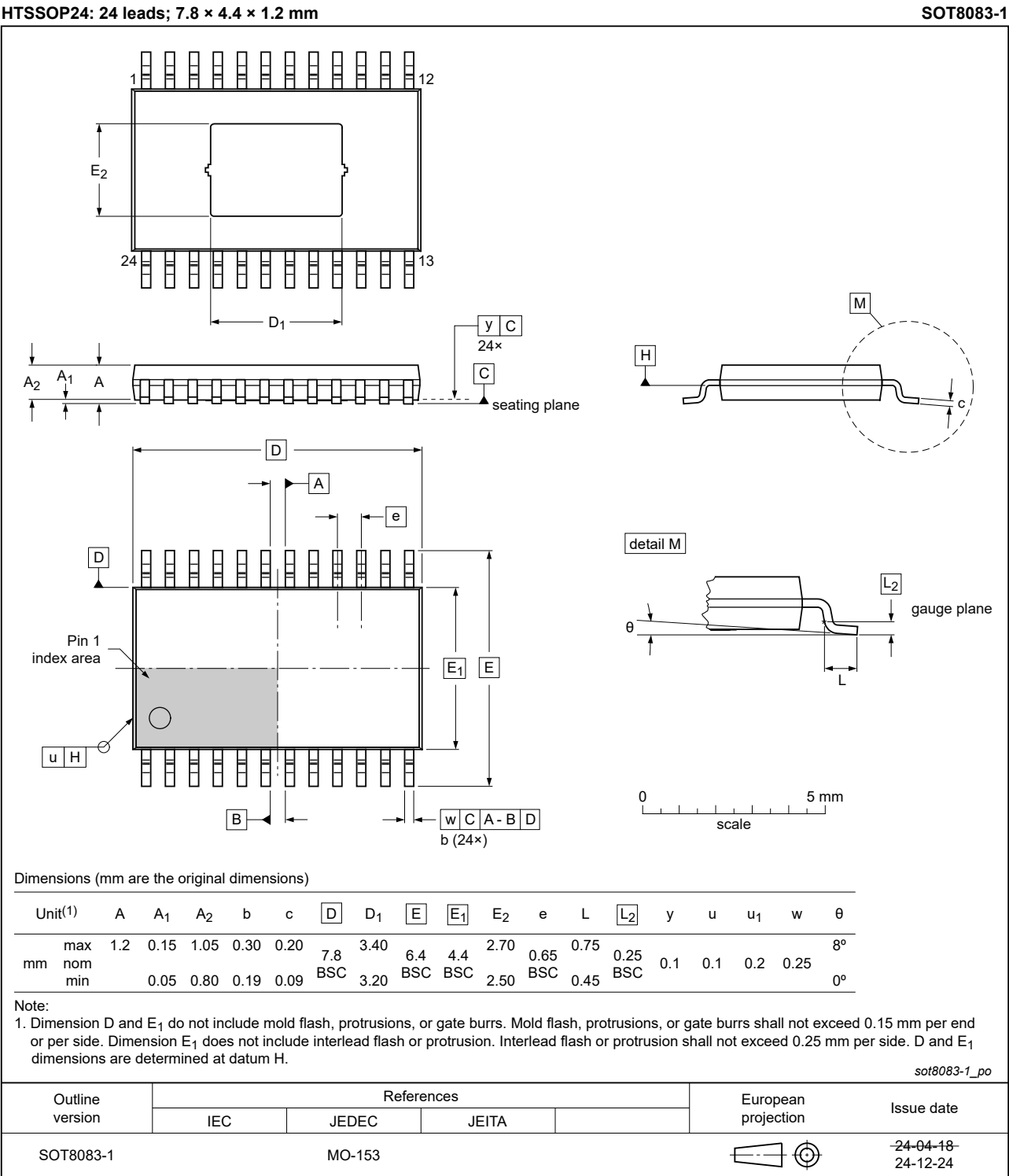


Fig. 43. Pin configuration SOT8083-1 (HTSSOP24)

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16. Abbreviations

Table 28. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
AEC	Automotive Electronics Council
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CAN	Controller Area Network
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CRC	Cyclic Redundancy Check
DCO	Dynamic Controlled Output
DUT	Device Under Test
ECC	Error Correction Code
ECP	Enhanced Capability Port
EDNMOS	Extended Drain Negative Metal-Oxide Semiconductor
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESDA	Electrostatic Discharge Association
EPP	Enhanced Parallel Port
FET	Field-Effect Transistor
FIFO	First In First Out
HBM	Human Body Model
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
JEDEC	Joint Electron Device Engineering Council
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LIN	Local Interconnect Network
LSB	Least Significant Bit
LSTTL	Low-power Schottky Transistor-Transistor Logic
MCU	Microcontroller Unit
MM	Machine Model
MSB	Most Significant Bit
MTP	Multi-time Programming
NMOS	N-channel Metal-Oxide Semiconductor
NTC	Negative Temperature Coefficient
ODPW	Output Diagnostic and PWM Time
OSC	Oscillator
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide Semiconductor
POR	Power-On Reset
PRR	Pulse Rate Repetition
PTC	Positive Temperature Coefficient

Acronym	Description
PWM	Pulse Width Modulation
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
UVLO	Under-Voltage Lockout
VLDO	Very Low Dropout Regulator

## 17. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX13120F_Q100 v.1	May 29, 2025	Preliminary data sheet	-	-

## 18. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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