

ASPM34 Series

Automotive 3-Phase 1200 V, 35 A IGBT Intelligent Power Module



ON Semiconductor®

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NFVA23512NP2T

General Description

NFVA23512NP2T is an advanced Auto IPM module providing a fully-featured, high-performance inverter output stage for hybrid and electric vehicles. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

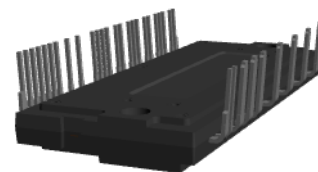
- Automotive SPM® in 34 pin DIP package
- AEC & AQG324 Qualified and PPAP Capable
- 1200 V – 35 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low-Loss, Short-Circuit Rated IGBTs
- Very Low Thermal Resistance using Al₂O₃ DBC Substrate
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply Supported
- Built-In NTC Thermistor for Temperature Monitoring and Management
- Adjustable Over-Current Protection via Integrated Sense-IGBTs
- Isolation Rating of 2500 Vrms/1 min
- This is a Pb-Free Device

Applications

- Automotive High Voltage Auxiliary Motors
 - ◆ Climate e-Compressors
 - ◆ Oil/Water Pumps
 - ◆ Super/Turbo Chargers
 - ◆ Variety Fans
- Motion Control
 - ◆ Industrial Motor

Related Resources

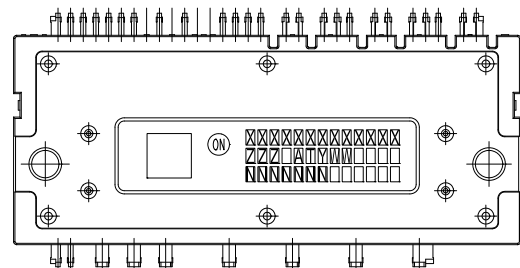
- [AN-9075](#) – Users Guide for 1200V SPM® 2 Series
- [AN-9076](#) – Mounting Guide for New SPM® 2 Package
- [AN-9079](#) – Thermal Performance of 1200V Motion SPM® 2 Series by Mounting Torque



3D Package Drawing
(Click to Activate 3D Content)

**DIP34 80x33, AUTOMOTIVE MODULE
CASE MODGL**

MARKING DIAGRAM



XXXXXXXXXXXX = Specific Device Code
 ZZZ = Lot ID
 AT = Assembly & Test Location
 Y = Year
 W = Work Week
 NNN = Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NFVA23512NP2T

Integrated Power Functions

- 1200 V–35 A IGBT inverter for three–phase DC/AC power conversion (Refer to Figure 1)

Integrated Drive, Protection and System Control Functions

- For inverter high–side IGBTs: gate drive circuit, high–voltage isolated high–speed level shifting control circuit, Under–Voltage Lock–Out Protection (UVLO)

- For inverter low–side IGBTs: gate drive circuit, Short–Circuit Protection (SCP) control supply circuit, Under–Voltage Lock–Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low–side supply) and SC faults
- Input interface: active–high interface, works with 3.3/5 V logic, schmitt–trigger input

PIN CONFIGURATION

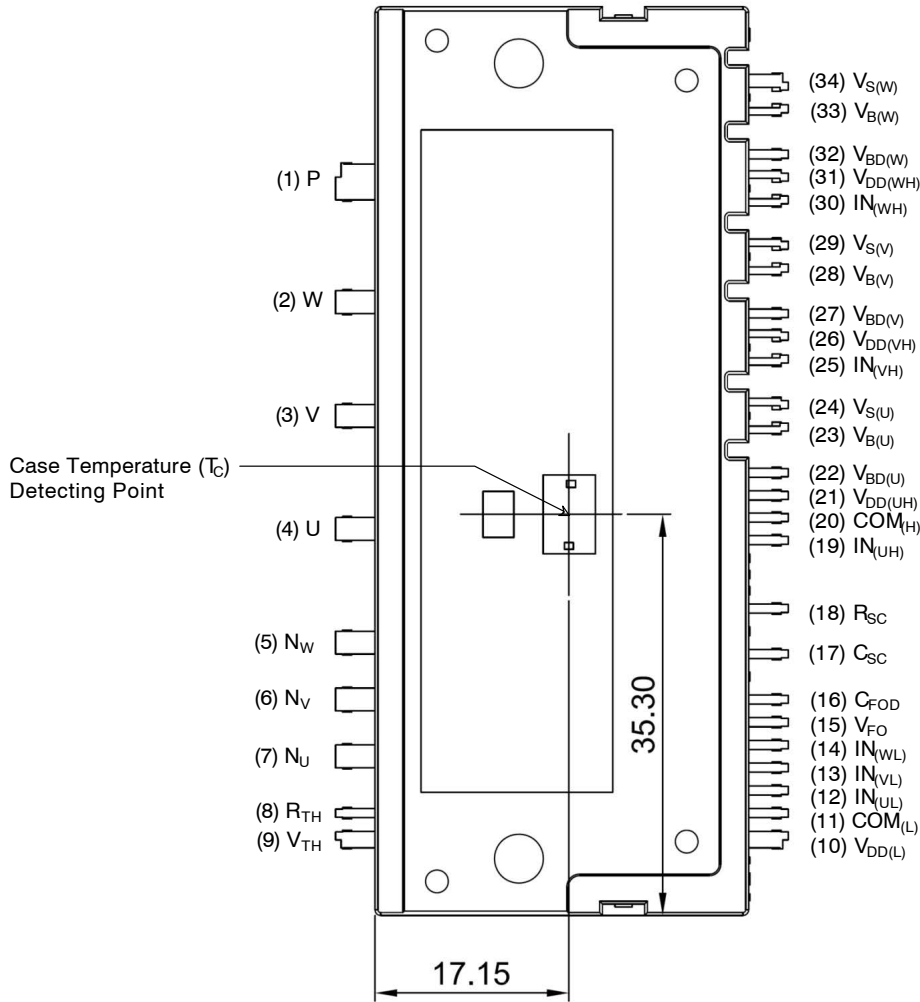


Figure 1. Top View

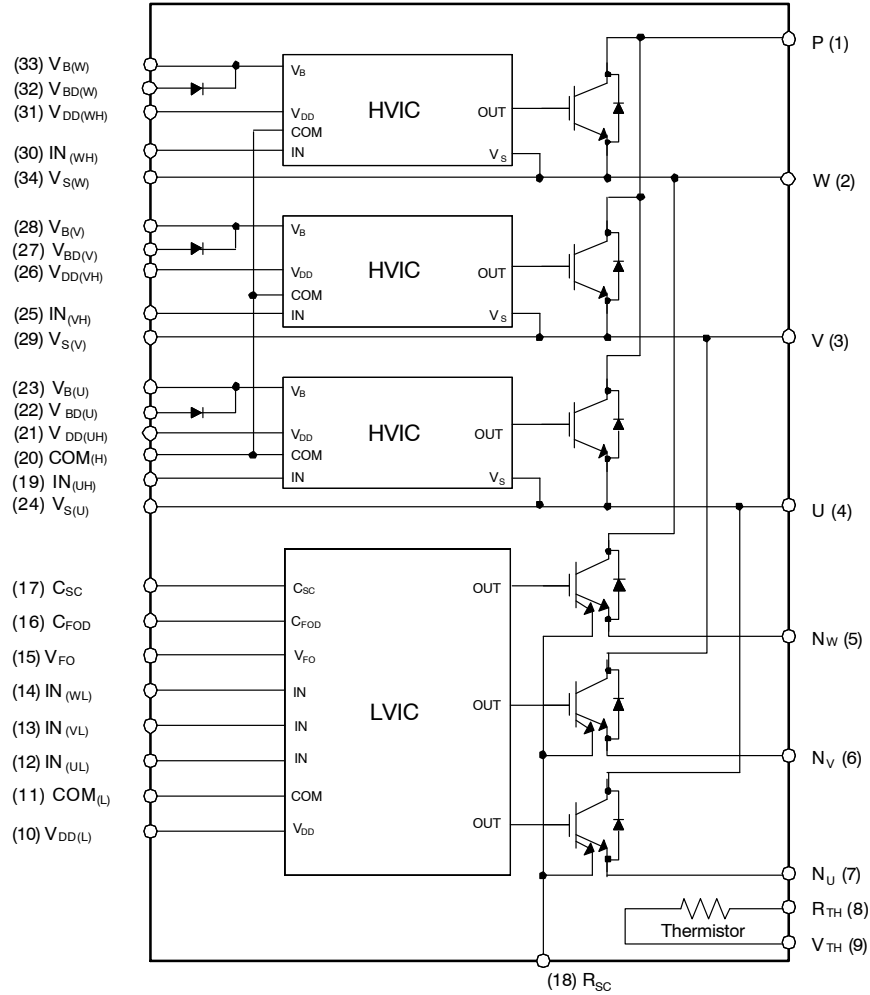
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PIN DESCRIPTIONS

| Pin Number | Pin Name | Pin Description |
|------------|---------------------|--|
| 1 | P | Positive DC-Link Input |
| 2 | W | Output for W Phase |
| 3 | V | Output for V Phase |
| 4 | U | Output for U Phase |
| 5 | N _W | Negative DC-Link Input for W Phase |
| 6 | N _V | Negative DC-Link Input for V Phase |
| 7 | N _U | Negative DC-Link Input for U Phase |
| 8 | R _{TH} | Series Resistor for Thermistor (Temperature Detection) |
| 9 | V _{TH} | Thermistor Bias Voltage |
| 10 | V _{DD(L)} | Low-Side Bias Voltage for IC and IGBTs Driving |
| 11 | COM _(L) | Low-Side Common Supply Ground |
| 12 | IN _(UL) | Signal Input for Low-Side U Phase |
| 13 | IN _(VL) | Signal Input for Low-Side V Phase |
| 14 | IN _(WL) | Signal Input for Low-Side W Phase |
| 15 | V _{FO} | Fault Output |
| 16 | C _{FOD} | Capacitor for Fault Output Duration Selection |
| 17 | C _{SC} | Shut Down Input for Short-Circuit Current Detection Input |
| 18 | R _{SC} | Resistor for Short-Circuit Current Detection |
| 19 | IN _(UH) | Signal Input for High-Side U Phase |
| 20 | COM _(H) | High-Side Common Supply Ground |
| 21 | V _{DD(UH)} | High-Side Bias Voltage for U Phase IC |
| 22 | V _{BD(U)} | Anode of Bootstrap Diode for U Phase High-Side Bootstrap Circuit |
| 23 | V _{B(U)} | High-Side Bias Voltage for U Phase IGBT Driving |
| 24 | V _{S(U)} | High-Side Bias Voltage Ground for U Phase IGBT Driving |
| 25 | IN _(VH) | Signal Input for High-Side V Phase |
| 26 | V _{DD(VH)} | High-Side Bias Voltage for V Phase IC |
| 27 | V _{BD(V)} | Anode of Bootstrap Diode for V Phase High-Side Bootstrap Circuit |
| 28 | V _{B(V)} | High-Side Bias Voltage for V Phase IGBT Driving |
| 29 | V _{S(V)} | High-Side Bias Voltage Ground for V Phase IGBT Driving |
| 30 | IN _(WH) | Signal Input for High-Side W Phase |
| 31 | V _{DD(WH)} | High-Side Bias Voltage for W Phase IC |
| 32 | V _{BD(W)} | Anode of Bootstrap Diode for W Phase High-Side Bootstrap Circuit |
| 33 | V _{B(W)} | High-Side Bias Voltage for W Phase IGBT Driving |
| 34 | V _{S(W)} | High-Side Bias Voltage Ground for W Phase IGBT Driving |

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INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTES:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

Figure 2. Internal Block Diagram

NFVA23512NP2T

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Rating | Unit |
|------------------------|------------------------------------|---|---------|------|
| INVERTER PART | | | | |
| V _{PN} | Supply Voltage | Applied between P–N _U , N _V , N _W | 900 | V |
| V _{PN(Surge)} | Supply Voltage (Surge) | Applied between P–N _U , N _V , N _W | 1000 | V |
| V _{CES} | Collector–Emitter Voltage | | 1200 | V |
| ±I _C | Each IGBT Collector Current | T _C = 100°C, T _J ≤ 150°C, V _{DD} ≥ 15 V (Note 4) | 35 | A |
| ±I _{CP} | Each IGBT Collector Current (Peak) | T _C = 25°C, T _J ≤ 150°C, Under 1 ms Pulse Width (Note 4) | 70 | A |
| P _C | Collector Dissipation | T _C = 25°C per One Chip (Note 4) | 171 | W |
| T _J | Operating Junction Temperature | V _{CES} = 960 V | –40–150 | °C |
| | | V _{CES} = 1200 V | –40–125 | |

CONTROL PART

| | | | | |
|-----------------|--------------------------------|---|---------------------------|----|
| V _{DD} | Control Supply Voltage | Applied between V _{DD(H)} , V _{DD(L)} – COM | 20 | V |
| V _{BS} | High–Side Control Bias Voltage | Applied between V _{B(U)} –V _{S(U)} , V _{B(V)} –V _{S(V)} , V _{B(W)} –V _{S(W)} | 20 | V |
| V _{IN} | Input Signal Voltage | Applied between I _{N(UH)} , I _{N(VH)} , I _{N(WH)} , I _{N(UL)} , I _{N(VL)} , I _{N(WL)} – COM | –0.3–V _{DD} +0.3 | V |
| V _{FO} | Fault Output Supply Voltage | Applied between V _{FO} – COM | –0.3–V _{DD} +0.3 | V |
| I _{FO} | Fault Output Current | Sink Current at V _{FO} pin | 2 | mA |
| V _{SC} | Current Sensing Input Voltage | Applied between C _{SC} – COM | –0.3–V _{DD} +0.3 | V |

BOOTSTRAP DIODE PART

| | | | | |
|------------------|---|--|---------|----|
| V _{RRM} | Maximum Repetitive Reverse Voltage | | 1200 | V |
| I _F | Forward Current | T _C = 25°C, T _J ≤ 150°C (Note 4) | 1.0 | A |
| I _{FP} | Forward Current (Peak) | T _C = 25°C, T _J ≤ 150°C, Under 1 ms Pulse Width (Note 4) | 2.0 | A |
| T _J | Operating Junction Temperature (Note 5) | | –40–150 | °C |

TOTAL SYSTEM

| | | | | |
|------------------|------------------------------|--|---------|------------------|
| t _{SC} | Short Circuit Withstand Time | V _{DD} = V _{BS} ≤ 16.5 V, V _{PN} ≤ 800 V, T _J = 150°C Non-repetitive | 3 | μs |
| T _{STG} | Storage Temperature | | –40–150 | °C |
| V _{ISO} | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate | 2500 | V _{rms} |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. These values had been made an acquisition by the calculation considered to design factor.

THERMAL RESISTANCE

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--|--|------|------|------|------|
| R _{th(j-c)Q} | Junction to Case Thermal Resistance (Note 5) | Inverter IGBT part (per 1/6 module) | – | – | 0.73 | °C/W |
| R _{th(j-c)F} | | Inverter FWD part (per 1/6 module) | – | – | 1.26 | °C/W |
| L _σ | Package Stray Inductance | P to N _U , N _V , N _W (Note 6) | – | 32 | – | nH |

5. For the measurement point of case temperature (T_C), please refer to Figure 1. DBC discoloration and Picker Circle Printing allowed, please refer to application note [AN-9190](#) (Impact of DBC Oxidation on SPM[®] Module Performance).

6. Stray inductance per phase measured per IEC 60747–15.

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ELECTRICAL CHARACTERISTICS – INVERTER PART (T_J as specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit | |
|---------------|--|--|--------------|------|------|---------------|---------------|
| $V_{CE(SAT)}$ | Collector – Emitter Saturation Voltage | $V_{DD} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_C = 35\text{ A}$, $T_J = 25^\circ\text{C}$ | – | 1.90 | 2.50 | V | |
| | | $V_{DD} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_C = 35\text{ A}$, $T_J = 150^\circ\text{C}$ | | 2.35 | 2.95 | V | |
| V_F | FWDi Forward Voltage | $V_{IN} = 0\text{ V}$, $I_F = 35\text{ A}$, $T_J = 25^\circ\text{C}$ | – | 2.10 | 2.70 | V | |
| | | $V_{IN} = 0\text{ V}$, $I_F = 35\text{ A}$, $T_J = 150^\circ\text{C}$ | | 2.05 | 2.65 | V | |
| HS | t_{ON} | High Side Switching Times $V_{PN} = 600\text{ V}$, $V_{DD} = 15\text{ V}$, $I_C = 35\text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \Leftrightarrow 5\text{ V}$, Inductive Load See Figure 4 (Note 7) | 0.70 | 1.20 | 1.80 | μs | |
| | | | $t_{C(ON)}$ | – | 0.40 | 0.85 | μs |
| | | | t_{OFF} | – | 1.20 | 1.80 | μs |
| | | | $t_{C(OFF)}$ | – | 0.15 | 0.55 | μs |
| | | | t_{rr} | – | 0.20 | – | μs |
| LS | t_{ON} | Low Side Switching Times $V_{PN} = 600\text{ V}$, $V_{DD} = 15\text{ V}$, $I_C = 35\text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \Leftrightarrow 5\text{ V}$, Inductive Load See Figure 4 (Note 7) | 0.50 | 1.00 | 1.60 | μs | |
| | | | $t_{C(ON)}$ | – | 0.40 | 0.85 | μs |
| | | | t_{OFF} | – | 1.40 | 2.00 | μs |
| | | | $t_{C(OFF)}$ | – | 0.20 | 0.60 | μs |
| | | | t_{rr} | – | 0.25 | – | μs |
| I_{CES} | Collector–Emitter Leakage Current | $T_J = 25^\circ\text{C}$, $V_{CE} = V_{CES}$ | – | – | 3 | mA | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information see Figure 3.

PACKAGE MARKING AND ORDERING INFORMATION

| Device | Device Marking | Package | Shipping |
|---------------|----------------|-------------------------|--------------|
| NFVA23512NP2T | NFVA23512NP2T | ASPM34-CAA (Pb-Free) | 6 Units/Tube |

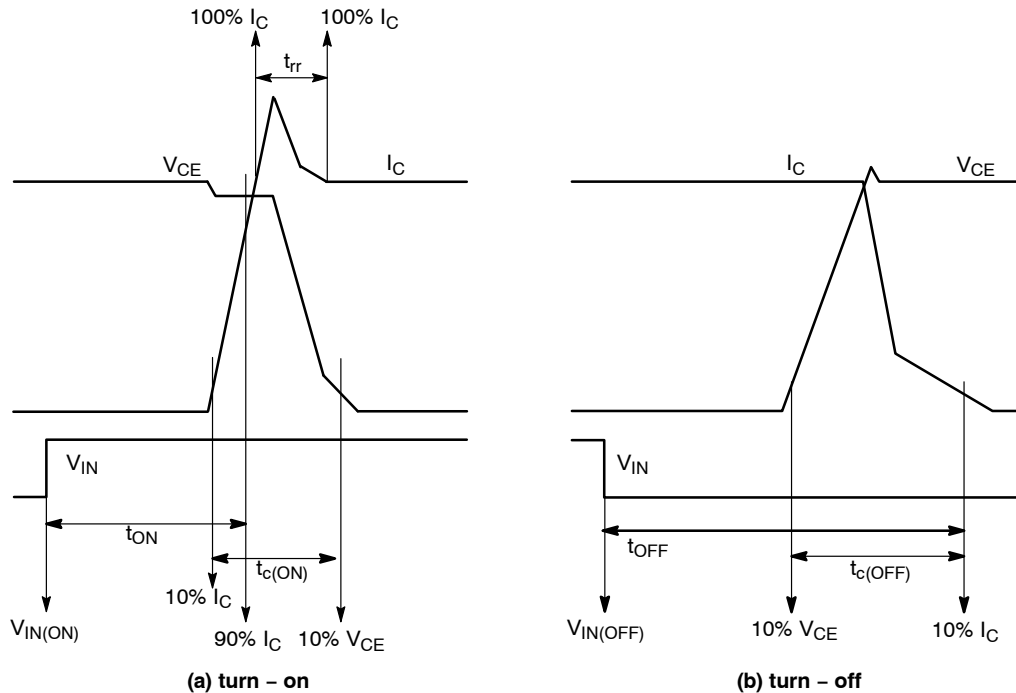


Figure 3. Switching Time Definition

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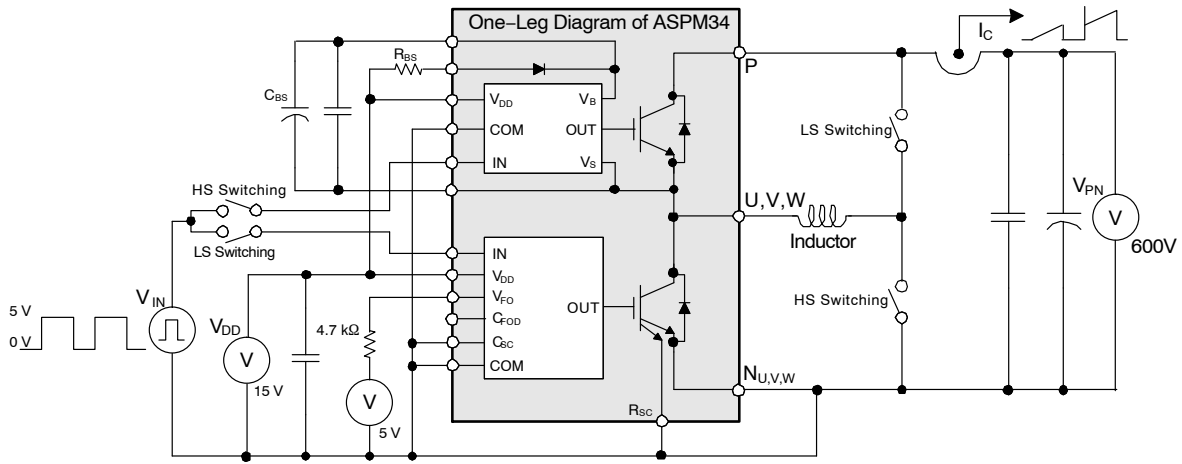


Figure 4. Example Circuit for Switching Test

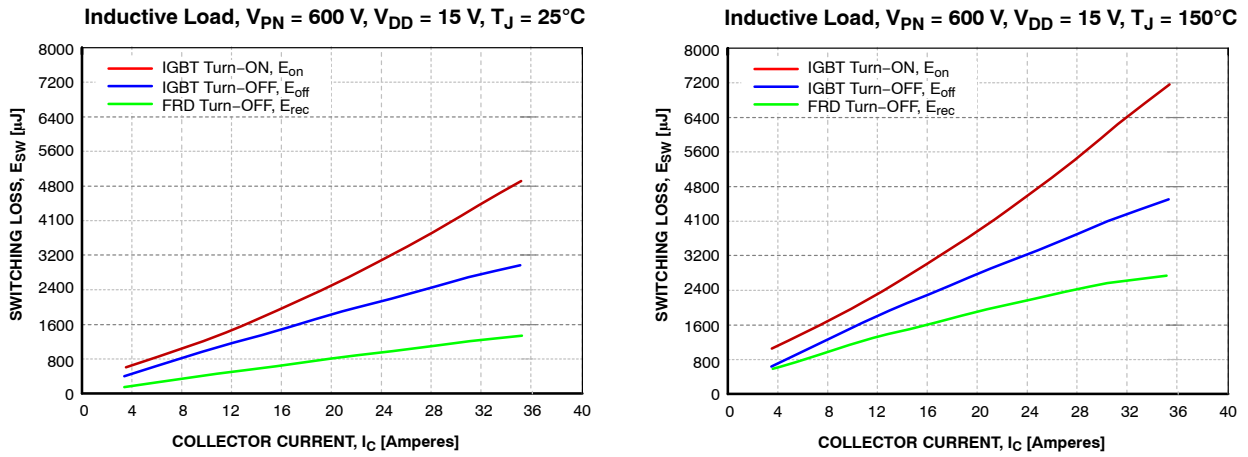


Figure 5. Switching Loss Characteristics

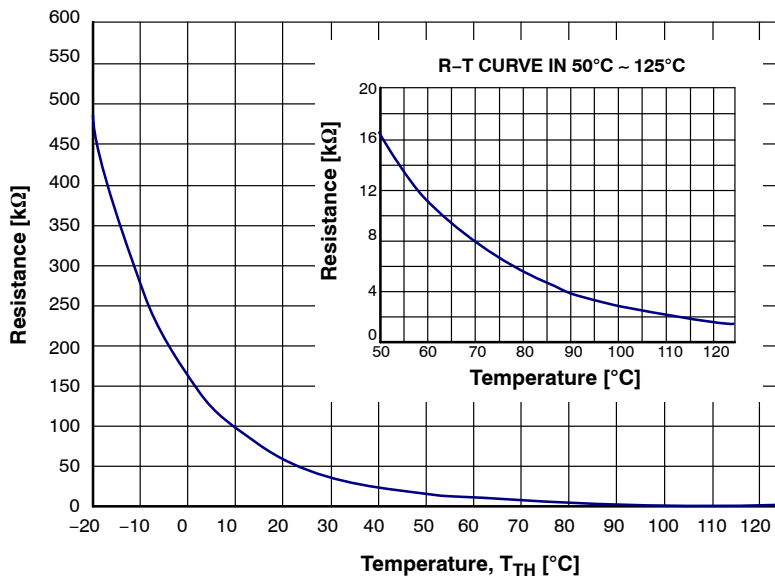


Figure 6. R-T Curve of Built-in Thermistor

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BOOTSTRAP DIODE PART (T_J as specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|-----------------------|--|------|------|------|------|
| V _F | Forward Voltage | I _F = 1.0 A, T _J = 25°C | - | 2.2 | - | V |
| t _{rr} | Reverse-Recovery Time | I _F = 1.0 A, dI _F /dt = 50 A/μs, T _J = 25°C | - | 80 | - | ns |

CONTROL PART (T_J = 25°C)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit | |
|----------------------|--|--|--|------|------|------|----|
| I _{QDDH} | Quiescent V _{DD} Supply Current | V _{DD(H)} = 15 V, I _{N(UH,VH,WH)} = 0 V | | - | 0.15 | mA | |
| I _{QDDL} | | V _{DD(L)} = 15 V, I _{N(UL,VL,WL)} = 0 V | V _{DD(UH) - COM(H), V_{DD(VH) - COM(H), V_{DD(WH) - COM(H)}}} | | - | 4.80 | mA |
| I _{PDDH} | Operating V _{DD} Supply Current | V _{DD(H)} = 15 V, f _{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High-Side | V _{DD(UH) - COM(H), V_{DD(VH) - COM(H), V_{DD(WH) - COM(H)}}} | - | - | 0.30 | mA |
| I _{PDDL} | | V _{DD(L)} = 15 V, f _{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for Low-Side | V _{DD(L) - COM(L)} | - | - | 15.5 | mA |
| I _{QBS} | Quiescent V _{BS} Supply Current | V _{BS} = 15 V, I _{N(UH,VH,WH)} = 0 V | V _{B(U) - V_{S(U), V_{B(V) - V_{S(V), V_{B(W) - V_{S(W)}}}}}} | - | - | 0.30 | mA |
| I _{PBS} | Operating V _{BS} Supply Current | V _{DD} = V _{BS} = 15 V, f _{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High-Side | V _{B(U) - V_{S(U), V_{B(V) - V_{S(V), V_{B(W) - V_{S(W)}}}}}} | - | - | 12.0 | mA |
| V _{FOH} | Fault Output Voltage | V _{DD} = 15 V, V _{SC} = 0 V, V _{FO} Circuit: 4.7 kΩ to 5 V Pull-up | | 4.5 | - | - | V |
| V _{FOL} | | V _{DD} = 15 V, V _{SC} = 1 V, V _{FO} Circuit: 4.7 kΩ to 5 V Pull-up | | - | - | 0.50 | V |
| I _{SEN} | Sensing Current of Each Sense IGBT | V _{DD} = 15 V, V _{IN} = 5 V, R _{SC} = 0 Ω, No Connection of Shunt Resistor at N _{U,V,W} terminal | I _C = 35 A | - | 36.0 | - | mA |
| V _{SC(ref)} | Short Circuit Trip Level | V _{DD} = 15 V (Note 8) | C _{SC} - COM(L) | 0.43 | 0.50 | 0.57 | V |
| I _{SC} | Short Circuit Current Level for Trip | R _{SC} = 16 Ω (±1%), No Connection of Shunt Resistor at N _{U,V,W} Terminal (Note 8) | | - | 70 | - | A |
| UV _{DDD} | Supply Circuit Under-Voltage Protection | Detection Level | | 10.3 | - | 12.8 | V |
| UV _{DDR} | | Reset Level | | 10.8 | - | 13.3 | V |
| UV _{BSD} | | Detection Level | | 9.5 | - | 12.0 | V |
| UV _{BSR} | | Reset Level | | 10.0 | - | 12.5 | V |
| t _{FOD} | Fault-Out Pulse Width | C _{FOD} = Open | (Note 9) | 50 | - | - | μs |
| | | C _{FOD} = 2.2 nF | | 1.7 | - | - | ms |
| V _{IN(ON)} | ON Threshold Voltage | Applied between I _{N(UH,VH,WH)} - COM(H) | | - | - | 2.6 | V |
| V _{IN(OFF)} | OFF Threshold Voltage | I _{N(UL,VL,WL)} - COM(L) | | 0.8 | - | - | V |
| R _{TH} | Resistance of Thermistor | at T _{TH} = 25°C | See Figure 6 (Note 10) | - | 47 | - | kΩ |
| | | at T _{TH} = 100°C | | - | 2.9 | - | kΩ |

8. Short-circuit current protection functions only at the low-sides because the sense current is divided from main current at low-side IGBTs. Inserting the shunt resistor for monitoring the phase current at N_U, N_V, N_W terminal, the trip level of the short-circuit current is changed.

9. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation :

$$t_{FOD} = 0.8 \times 10^6 \times C_{FOD}$$

10. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), conduct experiments considering the application.

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RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Value | | | Unit |
|--------------------------------|--|--|-------|------|------|--------------------|
| | | | Min. | Typ. | Max. | |
| V_{PN} | Supply Voltage | Applied between P – N_U , N_V , N_W | 300 | 600 | 800 | V |
| V_{DD} | Control Supply Voltage | Applied between $V_{DD(UH, VH, WH)} - COM_{(H)}$, $V_{DD(L)} - COM_{(L)}$ | 14.0 | 15 | 16.5 | V |
| V_{BS} | High-Side Bias Voltage | Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | 13.0 | 15 | 18.5 | V |
| dV_{DD}/dt , dV_{BS}/dt | Control Supply Variation | | -1 | - | 1 | V/ μ s |
| t_{dead} | Blanking Time for Preventing Arm-Short | For Each Input Signal | 2.0 | - | - | μ s |
| f_{PWM} | PWM Input Signal | $-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ | - | - | 20 | kHz |
| V_{SEN} | Voltage for Current Sensing | Applied between N_U , N_V , $N_W - COM_{(H, L)}$ (Including Surge Voltage) | -5 | - | 5 | V |
| $PW_{IN(ON)}$ | Minimum Input Pulse Width | $V_{DD} = V_{BS} = 15\text{ V}$, $I_C \leq 70\text{ A}$, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10 nH (Note 11) | 2.0 | - | - | μ s |
| $PW_{IN(OFF)}$ | | | 2.0 | - | - | |
| T_J | Junction Temperature | | -40 | - | 150 | $^{\circ}\text{C}$ |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. This product might not make response if input pulse width is less than the recommended value.

MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Conditions | Value | | | Unit | |
|---------------------------|------------------------------------|------------------------|------|------|---------------|-------|
| | | Min. | Typ. | Max. | | |
| Device Flatness | See Figure 7 | 0 | - | +200 | μm | |
| Mounting Torque | Mounting Screw: M4 See Figure 8 | Recommended 1.0 N•m | 0.9 | 1.0 | 1.5 | N•m |
| | | Recommended 10.1 kg•cm | 9.1 | 10.1 | 15.1 | kg•cm |
| Terminal Pulling Strength | Load 19.6 N | 10 | - | - | s | |
| Terminal Bending Strength | Load 9.8 N, 90 degrees Bend | 2 | - | - | times | |
| Weight | | - | 50 | - | g | |

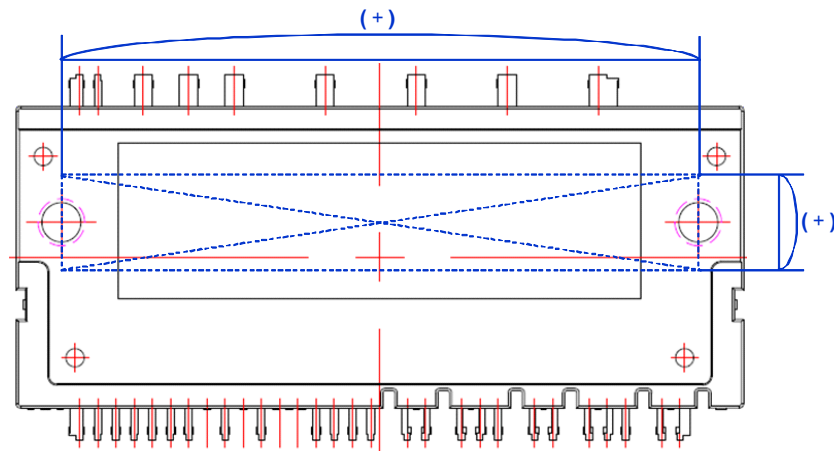
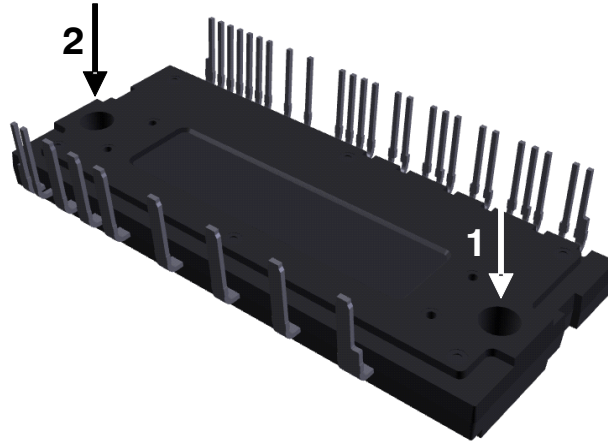


Figure 7. Flatness Measurement Position

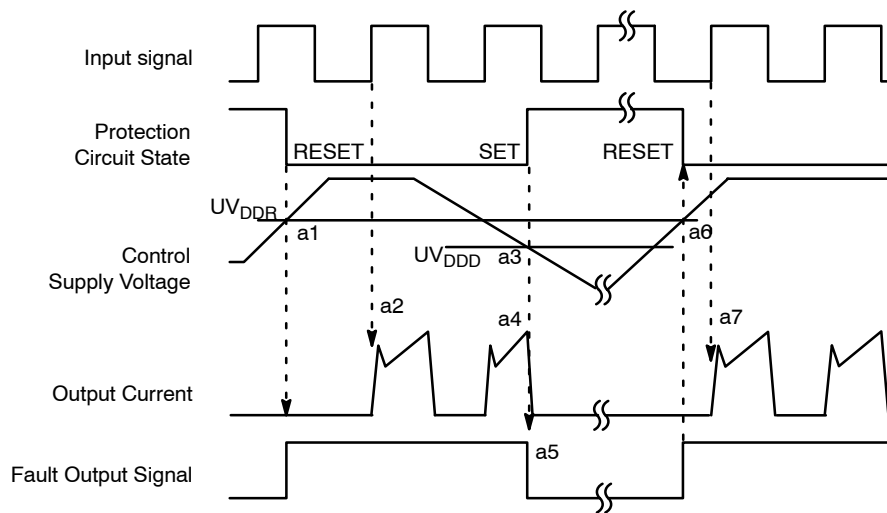
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NOTES:

- 12. Do not make over torque when mounting screws. Much mounting torque may cause DBC cracks, as well as bolts and Al heat-sink destruction.
- 13. Avoid one-sided tightening stress. Figure 8 shows the recommended torque order for mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre-screwing torque is set to 20–30% of maximum torque rating.

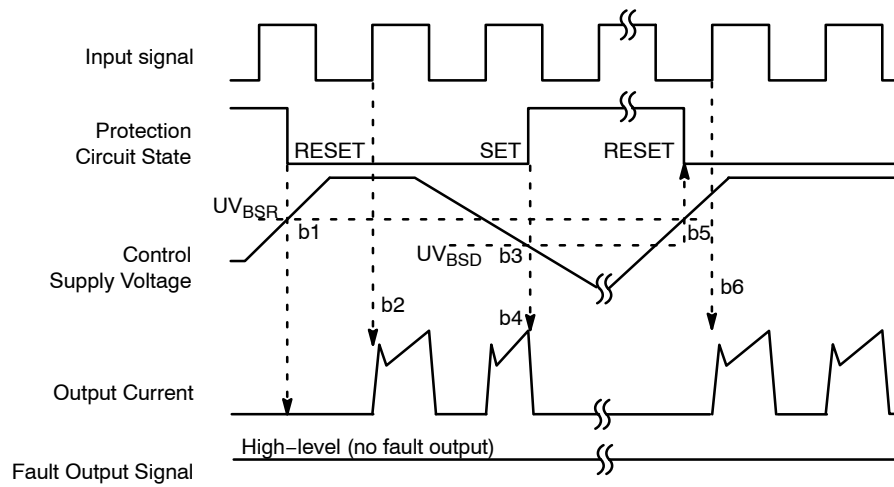
Figure 8. Mounting Screws Torque Order



- a1: Control supply voltage rises: After the voltage rises UV_{DDR} , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UV_{DDD}).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .
- a6: Under voltage reset (UV_{DDR}).
- a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 9. Under-Voltage Protection (Low-Side)

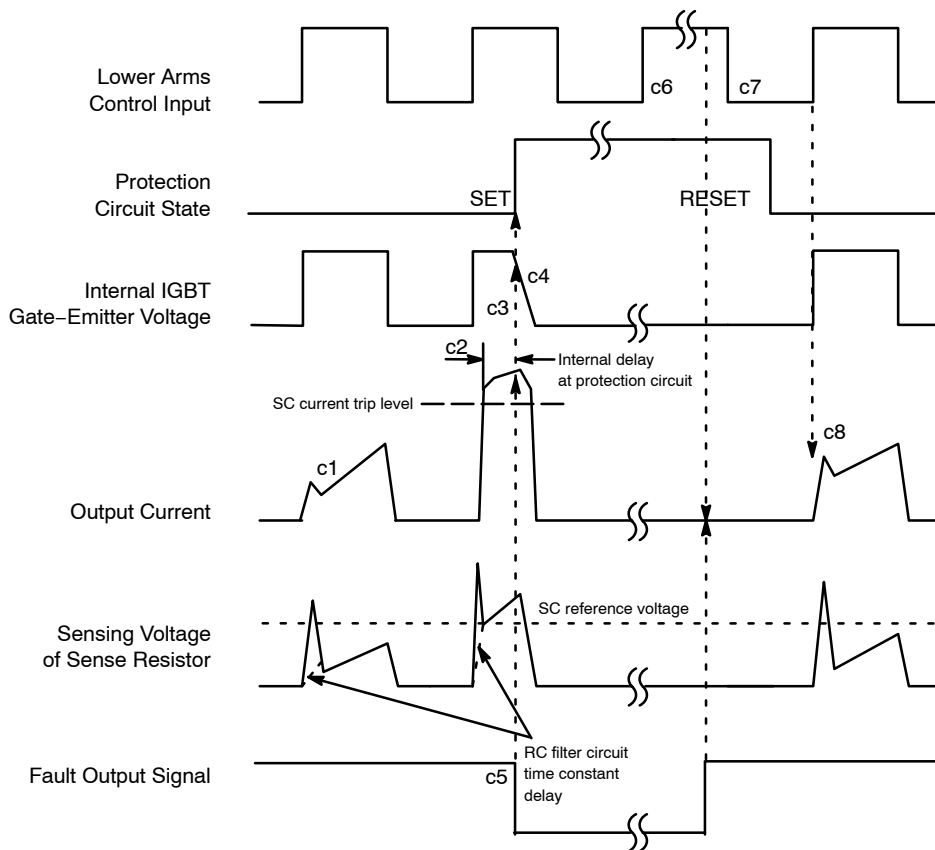
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- b1: Control supply voltage rises: After the voltage rises UV_{BSR} , the circuits start to operate when next input is applied.
 b2: Normal operation: IGBT ON and carrying current.
 b3: Under voltage detection (UV_{BSD}).
 b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
 b5: Under-voltage reset (UV_{BSR}).
 b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 10. Under-Voltage Protection (High-Side)

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(with the external sense resistance and RC filter connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short-circuit current detection (SC trigger).

c3: All low-side IGBT's gate are hard interrupted.

c4: All low-side IGBTs turn OFF.

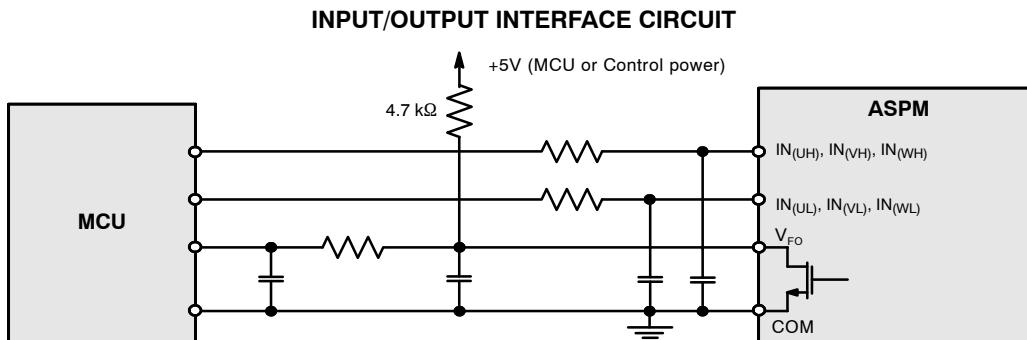
c5: Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .

c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7: Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.

c8: Normal operation: IGBT ON and carrying current.

Figure 11. Short-Circuit Current Protection (Low-Side Operation Only)

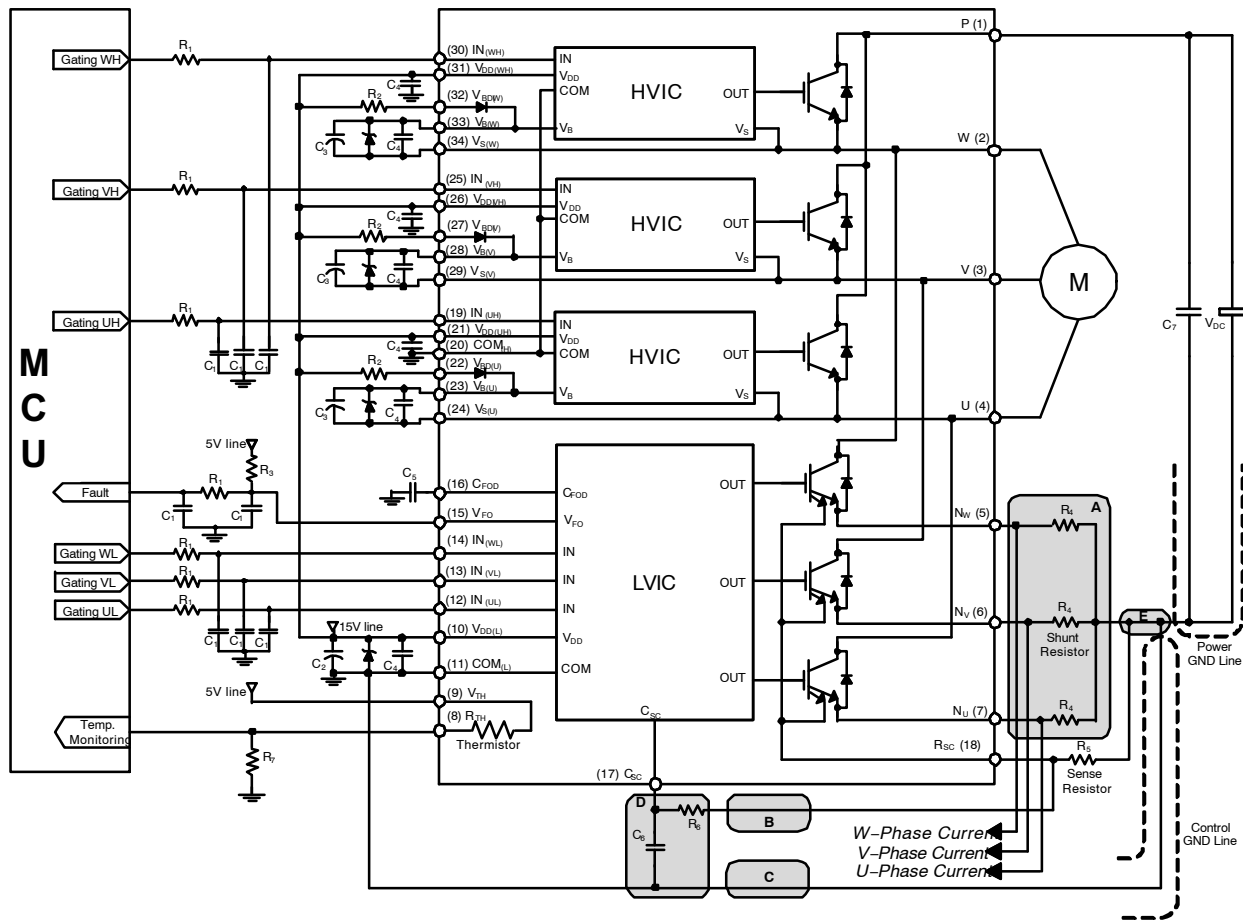


NOTE:

14. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 2 product integrates 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 12. Recommended CPU I/O Interface Circuit

NFVA23512NP2T



NOTES:

15. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 – 3 cm)
16. V_{FO} output is open-drain type. The signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 2 mA. Refer to Figure 13.
17. Fault out pulse width can be adjust by capacitor C_5 connected to the C_{FOD} terminal.
18. Input signal is active-HIGH type. There is a 5 k Ω resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R_1C_1 time constant should be selected in the range 50–150 ns. (Recommended $R_1 = 100 \Omega$, $C_1 = 1$ nF)
19. Each wiring pattern inductance of A point should be minimized (Recommended less than 10 nH). Use the shunt resistor R_4 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R_4 as close as possible.
20. To insert the shunt resistor to measure each phase current at N_U , N_V , N_W terminal, it makes to change the trip level I_{SC} about the short-circuit current.
21. To prevent errors of the protection function, the wiring of B, C and D point should be as short as possible. The wiring of B between C_{SC} filter and R_{SC} terminal should be divided at the point that is close to the terminal of sense resistor R_5 .
22. For stable protection function, use the sense resistor R_5 with resistance variation within 1% and low inductance value.
23. In the short-circuit protection circuit, please select the R_6C_6 time constant in the range 1.0–1.5 μ s. R_6 should be selected with minimum of 10 times larger resistance than sense resistor R_5 . Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the R_6C_6 time constant.
24. Each capacitor should be mounted as close to the pins of the ASPM34 product as possible.
25. To prevent surge destruction, the wiring between the smoothing capacitor C_7 and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor between the P & GND pins is recommended.
26. Relays are used at almost every systems of electrical equipment at industrial application. In these cases, there should be sufficient distance between the MCU and the relays.
27. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended Zener diode is 22 V/1 W, which has the lower Zener impedance characteristic than about 15 Ω).
28. C_2 of around seven times larger than bootstrap capacitor C_3 is recommended.
29. Choose the electrolytic capacitor with good temperature characteristic in C_3 . Choose 0.1–0.2 μ F R-category ceramic capacitors with good temperature and frequency characteristics in C_4 .

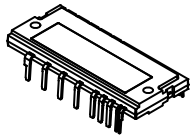
Figure 13. Typical Application Circuit

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

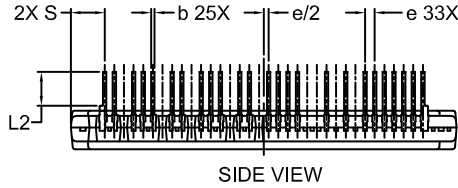


DIP34 80x33, AUTOMOTIVE MODULE

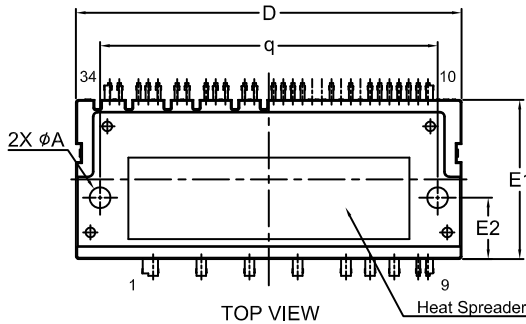
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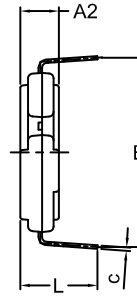
DATE 19 OCT 2018



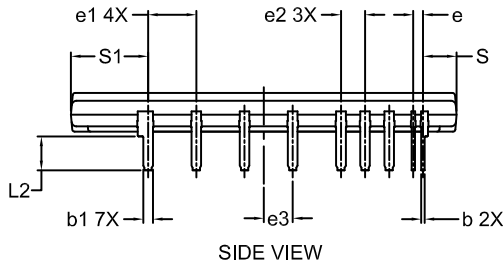
SIDE VIEW



TOP VIEW



END VIEW



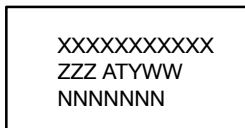
SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER, ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A2 | 7.90 | 8.00 | 8.10 |
| b | 0.60 | 0.70 | 0.80 |
| b1 | 1.90 | 2.00 | 2.10 |
| c | 0.65 | 0.70 | 0.80 |
| D | 79.70 | 80.00 | 80.30 |
| E | 38.76 | 39.26 | 39.76 |
| E1 | 32.70 | 33.00 | 33.30 |
| E2 | 12.50 | 12.70 | 12.90 |
| e | 1.70 | 2.00 | 2.30 |
| e1 | 9.70 | 10.00 | 10.30 |
| e2 | 4.70 | 5.00 | 5.30 |
| e3 | 5.70 | 6.00 | 6.30 |
| L | 15.50 | 16.00 | 16.50 |
| L2 | 6.70 | 7.00 | 7.30 |
| q | 69.75 | 70.00 | 70.25 |
| S | 7.00 REF | | |
| S1 | 16.00 REF | | |
| φA | 4.10 | 4.30 | 4.50 |

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 ZZZ = Lot ID
 AT = Assembly & Test Location
 Y = Year
 W = Work Week
 NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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| DESCRIPTION: | DIP34 80x33, AUTOMOTIVE MODULE | PAGE 1 OF 1 |

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