

# NGD18N45CLB

## Ignition IGBT 18 Amps, 450 Volts

### N-Channel DPAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

#### Features

- Ideal for Coil-on-Plug Applications
- DPAK Package Offers Smaller Footprint for Increased Board Space
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Low Threshold Voltage Interfaces Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Emitter Ballasting for Short-Circuit Capability
- This is a Pb-Free Device

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CES}$	500	$V_{DC}$
Collector-Gate Voltage	$V_{CER}$	500	$V_{DC}$
Gate-Emitter Voltage	$V_{GE}$	18	$V_{DC}$
Collector Current-Continuous @ $T_C = 25^\circ\text{C}$ - Pulsed	$I_C$	18 50	$A_{DC}$ $A_{AC}$
ESD (Human Body Model) $R = 1500 \Omega$ , $C = 100 \text{ pF}$	ESD	8.0	kV
ESD (Machine Model) $R = 0 \Omega$ , $C = 200 \text{ pF}$	ESD	400	V
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	115 0.77	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

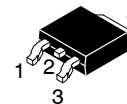
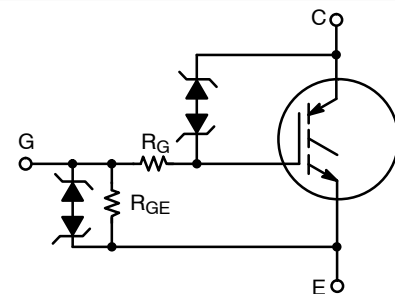


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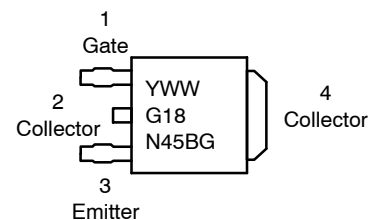
**18 AMPS  
450 VOLTS**

$V_{CE(on)} \leq 2.1 \text{ V @}$   
 $I_C = 10 \text{ A}, V_{GE} \geq 4.5 \text{ V}$



**DPAK  
CASE 369C  
STYLE 7**

#### MARKING DIAGRAM



G18N45B = Device Code  
Y = Year  
WW = Work Week  
G = Pb-Free Device

#### ORDERING INFORMATION

Device	Package	Shipping†
NGD18N45CLBT4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



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## ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b> (Note 2)							
Gate Threshold Voltage	$V_{GE(th)}$	$I_C = 1.0 \text{ mA}$ , $V_{GE} = V_{CE}$	$T_J = 25^\circ\text{C}$	1.1	1.56	1.9	$V_{DC}$
			$T_J = 150^\circ\text{C}$	0.75	1.08	1.4	
			$T_J = -40^\circ\text{C}$	1.2	1.75	2.1	
Collector-to-Emitter On-Voltage	$V_{CE(on)}$	$I_C = 7 \text{ A}$ , $V_{GE} = 4.5 \text{ V}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	1.10	1.84	2.30	V
			$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	1.15	1.89	2.35	
			$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	1.20	1.93	2.50	
			$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	1.45	2.07	2.65	
			$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	1.50	2.13	2.80	
			$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	1.55	2.19	2.85	
			$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	-	0.65	1.00	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.5	-	mV/°C
Forward Transconductance	gfs	$V_{CE} = 5.0 \text{ V}$ , $I_C = 6.0 \text{ A}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	6.0	14	25	Mhos

## DYNAMIC CHARACTERISTICS (Note 2)

Input Capacitance	$C_{ISS}$	$V_{CC} = 25 \text{ V}$ , $V_{GE} = 0 \text{ V}$ $f = 1.0 \text{ MHz}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	400	780	1000	pF
Output Capacitance	$C_{OSS}$			50	72	100	
Transfer Capacitance	$C_{RSS}$			4.0	6	10	

## SWITCHING CHARACTERISTICS (Note 2)

Turn-Off Delay Time	$t_{d(off)}$	$V_{CC} = 300 \text{ V}$ , $V_{GE} = 5 \text{ V}$ $R_G = 1.0 \text{ k}\Omega$ , $R_L = 46 \Omega$	$T_J = 25^\circ\text{C}$	1.0	2.9	12	$\mu\text{Sec}$
Fall Time	$t_f$	$V_{CC} = 300 \text{ V}$ , $V_{GE} = 5 \text{ V}$ $R_G = 1.0 \text{ k}\Omega$ , $R_L = 46 \Omega$	$T_J = 25^\circ\text{C}$	1.0	2.5	7.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{CC} = 14 \text{ V}$ , $V_{GE} = 5 \text{ V}$ $R_G = 1.0 \text{ k}\Omega$ , $R_L = 1 \Omega$	$T_J = 25^\circ\text{C}$	0.1	0.42	1.4	$\mu\text{Sec}$
Rise Time	$t_r$	$V_{CC} = 14 \text{ V}$ , $V_{GE} = 5 \text{ V}$ $R_G = 1.0 \text{ k}\Omega$ , $R_L = 1 \Omega$	$T_J = 25^\circ\text{C}$	1.0	2.5	9.0	

2. Electrical Characteristics at temperature other than 25°C, Dynamic and Switching characteristics are not subject to production testing.

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## TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

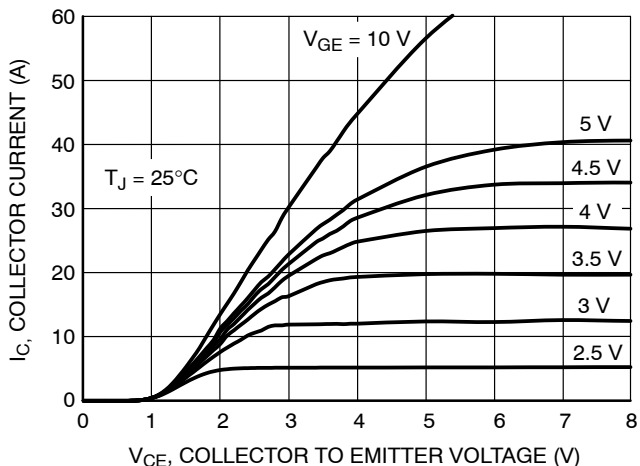


Figure 1. Output Characteristics

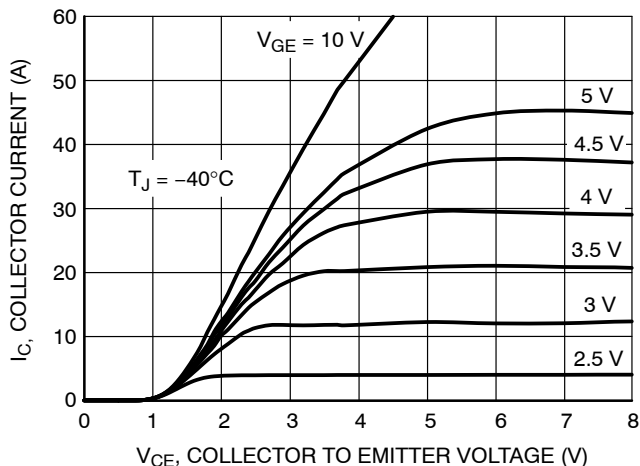


Figure 2. Output Characteristics

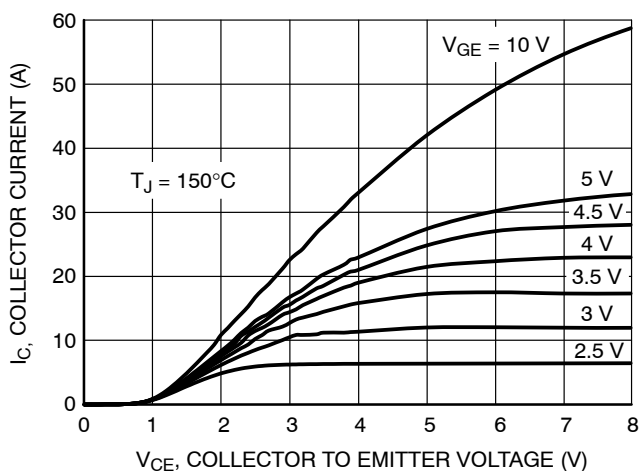


Figure 3. Output Characteristics

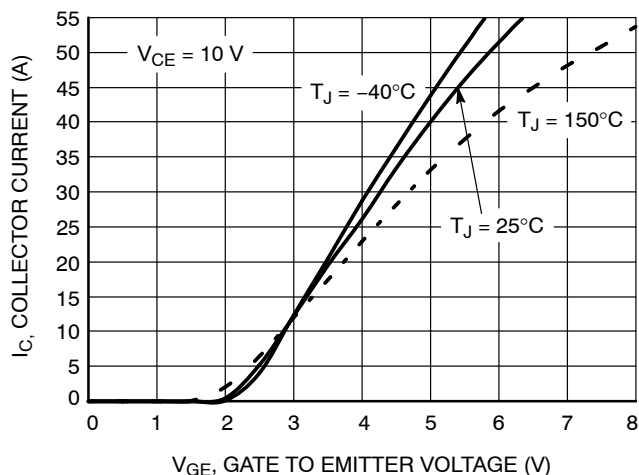


Figure 4. Transfer Characteristics

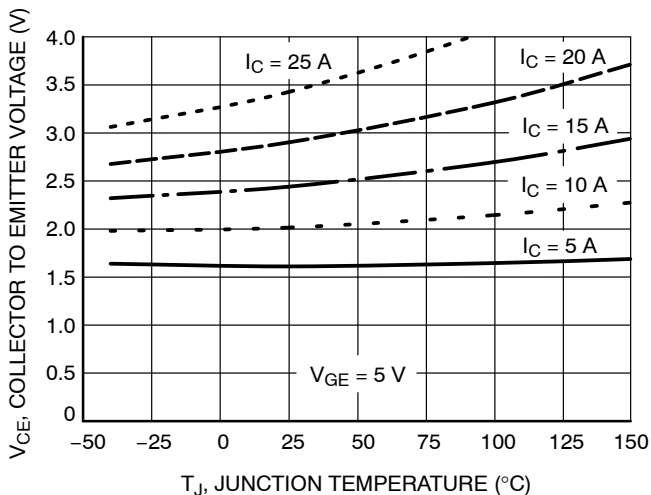


Figure 5. Collector-to-Emitter Saturation Voltage vs. Junction Temperature

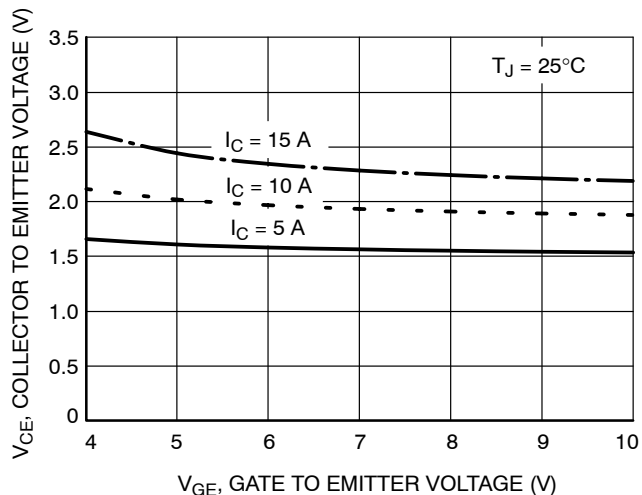
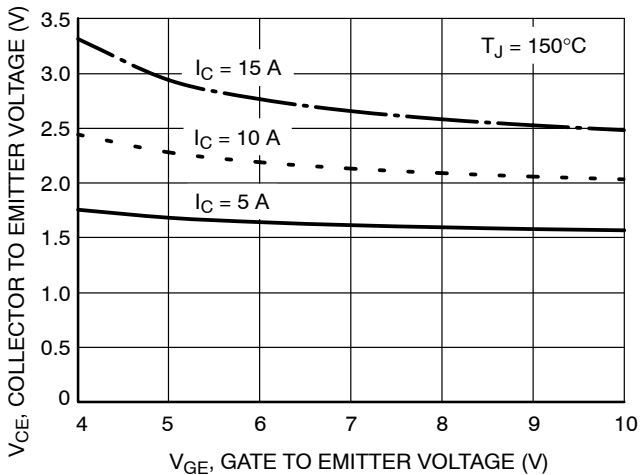
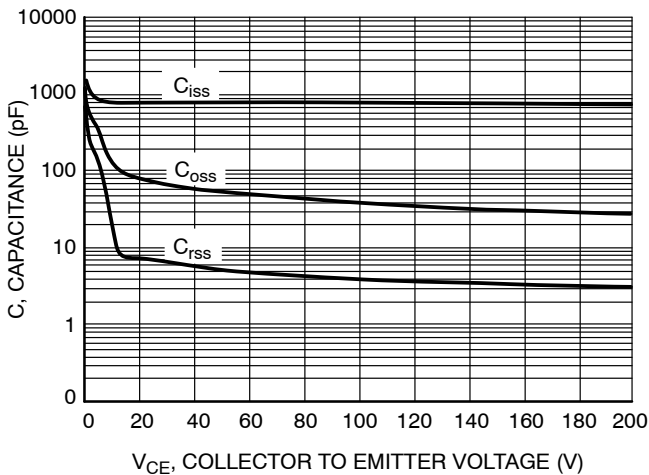


Figure 6. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

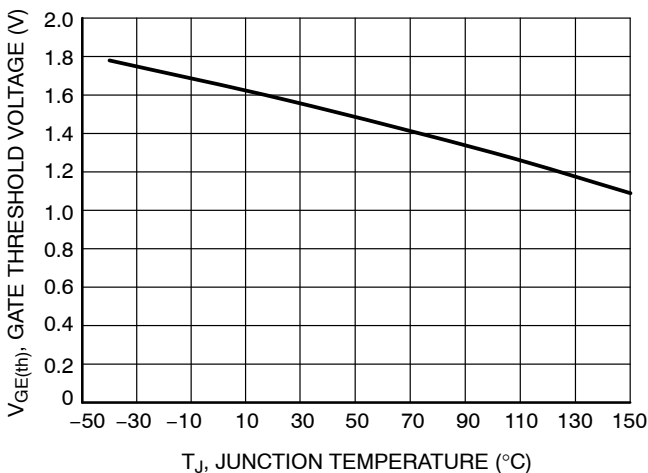
# NGD18N45CLB



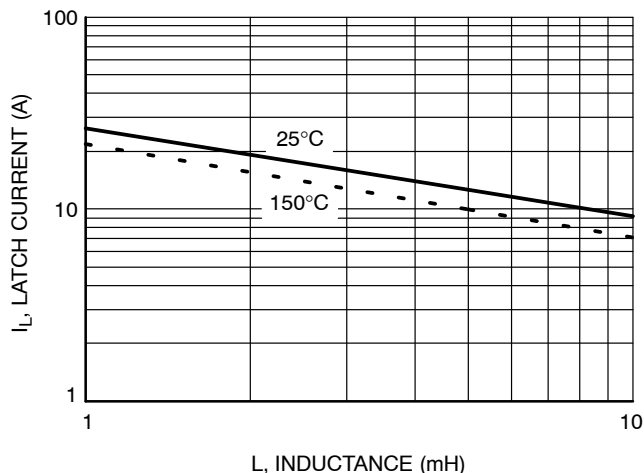
**Figure 7. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage**



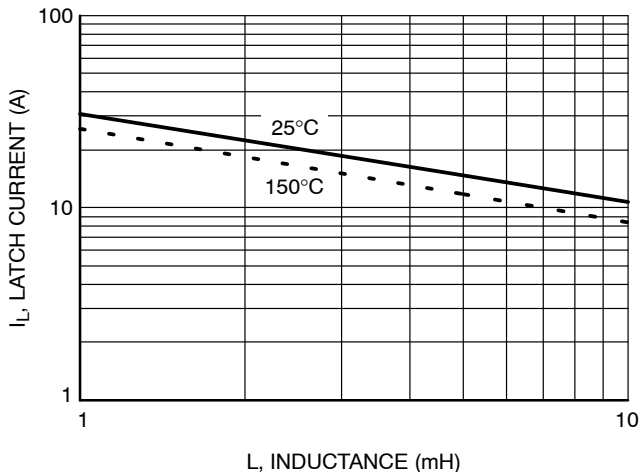
**Figure 8. Capacitance Variation**



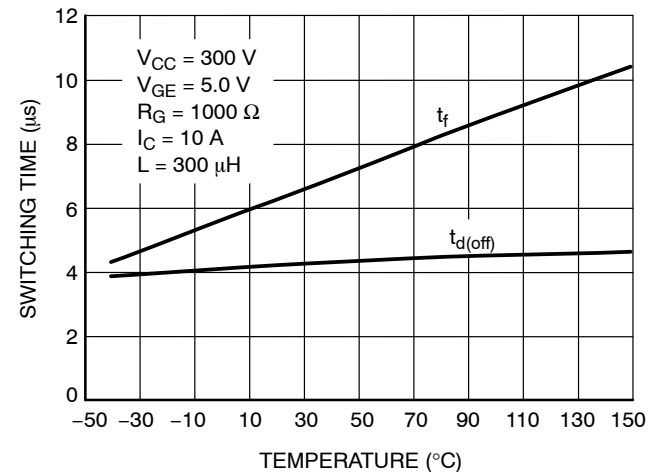
**Figure 9. Gate Threshold Voltage vs. Junction Temperature**



**Figure 10. Minimum Open Secondary Latch Current vs. Inductance**

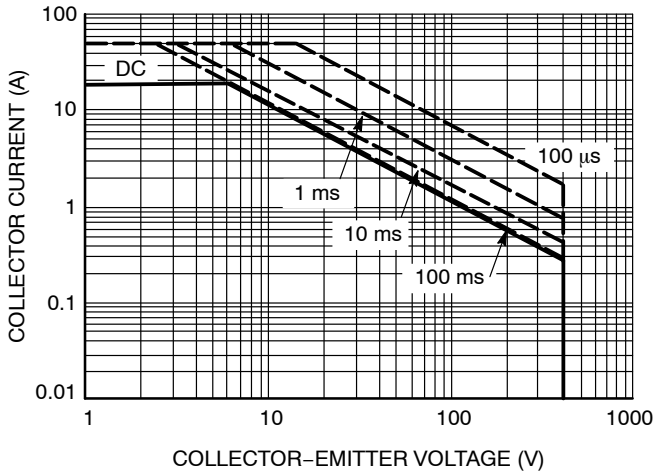


**Figure 11. Typical Open Secondary Latch Current vs. Inductance**

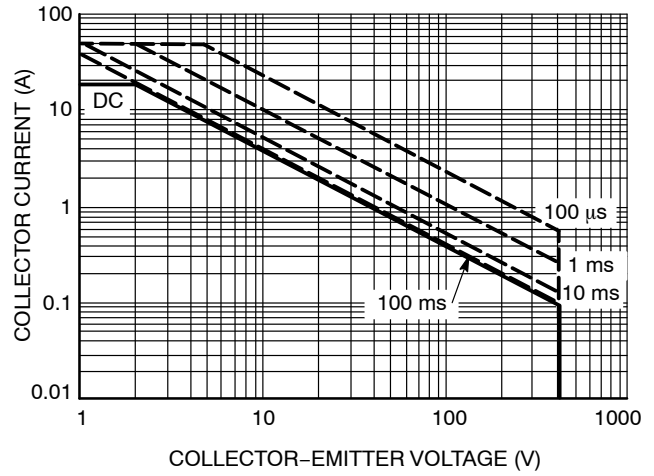


**Figure 12. Inductive Switching Fall Time vs. Temperature**

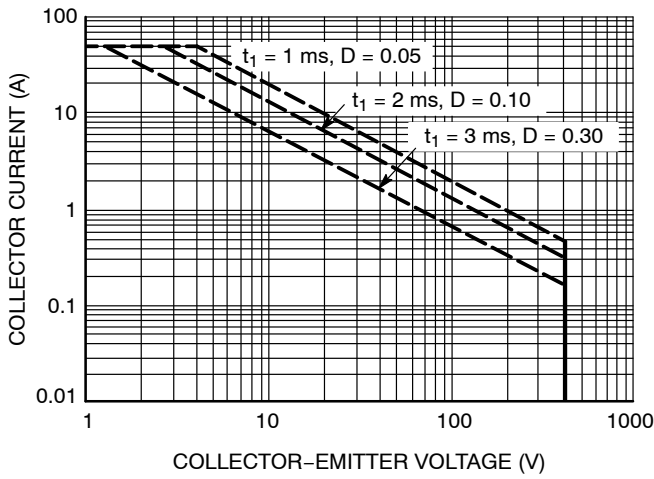
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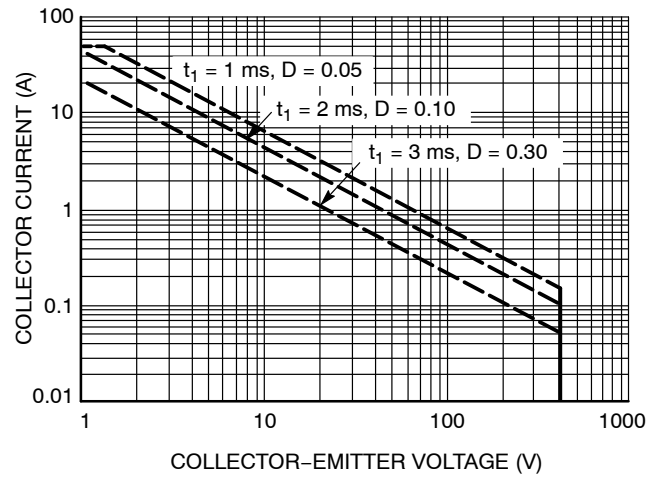
**Figure 13. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at  $T_A = 25^\circ\text{C}$ )**



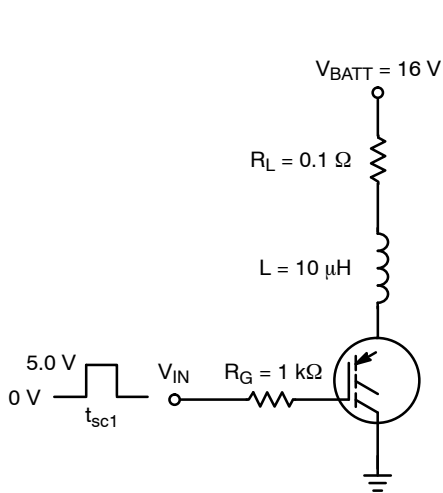
**Figure 14. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at  $T_A = 125^\circ\text{C}$ )**



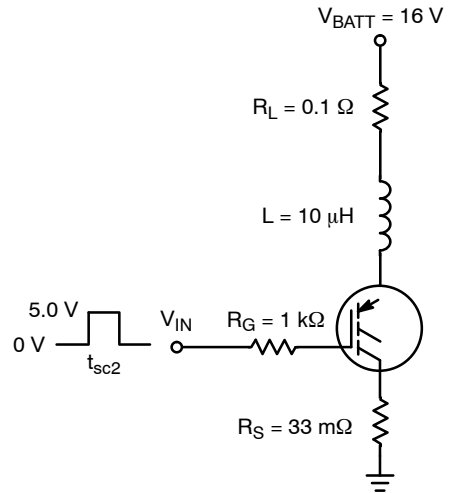
**Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at  $T_C = 25^\circ\text{C}$ )**



**Figure 16. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at  $T_C = 125^\circ\text{C}$ )**

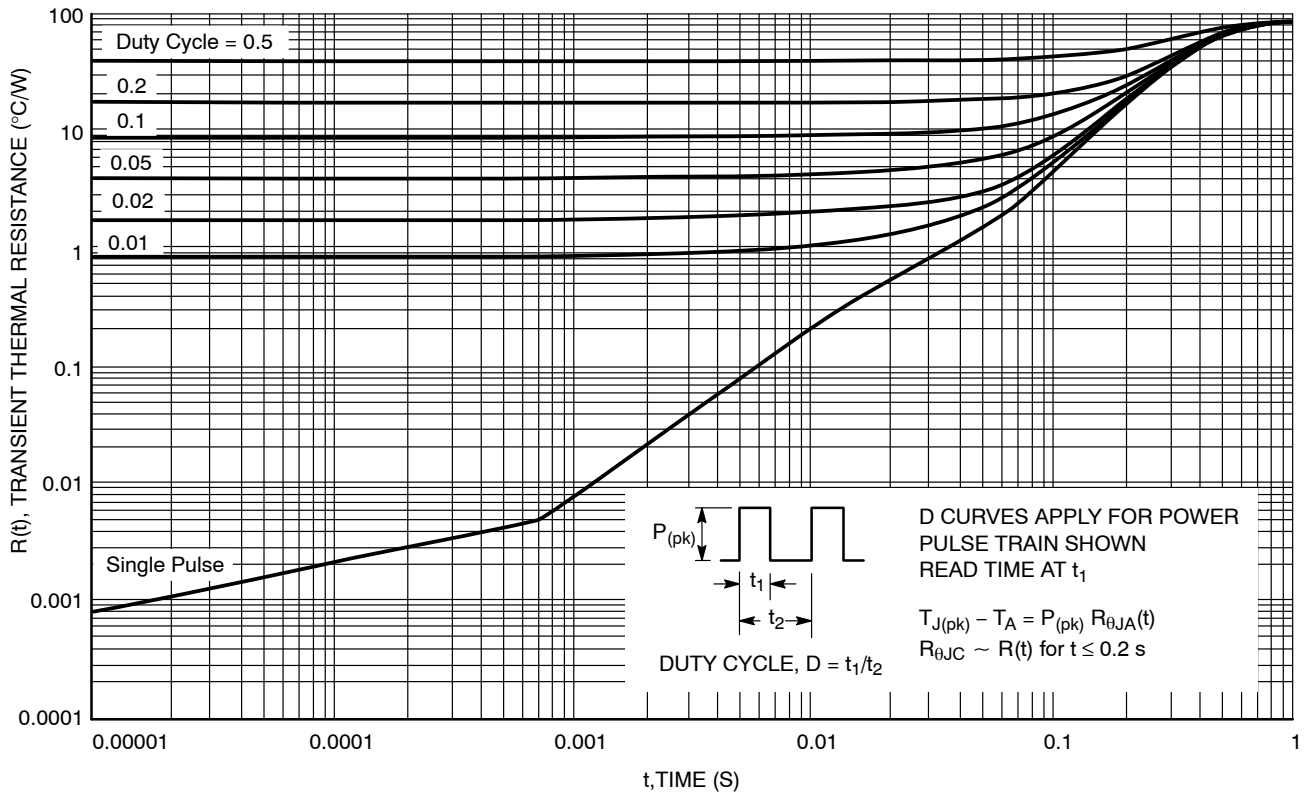


**Figure 17. Circuit Configuration for Short Circuit Test #1**



**Figure 18. Circuit Configuration for Short Circuit Test #2**

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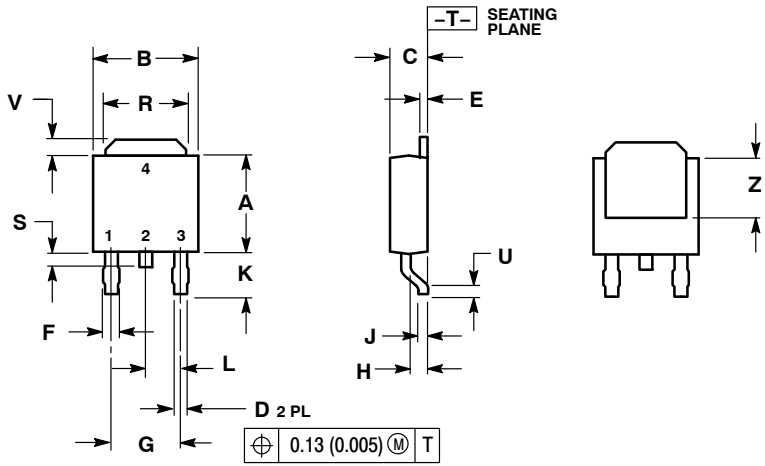


**Figure 19. Transient Thermal Resistance  
(Non-normalized Junction-to-Ambient mounted on minimum pad area)**

# NGD18N45CLB

## PACKAGE DIMENSIONS

### DPAK CASE 369C ISSUE C



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 7:  
 PIN 1. GATE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

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