NGD31251

28 V, 5 A dual channel non-isolation gate driver

Rev. 1.2 — 22 May 2025 Product data sheet

1. General description

NGD31251 is a high-frequency, dual channel, non-isolation MOSFET gate driver for high power automotive application.

NGD31251 has typical 5 A sink and 5 A source drive current and it can handle -10 V on its input pins, which improves robustness in systems with moderate ground bouncing. The inputs are independent of supply voltage and can be connected to most controller outputs.

NGD31251 has 11 ns rising and 13 ns falling propagation delay which allows the systems operating at high frequency with less delay matching variations. These delays are very suited for applications requiring dual-gate drivers with critical timing, such as synchronous rectifiers. When connecting two channels in parallel to increase current-drive capability, delay matching between 2 channels (2 ns) is used to avoid shoot through current without adding external series resistor.

2. Features and benefits

- Absolute maximum VDD pin voltage: 28 V
- Typical 5 A sink and 5 A source output currents
- Input pins capable of withstanding up to -10 V and are independent of power supply
- Operation switching frequency up to 1 MHz
- VDD UVLO point: 4.2 V
- Symmetrical undervoltage lockout for both channels
- -40 °C to 140 °C junction temperature range
- SOT96-2 package

3. Applications

- Power supplies for telecom, datacom and industrial inverters
- Power factor correction (PFC) circuits
- Solar power supplies
- Residential EV chargers
- Motor drives
- Pulse transformer drivers

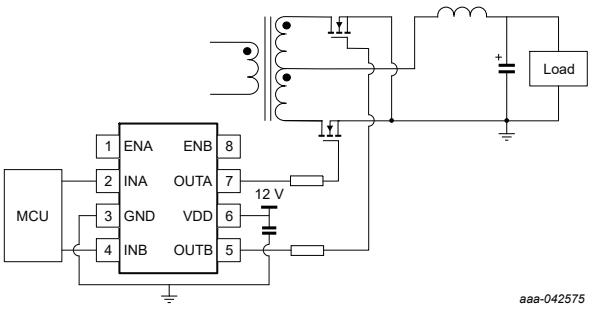


Fig. 1. Application for synchronous rectification

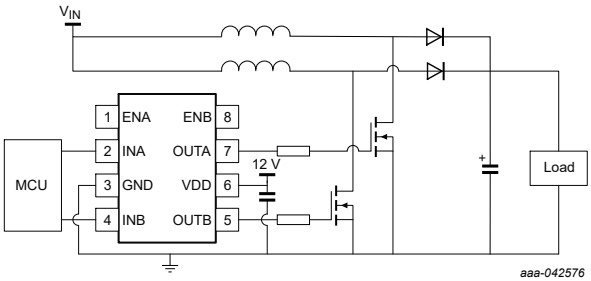


Fig. 2. Application for interleaved PFC

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range (T_j)	Name	Description	Version
NGD31251D	-40 °C to 140 °C	SO8	Plastic, small outline package; 8 leads; 1.27mm pitch; 4.9 mm x 3.9 mm x 1.75mm body	SOT96-2

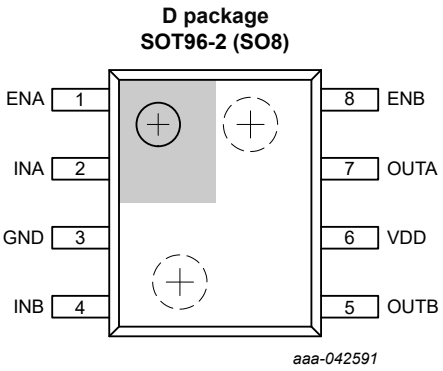
5. Marking

Table 2. Marking codes

Type number	Marking code
NGD31251D	N31251

6. Pinning information

6.1. Pinning configuration



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
ENA	1	I	A channel enables control input
INA	2	I	A channel non-inverting PWM input
GND	3	G	driver ground
INB	4	I	A channel non-inverting PWM input
OUTB	5	O	B channel output of driver
VDD	6	P	positive gate drive supply
OUTA	7	O	A channel output of driver
ENB	8	I	B channel enables control input

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	positive gate driver supply		-0.3	28	V
V_{OUT}	DC	pins OUTA and OUTB	GND - 0.3	VDD + 0.3	V
	transient, less than 10 ns [1]		GND - 5.0	VDD + 0.3	V
V_I	input voltage	pins INA, INB, ENA and ENB	-10	28	V
T_j	junction temperature		-40	150	°C
T_{stg}	storage temperature		-65	150	°C

[1] Values are verified by characterization on bench.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	positive gate drive supply		4.5	24	V
V_I	input voltage	pins INA, INB, ENA and ENB	-5	24	V
T_j	junction temperature		-40	140	°C
T_{amb}	ambient temperature		-40	125	°C

9. ESD ratings

Table 6. ESD ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 3A [1]	-4000	-	4000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3 [2]	-1000	-	1000	V

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

10. Thermal information

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	SOT96-2	Unit
$R_{\Theta jA}$	thermal resistance from junction to ambient [1]	in free air; JEDEC test board	129.33	°C/W
$R_{\Theta jC(top)}$	thermal resistance from junction to case (top)	in free air; JEDEC test board	72.8	°C/W
$R_{\Theta jB}$	thermal resistance from junction to board	in free air; JEDEC test board	88.9	°C/W

[1] Measured in still air-free convection condition (conforms to EIA/JESD51-2) on high effective thermal conductivity JESD51-9 with a test board PCB.

11. Electrical characteristics

Table 8. Electrical characteristics

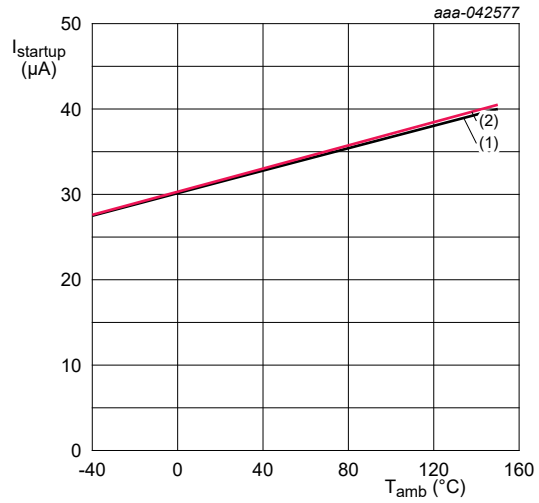
VDD = 12 V; 1 µF capacitor from VDD to GND; C_{Load} = 0 pF; unless otherwise noted voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_j = -40 °C to 140 °C			Unit
			Min	Typ [1]	Max	
Supply current						
I_{VDDQ1}	quiescent current 1 on pin VDD	VDD = 3.4 V; Input = high	-	32	50	µA
I_{VDDQ2}	quiescent current 2 on pin VDD	VDD = 3.4 V; Input = low	-	32	50	µA
VDD UVLO thresholds						
V_{DD_UVR}	VDD UVLO rising threshold		3.8	4.2	4.6	V
V_{DD_UVF}	VDD UVLO failing threshold		3.6	3.9	4.2	V
V_{DD_UVHYS}	VDD UVLO hysteresis		-	0.3	-	V
Input function						
V_{INH}	input high threshold voltage	Output high for IN and EN pin	1.8	2.1	2.4	V
V_{INL}	input low threshold voltage	Output low for IN and EN pin	1.0	1.2	1.4	V
V_{IN_HYS}	input threshold hysteresis		-	0.9	-	V
R_{IN_DOWN}	input pulls down resistance		-	180	-	kΩ
R_{EN_UP}	input pulls up resistance		-	180	-	kΩ
Gate driver function						
I_{SINK}	output peak sink current [2]	C_{VDD} = 10 µF; C_L = 0.1 µF; f = 1 kHz	-	5	-	A
I_{SOURCE}	output peak source current [2]	C_{VDD} = 10 µF; C_L = 0.1 µF; f = 1 kHz	-	-5	-	A
R_{OH}	pull up resistance	I_{OUT} = -10 mA	-	1	1.9	Ω
R_{OL}	pull down resistance	I_{OUT} = 10 mA	-	0.6	1.1	Ω
V_{OH}	high level output voltage	I_{OUT} = -10 mA	-	10	19	mV
V_{OL}	low level output voltage	I_{OUT} = 10 mA	-	6	11	mV
Switching characteristics						
t_R	output rise time	C_L = 1.8 nF	-	8	12	ns
t_F	output fall time	C_L = 1.8 nF	-	7	11	ns
$t_{PD\_IN\_R}$	INA/B to output turn-on propagation delay	5 V input pulse; C_L = 1.8 nF	-	11	18	ns
$t_{PD\_IN\_F}$	INA/B to output turn-off propagation delay	5 V input pulse; C_L = 1.8 nF	-	13	20	ns
$t_{PD\_EN\_R}$	ENA/B to output turn-on propagation delay	5 V input pulse; C_L = 1.8 nF	-	11	18	ns
$t_{PD\_EN\_F}$	ENA/B to output turn-off propagation delay	5 V input pulse; C_L = 1.8 nF	-	13	20	ns
t_M	delay matching between 2 channels		-	2	4	ns
t_{INMIN}	minimum input pulse width that passes to output		-	10	20	ns

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Values are verified by characterization on bench, not tested in production.

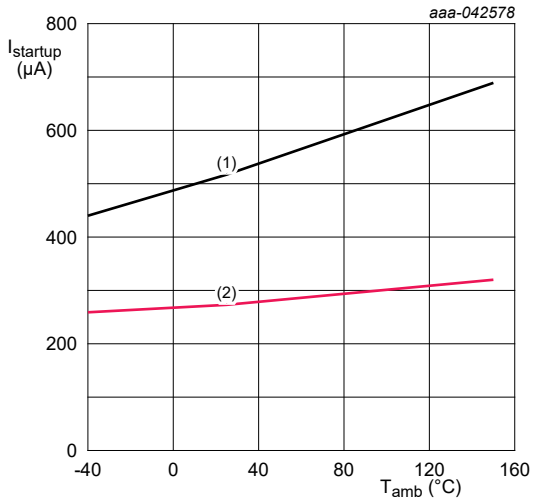
12. Typical characteristics

Unless otherwise specified, T_j = 25 °C, no load.



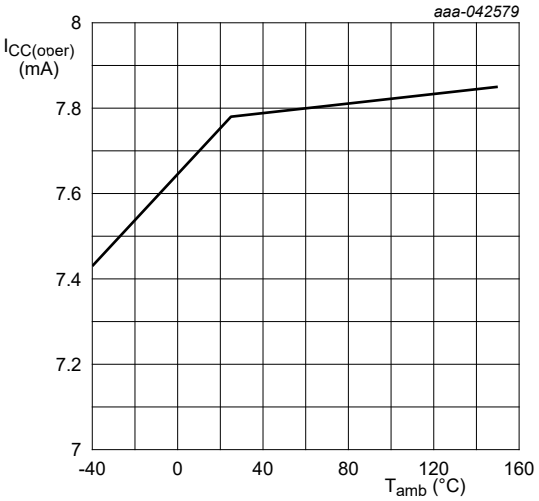
VDD = 3.4 V
(1) INx = 3.4 V
(2) INx = 0 V

Fig. 3. Start-up current



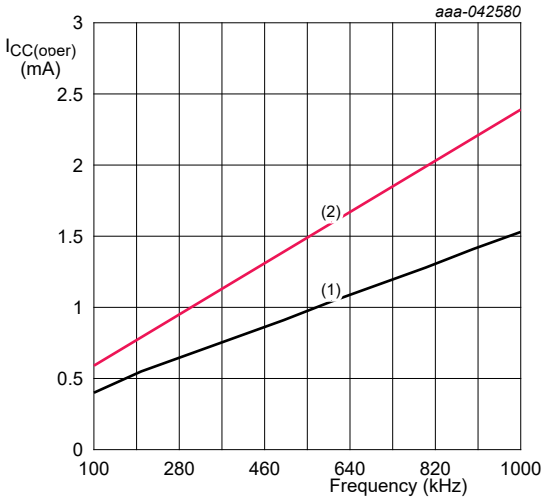
VDD = 12 V
(1) INx = High
(2) INx = Low

Fig. 4. State supply current



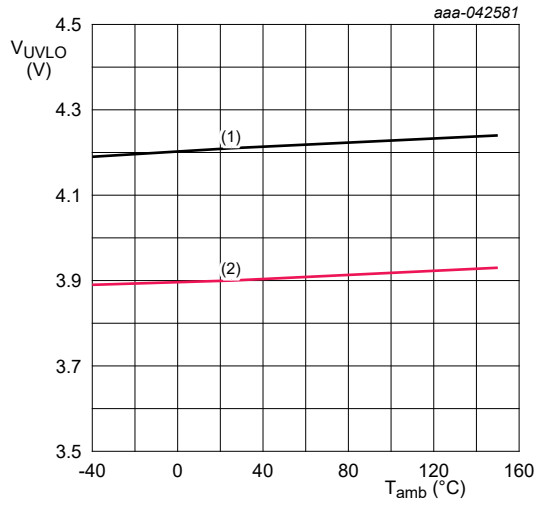
VDD = 12 V; C_{OUTA} = C_{OUTB} = 500 pF;
Frequency = 500 kHz

Fig. 5. Operation supply current (both outputs switching)



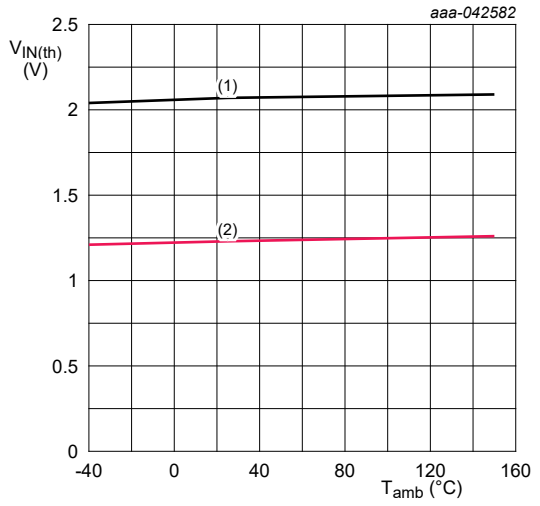
VDD = 4.5 V and 12 V
(1) VDD = 4.5 V
(2) VDD = 12 V

Fig. 6. Operation supply current (both outputs switching)



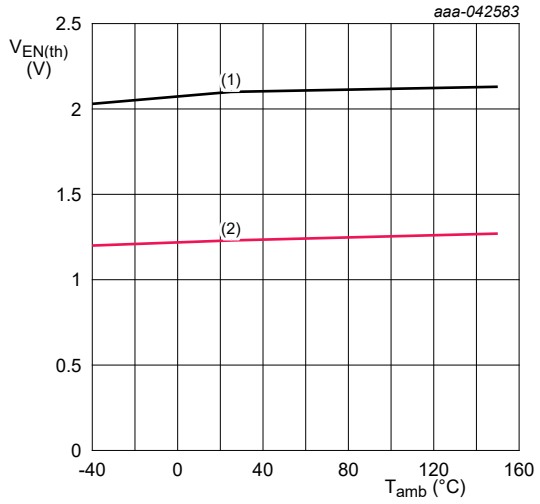
Input = High
(1) Rise
(2) Fall

Fig. 7. VDD UVLO threshold



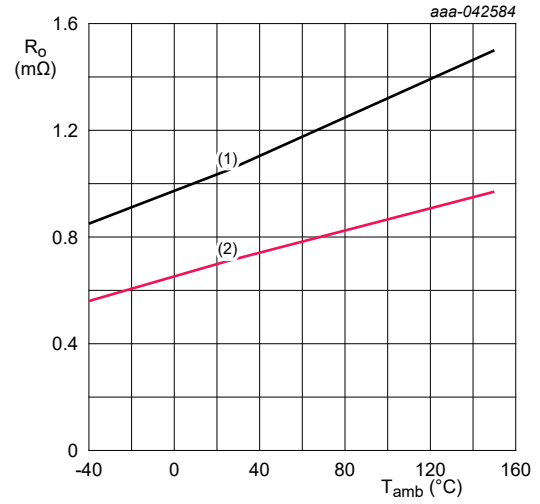
VDD = 12 V
(1) Rise
(2) Fall

Fig. 8. Input threshold



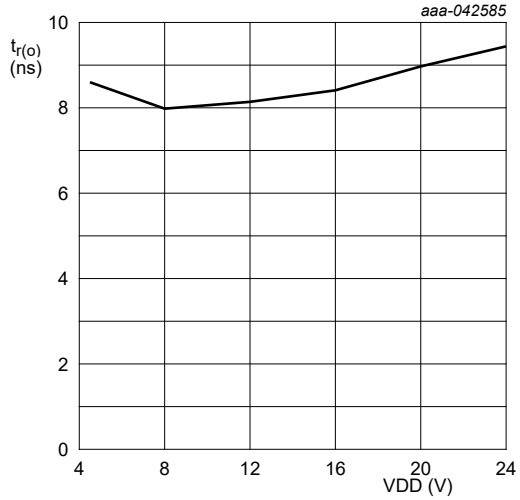
VDD = 12 V
(1) Rise
(2) Fall

Fig. 9. Enable threshold



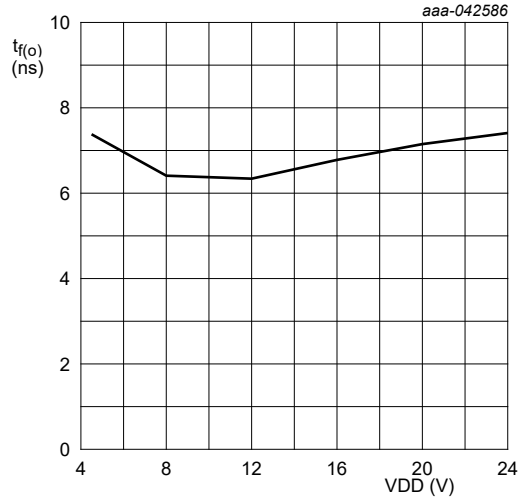
VDD = 12 V
(1) Pull-up
(2) Pull-down

Fig. 10. Output resistance



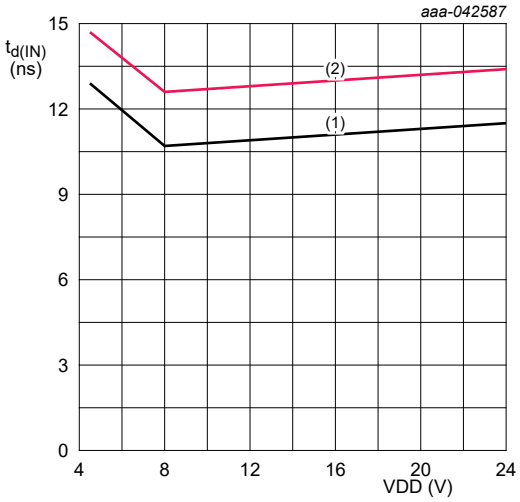
C_{OUTA} = C_{OUTB} = 1.8 pF
(1) Rise
(2) Fall

Fig. 11. Output rise time



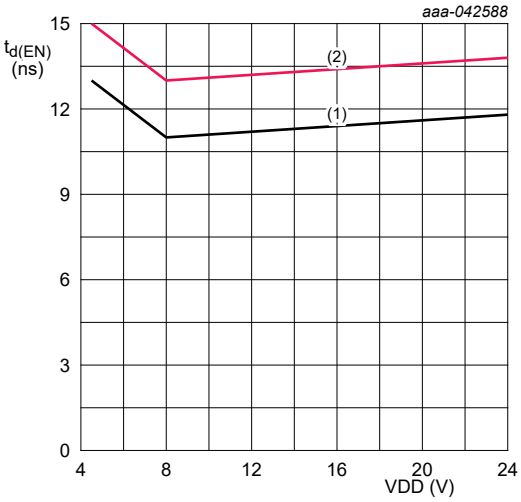
C_{OUTA} = C_{OUTB} = 1.8 pF
(1) Rise
(2) Fall

Fig. 12. Output fall time



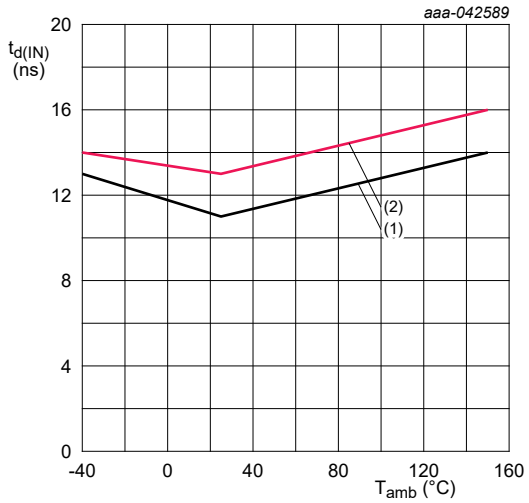
C_{OUTA} = C_{OUTB} = 1.8 pF
(1) Rise
(2) Fall

Fig. 13. Input to output propagation delay



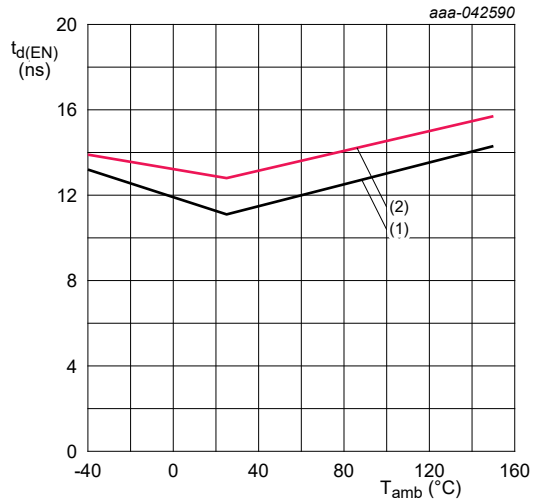
C_{OUTA} = C_{OUTB} = 1.8 pF
(1) Rise
(2) Fall

Fig. 14. Enable to output propagation delay



VDD = 12 V; C_{OUTA} = C_{OUTB} = 1.8 pF
(1) Rise
(2) Fall

Fig. 15. Input to output propagation delay



VDD = 12 V; C_{OUTA} = C_{OUTB} = 1.8 pF
(1) Rise
(2) Fall

Fig. 16. Enable to output propagation delay

13. Detailed description

13.1. Overview

NGD31251 is a dual channel, high-speed, non-isolation MOSFET and IGBT gate driver for high power application. The device supports up to 24 V wide supply voltage.

NGD31251 has a typical 5 A sink and 5 A source drive current, and it can handle -5 V on its input pins, which improves robustness in systems with moderate ground bouncing. The inputs are independent of supply voltage and can be connected to most controller outputs, even digital insulators.

13.2. Function block diagram

The NGD31251 function block diagram is shown in Fig. 17.

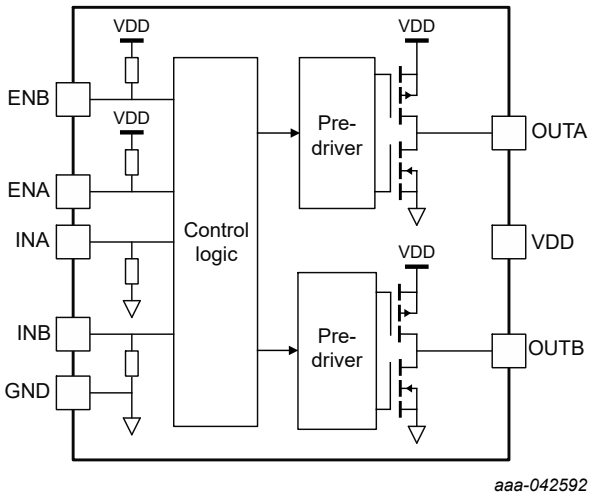


Fig. 17. Function block diagram

13.3. Function modes

NGD31251 operates in normal mode and UVLO mode. In normal mode, the output state is dependent on states of the input pins.

Table 9. Function modes

Input		Output
INx	**ENx**	**OUTx**
high	high	high
low	high	low
high	low	low
low	low	low
high	floating	high
low	floating	low
floating	high	low
floating	low	low

13.4. Power supply and VDD UVLO

NGD31251 operates with a supply voltage from 4.5 V to 24 V. This feature makes the driver capable of driving both Si MOSFET and IGBT. For the best performance, use a typical 0.1 µF decoupling cap as close as possible between VDD and GND pins of NGD31251. VDD bypass capacitor (1 µF to 10 µF) in parallel is also recommended to reduce noise ripple during switching.

The following figure shows the timing diagram illustrating the definition of VDD UVLO ON/OFF threshold.

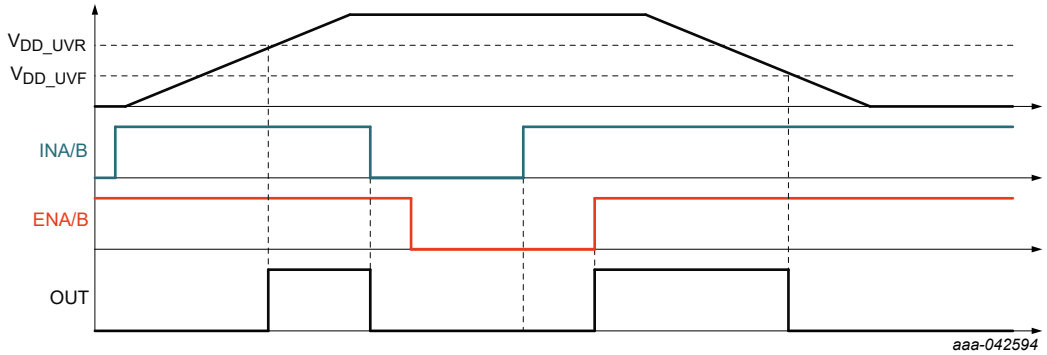


Fig. 18. NGD31251 VDD UVLO protection diagram

13.5. Input stage

The input pins of NGD31251 gate-driver device are based on a TTL and CMOS compatible input-threshold logic. That is independent of the VDD supply voltage. With typically high threshold = V_{INH} and typically low threshold = V_{INL}, the logic level thresholds are conveniently driven by PWM control signals derived from 3.3 V and 5 V digital power-controller devices.

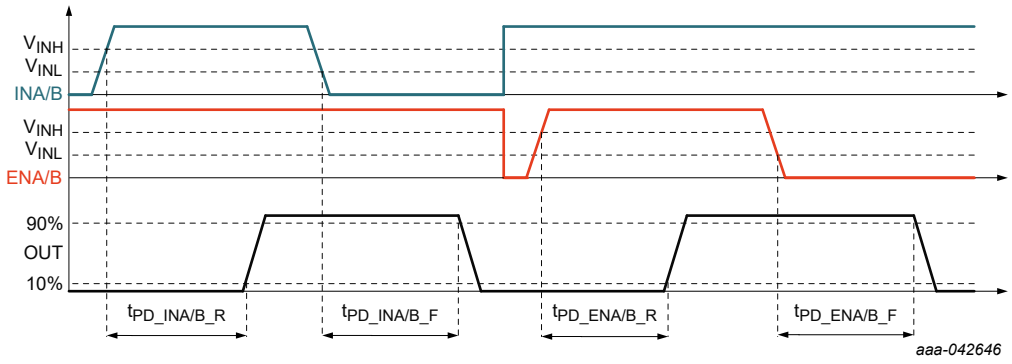


Fig. 19. NGD31251 input propagation delay

13.6. Driver stage

The device has ±5 A peak drive strength and is suitable for high power applications. The high drive strength can drive MOSFET, IGBT. The driver has rail-to-rail output by implementing a pull-up PMOS and a NMOS to pull-down. The output pull-up and pull-down resistance can be found in the Table 8.

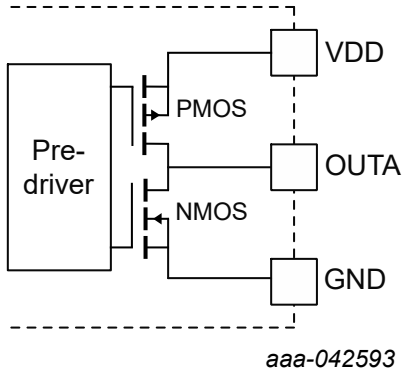


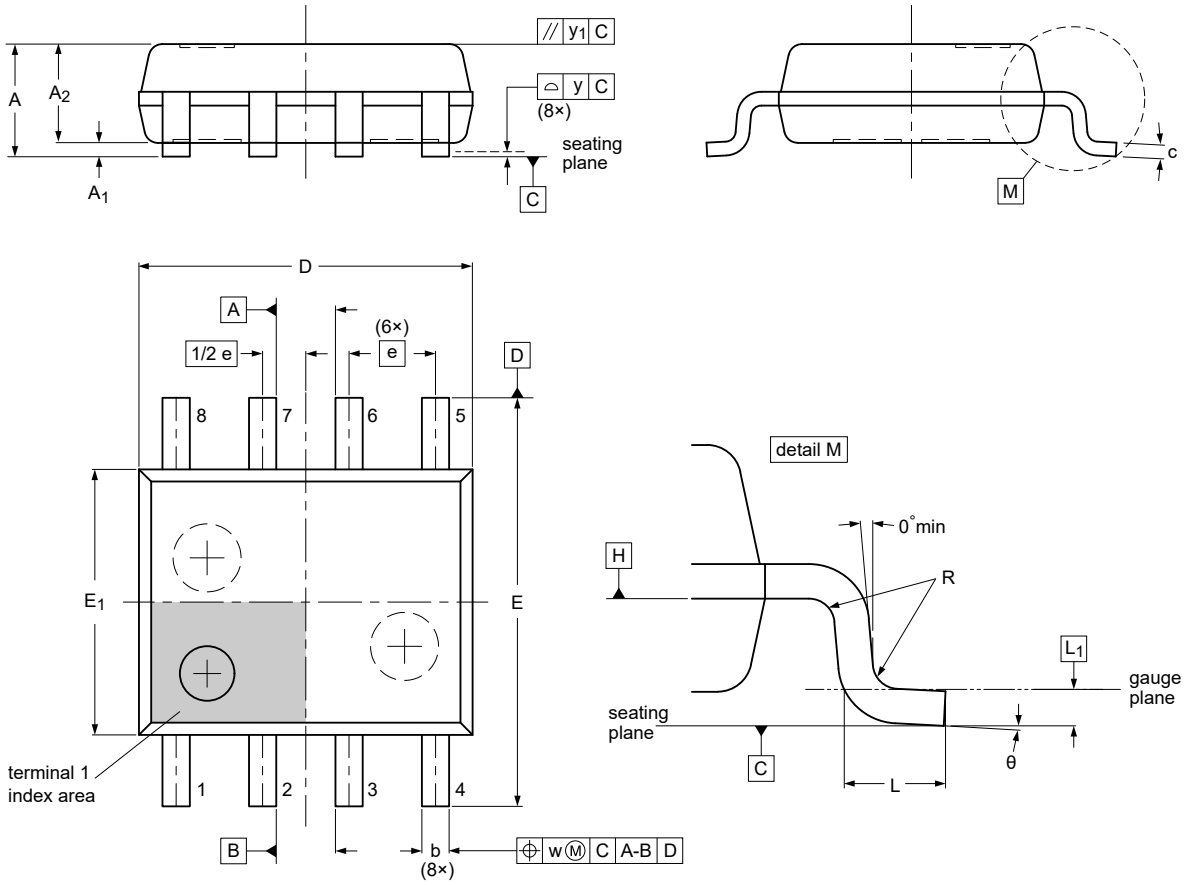
Fig. 20. Gate driver output stage

13.7. Output parallel capability

The NGD31251 features 2 ns (typical) delay matching between dual channels, which enables dual channel outputs to be paralleled when the driven power device required higher driving capability. For example, there are two or more power MOSFETs in parallel to support high current output capability. The parallel power MOSFETs are preferred to be driven by a common gate control signal. By using NGD31251, the OUTA and OUTB can be connected to provide the higher driving capability, so do the INA and INB.

14. Package outline

Plastic, small outline package; 8 leads; 1.27mm pitch; 4.9 mm x 3.9 mm x 1.75mm body **SOT96-2**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	L	L_1	R	w	y	y_1	θ
mm	max	1.75	0.25	1.55	0.51	0.25	5.10	6.20	4.00	1.27 BSC	1.27	0.25 BSC	0.15 REF	0.25	0.10	0.10	8°
	nom																
	min	1.45	0.10	1.35	0.33	0.17	4.70	5.80	3.80		0.40						0°

Note

1. Dimension D does not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burr shall not exceed 0.15 mm per end. Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side. D and E_1 dimensions are determined at datum H.
2. Datums A and B to be determined at datum H.

sot96-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT96-2						25-03-12

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
TTL	Transistor-Transistor Logic
UVLO	UnderVoltage LockOut

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NGD31251 v.1.2	20250522	Product data sheet	-	NGD31251 v.1.1
Modifications:	Section 3 updated.			
NGD31251 v.1.1	20250519	Product data sheet	-	NGD31251 v.1
Modifications:	The document status changed from Preliminary to Product.			
NGD31251 v.1	20250429	Preliminary data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents

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