NGD8209N

Ignition IGBT 12 A, 410 V
N−Channel DPAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over−Voltage clamped protection for use in inductive coil drivers applications. Primary uses include motorbike ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil−on−Plug Applications
- DPAK Package Offers Smaller Footprint and Increased Board Space
- Gate−Emitter ESD Protection
- Temperature Compensated Gate−Collector Voltage Clamp Limits Stress Applied to Load
- Low Saturation Voltage
- High Pulsed Current Capability
- These are Pb−Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

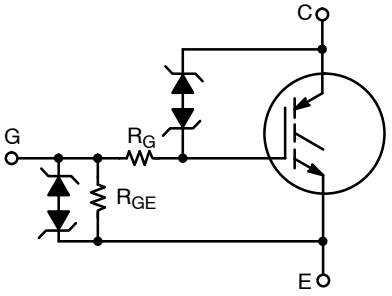
Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CES}	445	V_{DC}
Collector−Gate Voltage	V_{CER}	445	V_{DC}
Gate−Emitter Voltage	V_{GE}	15	V_{DC}
Collector Current−Continuous @ T_C = 25°C − Pulsed	I_C	12 30	A_{DC} A_{AC}
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	800	V
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	94 0.63	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +175	°C

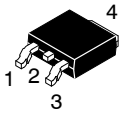
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ON Semiconductor®

http://onsemi.com

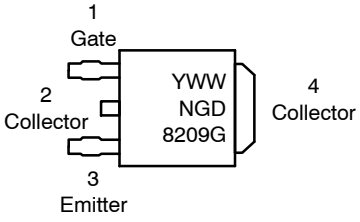
12 AMPS
410 VOLTS
$V_{CE(on)}$ ≤ 2.0 V @
I_C = 6.0 A, V_{GE} ≥ 4.0 V





DPAK
CASE 369C
STYLE 7

MARKING DIAGRAM



Y = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NGD8209NT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

UNCLAMPED COLLECTOR−TO−EMITTER AVALANCHE CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Single Pulse Collector−to−Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 7.4 A, L = 10 mH, Starting T_J = 25°C	E_{AS}	274	mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W
Thermal Resistance, Junction to Ambient (Note 1)	$R_{\theta JA}$	105	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector−Emitter Clamp Voltage	BV_{CES}	I_C = 2.0 mA	T_J = −40°C to 150°C	380	410	435	V_{DC}
		I_C = 10 mA	T_J = −40°C to 150°C	390	420	445	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 350 V, V_{GE} = 0 V	T_J = 25°C	–	1.0	25	μA_{DC}
			T_J = 150°C	–	9.0	50	
			T_J = −40°C	–	0.5	15	
Reverse Collector−Emitter Leakage Current	I_{ECS}	V_{CE} = −24 V	T_J = 25°C	–	0.5	1.0	mA
			T_J = 150°C	–	10	30	
			T_J = −40°C	–	0.05	0.5	
Reverse Collector−Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = −75 mA	T_J = 25°C	26	33	38	V_{DC}
			T_J = 150°C	29	36	41	
			T_J = −40°C	24	32	36	
Gate−Emitter Clamp Voltage	BV_{GES}	I_G = 5.0 mA	T_J = −40°C to 150°C	10	13	16	V_{DC}
Gate−Emitter Leakage Current	I_{GES}	V_{GE} = 10 V	T_J = −40°C to 150°C	380	635	1000	μA_{DC}
Gate Resistor	R_G	–	T_J = −40°C to 150°C	–	70	–	Ω
Gate Emitter Resistor	R_{GE}	–	T_J = −40°C to 150°C	10	16	26	kΩ
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GE(th)}$	I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = 25°C	1.0	1.42	2.0	V_{DC}
			T_J = 150°C	0.7	0.95	1.5	
			T_J = −40°C	1.1	1.62	2.2	
Threshold Temperature Coefficient (Negative)	–	–	–	–	3.5	–	mV/°C

2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
ON CHARACTERISTICS (continued) (Note 3)							
Collector−to−Emitter On−Voltage	$V_{CE(on)}$	I_C = 6.0 A, V_{GE} = 4.0 V	T_J = 25°C	0.8	1.45	2.0	V_{DC}
			T_J = 150°C	0.85	1.44	1.85	
			T_J = −40°C	1.0	1.5	1.95	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = 25°C	1.1	1.79	2.3	
			T_J = 150°C	1.2	1.9	2.2	
			T_J = −40°C	1.3	1.77	2.2	
Forward Transconductance	gfs	V_{CE} = 5.0 V, I_C = 6.0 A	T_J = −40°C to 150°C	5.0	14	30	Mhos

3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

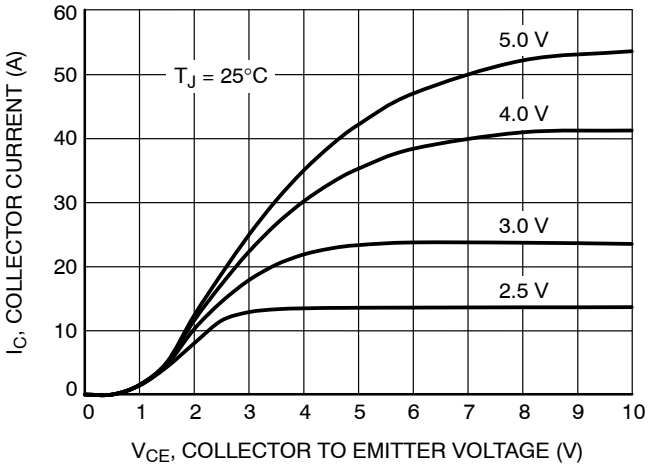


Figure 1. Output Characteristics

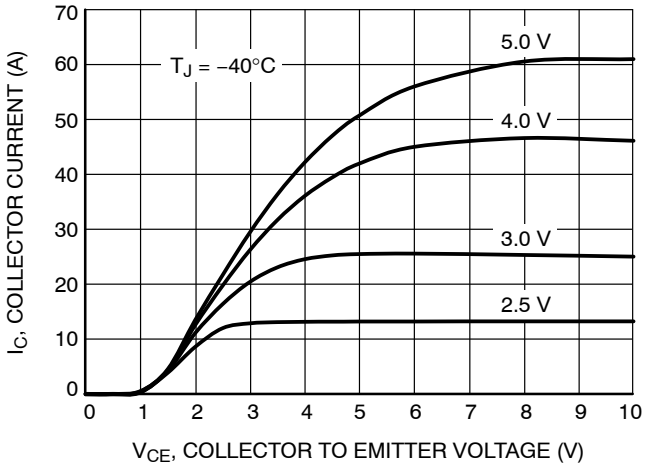


Figure 2. Output Characteristics

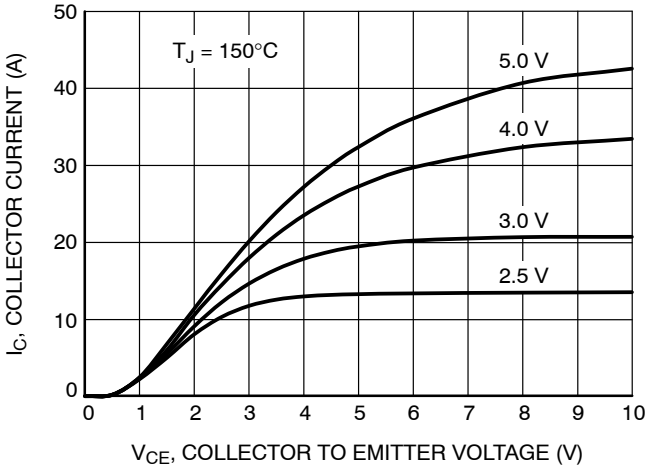


Figure 3. Output Characteristics

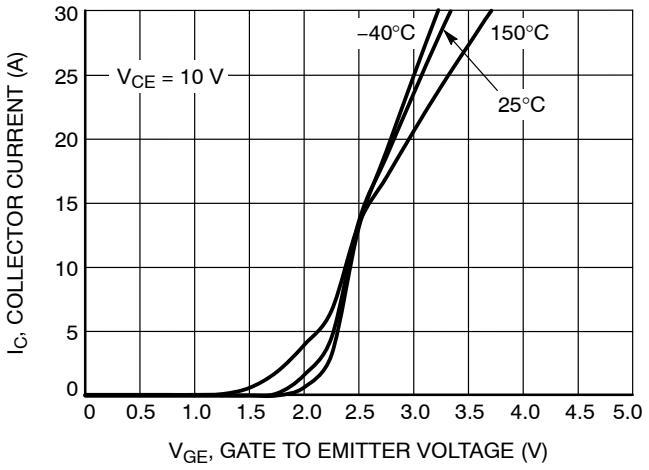


Figure 4. Transfer Characteristics

TYPICAL CHARACTERISTICS

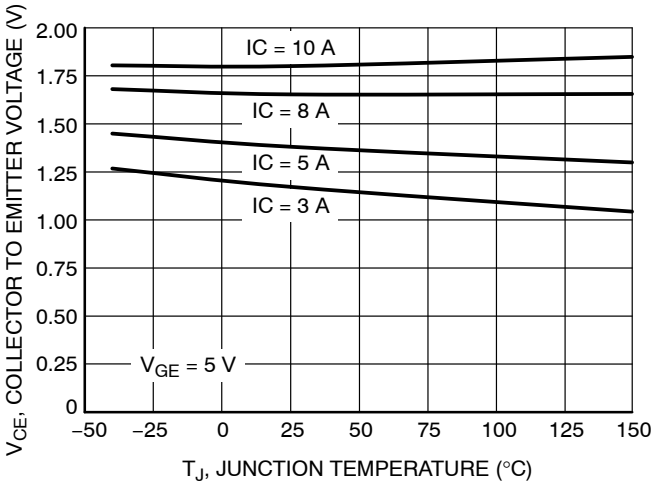


Figure 5. Collector−to−Emitter Saturation Voltage vs. Junction Temperature

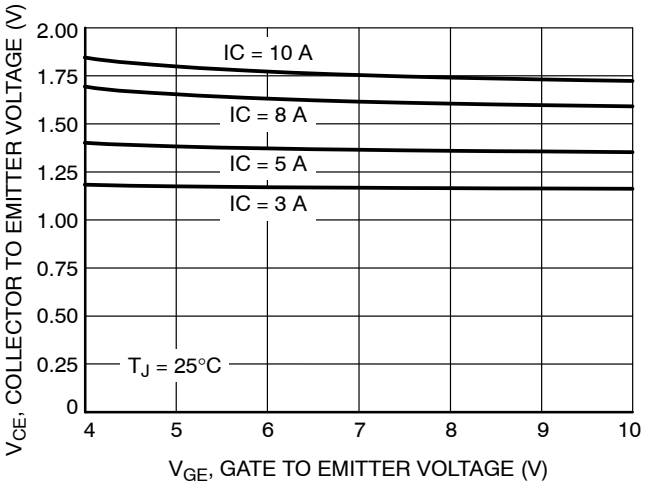


Figure 6. Collector−to−Emitter Voltage vs. Gate−to−Emitter Voltage

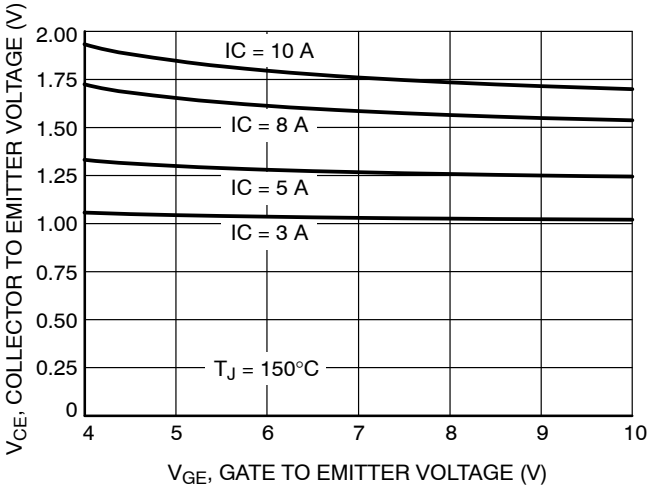


Figure 7. Collector−to−Emitter Voltage vs. Gate−to−Emitter Voltage

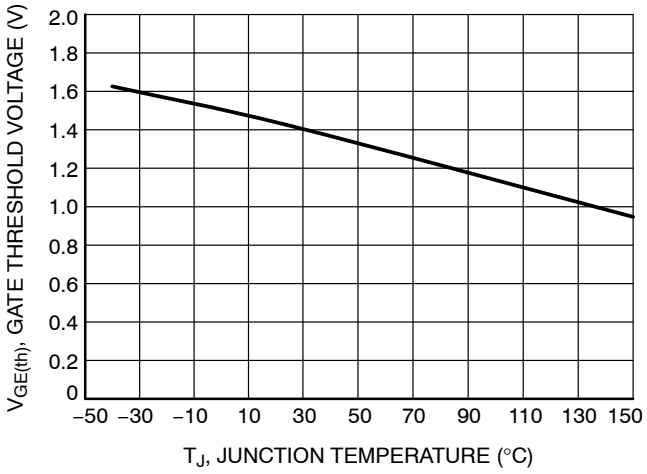
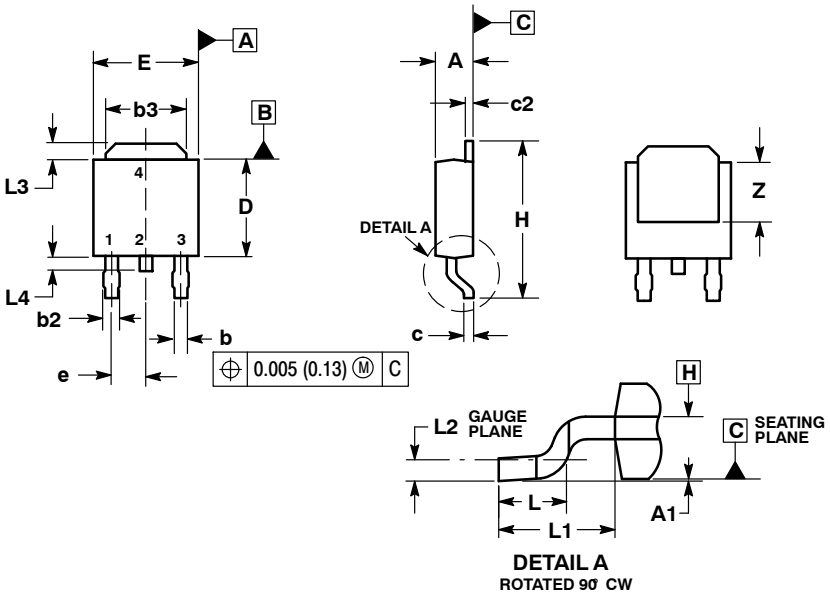


Figure 8. Gate Threshold Voltage vs. Junction Temperature

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE D

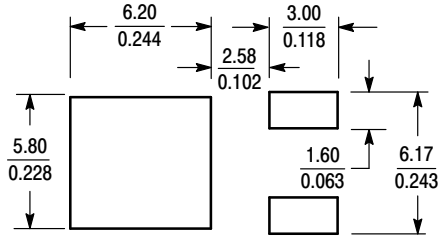


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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