

NGTB05N60R2DT4G



ON Semiconductor®

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IGBT 600V, 8A, N-Channel

Features

- Reverse Conducting II IGBT
- IGBT $V_{CE(sat)}=1.65V$ (typ) [$I_C=5A$, $V_{GE}=15V$]
- IGBT $t_f=95ns$ (typ)
- Diode $V_F=1.5V$ (typ) [$I_F=5A$]
- Diode $t_{rr}=70ns$ (typ)
- 5 μs Short Circuit Capability

Applications

- General Purpose Inverter

Specifications

Absolute Maximum Ratings at $T_a=25^\circ C$, Unless otherwise specified

Parameter	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CES}	600	V
Gate to Emitter Voltage	V_{GES}	± 20	V
Collector Current (DC)	I_C *1	16	A
Limited by T_{jmax}		@ $T_c=100^\circ C$ *2	8
Collector Current (Peak)	I_{CP}	20	A
Pulse width Limited by T_{jmax}			
Diode Average Output Current	I_O	8	A
Power Dissipation	P_D	56	W
$T_c=25^\circ C$ (Our ideal heat dissipation condition) *2			
Junction Temperature	T_j	175	$^\circ C$
Storage Temperature	T_{stg}	-55 to +175	$^\circ C$

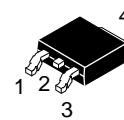
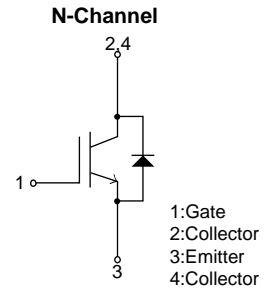
Note : *1 Collector Current is calculated from the following formula.

$$I_C(T_c) = \frac{T_{jmax} - T_c}{R_{th(j-c)} \times V_{CE(sat)}(I_C(T_c))}$$

*2 Our condition is radiation from backside.

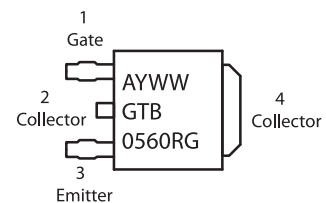
The method is applying silicone grease to the backside of the device and attaching the device to water-cooled radiator made of aluminum.

Electrical Connection



DPAK
CASE 369C

Marking Diagram



GTB0560R = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

NGTB05N60R2DT4G

Electrical Characteristics at Ta=25°C, Unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Collector to Emitter Breakdown Voltage	V(BR)CES	IC=1mA, VGE=0V	600			V
Collector to Emitter Cut off Current	ICES	VCE=600V, VGE=0V	Tc=25°C		10	μA
			Tc=150°C		1	mA
Gate to Emitter Leakage Current	IGES	VGE=±20V, VCE=0V			±100	nA
Gate to Emitter Threshold Voltage	VGE(th)	VCE=20V, IC=80μA	4.5		7.0	V
Collector to Emitter Saturation Voltage	VCE(sat)	VGE=15V, IC=5A	Tc=25°C	1.65	2.0	V
			Tc=100°C	1.85	2.2	V
Forward Diode Voltage	VF	IF=5A		1.5	2.1	V
Input Capacitance	Cies	VCE=20V, f=1MHz		740		pF
Output Capacitance	Coes			30		pF
Reverse Transfer Capacitance	Cres			20		pF
Turn-ON Delay Time	t _{d(on)}			44		ns
Rise Time	t _r	VCC=300V, IC=5A RG=30Ω, L=500μH VGE=0V/15V Vclamp=400V Tc=25°C See Fig.1, See Fig.2		26		ns
Turn-ON Time	ton			139		ns
Turn-OFF Delay Time	t _{d(off)}			82		ns
Fall Time	t _f			95		ns
Turn-OFF Time	toff			186		ns
Turn-ON Energy	Eon			188		μJ
Turn-OFF Energy	Eoff			60		μJ
Total Gate Charge	Qg			30		nC
Gate to Emitter Charge	Qge	VCE=300V, VGE=15V, IC=5A		6		nC
Gate to Collector "Miller" Charge	Qgc			14		nC
Diode Reverse Recovery Time	t _{rr}	IF=5A, di/dt=300A/μs, VCC=300V, See Fig.3		70		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

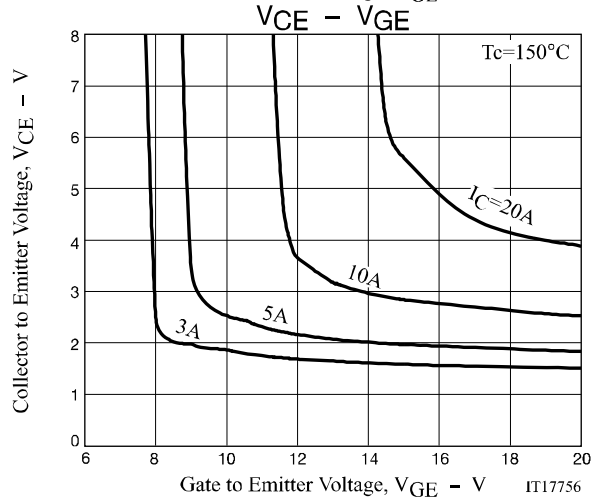
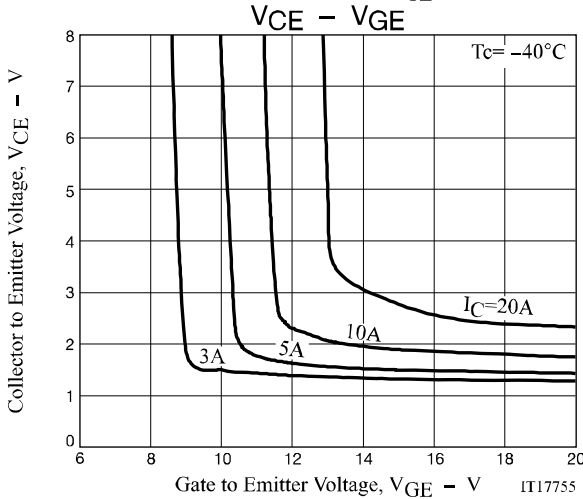
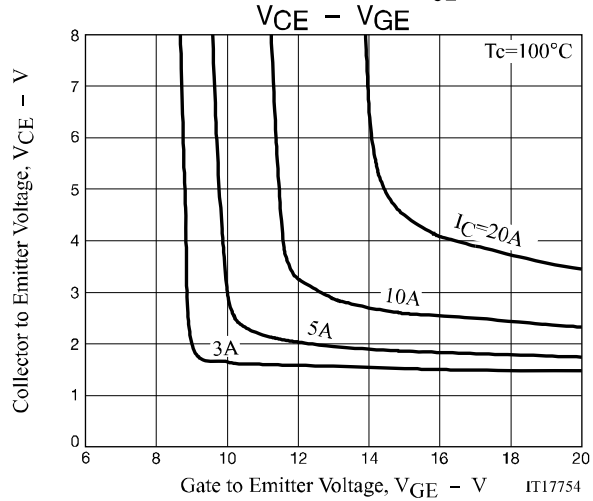
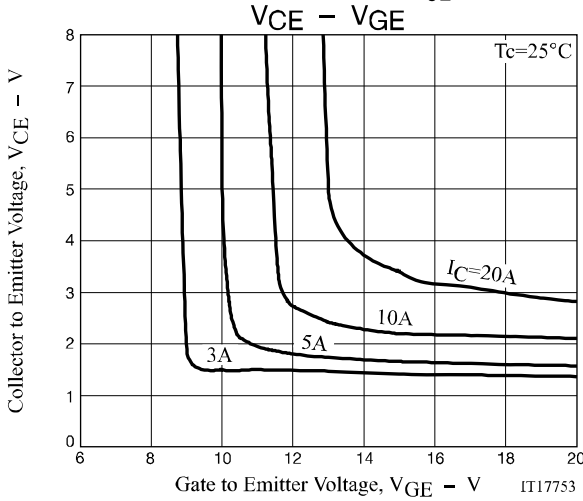
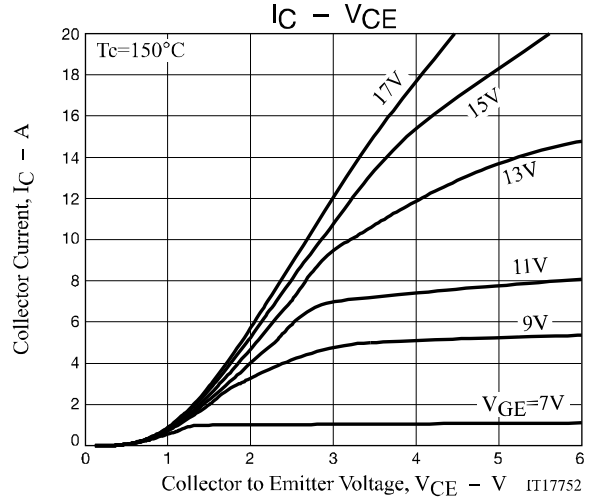
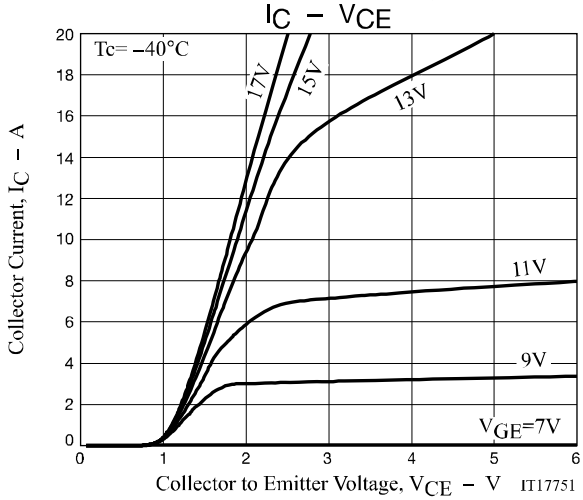
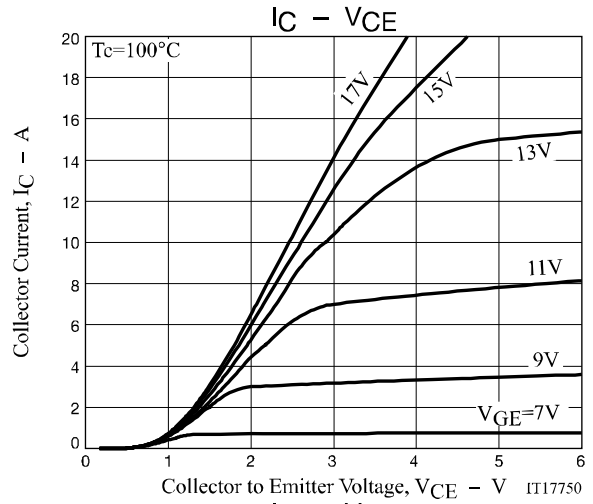
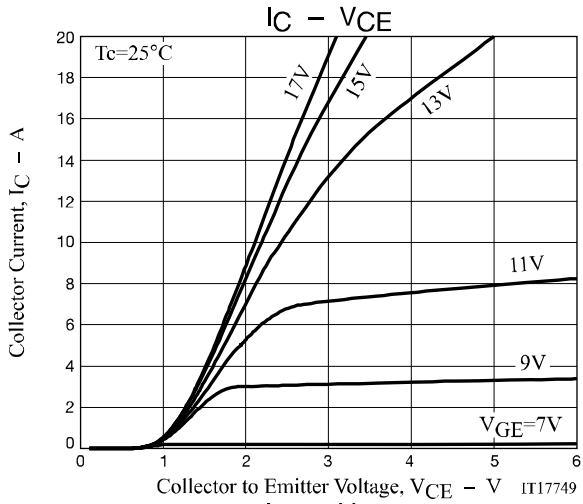
Thermal Characteristics at Ta=25°C, Unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Thermal Resistance IGBT (Junction to Case)	Rth(j-c) (IGBT)	Tc=25°C (Our ideal heat dissipation condition) *2	2.7	°C/W
Thermal Resistance (Junction to Ambient)	Rth(j-a)		100	°C/W

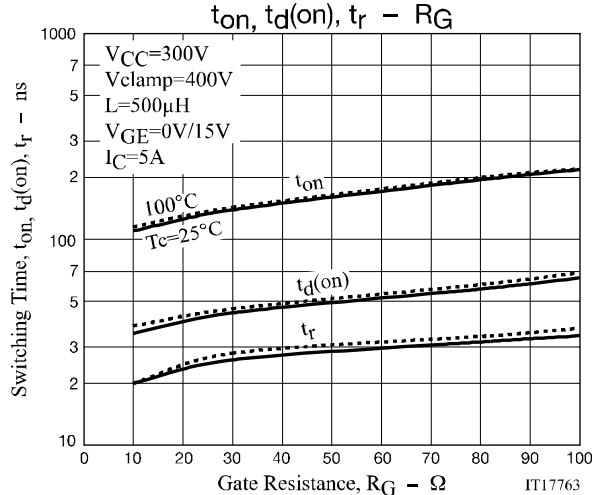
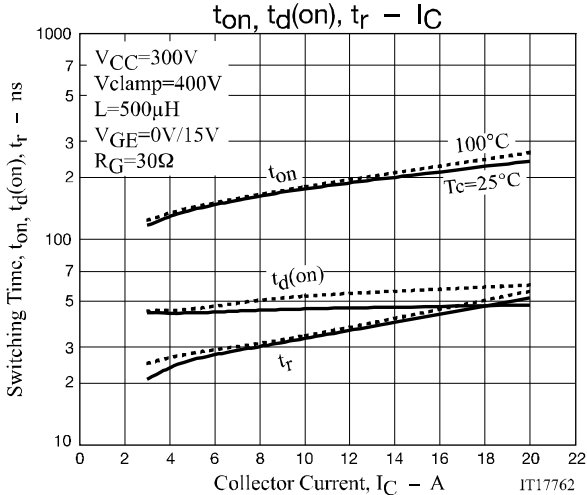
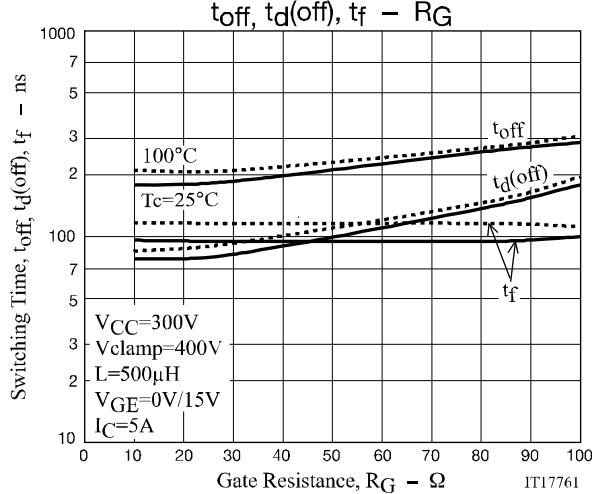
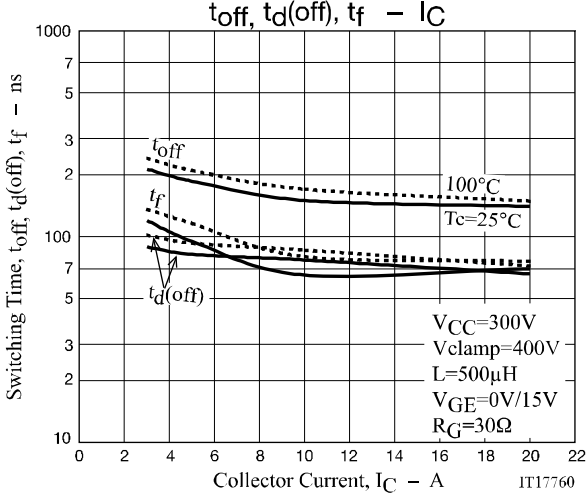
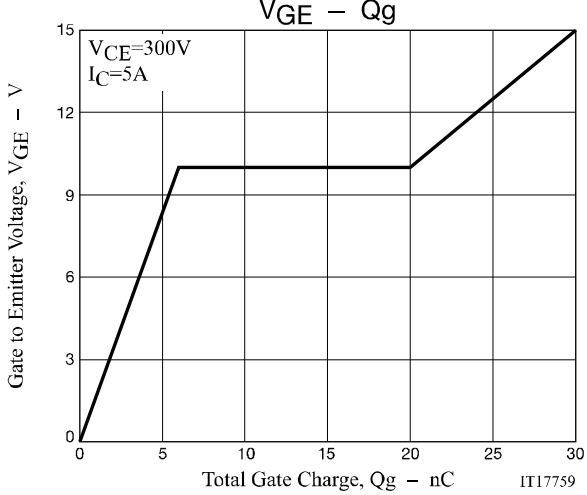
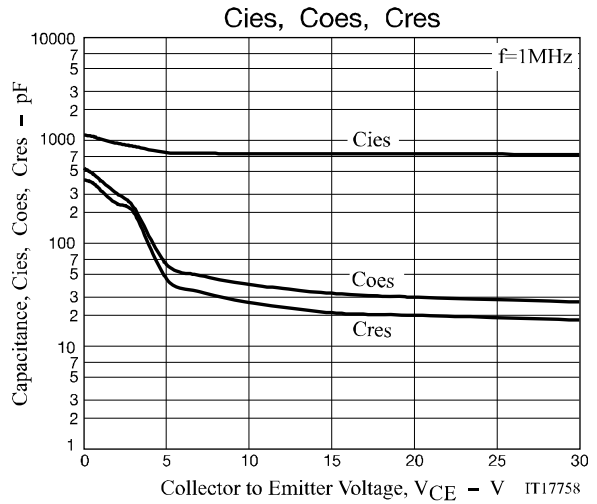
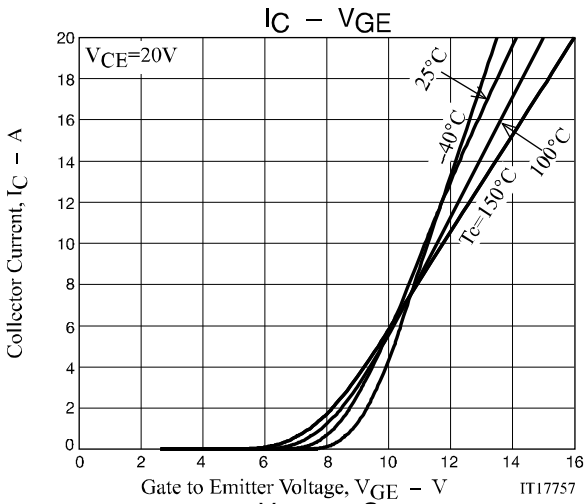
Note : *2 Our condition is radiation from backside.

The method is applying silicone grease to the backside of the device and attaching the device to water-cooled radiator made of aluminum.

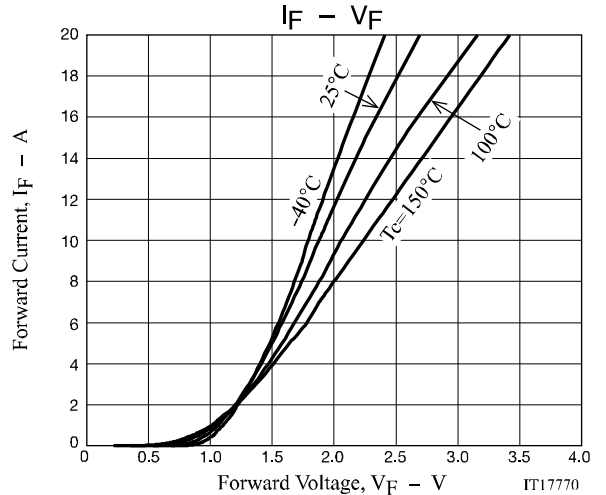
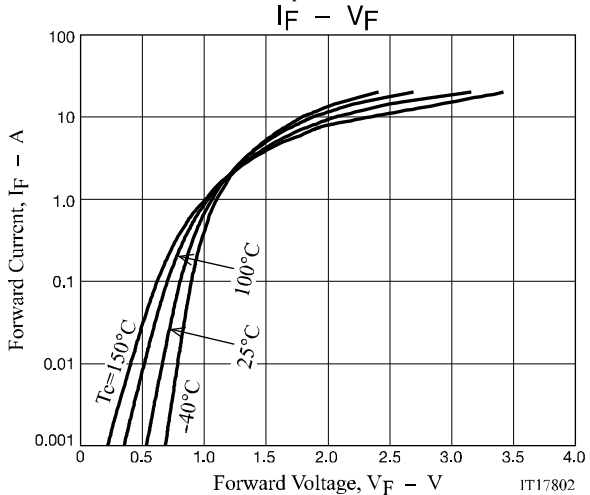
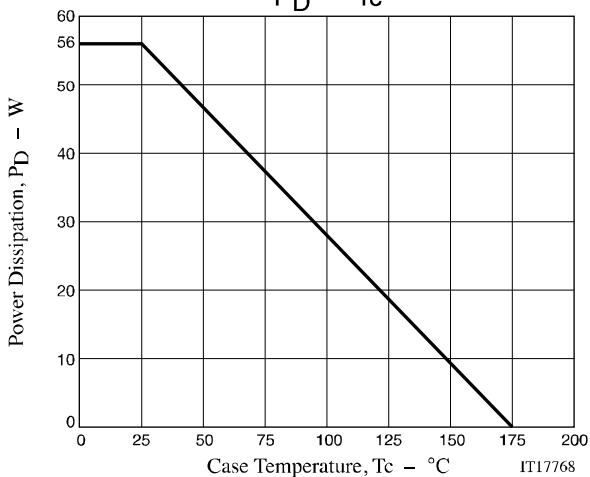
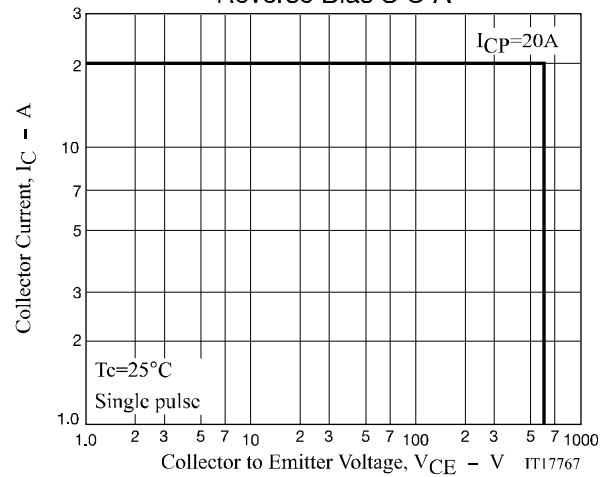
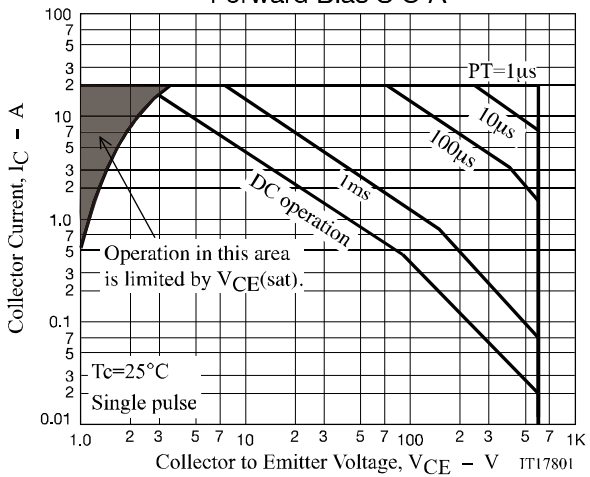
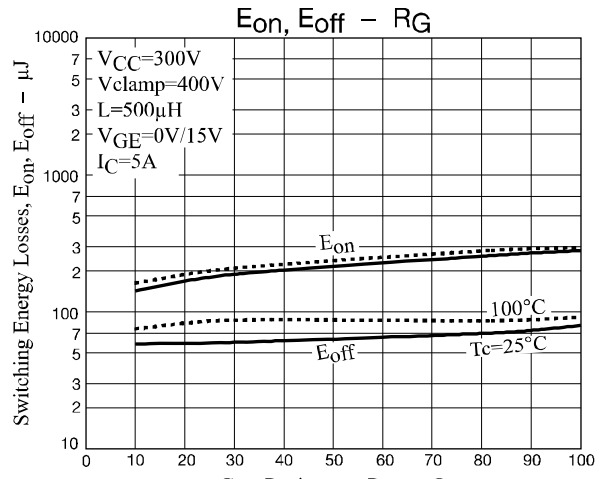
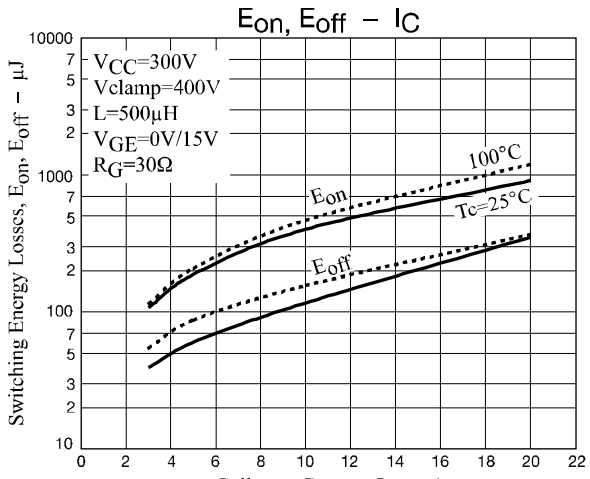
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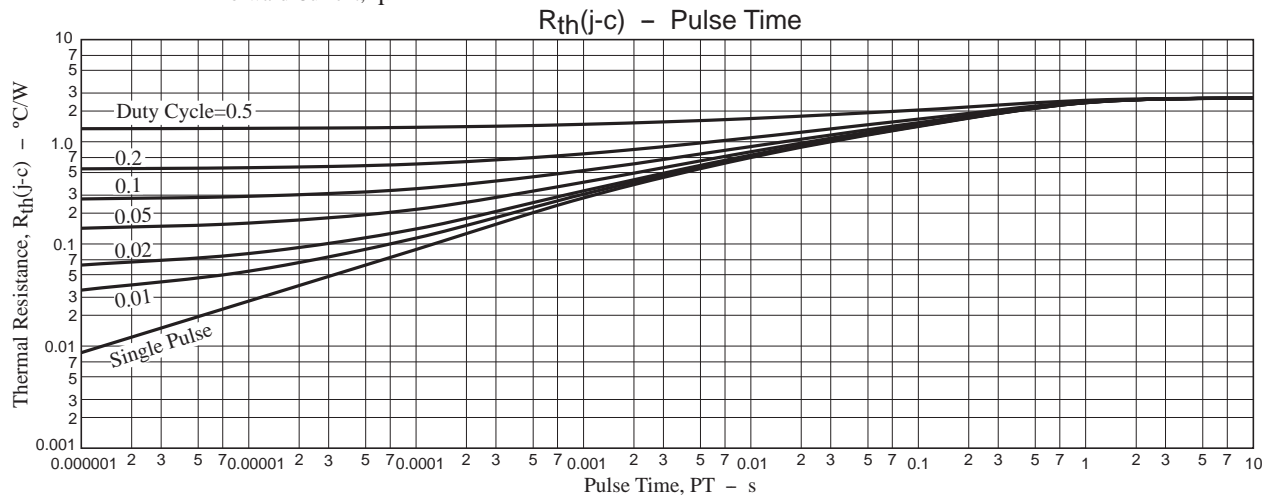
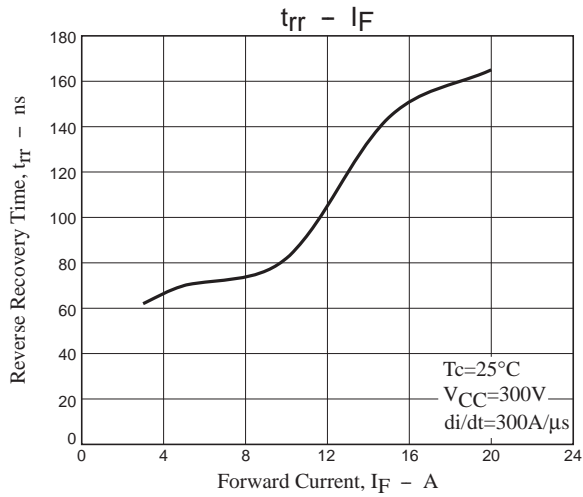


Fig.1 Switching Time Test Circuit

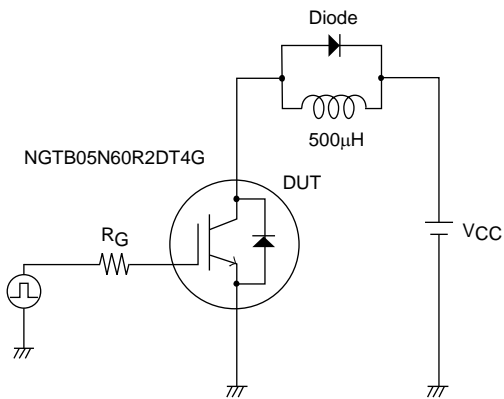


Fig.2 Timing Chart

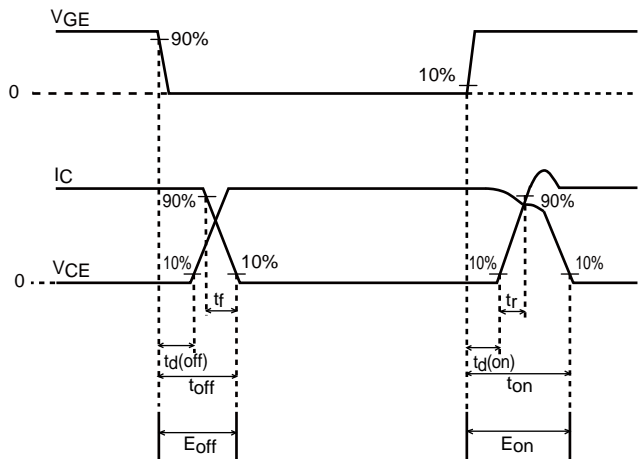
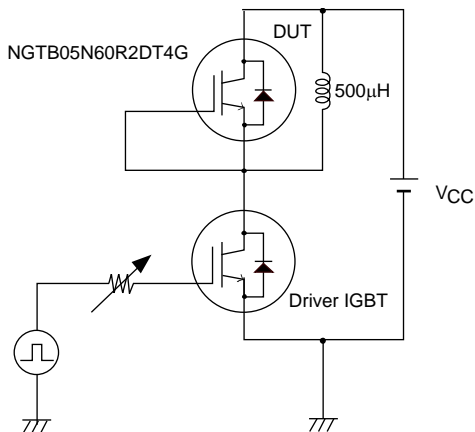


Fig.3 Reverse Recovery Time Test Circuit

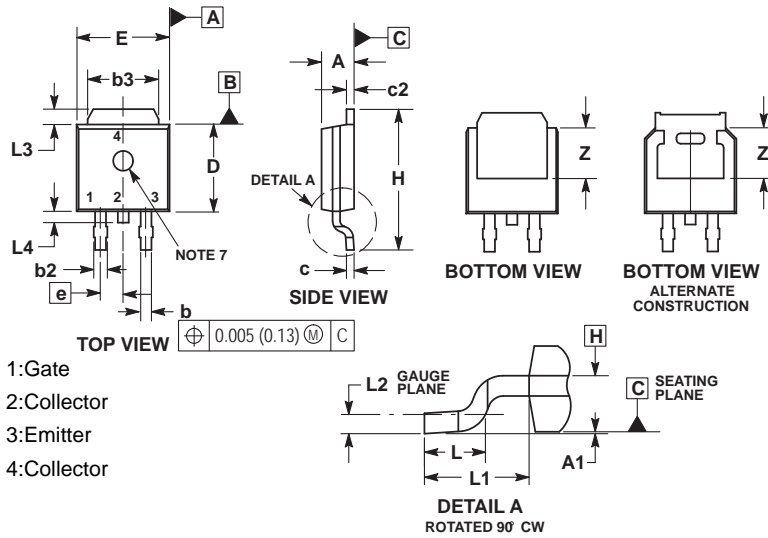


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Package Dimensions

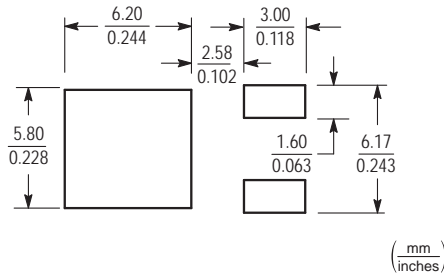
unit : mm

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE E



- | | | | | |
|---|---|--|--|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. ANODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE | STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE |
| STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2 | STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE | STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

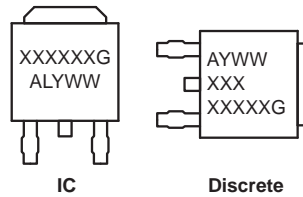
Device	Package	Shipping	note
NGTB05N60R2DT4G	DPAK	2500 pcs. / reel	Pb-Free And Halogen Free

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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