

# NGTB50N65FL2WAG

## IGBT - Field Stop II / 4 Lead

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Field Stop II Trench construction, and provides superior performance in demanding switching applications, offering both low on state voltage and minimal switching loss. In addition, this new device is packaged in a TO-247-4L package that provides significant reduction in  $E_{on}$  Losses compared to standard TO-247-3L package. The IGBT is well suited for UPS and solar applications. Incorporated into the device is a soft and fast co-packaged free wheeling diode with a low forward voltage.

### Features

- Extremely Efficient Trench with Field Stop Technology
- $T_{Jmax} = 175^{\circ}C$
- Improved Gate Control Lowers Switching Losses
- Separate Emitter Drive Pin
- TO-247-4L for Minimal  $E_{on}$  Losses
- Optimized for High Speed Switching
- This is a Pb-Free Device

### Typical Applications

- Solar Inverters
- Uninterruptible Power Supplies (UPS)
- Neutral Point Clamp Topology

### ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-emitter voltage	$V_{CES}$	650	V
Collector current @ $T_c = 25^{\circ}C$ @ $T_c = 100^{\circ}C$	$I_c$	160 50	A
Diode Forward Current @ $T_c = 25^{\circ}C$ @ $T_c = 100^{\circ}C$	$I_F$	160 50	A
Diode Pulsed Current $T_{PULSE}$ Limited by $T_J$ Max	$I_{FM}$	160	A
Pulsed collector current, $T_{pulse}$ limited by $T_{Jmax}$	$I_{CM}$	160	A
Gate-emitter voltage	$V_{GE}$	$\pm 20$	V
Transient gate-emitter voltage ( $T_{PULSE} = 5 \mu s, D < 0.10$ )		$\pm 30$	
Power Dissipation @ $T_c = 25^{\circ}C$ @ $T_c = 100^{\circ}C$	$P_D$	417 208	W
Operating junction temperature range	$T_J$	-55 to +175	$^{\circ}C$
Storage temperature range	$T_{stg}$	-55 to +175	$^{\circ}C$
Lead temperature for soldering, 1/8" from case for 5 seconds	$T_{SLD}$	260	$^{\circ}C$

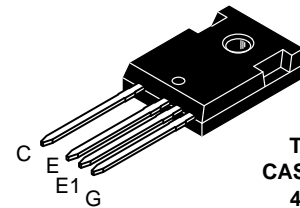
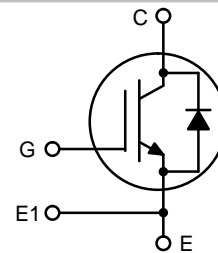
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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50 A, 650 V  
 $V_{CEsat} = 1.8 V$   
 $E_{on} = 0.48 mJ$



TO-247  
CASE 340AR  
4 LEAD

### MARKING DIAGRAM



50N65FL2 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
NGTB50N65FL2WAG	TO-247 (Pb-Free)	30 Units / Rail

# NGTB50N65FL2WAG

## THEMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal resistance junction-to-case, for IGBT	$R_{\theta JC}$	0.36	$^{\circ}\text{C}/\text{W}$
Thermal resistance junction-to-case, for Diode	$R_{\theta JC}$	0.62	$^{\circ}\text{C}/\text{W}$
Thermal resistance junction-to-ambient	$R_{\theta JA}$	40	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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### STATIC CHARACTERISTIC

Collector-emitter breakdown voltage, gate-emitter short-circuited	$V_{GE} = 0\text{ V}, I_C = 500\ \mu\text{A}$	$V_{(BR)CES}$	650	–	–	V
Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}, I_C = 50\text{ A}$ $V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_J = 175^{\circ}\text{C}$	$V_{CEsat}$	–	1.80 2.17	2.00 –	V
Gate-emitter threshold voltage	$V_{GE} = V_{CE}, I_C = 350\ \mu\text{A}$	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector-emitter cut-off current, gate-emitter short-circuited	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$ $V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}, T_J = 175^{\circ}\text{C}$	$I_{CES}$	–	– 5.5	0.3 –	mA
Gate leakage current, collector-emitter short-circuited	$V_{GE} = 20\text{ V}, V_{CE} = 0\text{ V}$	$I_{GES}$	–	–	200	nA

### DYNAMIC CHARACTERISTIC

Input capacitance	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 1\text{ MHz}$	$C_{ies}$	–	5160	–	pF
Output capacitance		$C_{oes}$	–	244	–	
Reverse transfer capacitance		$C_{res}$	–	141	–	
Gate charge total	$V_{CE} = 480\text{ V}, I_C = 50\text{ A}, V_{GE} = 15\text{ V}$	$Q_g$	–	215	–	nC
Gate to emitter charge		$Q_{ge}$	–	48	–	
Gate to collector charge		$Q_{gc}$	–	116	–	

### SWITCHING CHARACTERISTIC, INDUCTIVE LOAD

Turn-on delay time	$T_J = 25^{\circ}\text{C}$ $V_{CC} = 400\text{ V}, I_C = 50\text{ A}$ $R_g = 10\ \Omega$ $V_{GE} = 15\text{ V}$	$t_{d(on)}$	–	23	–	ns	
Rise time		$t_r$	–	35	–		
Turn-off delay time		$t_{d(off)}$	–	123	–		
Fall time			$t_f$	–	54	–	mJ
Turn-on switching loss		$E_{on}$	–	0.42	–		
Turn-off switching loss		$E_{off}$	–	0.55	–		
Total switching loss		$E_{ts}$	–	0.97	–		
Turn-on delay time	$T_J = 175^{\circ}\text{C}$ $V_{CC} = 400\text{ V}, I_C = 50\text{ A}$ $R_g = 10\ \Omega$ $V_{GE} = 15\text{ V}$	$t_{d(on)}$	–	22	–	ns	
Rise time		$t_r$	–	38	–		
Turn-off delay time		$t_{d(off)}$	–	130	–		
Fall time			$t_f$	–	93	–	mJ
Turn-on switching loss		$E_{on}$	–	0.58	–		
Turn-off switching loss		$E_{off}$	–	0.92	–		
Total switching loss		$E_{ts}$	–	1.50	–		

### DIODE CHARACTERISTIC

Forward voltage	$V_{GE} = 0\text{ V}, I_F = 50\text{ A}$ $V_{GE} = 0\text{ V}, I_F = 50\text{ A}, T_J = 175^{\circ}\text{C}$	$V_F$	–	2.10 2.20	2.60 –	V
Reverse recovery time	$T_J = 25^{\circ}\text{C}$ $I_F = 50\text{ A}, V_R = 400\text{ V}$ $di_F/dt = 200\text{ A}/\mu\text{s}$	$t_{rr}$	–	94	–	ns
Reverse recovery charge		$Q_{rr}$	–	0.36	–	$\mu\text{C}$
Reverse recovery current		$I_{rrm}$	–	6.5	–	A
Reverse recovery time	$T_J = 175^{\circ}\text{C}$ $I_F = 50\text{ A}, V_R = 400\text{ V}$ $di_F/dt = 200\text{ A}/\mu\text{s}$	$t_{rr}$	–	170	–	ns
Reverse recovery charge		$Q_{rr}$	–	1.40	–	$\mu\text{C}$
Reverse recovery current		$I_{rrm}$	–	13	–	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NGTB50N65FL2WAG

## TYPICAL CHARACTERISTICS

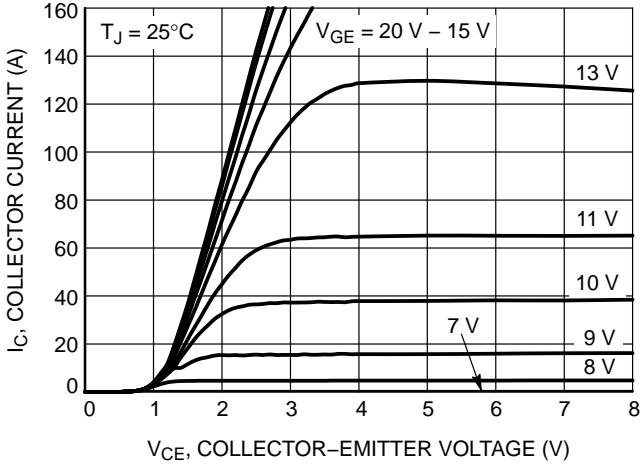


Figure 1. Output Characteristics

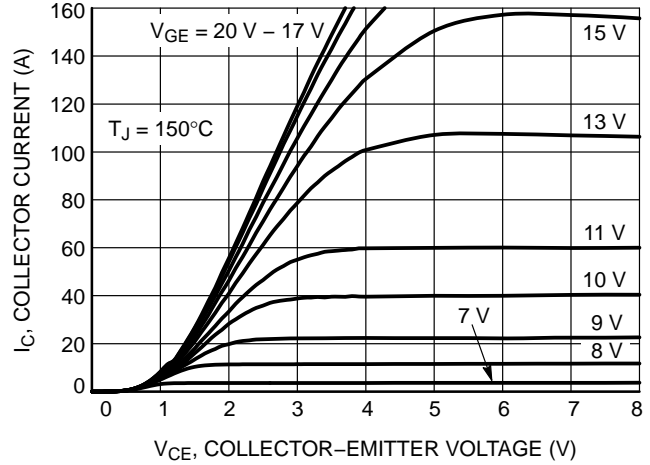


Figure 2. Output Characteristics

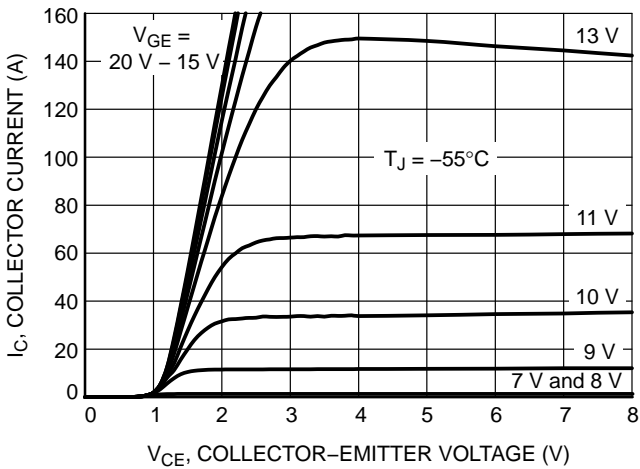


Figure 3. Output Characteristics

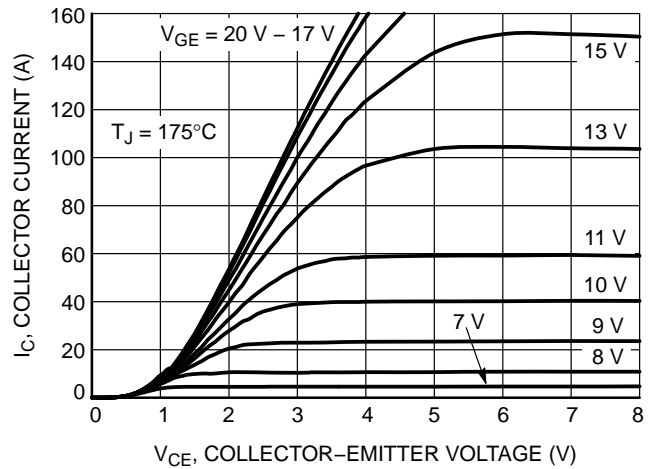


Figure 4. Output Characteristics

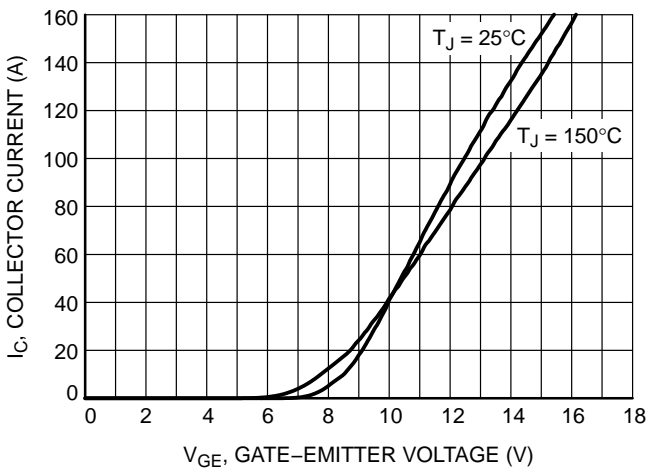


Figure 5. Typical Transfer Characteristics

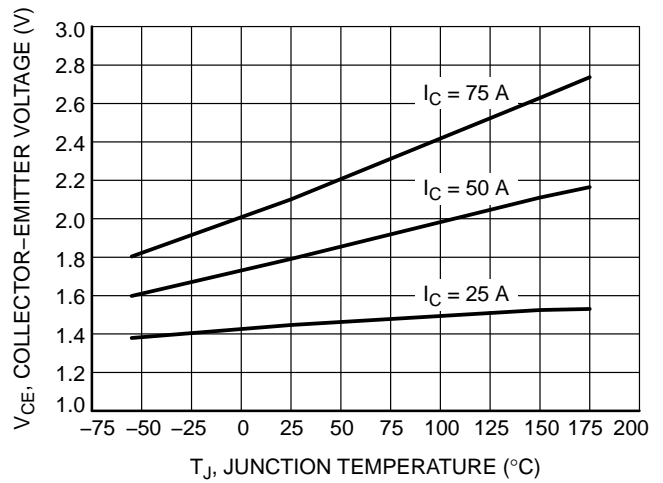


Figure 6.  $V_{CE(sat)}$  vs.  $T_J$

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## TYPICAL CHARACTERISTICS

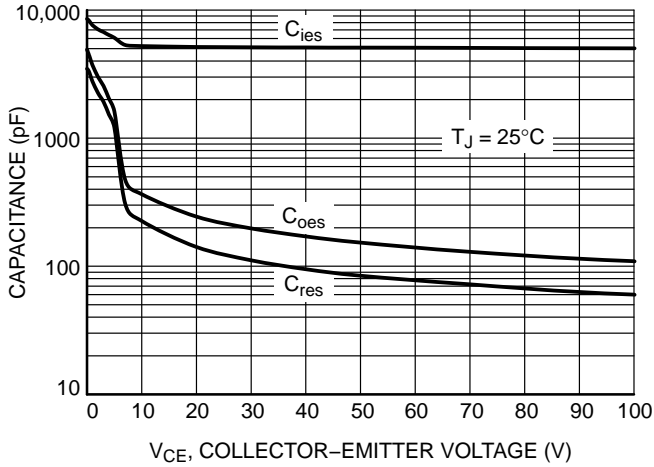


Figure 7. Typical Capacitance

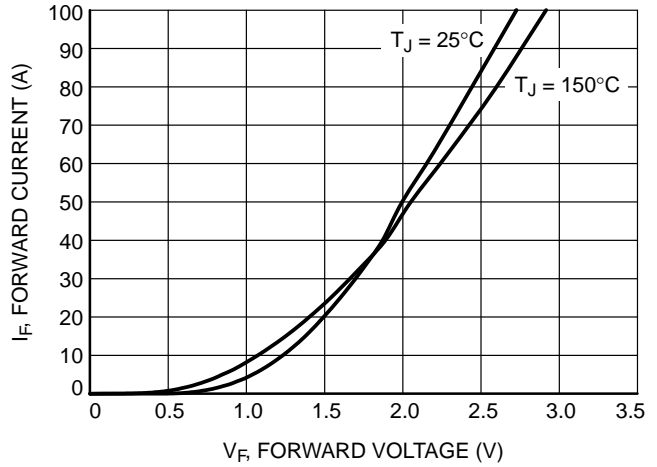


Figure 8. Diode Forward Characteristics

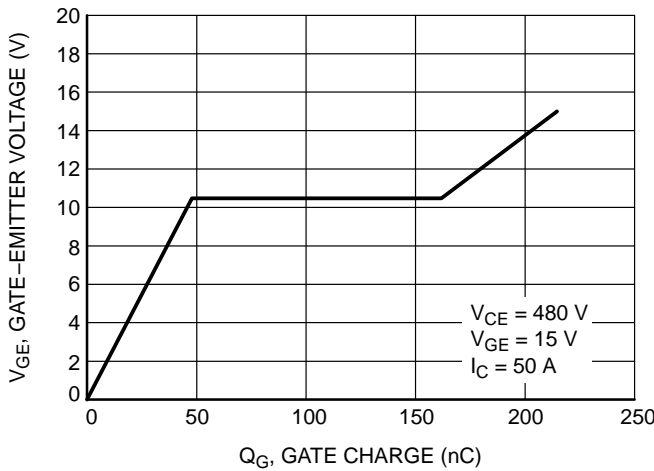


Figure 9. Typical Gate Charge

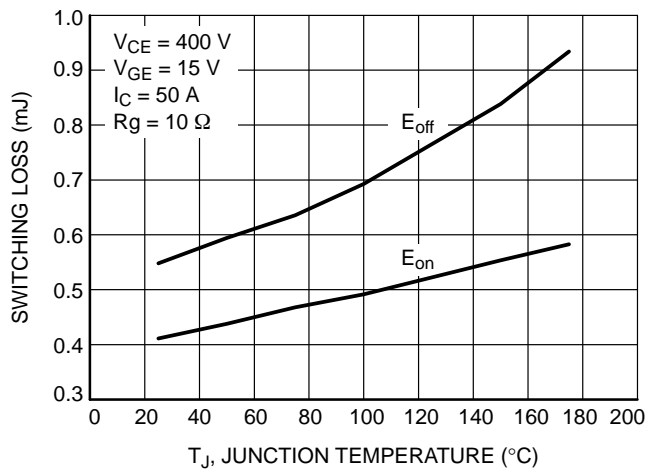


Figure 10. Switching Loss vs. Temperature

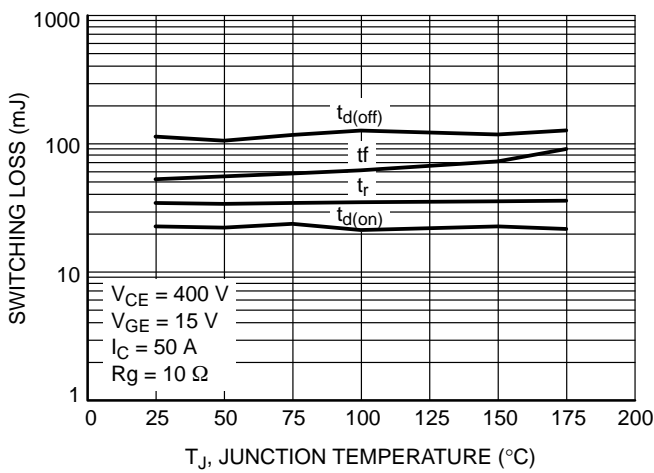


Figure 11. Switching Time vs. Temperature

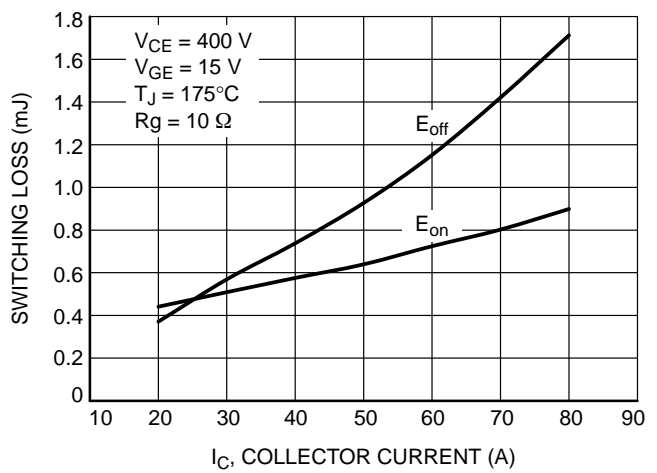


Figure 12. Switching Loss vs. IC

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## TYPICAL CHARACTERISTICS

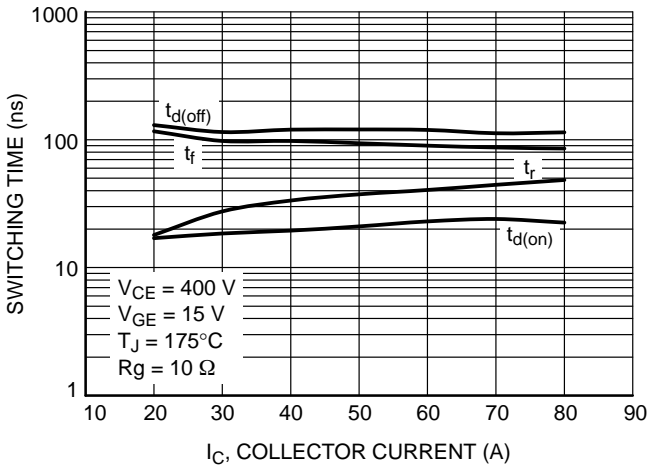


Figure 13. Switching Time vs.  $I_C$

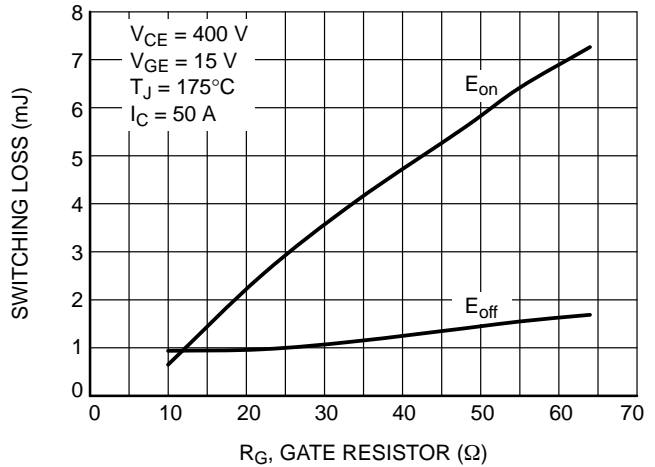


Figure 14. Switching Loss vs.  $R_G$

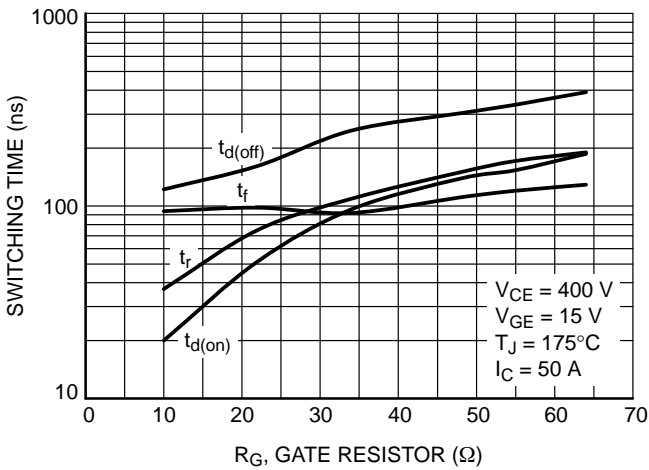


Figure 15. Switching Time vs.  $R_G$

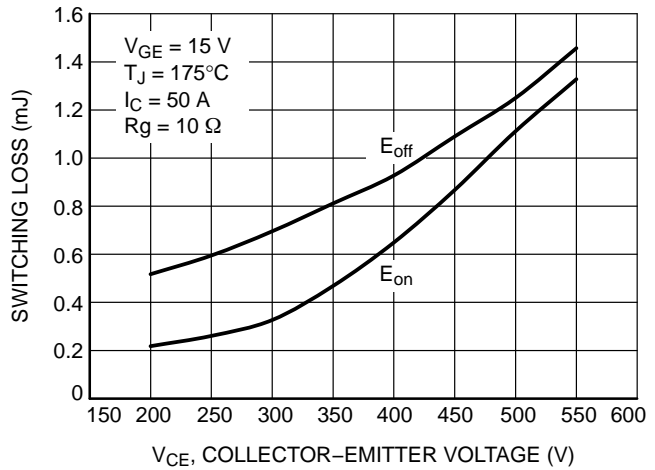


Figure 16. Switching Loss vs.  $V_{CE}$

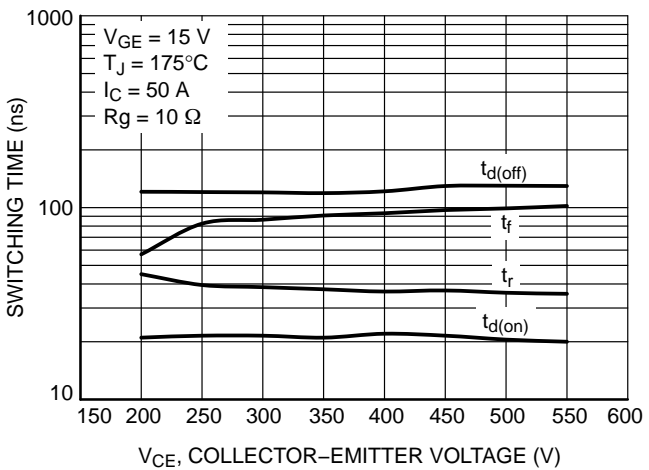


Figure 17. Switching Time vs.  $V_{CE}$

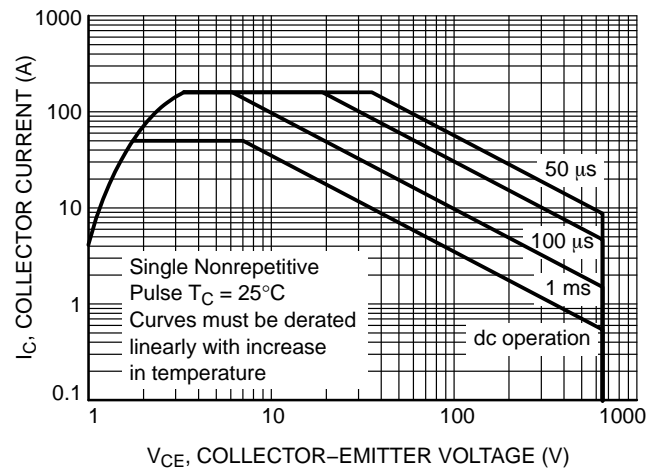


Figure 18. Safe Operating Area

# NGTB50N65FL2WAG

## TYPICAL CHARACTERISTICS

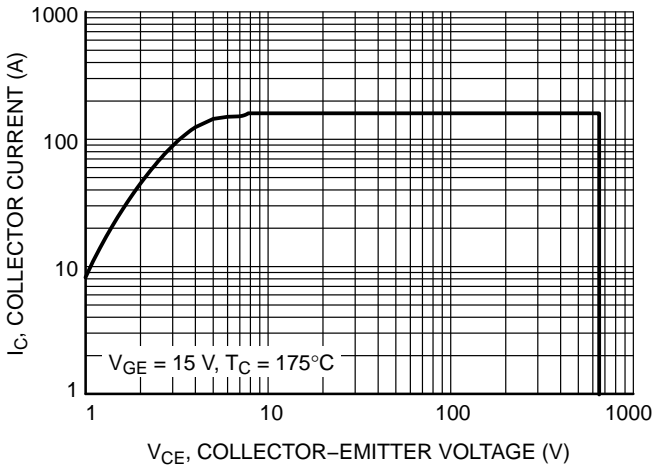


Figure 19. Reverse Bias Safe Operating Area

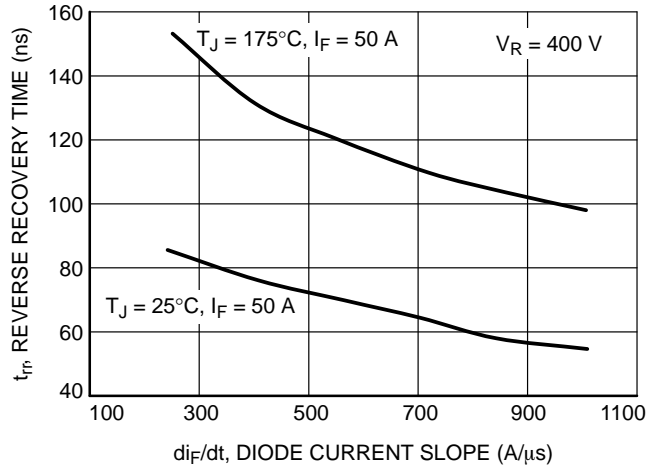


Figure 20.  $t_{rr}$  vs.  $di_F/dt$

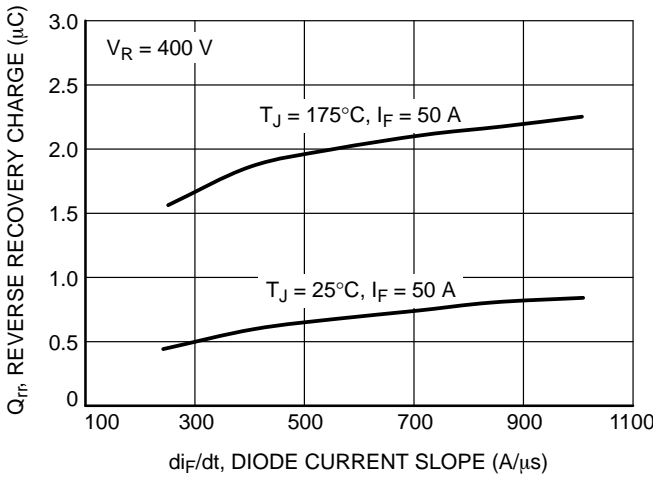


Figure 21.  $Q_{rr}$  vs.  $di_F/dt$

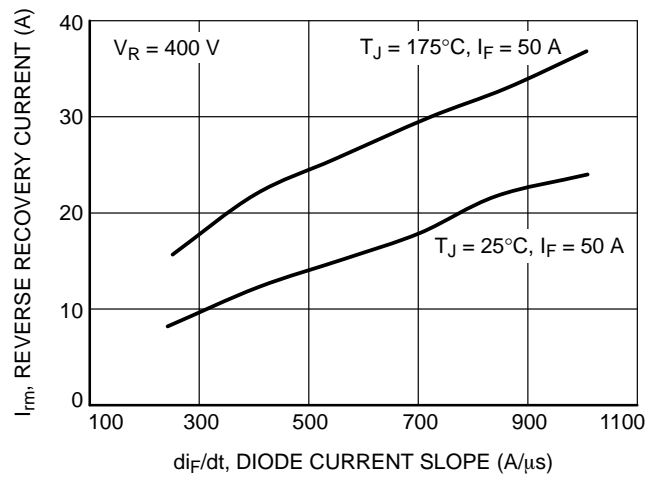


Figure 22.  $I_{rrm}$  vs.  $di_F/dt$

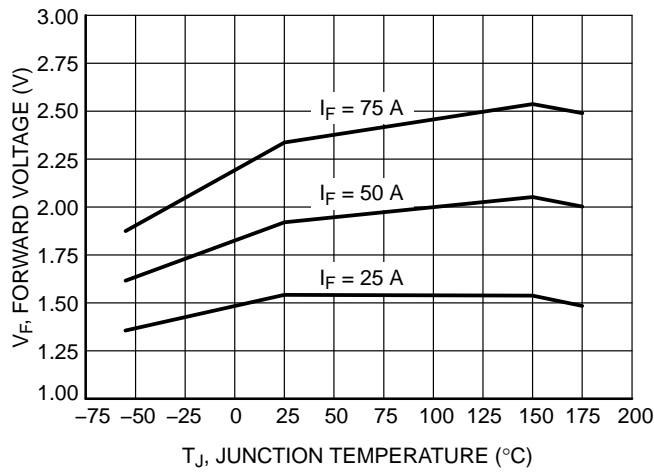


Figure 23.  $V_F$  vs.  $T_J$

# NGTB50N65FL2WAG

## TYPICAL CHARACTERISTICS

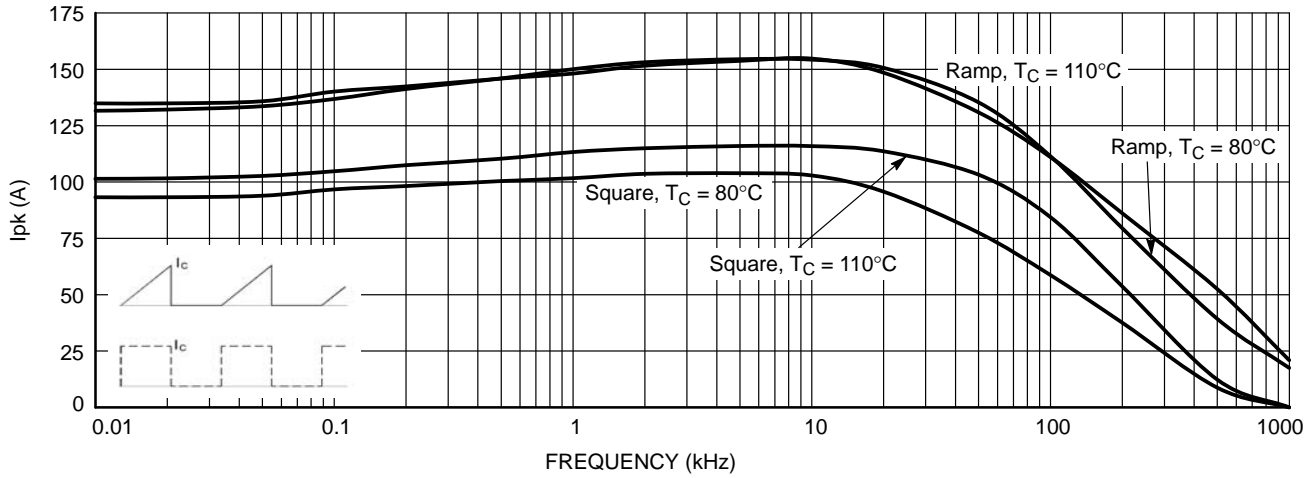


Figure 24. Collector Current vs. Switching Frequency

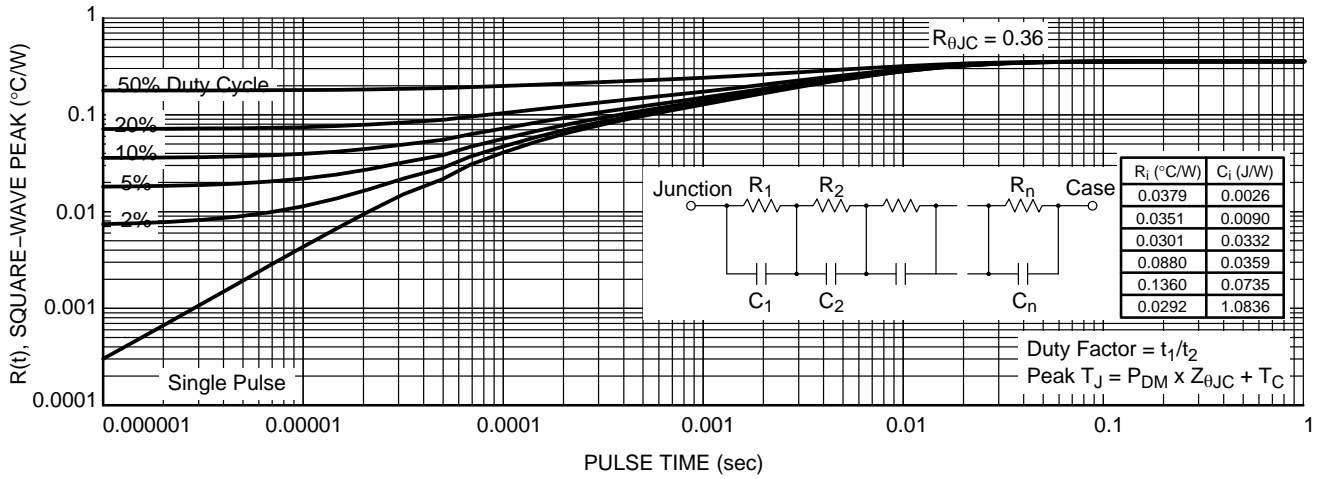


Figure 25. IGBT Transient Thermal Impedance

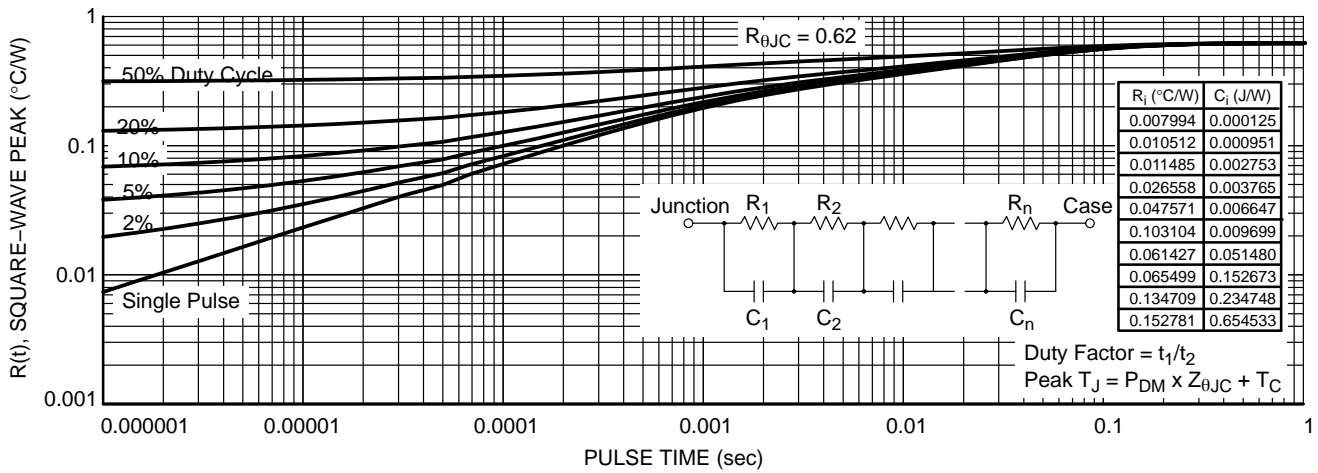


Figure 26. Diode Transient Thermal Impedance

# NGTB50N65FL2WAG

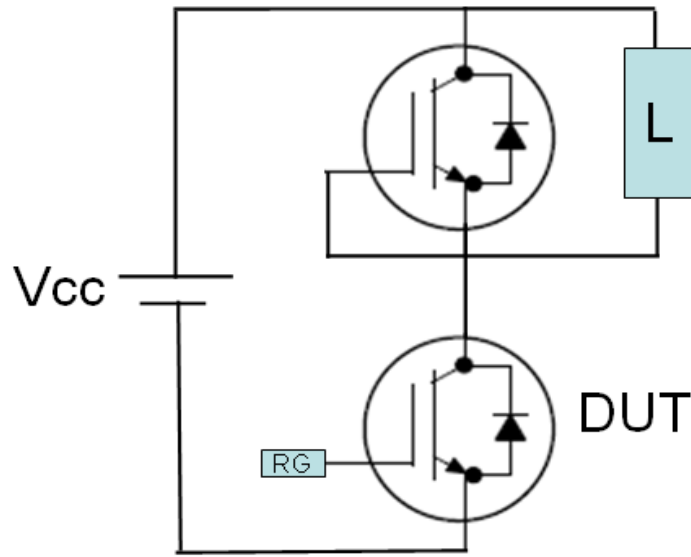


Figure 27. Test Circuit for Switching Characteristics



Figure 28. Definition of Turn On Waveform



# NGTB50N65FL2WAG

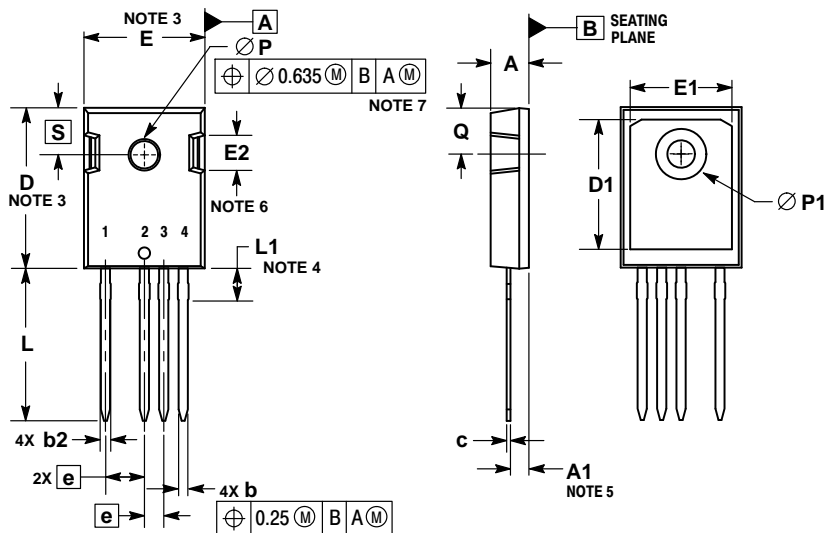


Figure 29. Definition of Turn Off Waveform

# NGTB50N65FL2WAG

## PACKAGE DIMENSIONS

### TO-247 4-LEAD CASE 340AR ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
  4. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.
  5. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
  6. NOTCHES ARE REQUIRED BUT THEIR SHAPE IS OPTIONAL.
  7. DIAMETER  $\phi P$  SHALL HAVE A MAXIMUM DRAFT ANGLE OF 3.5° TO THE TOP OF THE PART WITH A MAXIMUM DIAMETER OF 4.20.

DIM	MILLIMETERS	
	MIN	MAX
A	4.83	5.21
A1	2.29	2.54
b	1.10	1.30
b2	1.30	1.50
c	0.50	0.70
D	20.80	21.10
D1	16.25	17.65
E	15.75	16.13
E1	13.06	13.46
E2	4.32	4.83
e	2.54 BSC	
L	19.90	20.30
L1	4.00	4.40
P	3.50	3.70
P1	7.00	7.40
Q	5.59	6.20
S	6.15 BSC	

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