NID1100

1.5 V to 5.5 V, 1 A, ideal diode with forward voltage blocking

Rev. 2 — 17 March 2025 Product data sheet

1. General description

The NID1100 is a low forward-voltage drop ideal diode with forward and reverse voltage blocking. It can be used to replace rectifiers in low voltage systems unable to tolerate the high voltage drops of conventional Schottky diodes. The device operates over an input voltage range of 1.5 V to 5.5 V and can support up to 1 A continuous current. They can also be used in dual supply systems in an OR-ing configuration to switch the load seamlessly from one supply to the next.

The EN pin determines the operation mode of the NID1100. When EN is low, the NID1100 blocks voltages in both forward and reverse directions. When the enable input goes high, and the input voltage is higher than the output voltage, the NID1100 starts up in controlled manner limiting the inrush current. Once inrush is complete, the device regulates the voltage between the IN and OUT pins resulting in a forward voltage drop, V_{FWD}, approximately an order of magnitude smaller than similarly rated Schottky diodes. If at any time, the OUT voltage becomes higher than IN voltage, the NID1100 stops conducting with very low leakage currents.

NID1100 also includes short circuit current limiting and over temperature shut down to provide robust protection against load fault conditions. The open-drain ST pin can be used to monitor the status of the NID1100. The ST pin pulls low when the device is disabled, in reverse voltage blocking state or in over temperature shut down.

A variety of power OR-ing configurations are supported for system flexibility:

- Two, or more, NID1100 devices
- NID1100s and conventional Schottky diodes
- NID1100 and an external PMOS

The NID1100 is available in a standard SOT753 (SC-74A) package and is characterized for operation over a junction temperature range of –40 °C to 125 °C.

2. Features and benefits

- Input voltage range of 1.5 V to 5.5 V
- Low forward drop voltage: V_{FWD} = 120 mV (typ. at 3.6 V input and 1 A load current)
- Reverse voltage blocking always
  - Low leakage current when reverse biased
- Forward voltage blocking when disabled
- Low quiescent current
- Enhanced load transient response
- Controlled rise time at start-up
- Over temperature protection
- Short circuit protection
- SOT753 (SC-74A) 5 pins plastic surface-mounted package
- Specified over T_j= -40 °C to +125 °C

3. Applications

- IoT systems
- Gas meters, smart meters
- CO Detectors
- Battery backup systems
- USB powered devices

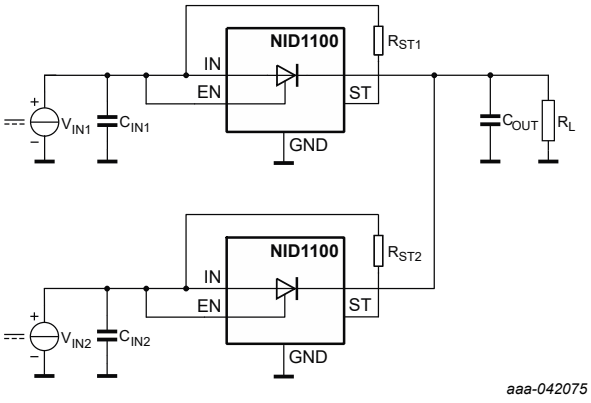


Fig. 1. Simplified application

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NID1100GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

5. Marking

Table 2. Marking code

Type number	Marking code
NID1100GV	u2

6. Functional diagram

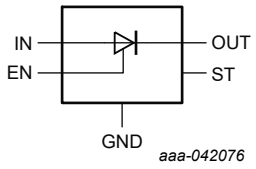


Fig. 2. Logic symbol

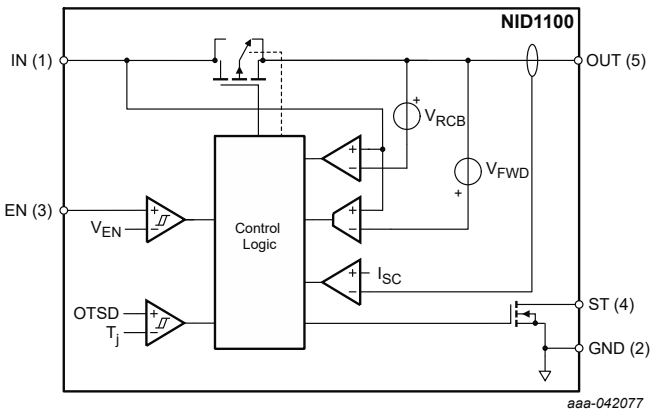


Fig. 3. Functional diagram

7. Pin configuration and description

7.1. Pin configuration

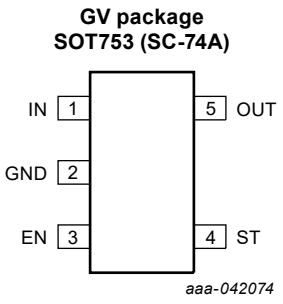


Fig. 4. Pin configuration SOT753 (SC-74A)

7.2. Pin description

Table 3. Pin description

Symbol	Pin	I/O	Description
IN	1	I	“Anode” connection of the ideal diode. Connect to a power supply. Bypass with a low ESR capacitance of at least 0.1 µF.
GND	2	GND	Ground (0 V)
EN	3	I	Active high enable input to the IC. Connect to IN to permanently enable the device. Connect to GND to disable. Connect EN to an I/O to control it. Do not leave this pin floating.
ST	4	O	Active Low status output. Pulls low during when device is disabled, in reverse voltage blocking state or in over temperature shut down. Pull up with a resistor to IN. Leave floating or connect to GND if not used.
OUT	5	O	“Cathode” connection of the ideal diode. Connect to the load. Bypass with a low ESR capacitance of at least 0.33 µF.

8. Specifications

8.1. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		-0.3	6	V
V_{OUT}	output voltage		-0.3	6	V
V_{EN}	EN pin voltage		-0.3	6	V
V_{ST}	ST pin voltage		-0.3	6	V
I_{ST}	max current into status pin		-	1	mA
T_j	junction temperature		-40	125	°C
T_{stg}	storage temperature		-65	150	°C

8.2. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge	HBM: ANSI/ESDA/JEDEC JS-001 class 2	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	±500	V

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		1.5	5.5	V
V_{OUT}	output Voltage		0	5.5	V
I_{OUT}	max continuous output current	>2.0 V input	-	1	A
		1.6 V to 1.9 V		0.5	A
		1.5 V		50	mA
$I_{OUT,SW}$	maximum pulsed switch current	≤120 ms, 2% duty-cycle, V_{IN} = 3.3 V/5.0 V	-	1.5	A
V_{EN}	EN Pin voltage		0	5.5	V
I_{ST}	current into ST pin		0	0.5	mA
C_{OUT}	total capacitance at OUT	including derating and tolerances	0.3	100	µF

8.4. Thermal information

Table 7. Thermal information

Thermal resistance according to JEDEC51-5 and -7

Symbol	Parameter	SOT753	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	206	°C/W
Ψ_{JT}	junction-to-top characterization parameter	111	°C/W

8.5. Electrical characteristics

Table 8. Static characteristics

V_{IN} = 3.6 V, V_{EN} = 3.6 V, R_{ST} = 36.5 kΩ pull-up resistor to 3.6 V, C_{OUT} = 0.33 µF unless otherwise specified.

Symbol	Parameter	Conditions	T_j = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Input						
$I_{IN,Q}$	input quiescent current	$V_{EN} = V_{IN}$	-	562	725	nA
$I_{IN,SD}$	input shutdown current	EN = LO	-	108	250	nA
Pass FET						
V_{FWD}	forward voltage drop	V_{IN} = 1.5 V; I_O= 50 mA	-	55	97	mV
		V_{IN} = 3.6 V; I_O= 100 mA	-	36	75	
		V_{IN} = 3.6 V; I_O= 500 mA [2]	-	62	100	mV
		V_{IN} = 3.6 V; I_O= 1000 mA [2]	-	119	180	mV
		V_{IN} = 5.5 V; I_O= 100 mA	-	40	70	mV
Reverse Current Blocking						
V_{RCBA}	RCB activation voltage	V_{OUT} - V_{IN}; ST pin goes from HI to LO	-	31	-	mV
V_{RCBD}	RCB deactivation voltage	V_{IN} - V_{OUT}; ST pin goes from LO to HI	-	41	-	mV
$I_{IN,LKGE}$	leakage current into IN, enabled	V_{OUT} = 4 V [2]	-220	331	615	nA
		V_{OUT} = 5 V	-220	332	615	nA
$I_{OUT,LKGE}$	leakage current into OUT, enabled	V_{OUT} = 4 V [2]	-200	372	1200	nA
		V_{OUT} = 5 V	-200	449	1200	nA
$I_{IN,LKGD}$	leakage current into IN, disabled	V_{OUT} = 4 V; EN = LO [2]	-500	-	500	nA
		V_{OUT} = 5 V; EN = LO	-500	-	500	nA
Enable iput						
$V_{EN,HI}$	enable high threshold	ST goes LO to HI	1.2	-	-	V
$V_{EN,LO}$	enable low threshold	ST goes HI to LO	-	-	0.4	V
$V_{EN,HYS}$	enable hysteresis		-	45	-	mV
$I_{EN,HI}$	enable input current	V_{EN} = 3.6 V	-	-	50	nA
Status pin						
$V_{OL,ST}$	status low threshold	ST pin sinking 100 µA	-	-	0.3	V
$I_{LKG,ST}$	status pin leakage current	EN = 3.6 V	-75	-	75	nA
Short Circuit Protection						
I_{LIM}	over current limit	R_L = 100 mΩ	-	2.8	-	A
Over Temperature Shutdown						
T_{OTSD}	overtemperature shut down	T_j rising [2]	170	175	-	°C
T_{OTHYS}	over temperature hysteresis	T_j falling [2]	-	35	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] *Not tested in production. Obtained by characterization.*

8.6. Dynamic characteristics

Table 9. Dynamic characteristics

V_{IN} = 3.6 V, R_{ST} = 36.5 kΩ pull-up resistor to 3.6 V, C_{OUT}= 1 µF, R_L = open unless otherwise specified.

Symbol	Parameter	Conditions	T_j = 25 °C			Unit
			Min	Typ	Max	
$t_{ON,ST}$	status ON delay time	EN = LO to HI step to ST = LO to HI step [1]	-	600	-	µs
$t_{OFF,ST}$	status OFF delay time	EN = HI to LO step to ST = HI to LO step [1]	-	45	-	µs
$t_{ON,DLY}$	turn-On delay time	V_{EN} = LO to HI step to V_{OUT} = 10 %	-	756	-	µs
t_{RISE}	rise time	V_{OUT} = 10 % to V_{OUT} = 90%	-	100	-	µs
t_{RCB}	reverse current blocking time	V_{OUT} = V_{IN}-100 mV to V_{IN} +100mV step to I_{IN} <1 mA [1]	-	8	-	µs
t_{LIM}	current limit response time	OUT shorted with 100 mΩ to I_{OUT} within 10% of I_{LIM} [1]	-	115	-	µs

[1] *Not tested in production. Obtained by characterization.*

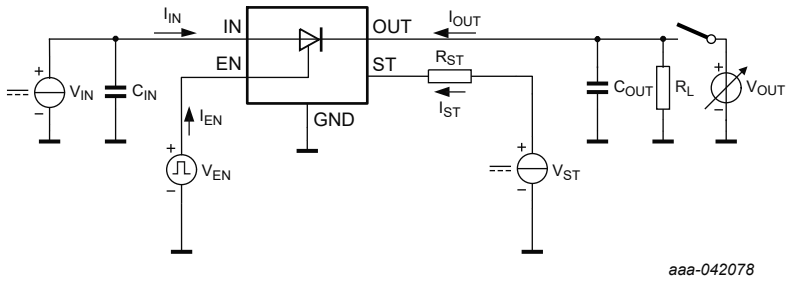


Fig. 5. Test circuit

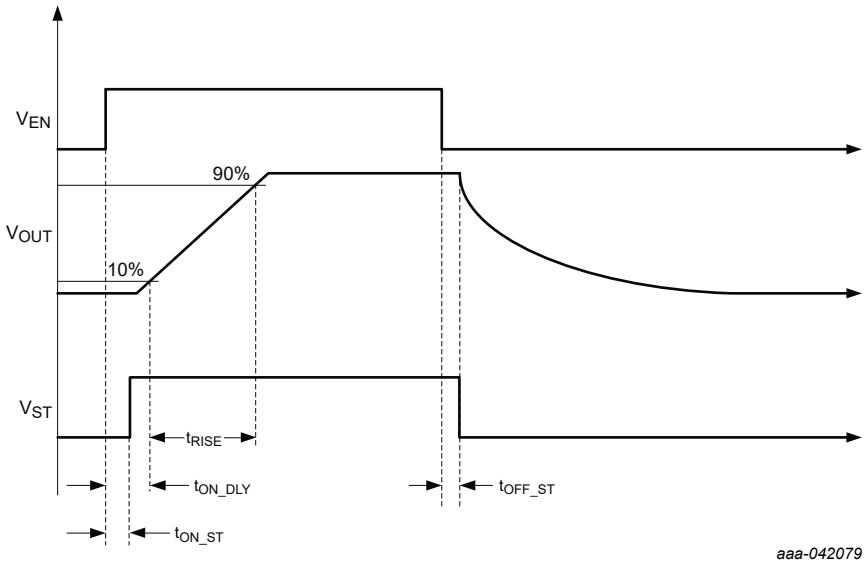
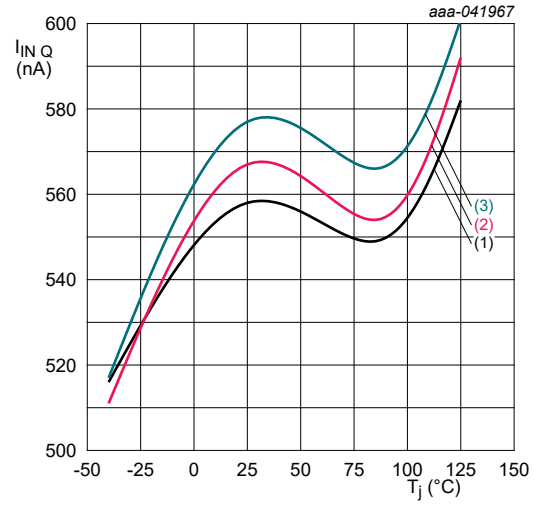


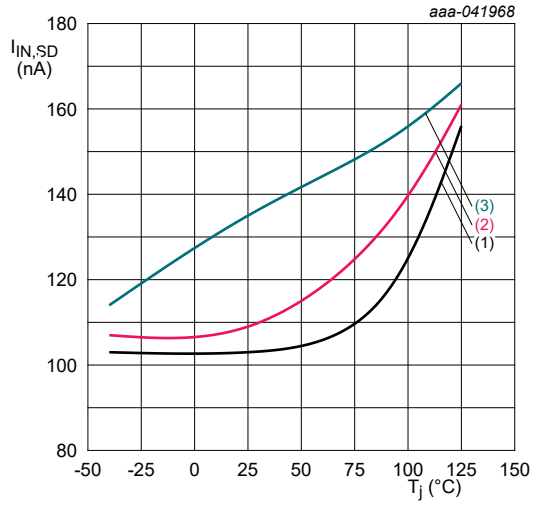
Fig. 6. Timing diagrams

8.7. Typical characteristics graphs



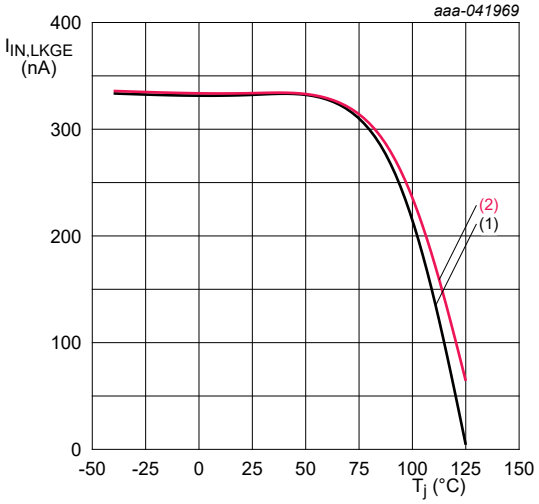
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.0 V

Fig. 7. Input quiescent current ($I_{IN,Q}$) versus junction temperature



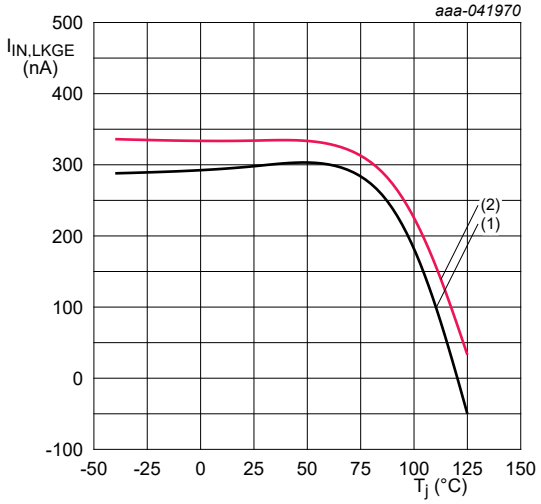
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.0 V

Fig. 8. Input shutdown current ($I_{IN,SD}$) versus junction temperature



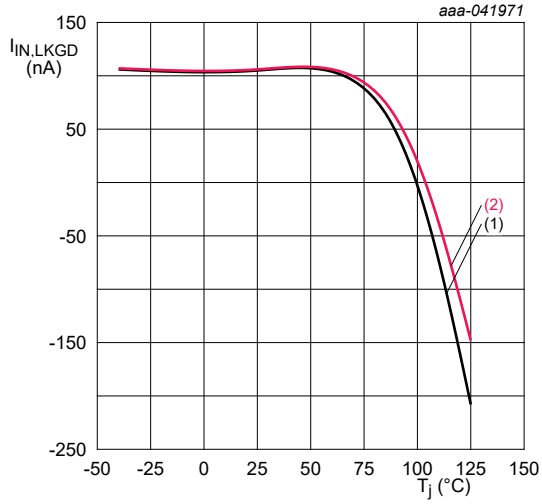
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V

Fig. 9. Input leakage current, enabled, ($I_{IN,LKGE}$) junction temperature at V_{OUT} = 4 V



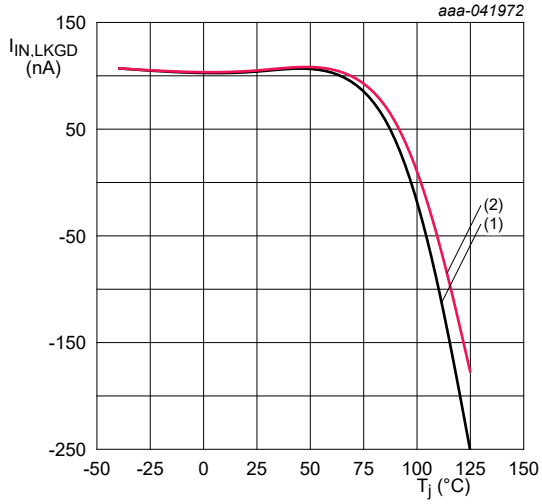
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V

Fig. 10. Input leakage current, enabled, ($I_{IN,LKGE}$) versus junction temperature at V_{OUT} = 5 V



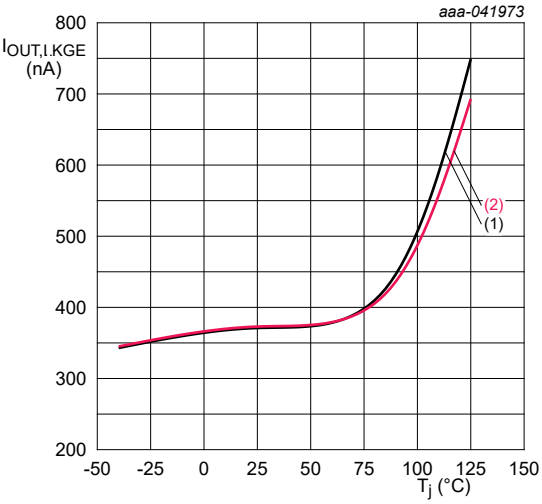
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V

Fig. 11. Input leakage current, disabled, ($I_{IN,LKGD}$) versus junction temperature at V_{OUT} = 4 V



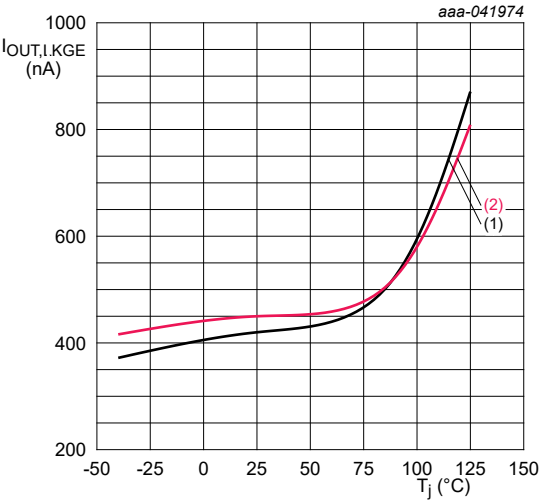
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V

Fig. 12. Input leakage current, disabled, ($I_{IN,LKGD}$) versus junction temperature at V_{OUT} = 5 V



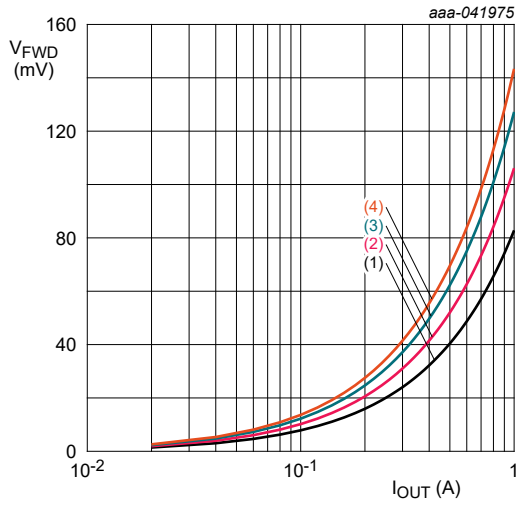
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V

Fig. 13. Output leakage current, enabled, ($I_{OUT,LKGE}$) versus junction temperature at V_{OUT} = 4 V



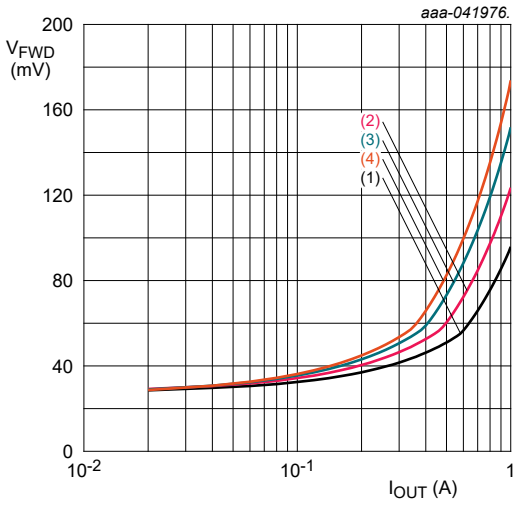
1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V

Fig. 14. Output leakage current, enabled, ($I_{OUT,LKGE}$) versus junction temperature at V_{OUT} = 5 V



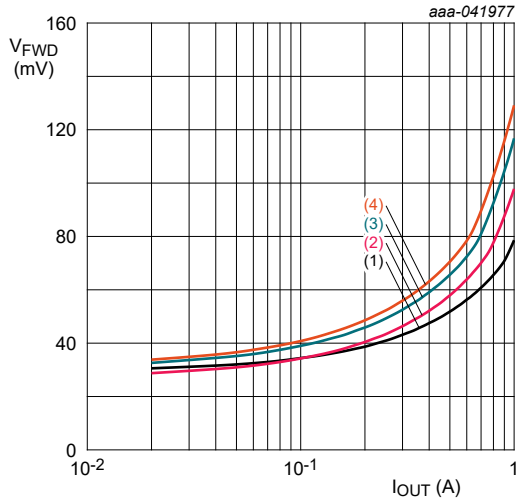
1) T_j = -40 °C
2) T_j = 25 °C
3) T_j = 85 °C
4) T_j = 125 °C

Fig. 15. Forward voltage drop versus load current at V_{IN} = 1.8 V



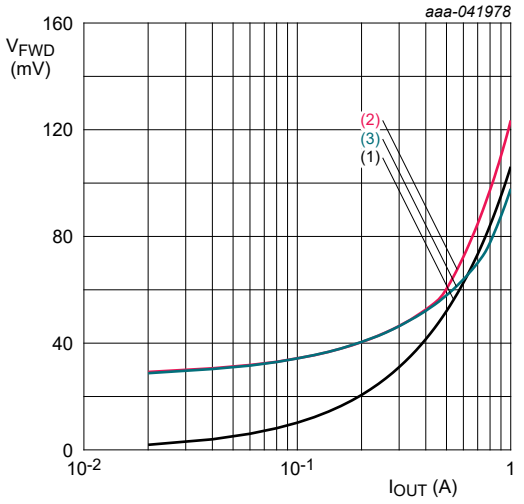
1) T_j = -40 °C
2) T_j = 25 °C
3) T_j = 85 °C
4) T_j = 125 °C

Fig. 16. Forward voltage drop versus load current at V_{IN} = 3.6 V



1) T_j = -40 °C
2) T_j = 25 °C
3) T_j = 85 °C
4) T_j = 125 °C

Fig. 17. Forward voltage drop versus load current at V_{IN} = 5.0 V



1) V_{IN} = 1.8 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.0 V

Fig. 18. Forward voltage drop versus load current at T_j = 25 °C

8.8. Typical characteristics graphs

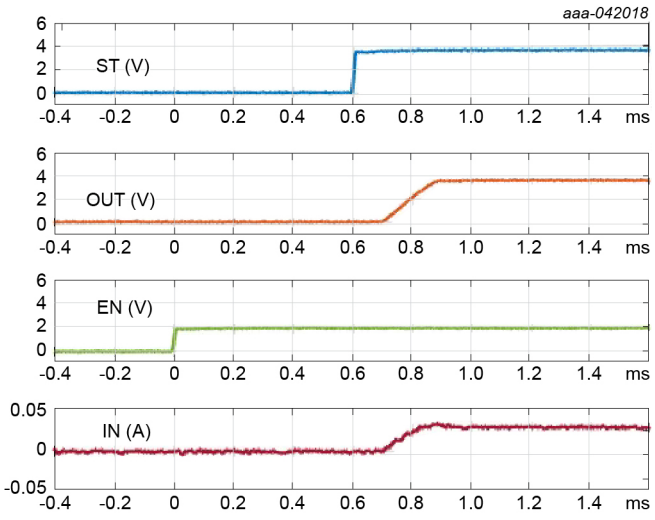


Fig. 19. Start-up with enable (R_L = 120 Ω)

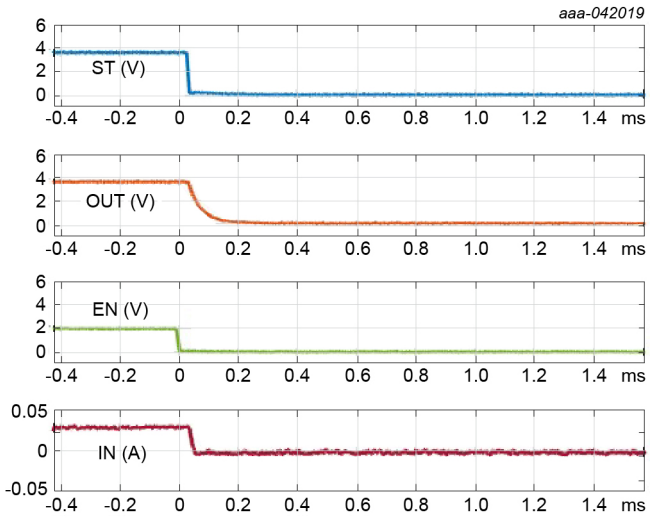


Fig. 20. Shutdown with Enable (R_L = 120 Ω)

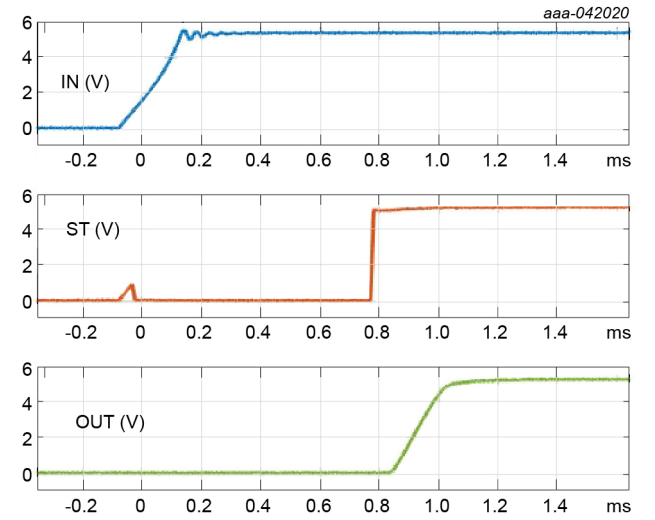


Fig. 21. Start-up with V_{IN} (V_{IN} ramp from 0 V to 5.5 V in 100 µs, EN tied to V_{IN}, R_L = 120 Ω)

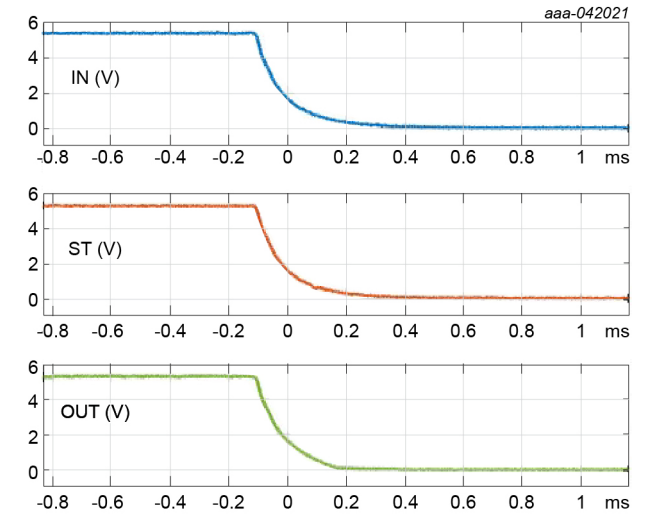


Fig. 22. Shutdown with V_{IN} (V_{IN} ramp from 5.5 V to 0 V in 100 µs, EN tied to V_{IN}, R_L = 120 Ω)

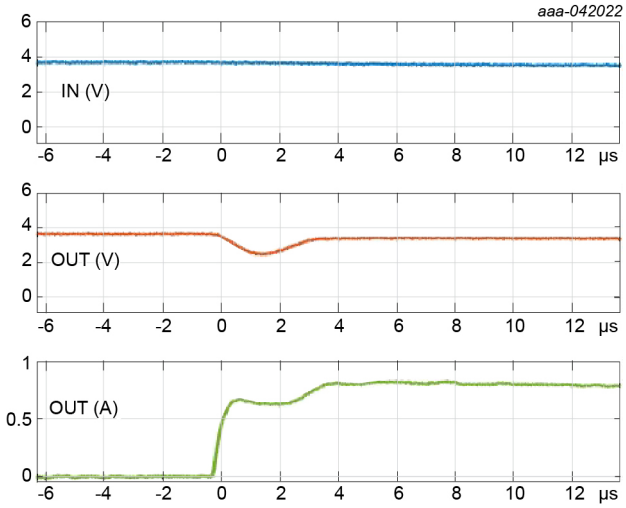


Fig. 23. Load step response (I_{OUT} step from 0 A to 0.75 A)

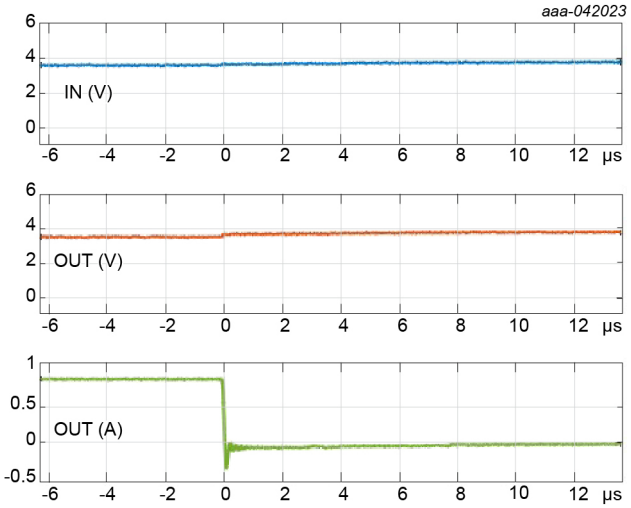


Fig. 24. Load step response (I_{OUT} step from 0.75 A to 0 A)

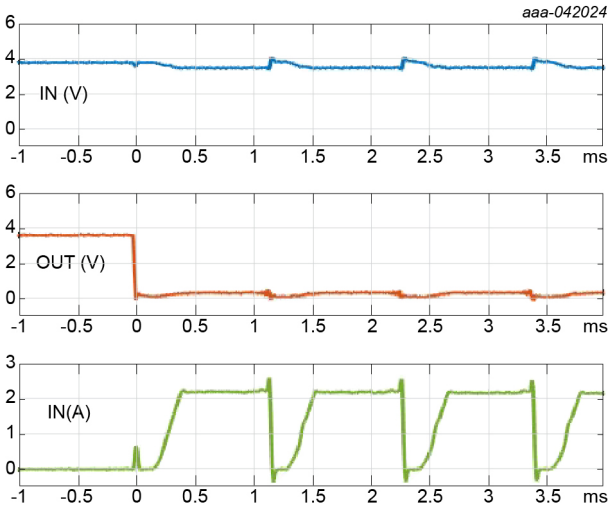


Fig. 25. Short circuit response (C_{IN} = 100 µF, output shorted with 0.1 Ω resistor)

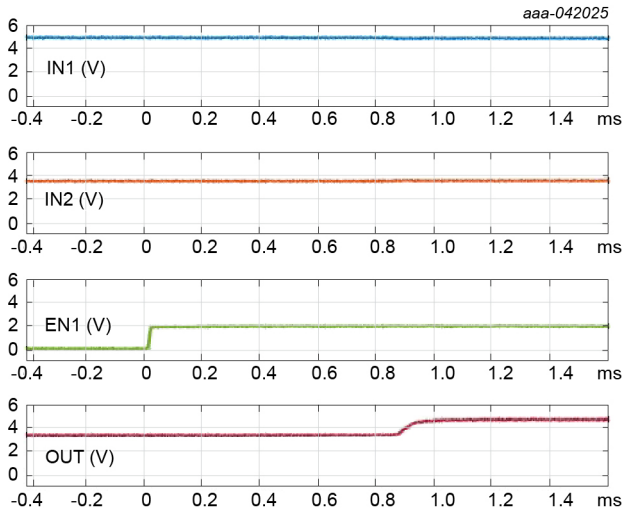


Fig. 26. OR-ing with enable (V_{IN1} = 5 V, V_{IN2} = 3.6 V; EN1 Low to High transition, EN2 tied to V_{IN2})

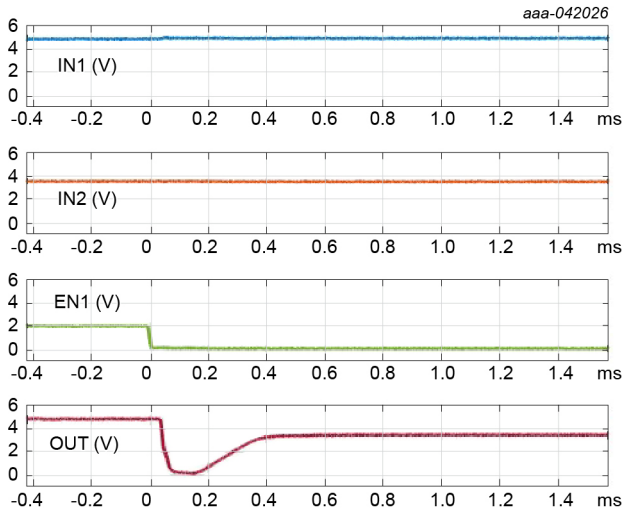


Fig. 27. OR-ing with enable (V_{IN1} = 5 V, V_{IN2} = 3.6 V; EN1 High to Low transition, EN2 tied to V_{IN2})

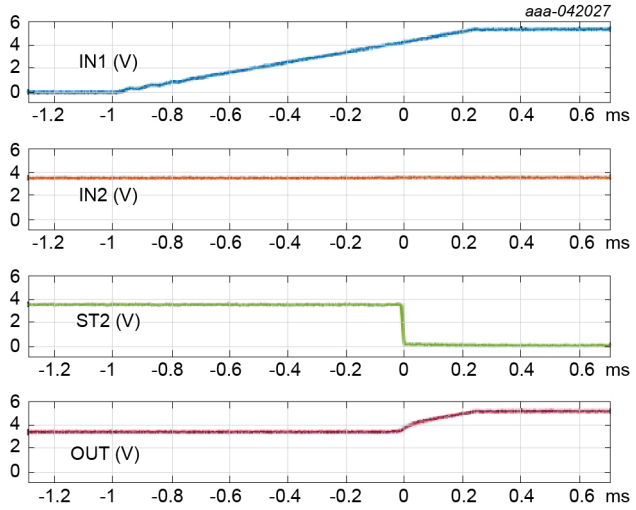


Fig. 28. FOR-ing with V_{IN} (V_{IN1} = 0 V to 5 V in 1 ms, V_{IN2} = 3.6 V; EN1 tied to V_{IN1}, EN2 tied to V_{IN2})

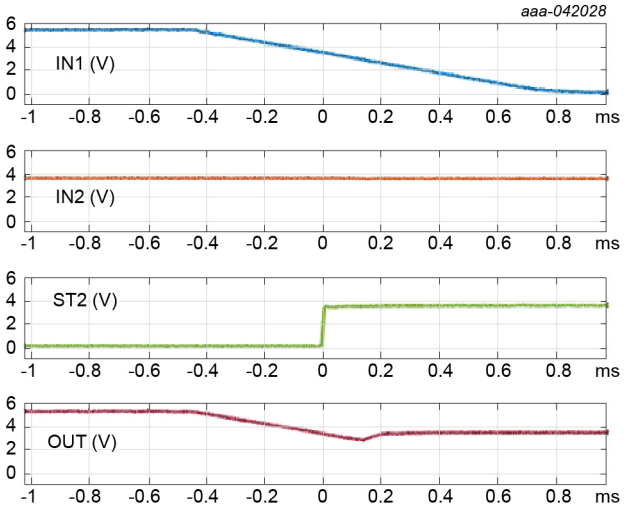


Fig. 29. OR-ing with V_{IN} (V_{IN1} = 5 V to 0 V in 1 ms, V_{IN2} = 3.6 V; EN1 tied to V_{IN1}, EN2 tied to V_{IN2})

9. Functional Description

9.1. Overview

NID1100 is a low voltage ideal diode capable of blocking voltages in either direction. It has integrated protection features like Inrush Current Limit, Reverse Voltage Blocking, and Over Temperature Protection. It comes in a small 5-pin SOT753 (SC-74A) package.

9.2. Startup

The device starts when the voltage at either IN or OUT pins reach 1.5 V. Until then, there is insufficient voltage to power up the internal circuitry.

When V_{IN} exceeds 1.5 V (and $V_{OUT} < V_{IN}$), the device enters Power-On-Reset (POR). In this situation, the switch is held OFF and the body diode is oriented such that the anode is at OUT and cathode is at IN. If EN pin goes high, the IC starts charging the output capacitor with an internally controlled slew rate. Once the capacitor is fully charged, the internal FET's gate is controlled by a transconductance amplifier to maintain a constant difference between V_{IN} and V_{OUT} to emulate a diode. If EN is pulled low at any time, the FET is turned OFF.

9.3. Functional modes

Table 10 summaries the various functional modes of the NID1100 and the status of the diode and the ST pin in each mode.

Table 10. Device functional modes ($V_{IN} \geq 1.5$ V)

Functional mode	EN pin	ST pin	Power device state
OFF	LOW	LOW	Forward blocking
ON	HIGH	High-Z	Forward conduction regulated V_{FWD}
Reverse current blocking	X	LOW	Reverse blocking
Output short	HIGH	High-Z	Forward conduction regulated I_{OUT}
Thermal fault	HIGH	LOW	Reverse blocking

The forward drop of the NID1100 depends on the input voltage and load current. Fig. 30 shows the internal block diagram of the NID1100 in forward regulation mode. Based on this figure, the drop seen between the IN and OUT pins (V_{FWD}) is given by the equation

$$V_{FWD} = I_{OUT} \times (R_{BW1} + R_{BW2}) + V_{FET}$$

where I_{OUT} is the load current, R_{BW1} and R_{BW2} are the bond wire impedances and V_{FET} is the voltage drop across the FET.

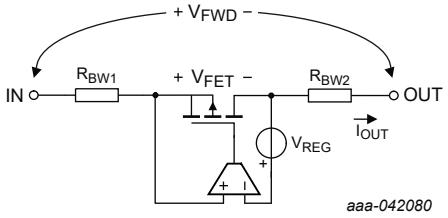


Fig. 30. NID1100 regulation scheme

The voltage drop across the FET is regulated to V_{REG} until the load current increases to a point where

$$I_{OUT} = \frac{V_{REG}}{R_{ON}}$$

Where R_{ON} is the resistance of the FET.

The overall variation of the forward voltage incorporating all these effects is shown in Fig. 31.

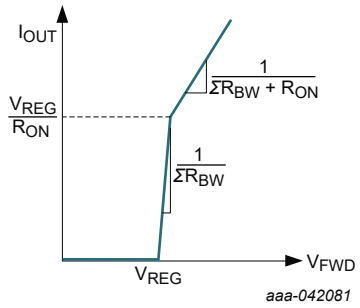


Fig. 31. NID1100 I-V curve

9.4. Reverse current blocking

Reverse Current Blocking (RCB) protection is always active, regardless of the state of EN. This protects the power supply from having to sink currents.

Two scenarios can activate the reverse current blocking functional mode.

- Output voltage starts rising and exceeds the input voltage (eg: OR-ing with two different voltage levels)
- Input voltage starts falling and goes below the output voltage (eg: loss of input power)

In either case, the NID1100 tries to maintain the forward drop between V_{IN} and V_{OUT}. As the V_{IN}-V_{OUT} differential starts reducing, the transconductance amplifier modulates the gate of the FET to increase its resistance to maintain the $V_{IN} – V_{OUT}$ differential. Once $V_{IN} \leq V_{OUT}$, the transconductance amplifier turns off the pass transistor and prevents reverse currents. An internal comparator detects when $V_{IN} \leq V_{OUT}$ - V_{RCBA} and flips the body diode polarity to ensure that the diode remains reverse biased.

When V_{IN} starts rising (or V_{OUT} starts falling) and V_{IN} exceeds V_{OUT} + V_{RCBD}, the diode polarity is flipped such that the anode is at IN and the pass FET starts conducting.

In case of an extremely fast transition from forward conduction to reverse bias, the comparator also acts to turn off the pass transistor before the transconductance amplifier has a chance to react.

9.5. Output overload and temperature protection

Unlike conventional diodes and other ideal diodes, the NID1100 is also protected from output short circuit and over temperature conditions. This is due to its unique feature of being able to block voltages in either direction.

When the output current exceeds I_{LIM}, the NID1100 limits the current through the device to I_{LIM}. It will stay in this current regulation mode until the output overload condition disappears or the junction temperature of the part exceeds T_{OTSD}.

Once an over temperature condition is detected, the NID1100 turns of the pass transistor. Once the NID1100 cools down such that $T_j < T_{OTSD} – T_{HYS}$, the part attempts restart in an inrush controlled manner.

10. Application information

Note: Application implementation information in the following sections is not part of the Nexperia component specification. Nexperia's device users are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The NID1100 ideal diode is a versatile device suitable for high side power switching, protecting against reverse current conditions, OR-ing and simple power multiplexing. The following sections provide application examples to aid the design of products using NID1100.

10.1. Startup

10.1.1. n+1 OR-ing using ideal diodes

There is no specific limitation to the number of NID1100 ideal diodes used for power OR-ing. The example below illustrates a common two power supply scenario with smooth transitions between supplies.

Some devices operate from a fixed power supply such as a standard 5 V USB port output in normal conditions but must quickly transition to a 3 V battery backup when the power supply is disabled or unplugged. Using two NID1100 devices in a power OR-ing configuration, the downstream load remains uninterrupted when either the DC supply or the backup battery are disconnected.

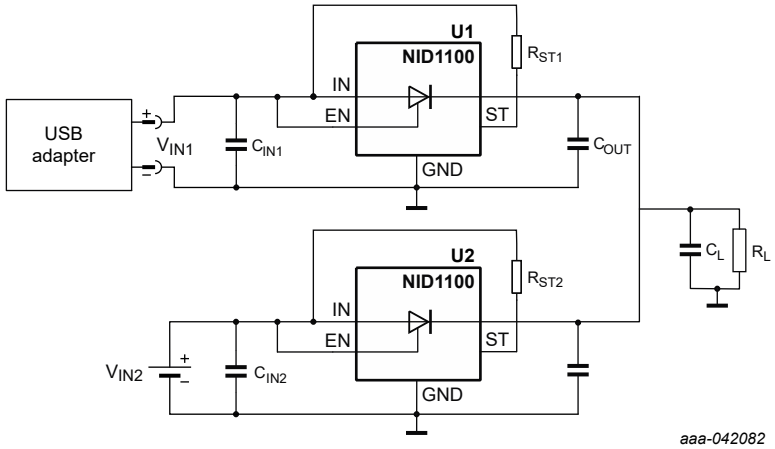


Fig. 32. OR-ing power supply and battery

The scope capture shows the output voltage (V_{OUT}) being initially powered by V_{IN1} at 5 V. When V_{IN1} is removed, V_{IN2} at 3.0 V powers V_{OUT}. When V_{IN1} is reconnected, V_{OUT} is once again powered by V_{IN1}. The ST pins of the NID1100's transition to indicate which ideal diode is supplying the load.

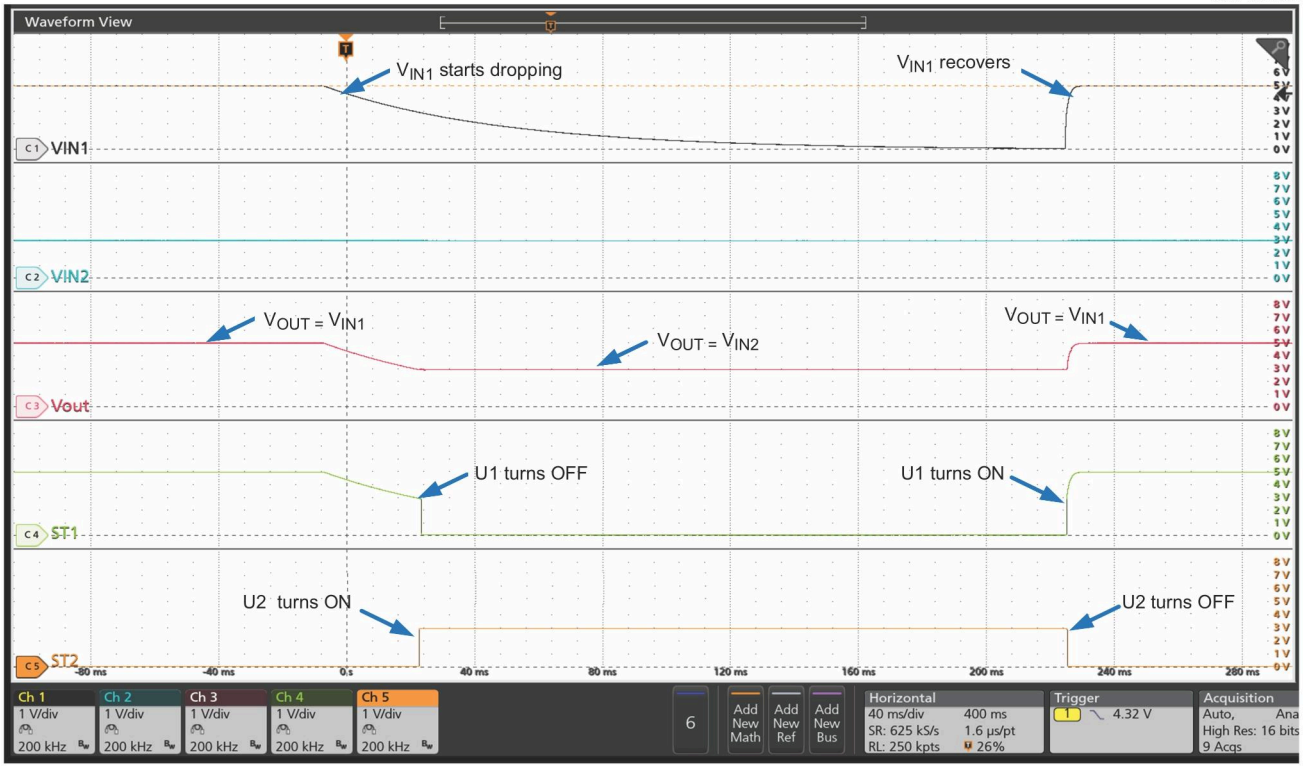


Fig. 33. Waveforms showing OR-ing behavior

10.1.2. OR-ing similar supply voltages

Some applications may require the OR-ing of supplies with similar voltages (eg: Fig. 34 and Fig. 35). In these examples, the primary DC supply is 3.3 V with a 3 V battery backup. Consider the scenario where V_{IN1}, which is initially supplying the load, is removed and subsequently restored.

In case of the OR-ing scenario with Schottky diodes, as the two supplies differ by only 300 mV, when V_{IN1} is restored, there may not be enough forward voltage, V_F, across the diode in the V_{IN1} path to forward bias it. Thus, V_{IN2} will continue to deliver power to the load until the battery voltage depletes sufficiently wasting energy in the backup source.

In case of the OR-ing scenario with NID1100s, when V_{IN1} is restored, the reverse current blocking deactivation threshold, V_{RCBD}, is easily exceeded allowing the 3.3 V supply to carry the full load. As the OUT is approximately 300 mV above V_{IN2}, the 3 V supplied NID1100 becomes reverse biased and the battery drain is minimized.

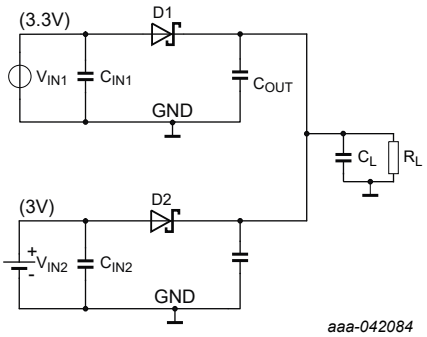


Fig. 34. OR-ing with Schottky diodes

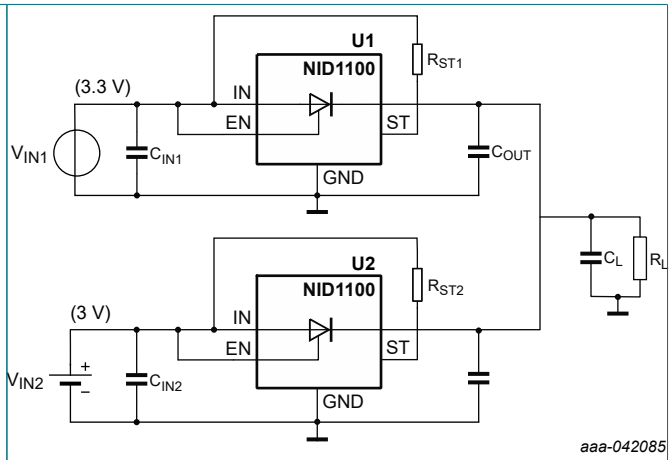


Fig. 35. OR-ing with NID1100

10.1.3. n+1 OR-ing using ideal and conventional diodes

When voltage drops and electrical losses of one of two power sources is not of concern, a combination of ideal diodes and conventional diodes can be implemented as shown in Fig. 36. In this example the AC-DC adapter is the primary power source supplying 5 V to the system with three alkaline cells providing a 4.5 V backup. As stated in Section 8.5, consideration should be given to the V_F rating of the Schottky diode as well as worst case tolerances of the supply voltages to ensure seamless transitions.

A resistor, R_{PD}, connected to ground in the Schottky diode path is recommended to prevent diode reverse leakage during blocking conditions from charging C_{IN1} and raising V_{IN1}.

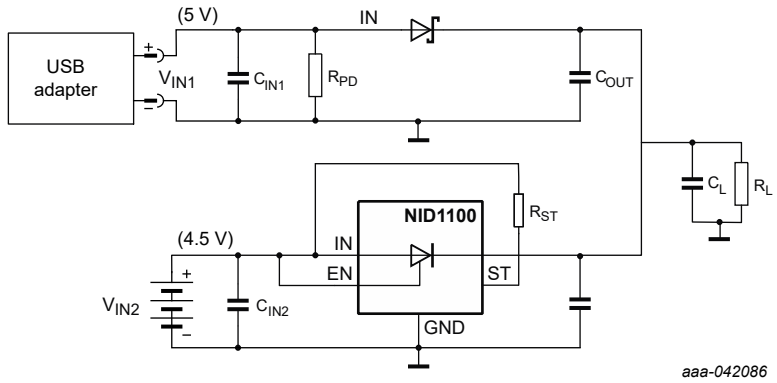


Fig. 36. OR-ing behavior with a combination of ideal and Schottky diodes

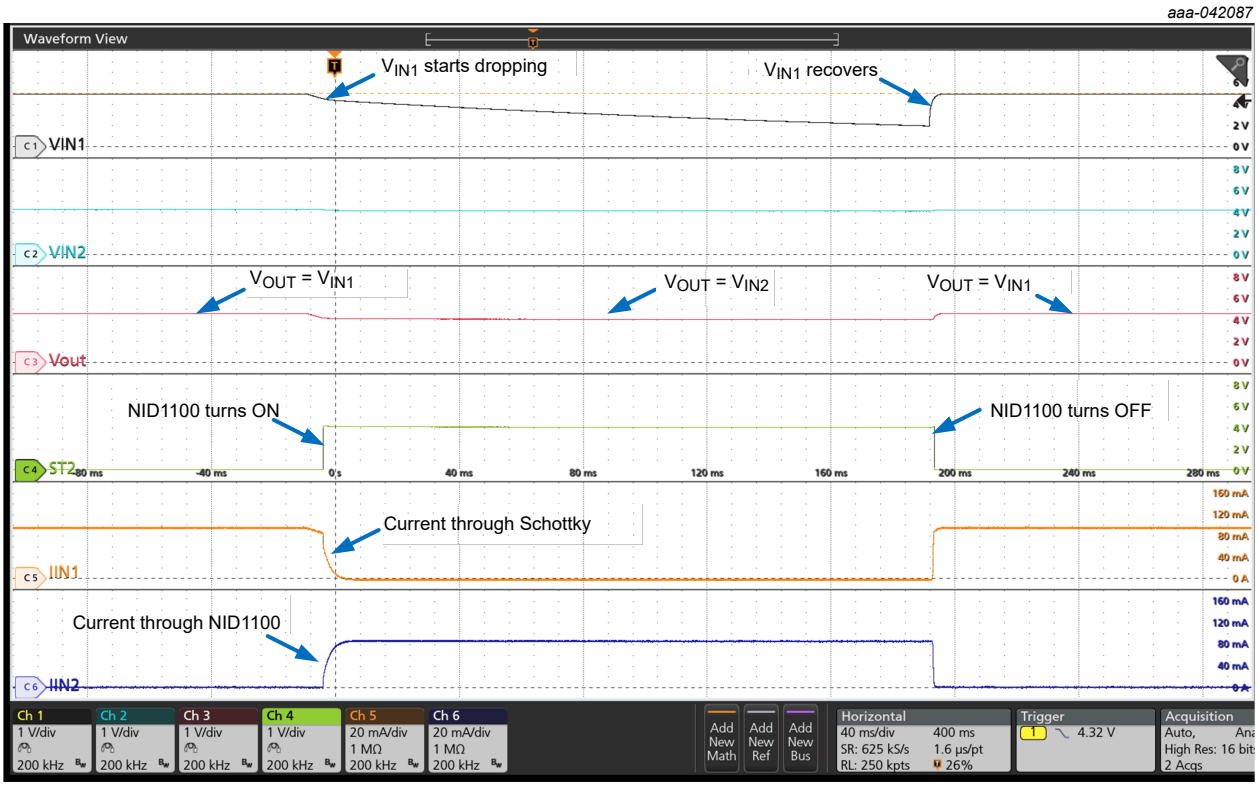


Fig. 37. Waveforms showing OR-ing behavior with a combination of ideal and Schottky diode (PMEG4010)

10.1.4. Paralleling NID1100 for thermal and sustained high current considerations

As with using any power semiconductor component, thermal ratings must be observed to maintain device reliability. Refer to the Section 8.4 table. System thermal analysis should be performed to ensure the device junction temperature, T_J, remains below 125 °C under all operating conditions. If analysis shows that using a single NID1100 would cause a thermal violation, two NID1100s can be paralleled to share the load current and lower internal power dissipation as shown in Fig. 38. Fig. 39 shows two NID1100's supporting a combined 2 A load current with 1 A current flowing in each NID1100.

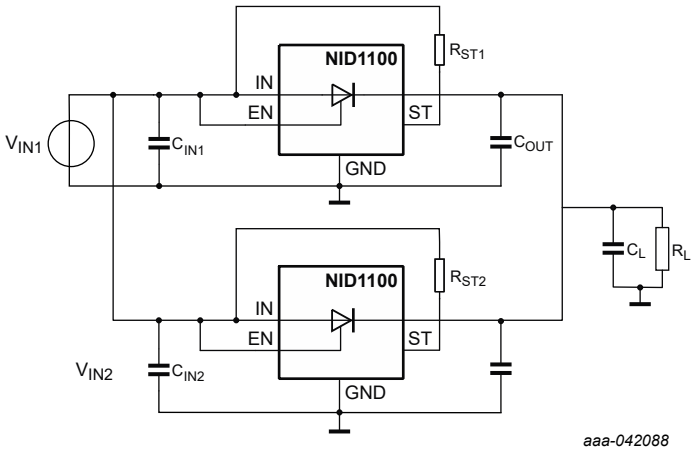


Fig. 38. Paralleling two NID1100 ideal diodes for high current

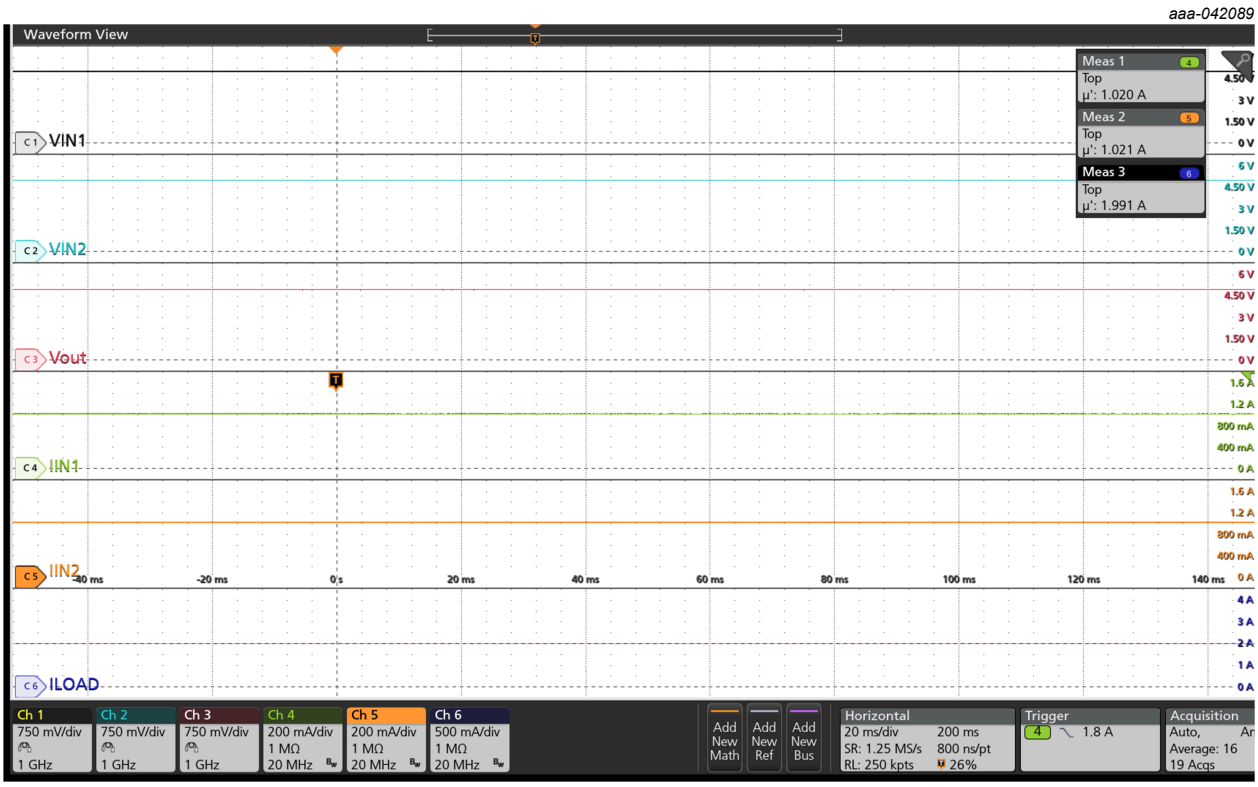


Fig. 39. Waveforms showing paralleling of two NID1100s

10.1.5. Power multiplexing and load switching

Because the NID1100 has forward voltage blocking, it is possible to use a single device as a high side load switch with short circuit protection or multiple devices for power multiplexing. Fig. 40 depicts an application example that can be used to switch between an USB-PD source, a wall wart and a Li-ion battery.

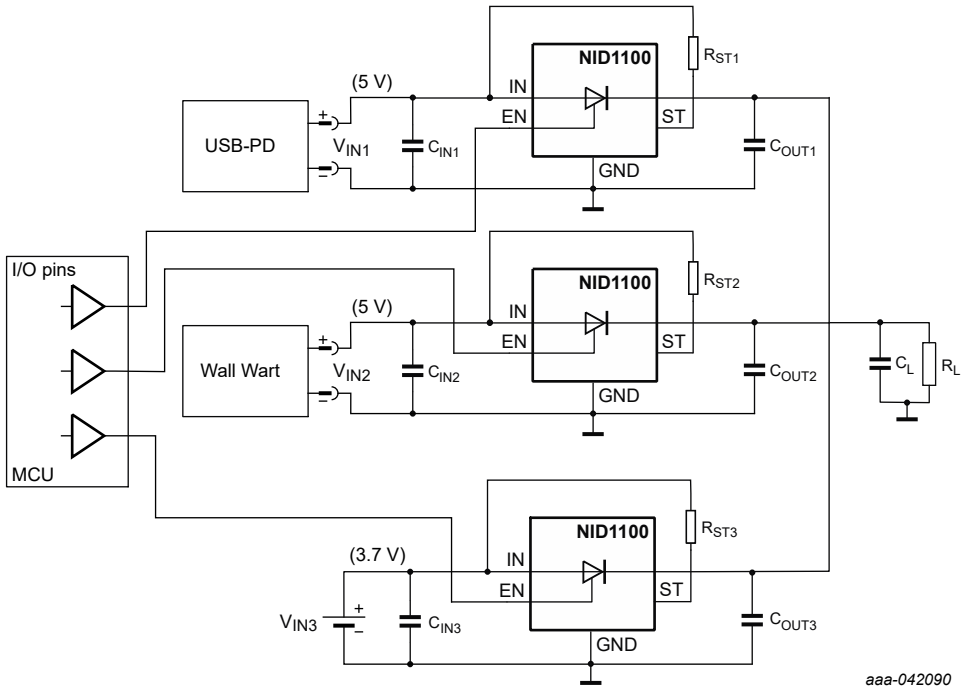


Fig. 40. Power multiplexing and load switching

10.1.6. OR-ing with discrete MOSFET

In this application, the EN pin of the NID1100 is always connected to V_{IN1} “enabling” the device. When both the 5 V and 3.3 V supplies are present, OUT is initially 5 V and the ST pin is high-Z with the R_{ST1} resistor pulled up to V_{IN1}, keeping the gate of the external PFET high.

- If V_{IN1} is quickly removed, the ST pin output will transition low, enhancing the external PMOS. The load is then supplied from V_{IN2}.
- If V_{IN1} is a slowly discharging battery, OUT will transition from being supplied by the NID1100 OUT pin to being supplied by the external PMOS when V_{IN1} decreases below V_{IN2} by $V_{FWD(ext\_PMOS)}$.
- Conversely, if V_{IN1} is slowly recharged, OUT will be supplied from the PMOS until $V_{IN1} + V_{REG} \geq V_{IN2} + V_{RDSON(ext\_PMOS)}$

Note: The supply to the NID1100 (V_{IN1}) should be the higher of the two supplies when both V_{IN1} and V_{IN2} are present. Fig. 42 shows the switchover performance between V_{IN1} and V_{IN2}. A resistor, R_{PD}, to ground is recommended to prevent any reverse leakage from charging the 3.3 V C_{IN2} capacitor and raising the V_{IN2} voltage in the event the 3.3 V supply is disconnected.

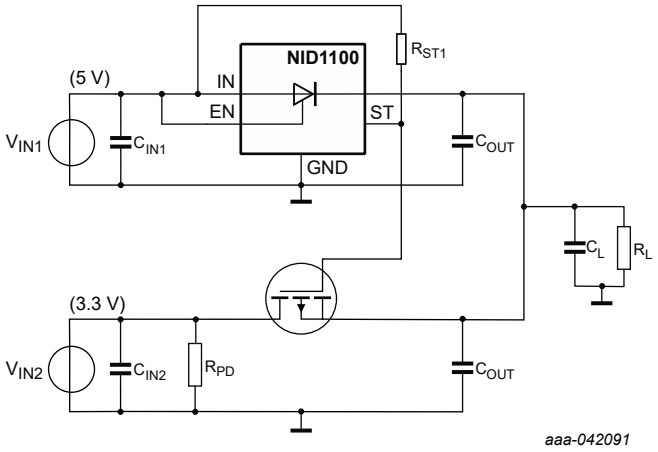


Fig. 41. OR-ing with external PMOS

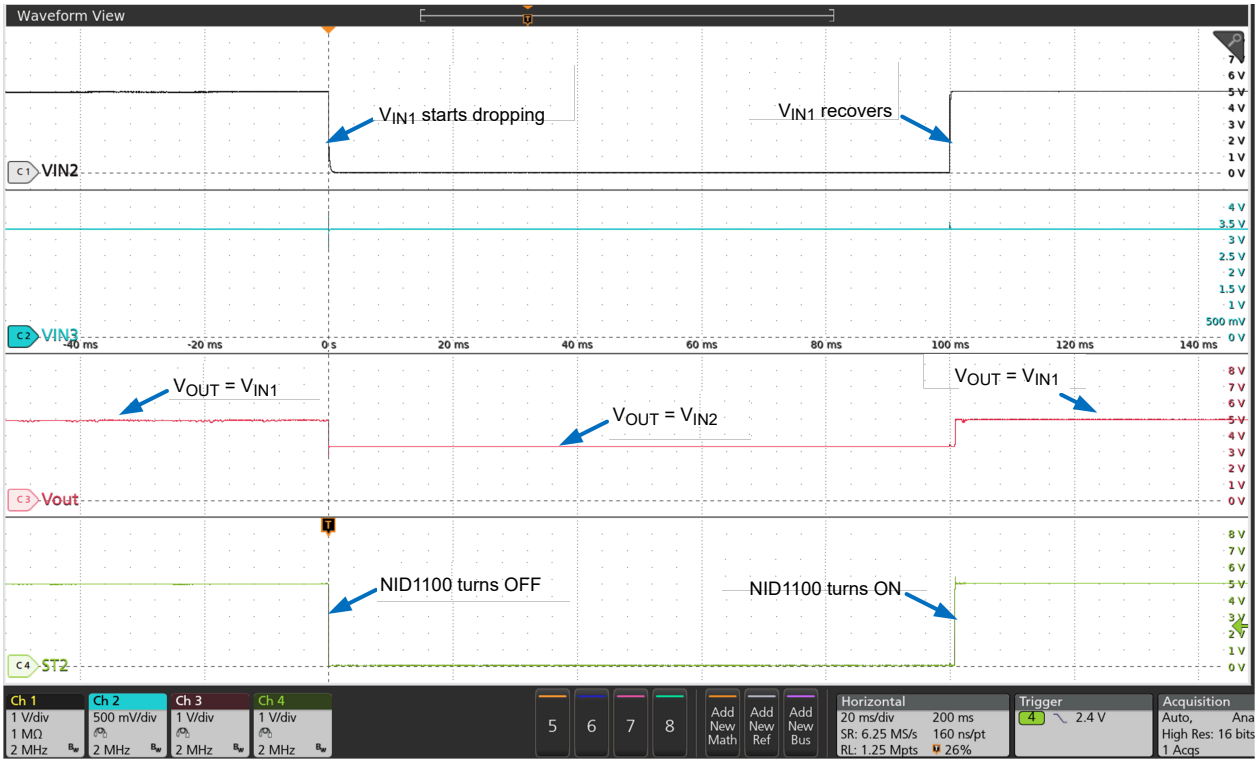


Fig. 42. Waveforms showing switchover from V_{IN1} (5 V) to V_{IN2} (3.3 V) and back to V_{IN1} (5 V)

10.2. Thermal characteristics and power dissipation

The junction temperature of a semiconductor device is determined by the internal power dissipation and its capacity to dissipate heat to the surrounding environment. The electronic equivalent is shown in Fig. 43.

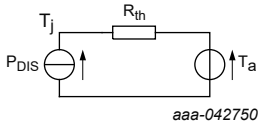


Fig. 43. Thermal diagram

From the diagram, the formula for calculating the junction temperature can be derived as follows:

$$T_j = P_{DIS} \times R_{th} + T_{amb}$$

Where T_j is the junction temperature, P_{DIS} is the power dissipation, R_{th} is the thermal resistance, and T_{amb} is the ambient temperature.

The internal power dissipation is given by:

$$P_{DIS} = I_{OUT} \times (V_{IN} - V_{OUT})$$

Where I_{OUT} is the output current, V_{IN} is the input voltage, and V_{OUT} is the output voltage.

It is a characteristic of semiconductor devices that power losses increase with rising temperatures. Operating the device above the specified maximum junction temperature of 125°C can lead to thermal runaway due to these increased losses, thereby reducing the device's lifespan or triggering thermal protection.

The aforementioned equations can be used to estimate the junction temperature for a given application. To verify the actual junction temperature, the specified Ψ_{JT} value can be used in conjunction with the measured top package temperature:

$$T_j = \Psi_{JT} \times P_{DIS} + T_{TOP}$$

where T_{TOP} is the top surface temperature of the package.

10.3. PCB Layout

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT} and GND helps minimize the parasitic electrical events.

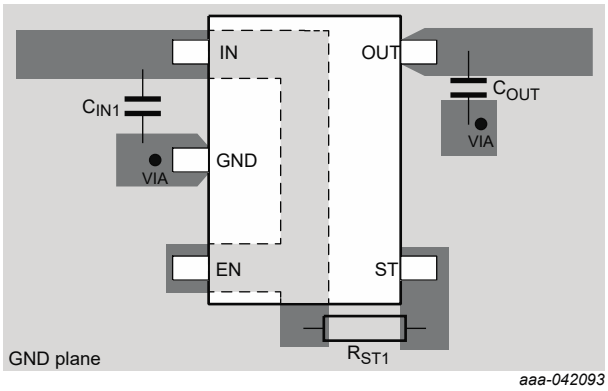
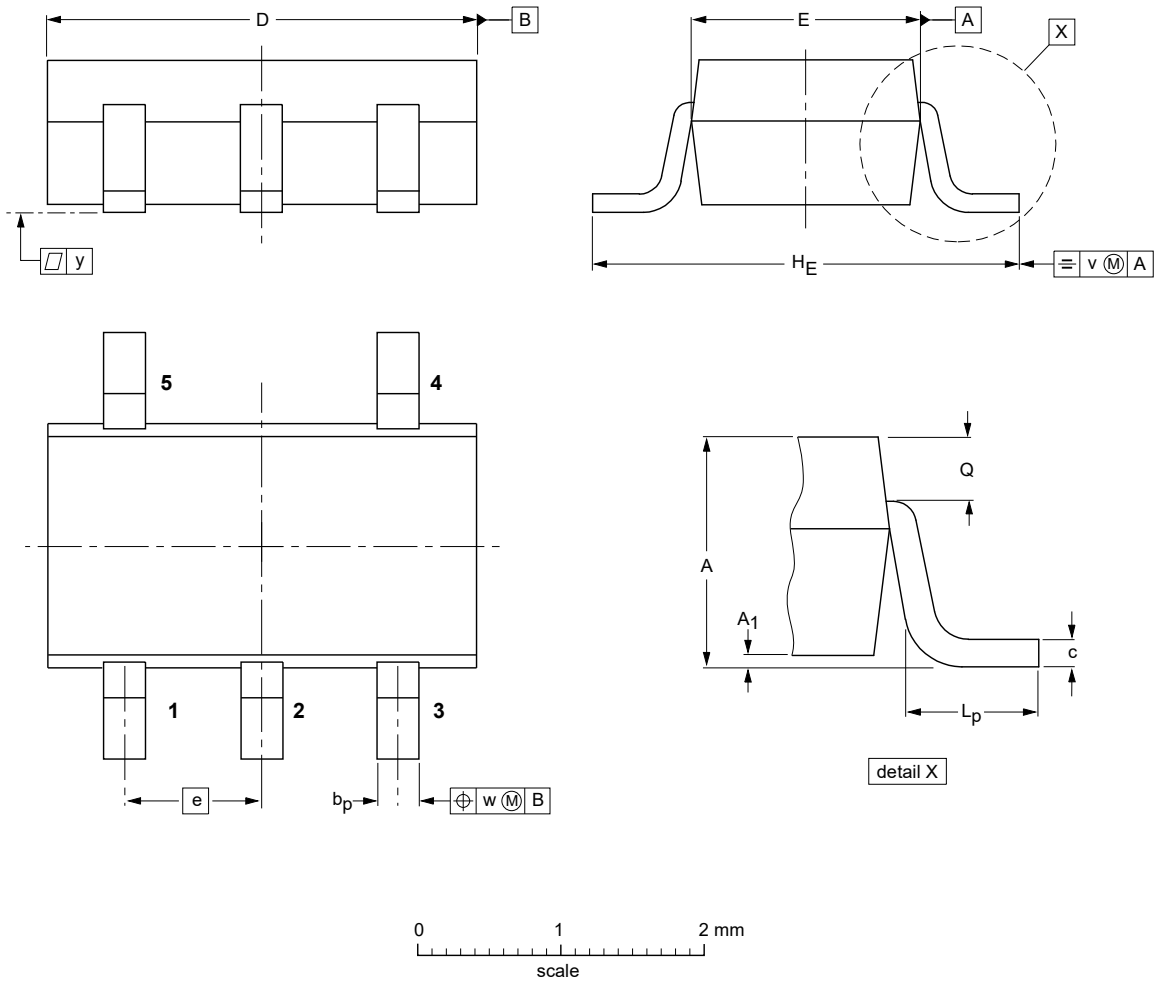


Fig. 44. PCB layout

11. Package outline

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 45. Package outline SOT753 (SC-74A)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
IEC	International Electrotechnical Commission
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide Semiconductor

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NID1100 v.2	20250317	Product data sheet	-	NID1100 v.1
Modifications:	• Section 9.3: Typo corrected in equation. • Fig. 40 moved to Section 10.1.5 and Section 10.2 updated.			
NID1100 v.1	20250120	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 17 March 2025