NIS6201

Floating, Regulated Charge Pump

The NIS6201 charge pump is designed to provide economical, low level power to circuits above ground level potential, such as the drive for ORing diodes. It is a very cost−effective replacement for a small, isolated, switching power supply.

It contains an internal linear regulator, and a versatile charge pump to allow bias voltage supplies to be transferred from a ground referenced source to a higher potential. The design of the charge pump allows for any isolation voltage required, as the high voltage components are external to the pump and can be sized accordingly.

Features

- Integrated Linear Regulator and Charge Pump
- Thermal Limit Protection
- Adjustable Voltage Output
- High Voltage Isolation
- This is a Pb−Free Device

Applications

- ORing Diodes
- Floating Supervisory Circuits
- LED Driver

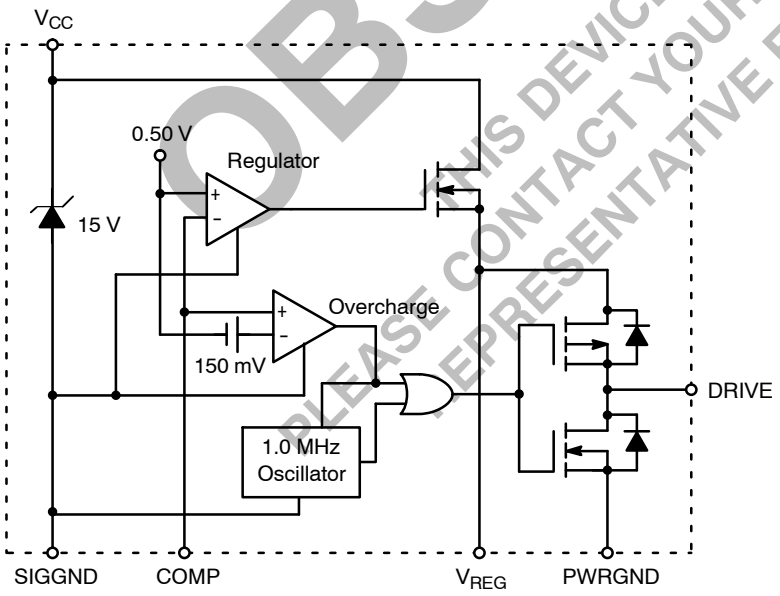

Figure 1. Charge Pump Block Diagram

ON Semiconductor®

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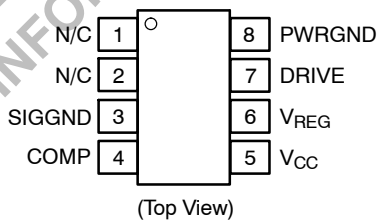
MARKING DIAGRAM

6201	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NIS6201DR2G	SOIC−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2	N/C	No connection.
3	SIGGND	Ground reference pin for control circuits. This should be connected to power ground on the PCB.
4	COMP	The feedback and compensation network of the linear regulator are connected to this pin.
5	V_{CC}	Input power to chip. There is an internal clamp at 15 V to allow for a shunt regulator circuit on this pin for high voltage inputs.
6	V_{REG}	This is the regulated output of the internal linear regulator.
7	DRIVE	Output drive of oscillator, that drives external diode/capacitor network.
8	PWRGND	Ground reference pin for driver current.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, Operating (Note 1)	V_{CC}	−0.3 to 15	V
Comp pin Voltage	V_{comp}	4.5	V
Drive Current, Peak	I_{Dpk}	3.0	A
Drive Current, Average	I_{Davg}	0.05	A
Thermal Resistance, Junction−to−Air Min copper area 1 in^2 copper (1 oz, single sided)	Q_{JA}	 175 114	°C/W
Thermal Resistance, Junction−to−Lead (Pin 1)	Q_{JL}	41	°C/W
Power Dissipation @ T_A = 25°C Min copper area 1 in^2 copper (1 oz, single sided)	P_{max}	 .57 .88	W
Operating Temperature Range	T_J	−40 to 125	°C
Non−operating Temperature Range	T_J	−55 to 150	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Above this voltage, a series resistor is necessary to limit current into the shunt regulator.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 15 V, V_{reg} = 12 V, DRIVE Pin open, T_J = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency	f_{osc}	0.9	1.3	1.45	MHz
DRIVER					
On Resistance, High Side FET	$R_{DSon(hi)}$	–	9.5	–	Ω
On Resistance, Low Side FET	$R_{DSon(low)}$	–	9.5	12	Ω
LINEAR REGULATOR					
Reference Voltage, Pin 4 T_J = −40 to 125°C	V_{ref}	490 475	500 505	510 525	mV
Headroom (V_{CC}–V_{reg}) V_{CC} = 7 V, I_{drive} = 10 mA	V_{head}	–	155	220	mV
TOTAL DEVICE					
Minimum Operational Input Voltage	V_{min}	7.0	–	–	V
Bias Current (Operational)	I_{Bias}	–	3.6	4.6	mA
Bias Current (COMP Pin = 600 mV)	I_{Bias_SD}	–	3.0	3.6	mA
V_{CC} Zener Breakdown Voltage	V_{Zener}	14.5	15	–	V

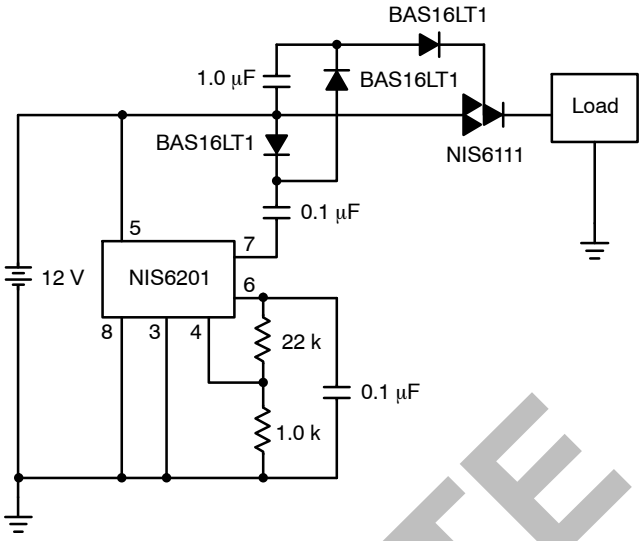


Figure 2. Application Circuit with Better ORing Diode

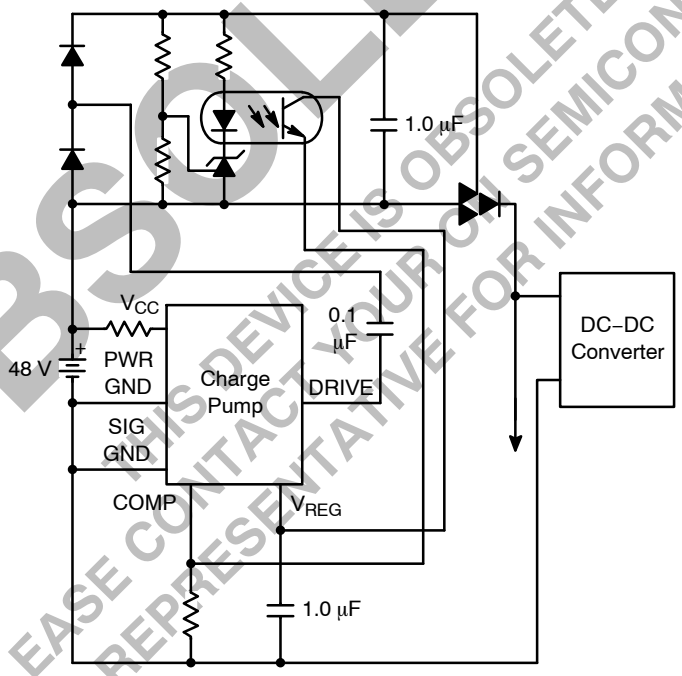


Figure 3. Application Circuit for Improved Regulation and Transient Response

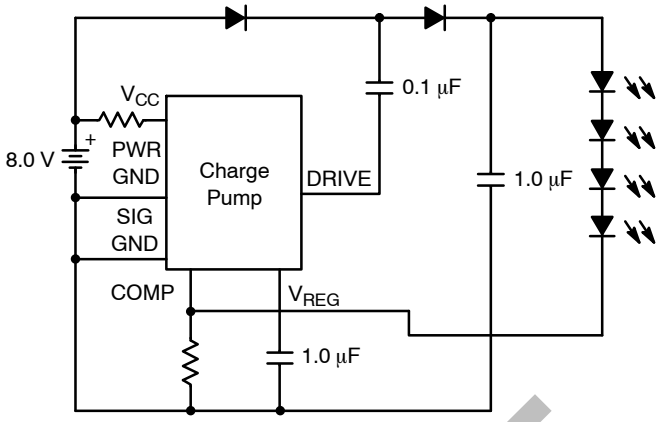


Figure 4. Current Regulated, Voltage Doubler

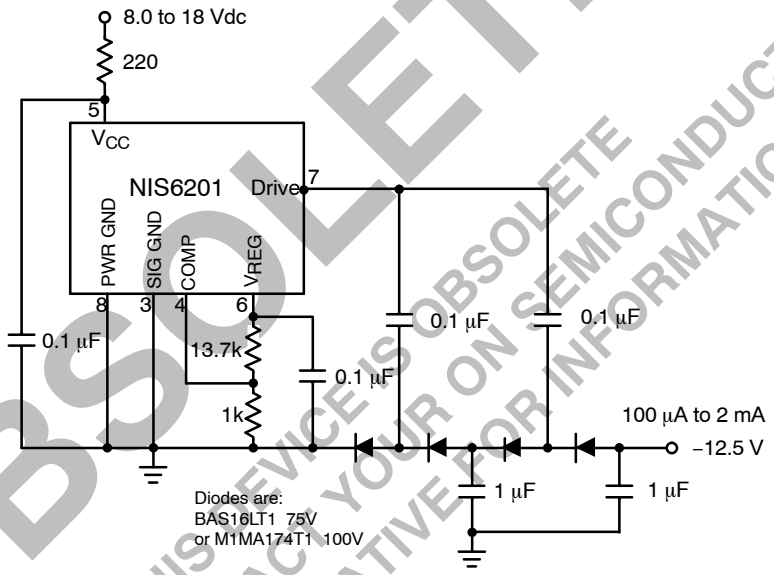


Figure 5. Regulated, Negative Doubler Circuit

OPERATING DESCRIPTION

DC Input

The Vcc pin is rated for a maximum dc voltage of 15 volts. An internal shunt diode is included for applications where the voltage may exceed 15 volts. For voltages greater than 15 volts an external shunt resistor must be added in series with the Vcc pin. This resistor must be sized such that at low line, the voltage drop across it will allow for an input voltage of greater than that of the output of the LDO and at high line such that the current into the chip does not exceed its power rating.

LDO

The internal LDO contains a P−Channel FET and error amplifier with a 0.5 volt reference. A voltage divider is required from the Vreg pin to the comp pin to set the output of the LDO. This output voltage (Vreg) is the voltage used for the charge pump oscillator. The divider can be calculated from the following formulas:

$$R_{bias} = 0.50 \frac{V}{I_{bias}}$$

Ibias is generally in the range of 100 μA to 1 mA and sets the bias current in the divider.

$$R_{set} = \frac{R_{bias}(V_{reg} - 0.50\ V)}{0.50\ V}$$

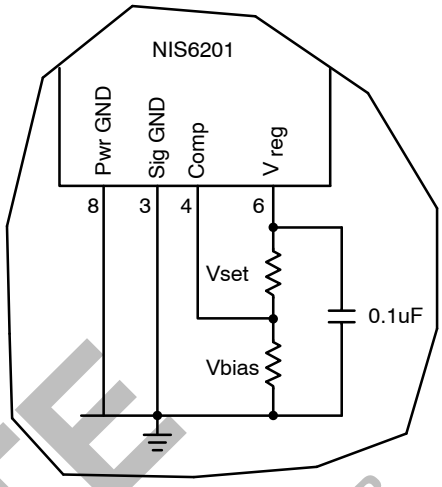


Figure 6. Bias Voltage Divider

Overcharge Comparator

The overcharge comparator provides a protection function from an overvoltage condition at turn−on.

Figure 7 shows a typical configuration for this charge pump. At turn−on there is a voltage divider consisting of two capacitors and two diodes. If this device is being operated at voltages significantly above the Vreg level, it is possible to charge the Vreg cap well beyond its intended level.

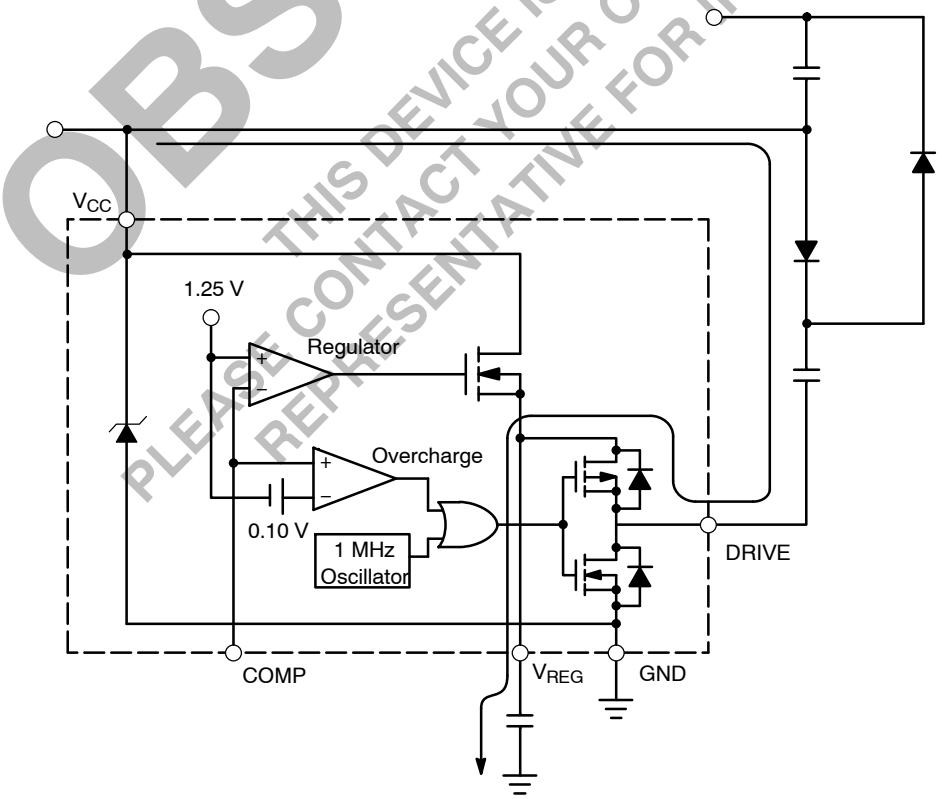


Figure 7. Overcharge Circuit

The overcharge comparator detects when the voltage at Vreg is 10% greater than its set level. If this situation occurs, the overcharge circuit overrides the oscillator and turns on the bottom FET of the driver stage. This shunts the start−up current directly to ground and bypasses the capacitor on Vreg thus allowing for safe start−ups at high input voltages.

Oscillator

The oscillator in this chip operates at a nominal frequency of 1 MHz. The FETs have an on resistance of 20 Ω and can drive loads in excess of 20 mA. Since the charge diodes and capacitors are external, this device can drive a "floating" voltage that is referenced to the input bus such as is shown in Figure 7. The "isolation" voltage for the regulated output is limited only by the ratings of these external components. The oscillator can also drive a conventional voltage doubler circuit or an inverting output stage.

Total Power Consumption

The SO−8 package used for this chip has a power rating of 570 milliwatts. The major losses in this device come from three circuits plus the bias current. These are the following:

Shunt Diode

The power dissipated in this diode is due to the current through the input series resistor when the input exceeds 15 volts. The current in the diode is the current through the input resistor less the output and bias currents in the chip. The output current is equal to the load current unless multiple pump stages are used in which case it is multiplied by the number of stages in use. An additional 2 mA of bias current is required to operate the charge pump.

$$P_{shunt\ diode} = V_{CC} \cdot \left[\left(\frac{(V_{in} - V_{CC})}{R_{series}}\right) - 2\ mA - (I_{out} \cdot n_{stages})\right]$$

LDO

The power lost in the LDO pass transistor is calculated by the voltage drop across it and the current through it. As was the case with the shunt diode, when calculating the load current, the number of pump stages must be accounted for.

$$P_{LDO} = (V_{CC} - Vreg) \cdot (2mA + (Iout \cdot n_{stages}))$$

Oscillator

The power dissipated in the oscillator section can be approximated by multiplying the square of the load current by the typical on resistance.

$$P_{Osc} = Iout^2 \cdot 20\ \Omega$$

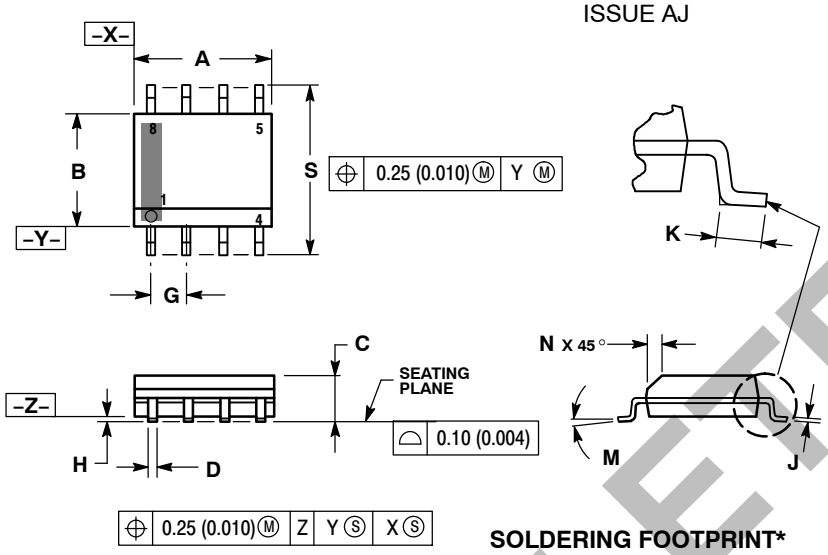
Bias Current

The bias current is simply the input voltage at the Vcc pin multiplied by 2 mA.

The total power dissipated by the chip is the sum of these four losses. If the input voltage does not exceed 15 volts, the shunt diode losses can be ignored. The sum of these losses should not exceed the power rating for the device. Note that the power rating is specified at 25°C and must be derated at higher operating temperatures.

PACKAGE DIMENSIONS

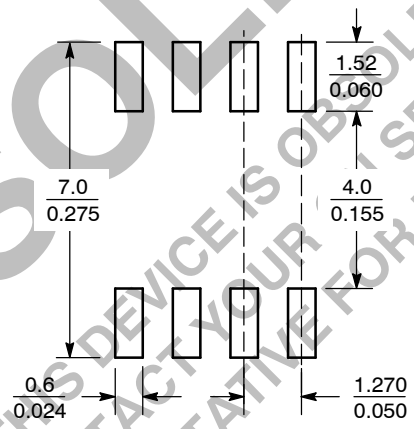
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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