UHF BAND LOW NOISE AMPLIFIER GaAs MMIC

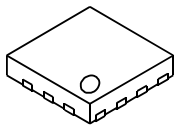
■ GENERAL DESCRIPTION

The NJG1129MD7 is a low noise amplifier GaAs MMIC designed for mobile digital TV application (470~770 MHz).

This IC has a LNA pass-through function to select high gain mode or low gain mode by single bit control.

Also, the ESD protection circuit is integrated into the IC to achieve high ESD tolerance.

■ PACKAGE OUTLINE



NJG1129MD7

■ APPLICATIONS

Wide band application from 470MHz to 770MHz
Mobile TV and Digital TV applications
Mobile phone and tablet PC applications

■ FEATURES

- Low voltage operation +2.8V typ.
- Low voltage control +1.85V typ.
- Package EQFN14-D7 (Package size: 1.6mm x 1.6mm x 0.397mm typ.)

[High gain mode]

- Low current consumption 5.0mA typ.
- High gain 15.0dB typ.
- Low noise figure 1.4dB typ.
- High input IP3 +1.0dBm typ.

[Low gain mode]

- Low current consumption 16μA typ.
- Gain -4.0dB typ.
- High input IP3 +20.0dBm typ.

■ PIN CONFIGURATION

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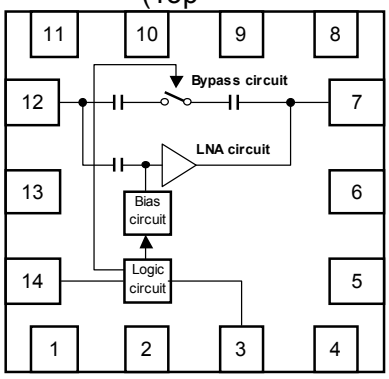


Pin Connection

1. GND	8. GND
2. GND	9. GND
3. VINV	10. GND
4. GND	11. GND
5. GND	12. RFIN
6. GND	13. GND
7. RFOUT	14. VCTL

* Exposed PAD: GND

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

V_{CTL}	LNA Mode
H	High Gain mode
L	Low Gain mode

Note: Specifications and description listed in this datasheet are subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

T_a=+25°C, Z_s=Z_l=50 ohm

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Drain voltage	V_{DD}		5.0	V
Inverter voltage	V_{INV}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{in}	V_{DD}=V_{INV}=2.8V	+15	dBm
Power dissipation	P_D	4-layer FR4 PCB with through-hole (74.2x74.2mm), T_j=150°C	1300	mW
Operating temperature	T_{opr}		-40~+85	°C
Storage temperature	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

General conditions: V_{DD}=V_{INV}=2.8V, T_a=+25°C, Z_s=Z_l=50 ohm, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		2.3	2.8	3.6	V
Inverter voltage	V_{INV}		2.3	2.8	3.6	V
Control voltage (High)	$V_{CTL(H)}$		1.5	1.85	3.6	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.3	V
Operating current1	$I_{DD}1$	RF OFF, V_{CTL}=1.85V	-	5.0	8.0	mA
Operating current2	$I_{DD}2$	RF OFF, V_{CTL}=0V	-	1	5	μA
Inverter current1	$I_{INV}1$	RF OFF, V_{CTL}=1.85V	-	90	180	μA
Inverter current2	$I_{INV}2$	RF OFF, V_{CTL}=0V	-	15	40	μA
Control current	I_{CTL}	RF OFF, V_{CTL}=1.85V	-	5	10	μA

■ **ELECTRICAL CHARACTERISTICS2** (High Gain mode)

General conditions: V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, T_a=+25°C, Z_s=Z_l=50 ohm, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	f_{RF}		470	620	770	MHz
Small signal gain1	Gain1		11.0	15.0	19.0	dB
Noise figure	NF	Exclude PCB & connector losses*1	-	1.4	1.9	dB
Input power at 1dB gain compression point1	$P_{-1dB(IN)}1$		-14.0	-6.0	-	dBm
Input 3rd order intercept point1	IIP3_1	f1=f_{RF}, f2=f_{RF}+100kHz, P_{IN}=-25dBm	-6.0	+1.0	-	dBm
RF IN VSWR1	VSWRi1		-	1.5	4.5	-
RF OUT VSWR1	VSWRo1		-	1.5	2.8	-

■ **ELECTRICAL CHARACTERISTICS3** (Low Gain mode)

General conditions: V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, T_a=+25°C, Z_s=Z_l=50 ohm, with application circuit.

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	f_{RF}		470	620	770	MHz
Small signal gain2	Gain2	Exclude PCB & connector losses*2	-6.0	-4.0	-	dB
Input power at 1dB gain compression point2	$P_{-1dB(IN)}2$		+5.0	+12.0	-	dBm
Input 3rd order intercept point2	IIP3_2	f1=f_{RF}, f2=f_{RF}+100kHz, P_{IN}=-12dBm	+14.0	+20.0	-	dBm
RF IN VSWR2	VSWRi2		-	1.5	3.0	-
RF OUT VSWR2	VSWRo2		-	1.5	2.8	-

*1 Input PCB and connector losses: 0.036dB(at 470MHz), 0.053dB(at 770MHz)

*2 Input & output PCB and connector losses: 0.072dB(at 470MHz), 0.105dB(at 770MHz)

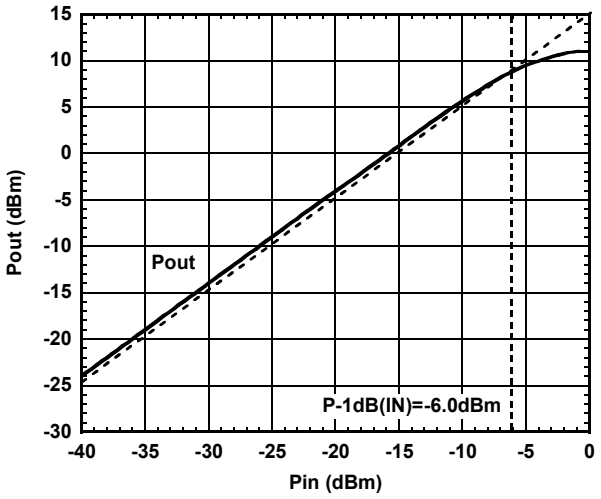
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1, 2, 4, 5, 6, 8, 9, 10, 11, 13	GND	Ground terminal. These terminals should be connected to the ground plane as close as possible for excellent RF performance.
3	VINV	Inverter voltage supply terminal.
7	RFOUT	RF Output terminal. RF signal comes out from this terminal, and goes through an external matching circuit connected to this. Inductor L4 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA.
12	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. Since this IC is integrated an input DC blocking capacitor.
14	VCTL	Control voltage supply terminal.

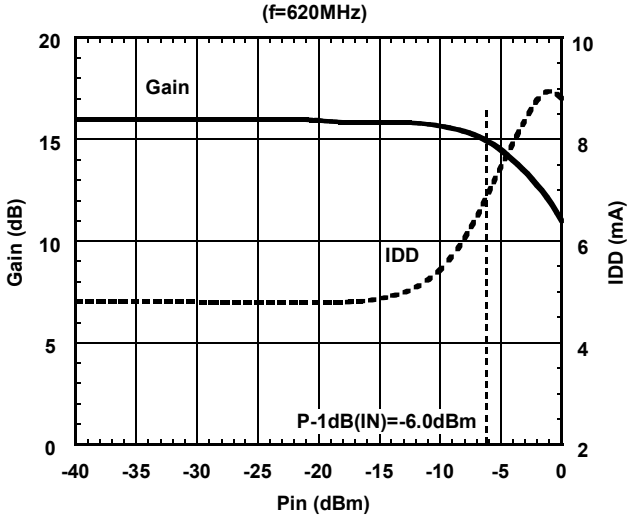
■ ELECTRICAL CHARACTERISTICS (High Gain mode)

Conditions: T_a=+25°C, V_{DD}= V_{INV}=2.8V, V_{CTL}=1.85V, Z_s=Z_l=50 ohm, with application circuit

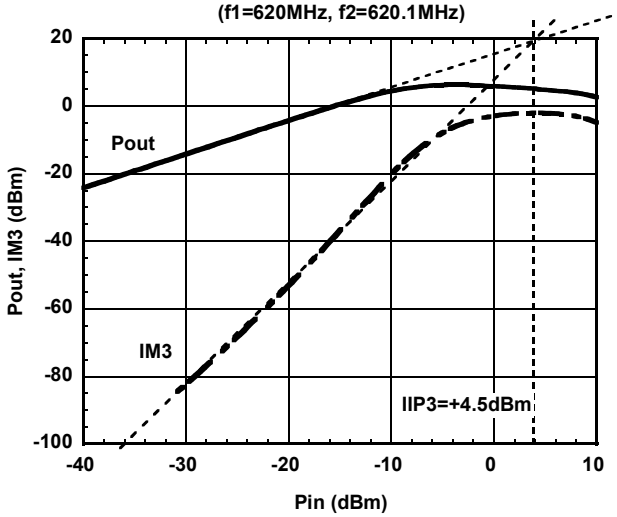
Pout vs. Pin
(f=620MHz)



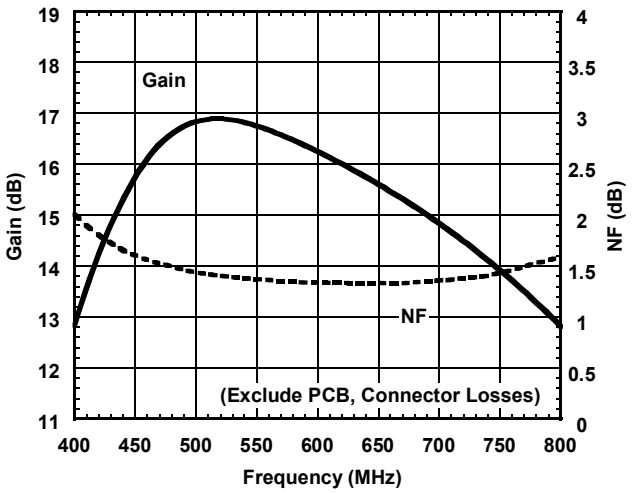
Gain, IDD vs. Pin
(f=620MHz)



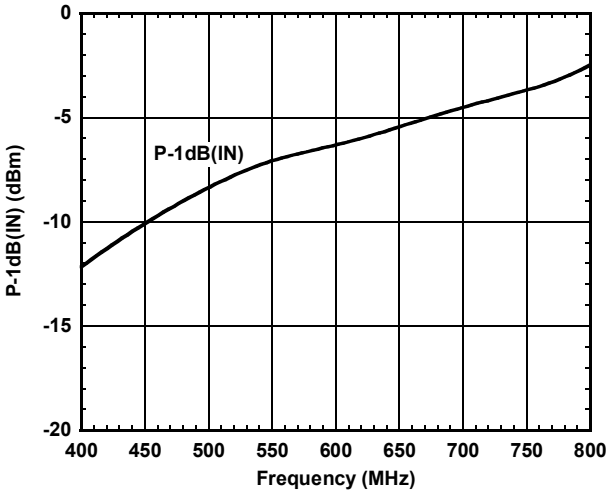
Pout, IM3 vs. Pin
(f1=620MHz, f2=620.1MHz)



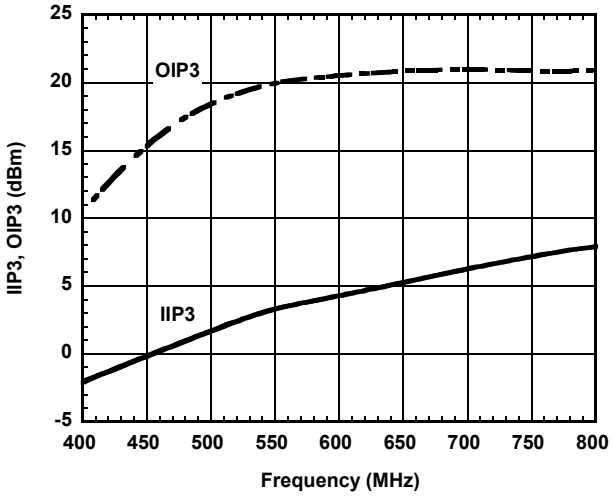
Gain, NF vs. Frequency



P-1dB(IN) vs. Frequency



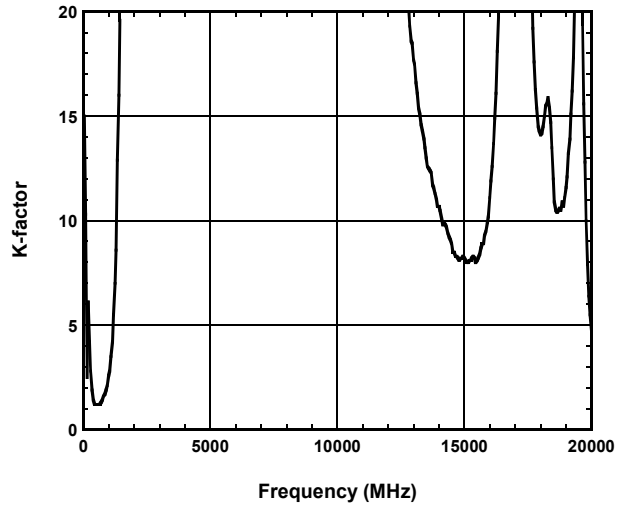
IIP3, OIP3 vs. Frequency
(f1=frequency, f2=f1+100kHz, Pin=-25dBm)



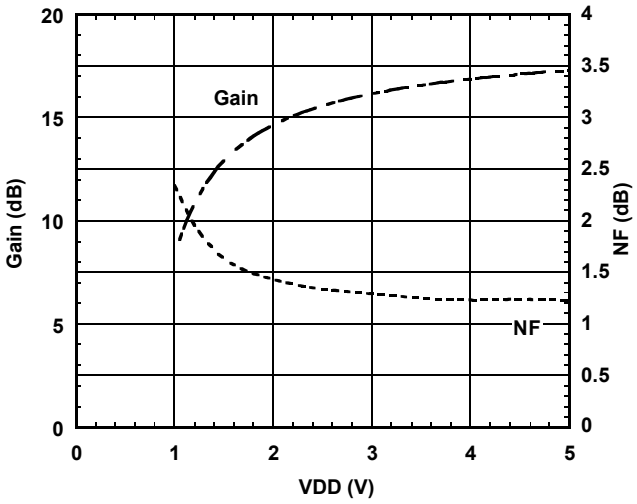
■ ELECTRICAL CHARACTERISTICS (High Gain mode)

Conditions: T_a=+25°C, V_{DD}= V_{INV}=2.8V, V_{CTL}=1.85V, Z_s=Z_l=50 ohm, with application circuit

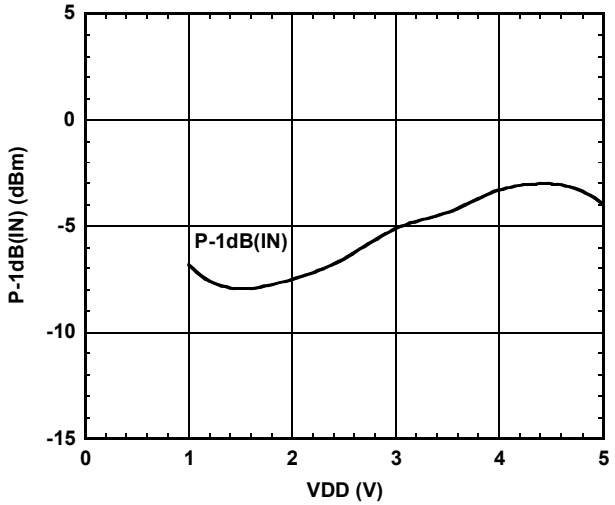
K-factor vs. Frequency



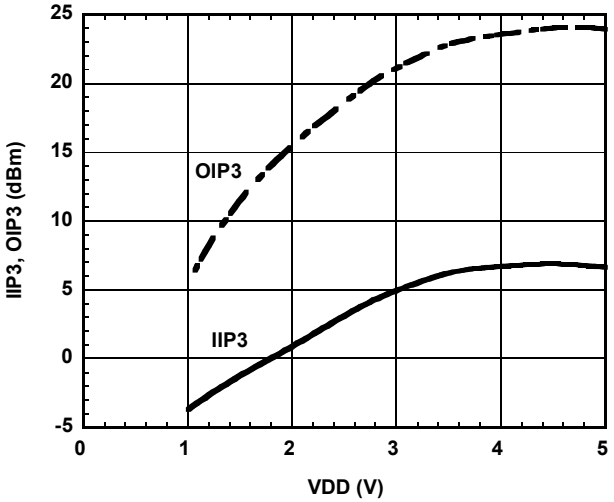
Gain, NF vs. VDD=VINV
(f=620MHz)



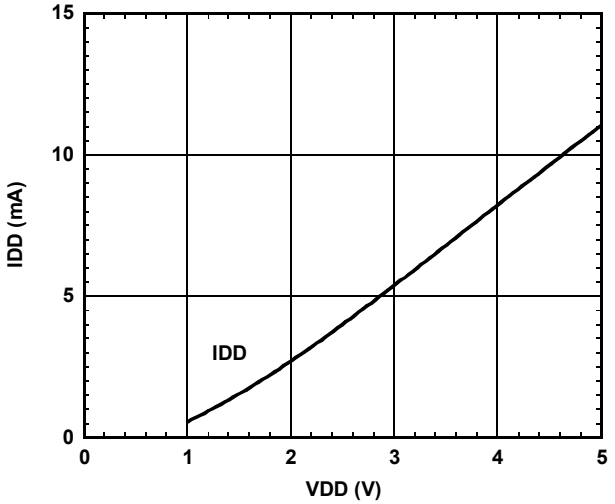
P-1dB(IN) vs. VDD=VINV
(f=620MHz)



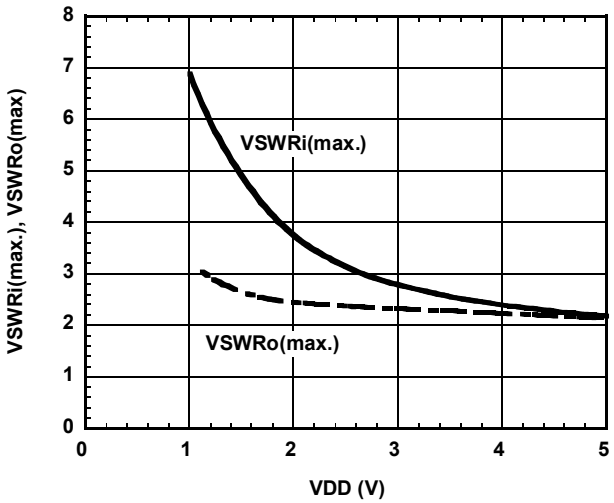
IIP3, OIP3 vs. VDD=VINV
(f1=620MHz, f2=620.1MHz, Pin=-25dBm)



IDD vs. VDD=VINV

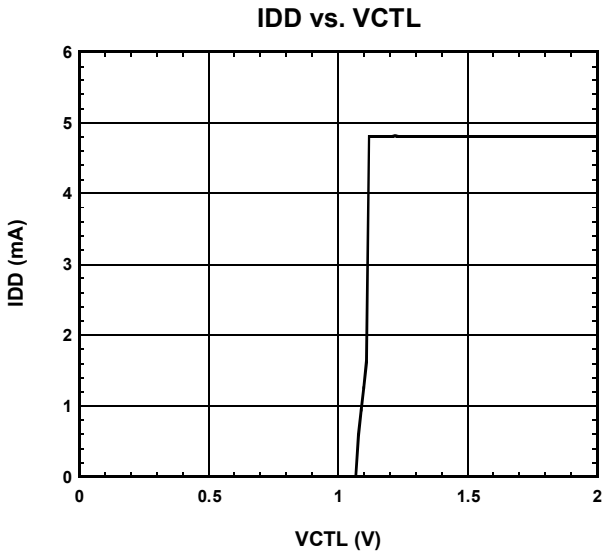


VSWR vs. VDD=VINV



■ **ELECTRICAL CHARACTERISTICS** (High Gain mode)

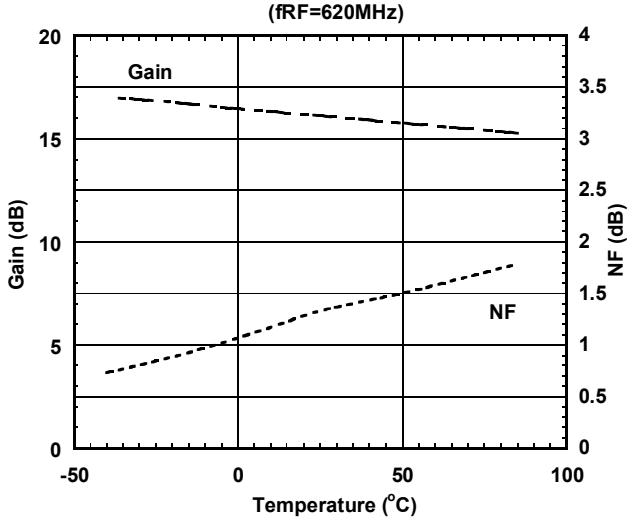
Conditions: T_a=+25°C, V_{DD}=2.8V, Z_s=Z_l=50 ohm, with application circuit



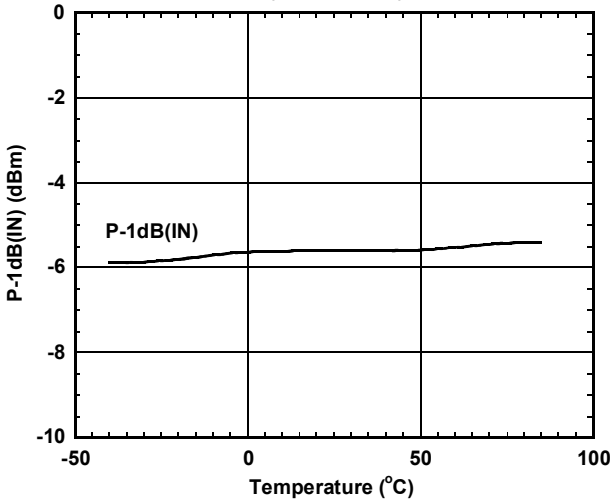
■ ELECTRICAL CHARACTERISTICS (High Gain mode)

Conditions: V_{DD}= V_{INV}=2.8V, V_{CTL}=1.85V, Z_s=Z_l=50 ohm, with application circuit

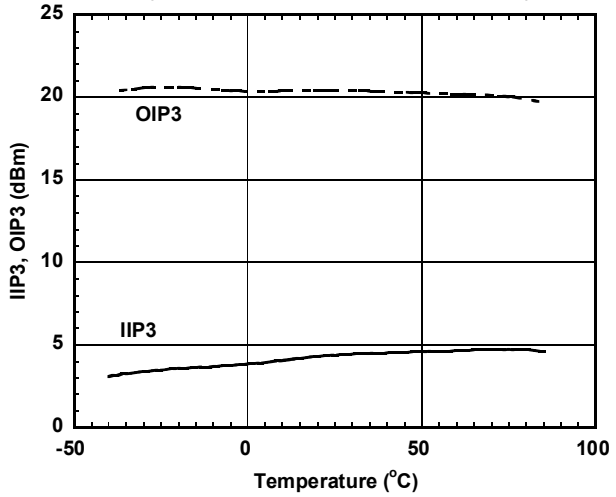
Gain, NF vs. Temp.
(fRF=620MHz)



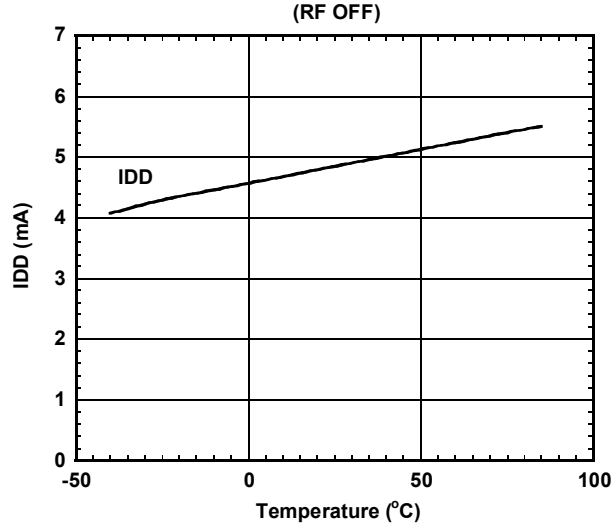
P-1dB(IN) vs. Temp.
(fRF=620MHz)



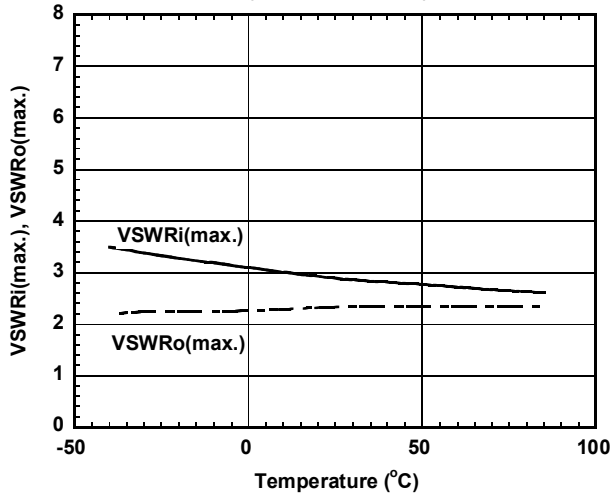
IIP3, OIP3 vs. Temp.
(f1=620MHz, f2=620.1MHz, Pin=-25dBm)



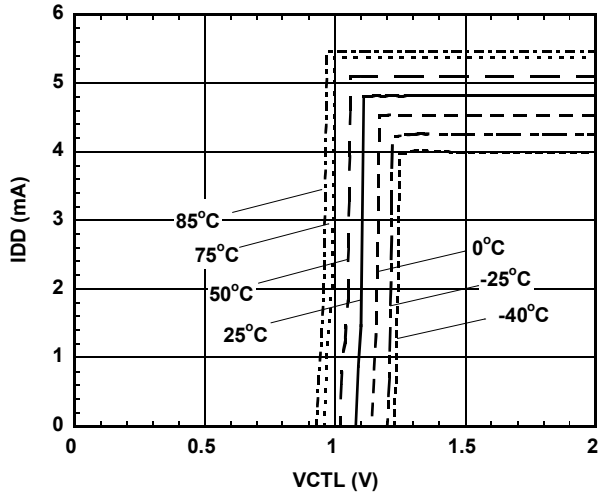
IDD vs. Temp.
(RF OFF)



VSWR vs. Temp.
(fRF=470~770MHz)

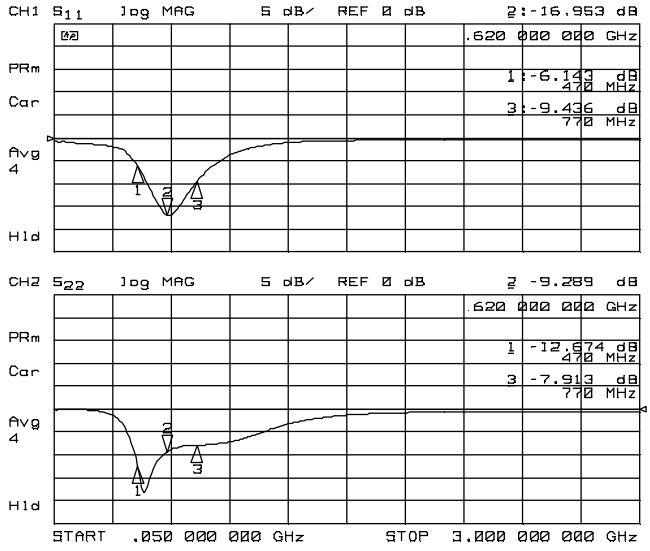


IDD vs. VCTL

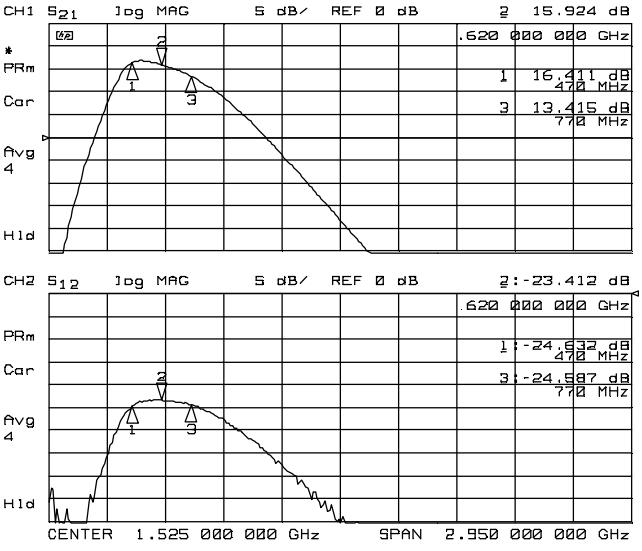


■ ELECTRICAL CHARACTERISTICS (High Gain mode)

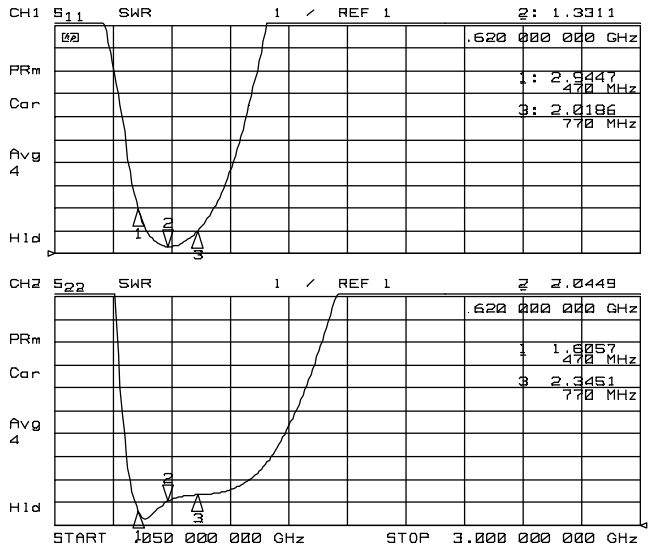
Conditions: T_a=+25°C, V_{DD}= V_{INV}=2.8V, V_{CTL}=1.85V, Z_s=Z_l=50 ohm, with application circuit



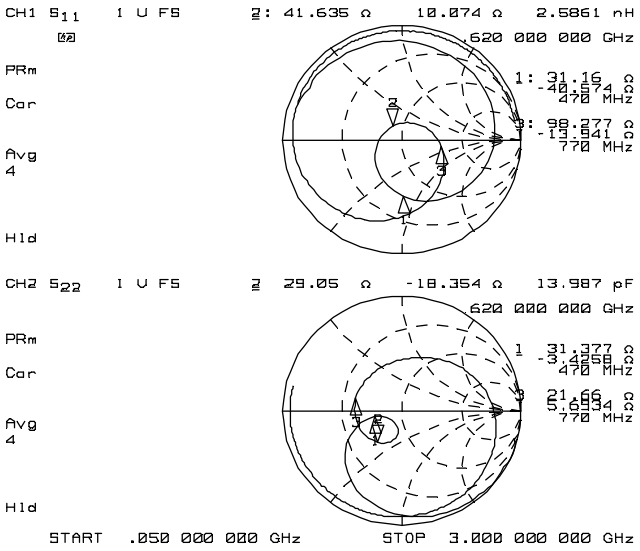
S_{11}, S_{22}



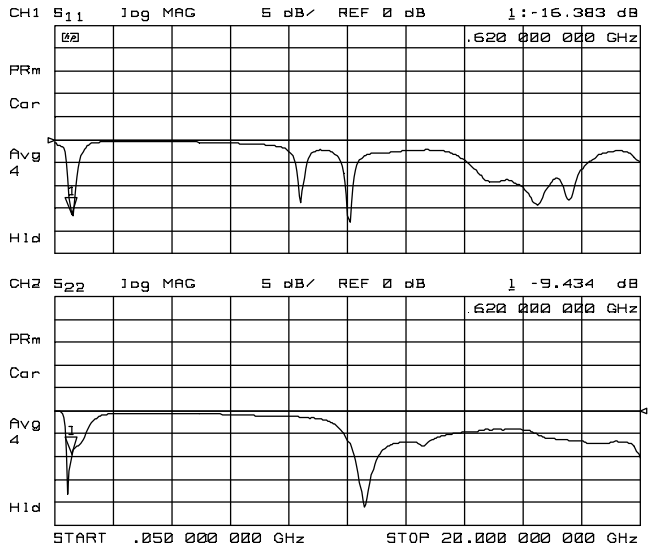
S_{21}, S_{12}



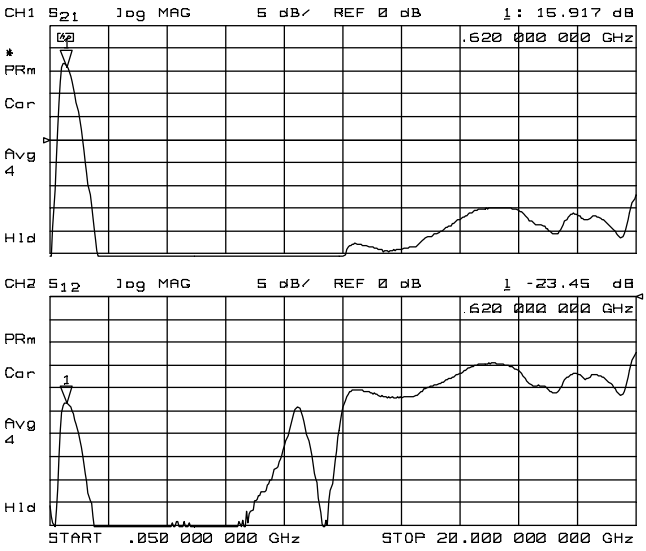
VSWR



Zin, Zout



S_{11}, S_{22} (50MHz~20GHz)

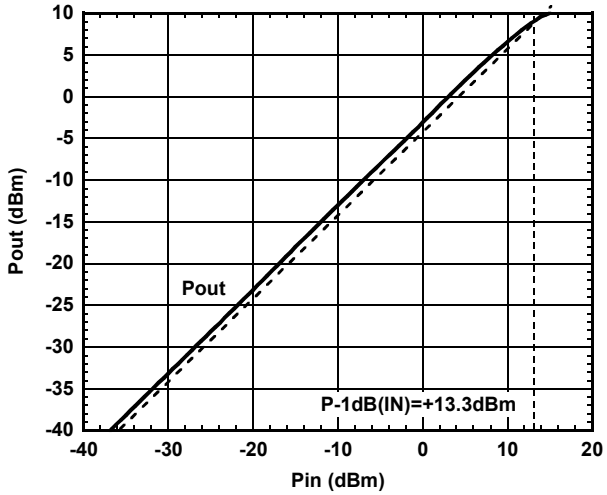


S_{21}, S_{12} (50MHz~20GHz)

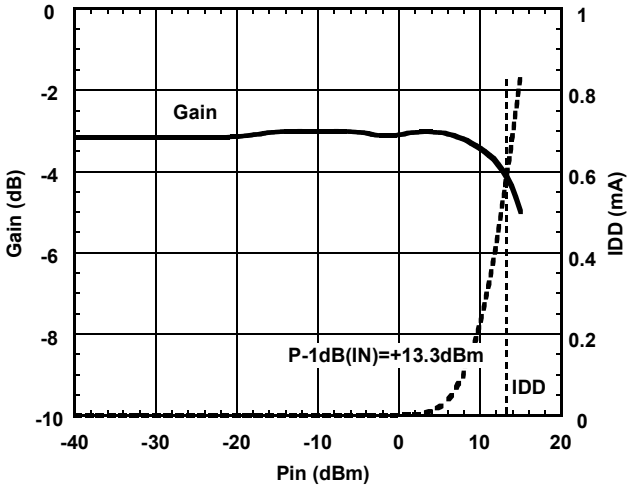
■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

Conditions: T_a=+25°C, V_{DD}= V_{INV}=2.8V, V_{CTL}=0V, Z_s=Z_l=50 ohm, with application circuit

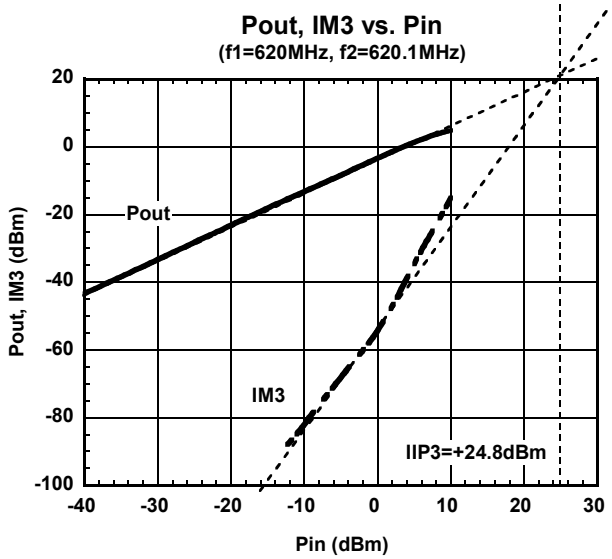
Pout vs. Pin
(f=620MHz)



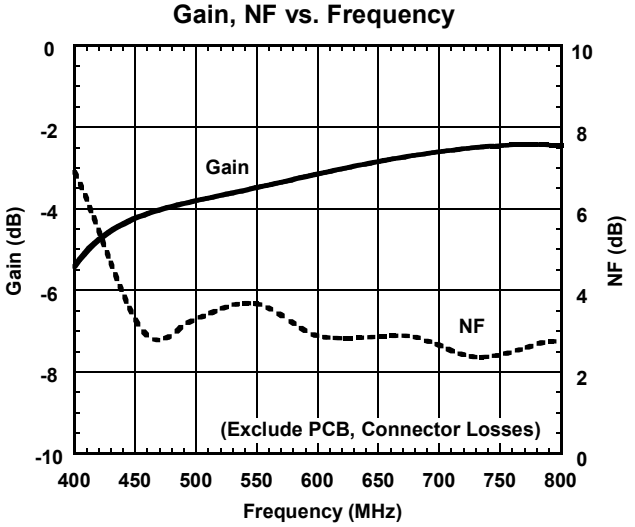
Gain, IDD vs. Pin
(f=620MHz)



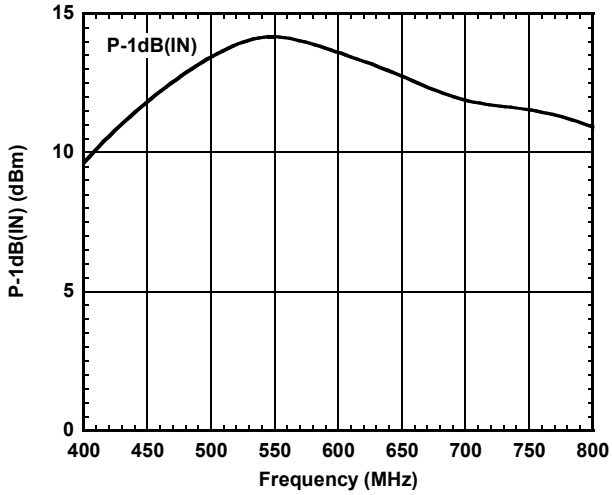
Pout, IM3 vs. Pin
(f1=620MHz, f2=620.1MHz)



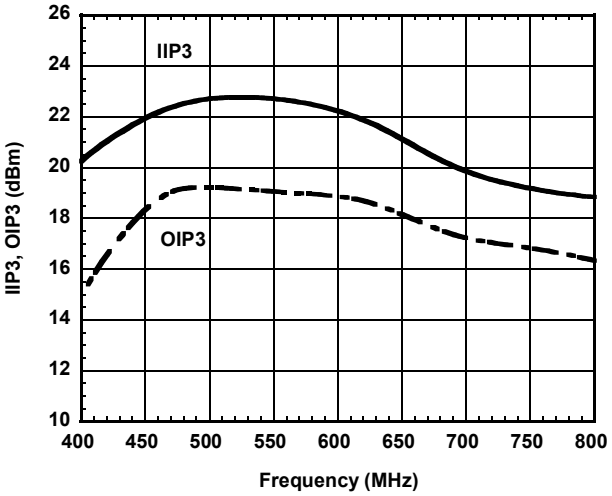
Gain, NF vs. Frequency



P-1dB(IN) vs. Frequency



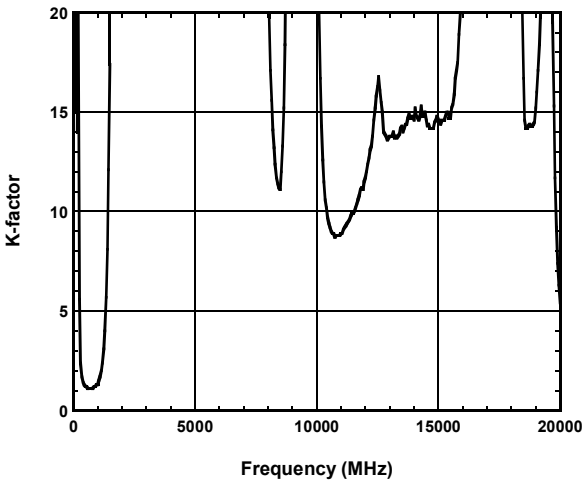
IIP3, OIP3 vs. Frequency
(f1=frequency , f2=f1+100kHz, Pin=-12dBm)



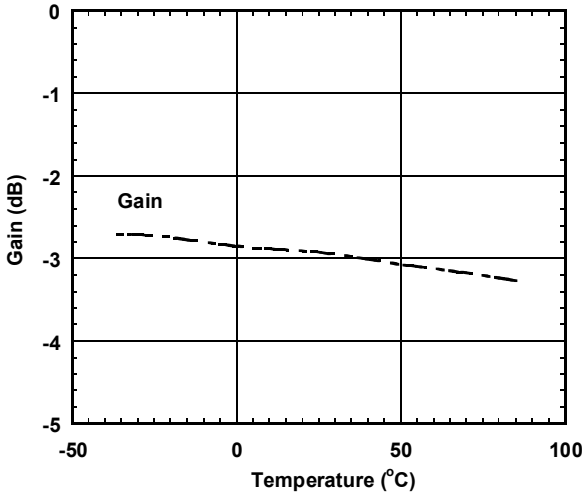
■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

Conditions: T_a=+25°C, V_{DD}= V_{INV}=2.8V, V_{CTL}=0V, Z_s=Z_l=50 ohm, with application circuit

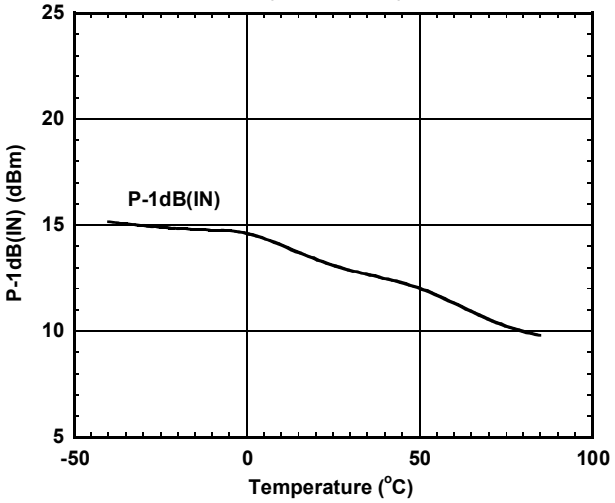
K-factor vs. Frequency



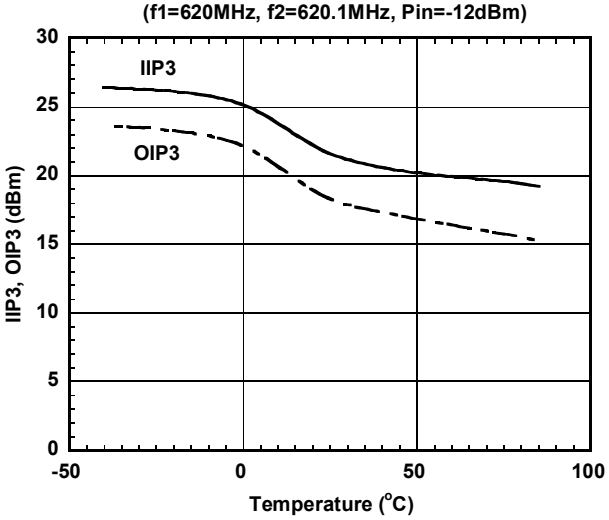
Gain vs. Temp.
(fRF=620MHz)



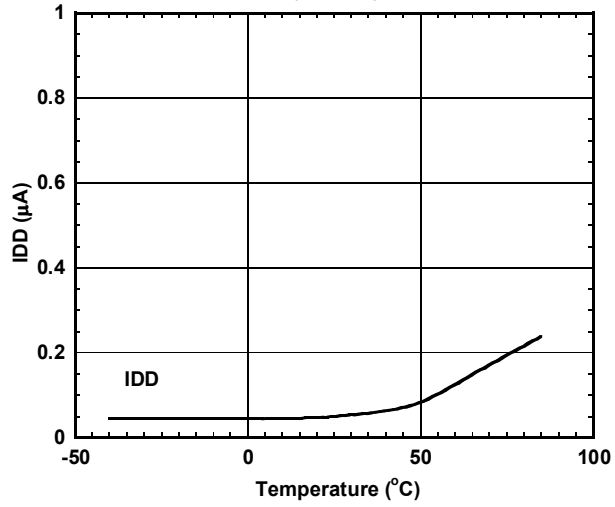
P-1dB(IN) vs. Temp.
(fRF=620MHz)



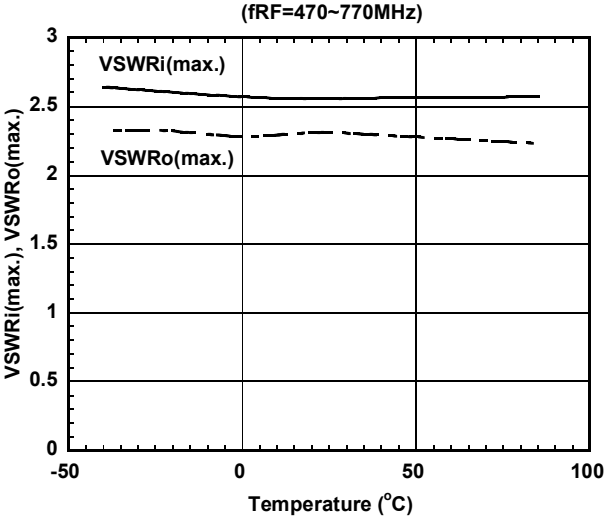
IIP3, OIP3 vs. Temp.
(f1=620MHz, f2=620.1MHz, Pin=-12dBm)



IDD vs. Temp.
(RF OFF)

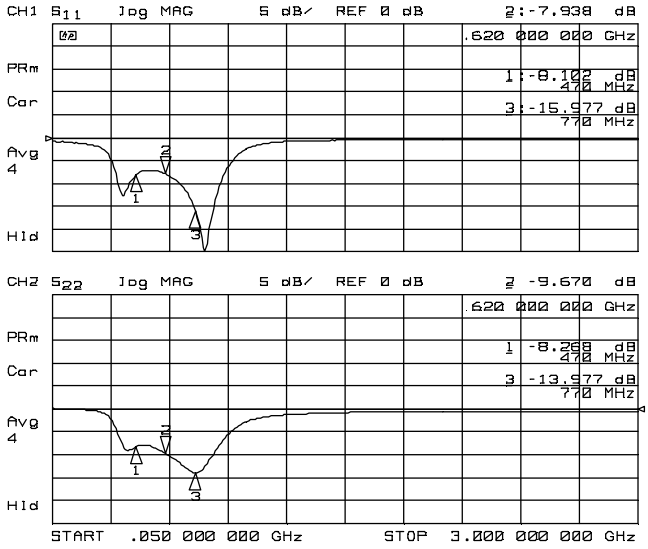


VSWR vs. Temp.
(fRF=470~770MHz)

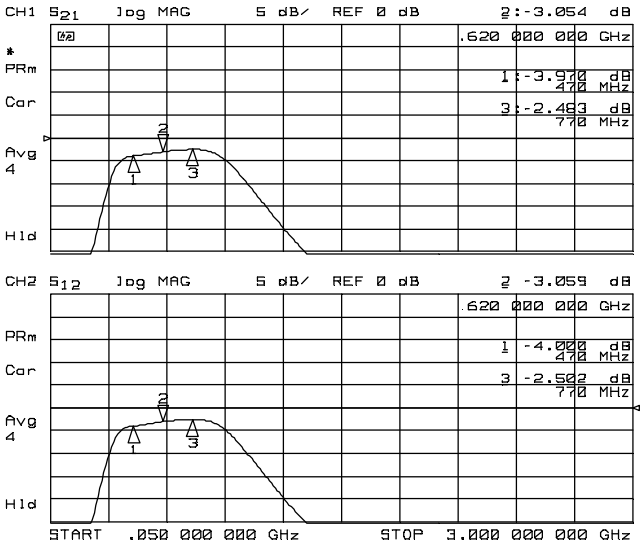


■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

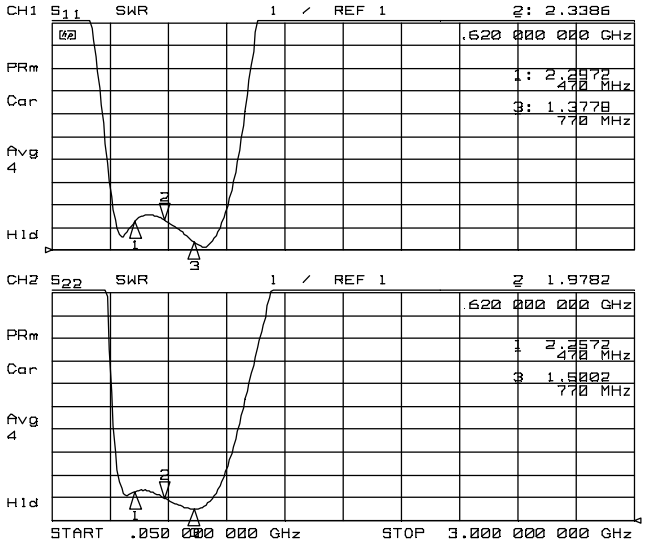
Conditions: T_a=+25°C, V_{DD}= V_{INV}=2.8V, V_{CTL}=0V, Z_s=Z_l=50 ohm, with application circuit



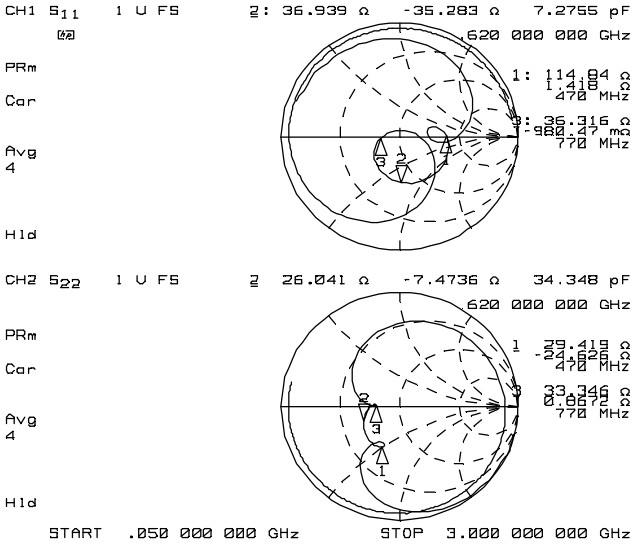
S_{11}, S_{22}



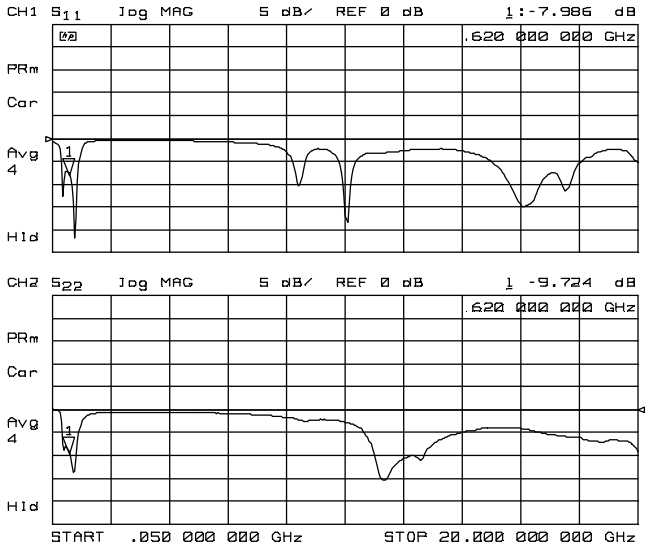
S_{21}, S_{12}



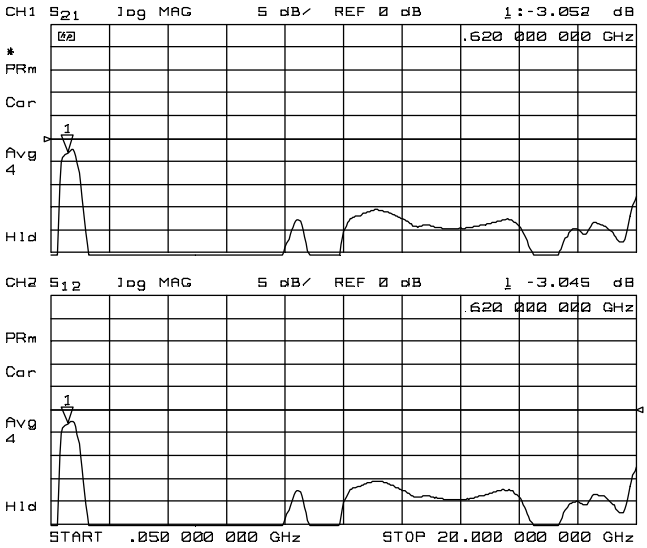
VSWR



Zin, Zout

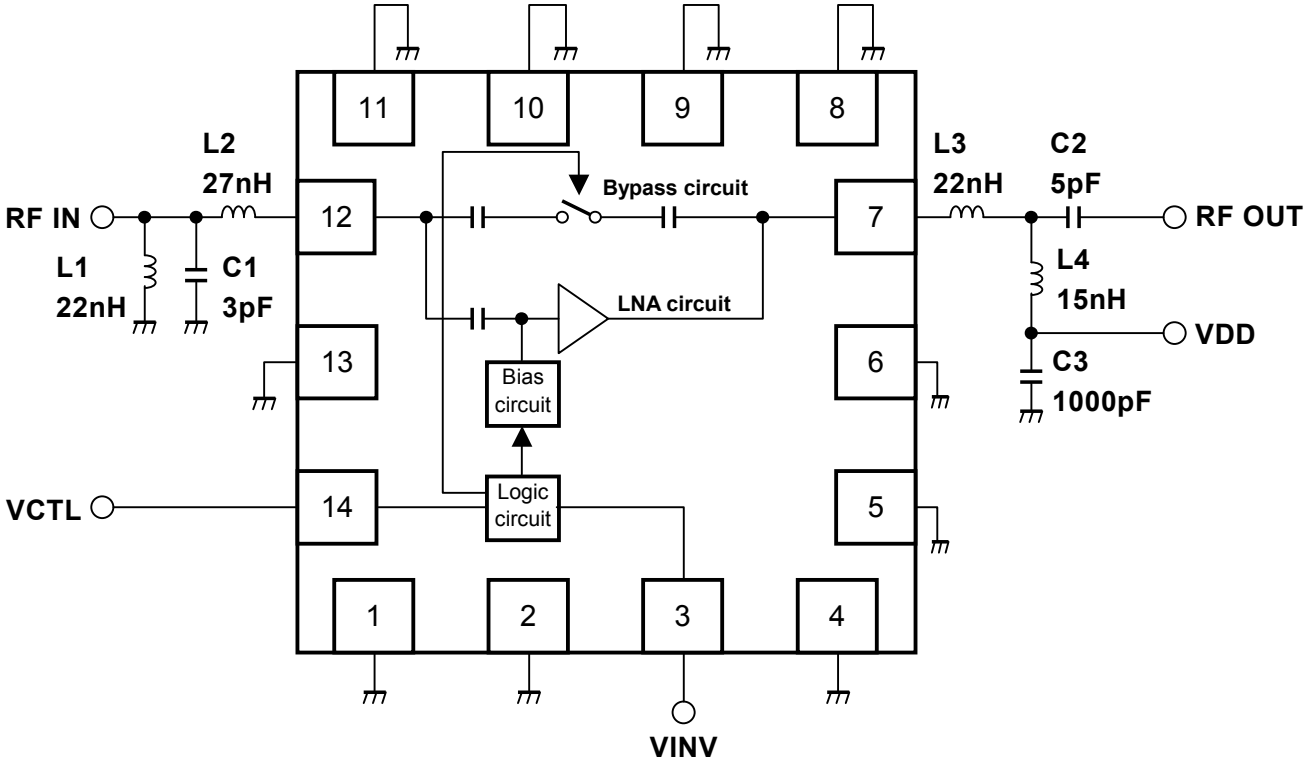


S_{11}, S_{22} (50MHz~20GHz)

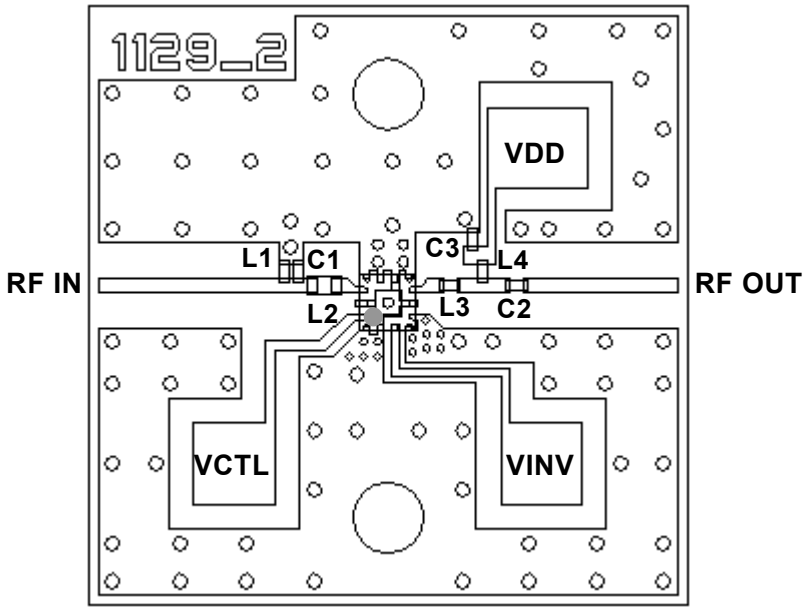


S_{21}, S_{12} (50MHz~20GHz)

■ APPLICATION CIRCUIT



■ TEST PCB LAYOUT



Parts List

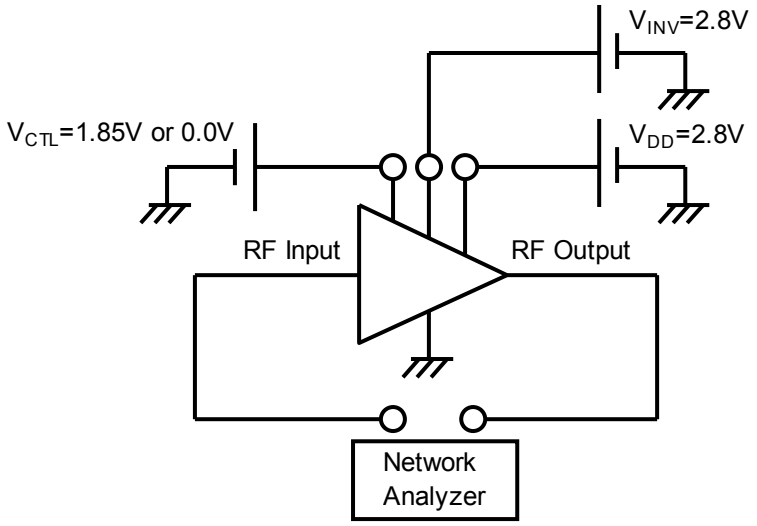
Parts ID	Notes
L1, L3, L4	MURATA LQP03T series
L2	TAIYO-YUDEN HK1005 series
C1~C3	MURATA GRM03 series

PCB (FR-4):
t=0.2mm
MICROSTRIP LINE
WIDTH=0.4mm (Z_0=50 ohm)
PCB SIZE=16.8mmx16.8mm

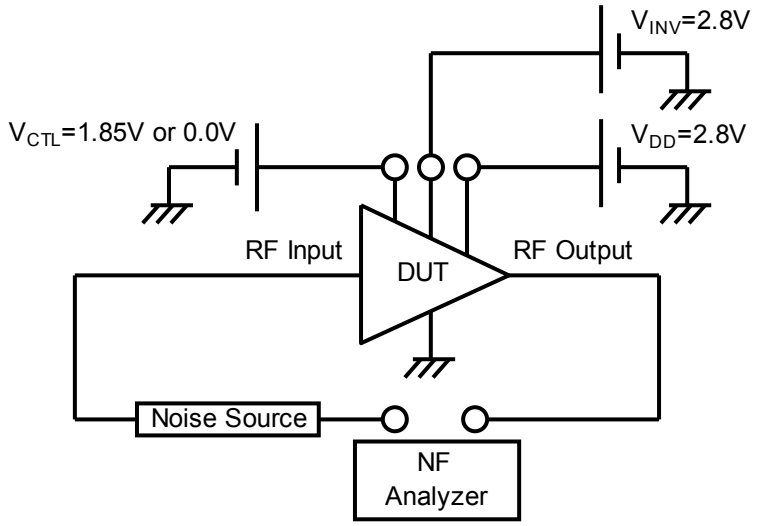
PRECAUTIONS

[1] L1-L4, C1 and C2 formed the external matching circuit.
[2] C3 is a bypass capacitor.
[3] Ground terminals should be connected with ground plane as close as possible in order to avoid parasitic inductance.
[4] Please place the ground trace between RFIN(12pin) and RFOUT(7pin) on the top PCB layout to have better isolation between input and output RF ports.
[5] Please place all external parts around the IC as close as possible.

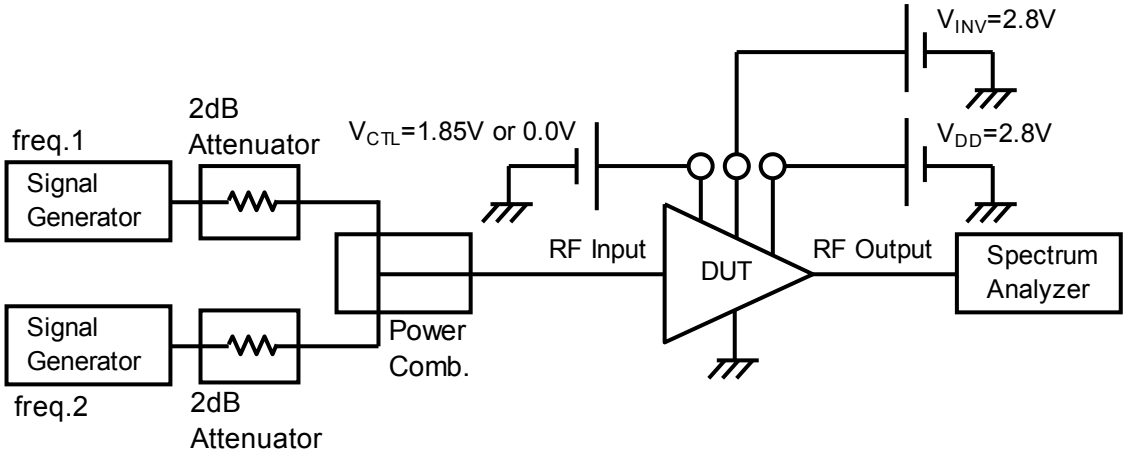
■ MEASUREMENT BLOCK DIAGRAM



S parameter Measurement Block Diagram

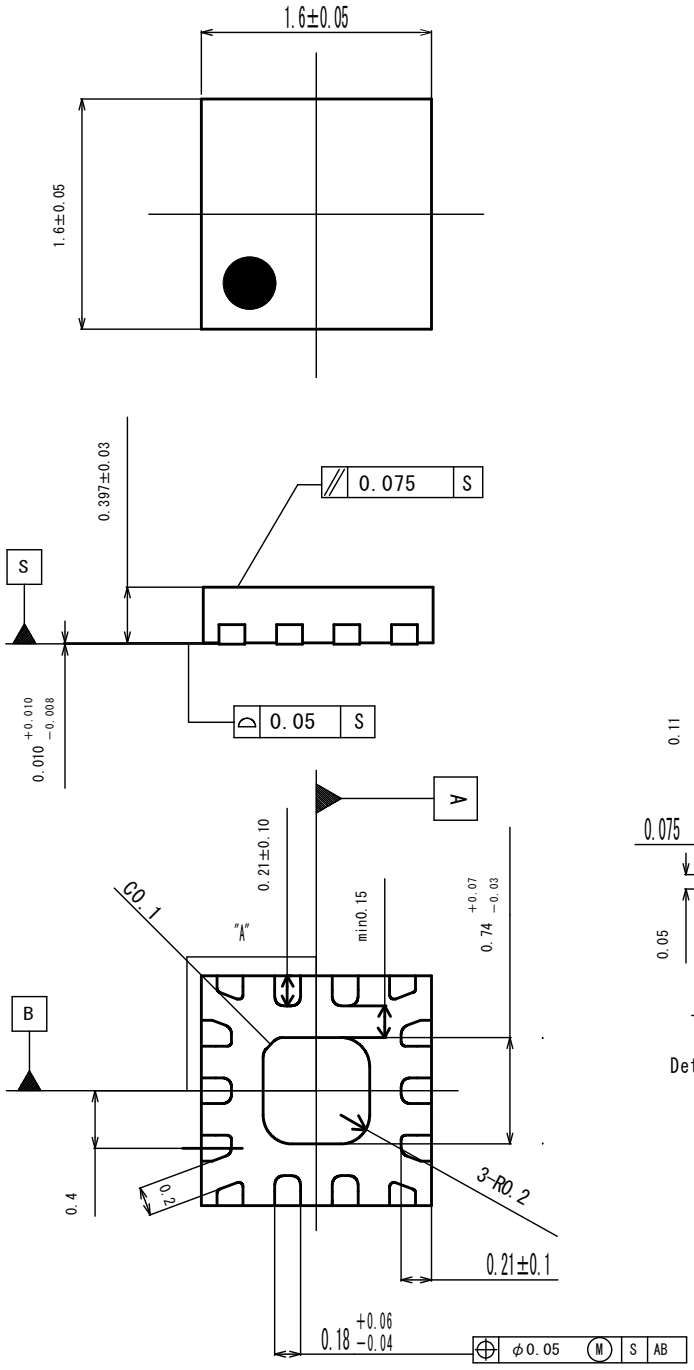


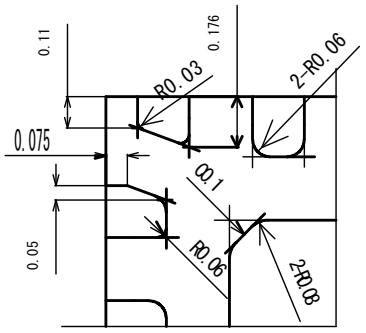
Noise Figure Measurement Block Diagram



Input IP3 Measurement Block Diagram

■ PACKAGE OUTLINE (EQFN14-D7)





Details of"A" part (×2)

UNIT : mm

SUBSTRATE MATERIAL : Copper
TERMINAL FINISH : Sn-Bi plating
MOLD MATERIAL : Epoxy resin
MASS (TYP.) : 0.0034 (g)

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.