

## SPDT SWITCH GaAs MMIC

### ■GENERAL DESCRIPTION

NJG1516KC3 is a GaAs SPDT switch IC suited for antenna switch of cellular phone handset.

This switch features low loss, high isolation at high power, and exhibits wide operating frequency range from 50MHz to 3GHz at low voltage of 2.7V.

The ultra small & ultra thin FLP6-C3 package is applied.

### ■PACKAGE OUTLINE

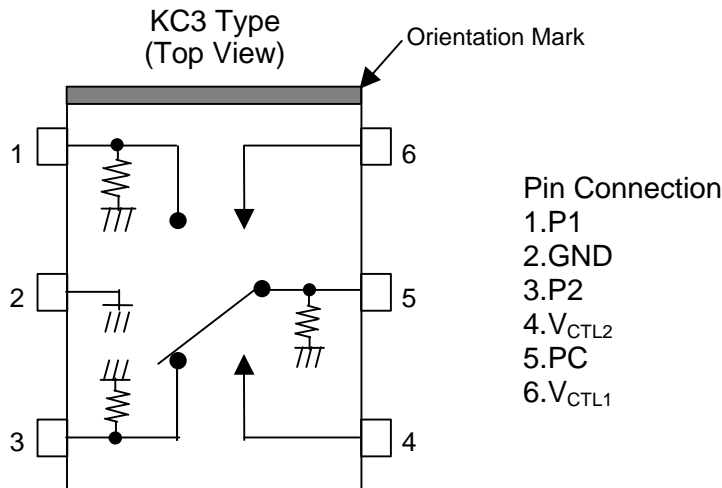


NJG1516KC3

### ■FEATURES

- Single, low voltage control +2.7~+9V
- Low insertion loss
  - 0.4dB typ. @f=1GHz,  $P_{in}=31\text{dBm}$ ,  $V_{CTL}=3.0\text{V}$
  - 0.5dB typ. @f=1GHz,  $P_{in}=34.5\text{dBm}$ ,  $V_{CTL}=3.0\text{V}$
  - 0.4dB typ. @f=1GHz,  $P_{in}=34.5\text{dBm}$ ,  $V_{CTL}=3.5\text{V}$
  - 0.7dB typ. @f=2GHz,  $P_{in}=31.5\text{dBm}$ ,  $V_{CTL}=3.0\text{V}$
- High isolation
  - 27dB typ. @f=1GHz,  $P_{in}=34.5\text{dBm}$ ,  $V_{CTL}=3.0\text{V}$
  - 25dB typ. @f=2GHz,  $P_{in}=31.5\text{dBm}$ ,  $V_{CTL}=3.0\text{V}$
- Handling power 36dBm typ. @f=2GHz,  $V_{CTL}=3.0\text{V}$
- Low current consumption 38uA typ. @f=2GHz,  $P_{in}=34.5\text{dBm}$ ,  $V_{CTL}=3.0\text{V}$
- Ultra small & ultra thin package FLP6-C3 (Mount size: 2.8x3.0x0.75mm)

### ■PIN CONFIGURATION



### ■TRUTH TABLE

“H”=V<sub>CTL(H)</sub>, “L”=V<sub>CTL(L)</sub>

|                   |     |     |
|-------------------|-----|-----|
| V <sub>CTL1</sub> | H   | L   |
| V <sub>CTL2</sub> | L   | H   |
| PC - P1           | ON  | OFF |
| PC - P2           | OFF | ON  |

# NJG1516KC3

## ■ABSOLUTE MAXIMUM RATINGS

(T<sub>a</sub>=25°C)

| PARAMETER         | SYMBOL           | CONDITIONS   | RATINGS  | UNITS |
|-------------------|------------------|--|----------|-------|
| Input Power       | P <sub>in</sub>  | V <sub>CTL(L)</sub> =0V, V <sub>CTL(H)</sub> =3.0V | 38       | dBm   |
| Control Voltage   | V <sub>CTL</sub> | V <sub>CTL(H)</sub> -V <sub>CTL(L)</sub>           | 12       | V     |
| Power Dissipation | P <sub>D</sub>   |  | 500      | mW    |
| Operating Temp.   | T <sub>opr</sub> |  | -40~+85  | °C    |
| Storage Temp.     | T <sub>stg</sub> |  | -55~+125 | °C    |

## ■ELECTRICAL CHARACTERISTICS

(V<sub>CTL(L)</sub>=0V, V<sub>CTL(H)</sub>=3V, Z<sub>S</sub>=Z<sub>I</sub>=50Ω, T<sub>a</sub>=25°C)

| PARAMETERS                         | SYMBOL               | CONDITIONS   | MIN  | TYP  | MAX  | UNITS |
|------------------------------------|----------------------|--|------|------|------|-------|
| Operating Voltage (LOW)            | V <sub>CTL(L)</sub>  |  | -0.2 | 0    | 0.2  | V     |
| Operating Voltage (HIGH)           | V <sub>CTL(H)</sub>  | f=1GHz, P <sub>in</sub> =34.5dBm   | 2.7  | 3.0  | 9.0  | V     |
| Control Current                    | I <sub>CTL</sub>     | f=1GHz, P <sub>in</sub> =34.5dBm   | -    | 38   | 55   | uA    |
| Insertion Loss 1                   | LOSS1                | f=1GHz, P <sub>in</sub> =31dBm   | -    | 0.4  | 0.5  | dB    |
| Insertion Loss 2                   | LOSS2                | f=1GHz, P <sub>in</sub> =34.5dBm<br>V <sub>CTL(H)</sub> =3.5V, V <sub>CTL(L)</sub> =0V | -    | 0.4  | 0.5  | dB    |
| Insertion Loss 3                   | LOSS3                | f=1GHz, P <sub>in</sub> =34.5dBm   | -    | 0.5  | 0.6  | dB    |
| Insertion Loss 4                   | LOSS4                | f=2GHz, P <sub>in</sub> =31.5dBm   | -    | 0.7  | 0.8  | dB    |
| Isolation 1<br>(PC-P1, PC-P2)      | ISL1                 | f=1GHz, P <sub>in</sub> =34.5dBm   | 26   | 27   | -    | dB    |
| Isolation 2<br>(PC-P1, PC-P2)      | ISL2                 | f=2GHz, P <sub>in</sub> =31.5dBm   | 22   | 25   | -    | dB    |
| Maximum Input Power 1 *1           | P <sub>in1</sub>     | V <sub>CTL(H)</sub> =2.7V, f=2GHz  | -    | -    | 33.5 | dBm   |
| Maximum Input Power 2 *1           | P <sub>in2</sub>     | V <sub>CTL(H)</sub> =3V, f=2GHz  | -    | -    | 34   | dBm   |
| Maximum Input Power 3 *1           | P <sub>in3</sub>     | V <sub>CTL(H)</sub> =4V, f=2GHz  | -    | -    | 37   | dBm   |
| Maximum Input Power 4 *1           | P <sub>in4</sub>     | V <sub>CTL(H)</sub> =6V, f=2GHz  | -    | -    | 38   | dBm   |
| Maximum Input Power 5 *1           | P <sub>in5</sub>     | V <sub>CTL(H)</sub> =9V, f=2GHz  | -    | -    | 34.5 | dBm   |
| Pout at 0.2dB<br>Compression point | P <sub>-0.2dB1</sub> | f=2GHz   | 34.5 | 36   | -    | dBm   |
| VSWR 1 (PC, P1, P2)                | VSWR                 | f=0.05~2.5GHz, ON<br>State   | -    | 1.45 | 1.55 |       |
| Switching Time                     | T <sub>SW</sub>      | f=0.05~2.5GHz  | -    | 70   | -    | ns    |

\*1: Maximum Input Power: This value is defined as maximum input power of linear operating region (such as Pout at 0.05dB Gain compression point) or damage free operating region.

## ■ ELECTRICAL CHARACTERISTICS (Cellular Band)

( $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=2.7V$ ,  $Z_s=Z_l=50\Omega$ ,  $T_a=25^\circ C$ )

| PARAMETERS                           | SYMBOL          | CONDITIONS  | MIN  | TYP  | MAX  | UNITS |
|--------------------------------------|-----------------|---|------|------|------|-------|
| Frequency range                      | $f_{in}$        |   | 800  | -    | 1000 | MHz   |
| Control voltage (HIGH)               | $V_{CTL(H)}$    | $P_{in}=25dBm$  | 2.7  | -    | 9    | V     |
| Insertion Loss 5                     | LOSS5           | $P_{in}=25dBm$  | -    | 0.4  | 0.5  | dB    |
| Isolation 3<br>(PC-P1, PC-P2)        | ISL3            | $P_{in}=25dBm$  | 26   | 27   | -    | dB    |
| Pout at 0.2dB<br>Compression point 2 | $P_{-0.2dB(2)}$ |   | 33.5 | 35   | -    | dBm   |
| Input 3rd Order<br>Intercept Point 1 | IIP3(1)         | $f=900+901MHz$ , $P_{in}=25dBm$ ,<br>$V_{CTL(H)}=3V$ , $V_{CTL(L)}=0V$ *2 | -    | 62   | -    | dBm   |
| Input 3rd Order<br>Intercept Point 2 | IIP3(2)         | $f=900+901MHz$ , $P_{in}=25dBm$<br>$V_{CTL(H)}=2.7V$ , $V_{CTL(L)}=0V$ *2 | -    | 60   | -    | dBm   |
| Second Harmonics                     | 2fo             | $f=900MHz$ , $P_{in}=25dBm$<br>2nd Harmonics of Input Signal<br>= -83dBc  |      | -80  | -    | dBc   |
| Third Harmonics                      | 3fo             | $f=900MHz$ , $P_{in}=25dBm$<br>3rd Harmonics of Input Signal<br>=-100dBc  | -    | -70  | -    | dBc   |
| VSWR 2 (PC, P1, P2)                  | VSWR2           | ON State  | -    | 1.15 | 1.25 |       |

\*2: The input IP3 is defined as following equation.

$$IIP3 = (3 \times P_{out} - IM3) / 2 + LOSS$$

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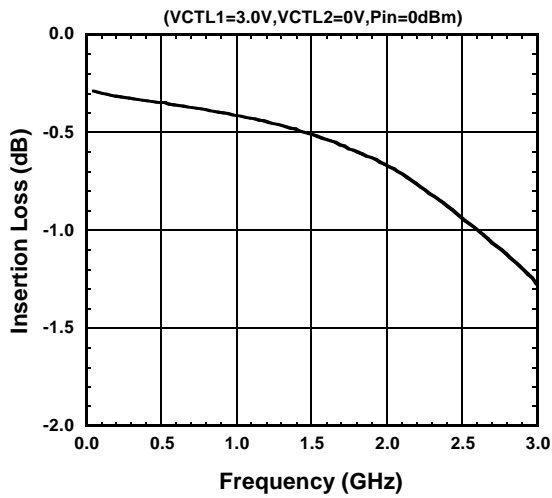
## ■ TERMINAL INFORMATION

| No. | SYMBOL     | EXPLANATION   |
|-----|------------|---|
| 1   | P1         | RF port. This port is connected with PC port by controlling 6 <sup>th</sup> pin ( $V_{CTL(H)}$ ) to 2.7~9.0V and 4 <sup>th</sup> pin ( $V_{CTL(L)}$ ) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01 $\mu$ F, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)  |
| 2   | GND        | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.  |
| 3   | P2         | RF port. This port is connected with PC port by controlling 4 <sup>th</sup> pin ( $V_{CTL(H)}$ ) to 2.7~9.0V and 6 <sup>th</sup> pin ( $V_{CTL(L)}$ ) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01 $\mu$ F, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)  |
| 4   | $V_{CTL2}$ | Control port 2. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.7~5.5V) or low-state (-0.2~+0.2V). The voltage of 6 <sup>th</sup> pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching speed delay from 10pF~1000pF range. |
| 5   | PC         | Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required. (50~100MHz: 0.01 $\mu$ F, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)   |
| 6   | $V_{CTL1}$ | Control port 1. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.7~5.5V) or low-state (-0.2~+0.2V). The voltage of 4 <sup>th</sup> pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching speed delay from 10pF~1000pF range. |

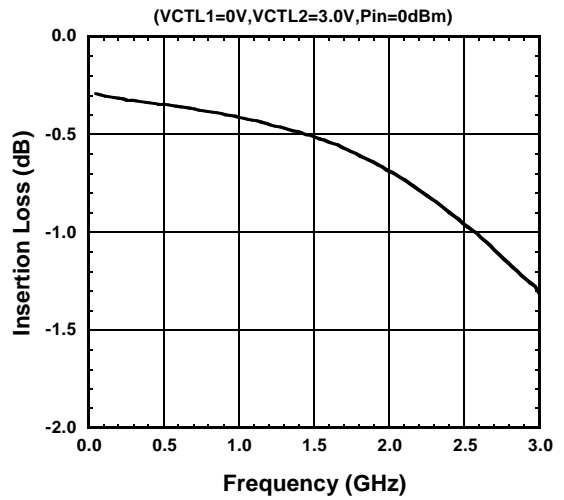
## ■ ELECTRICAL CHARACTERISTICS

(f=50MHz~3.0GHz, with application circuit, losses of external circuit are excluded)

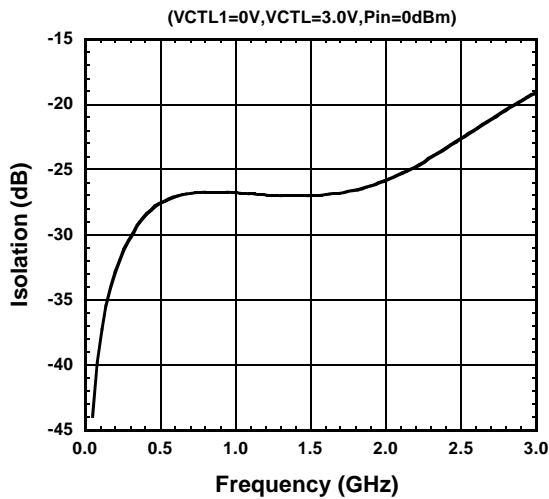
### PC-P1 Insertion Loss vs. Frequency



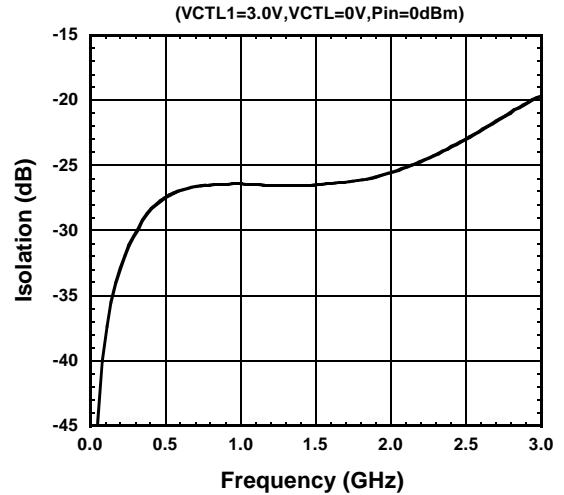
### PC-P2 Insertion Loss vs. Frequency



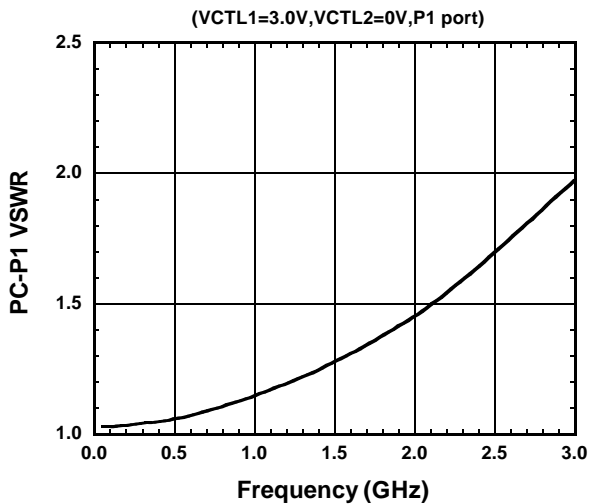
### PC-P1 Isolation vs. Frequency



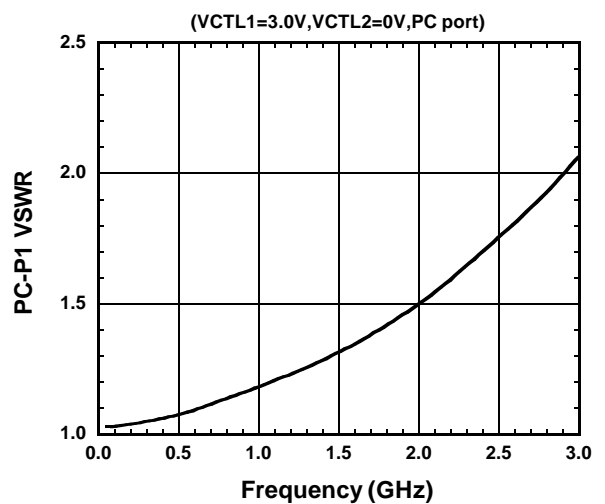
### PC-P2 Isolation vs. Frequency



### PC-P1 VSWR vs. Frequency



### PC-P1 VSWR vs. Frequency



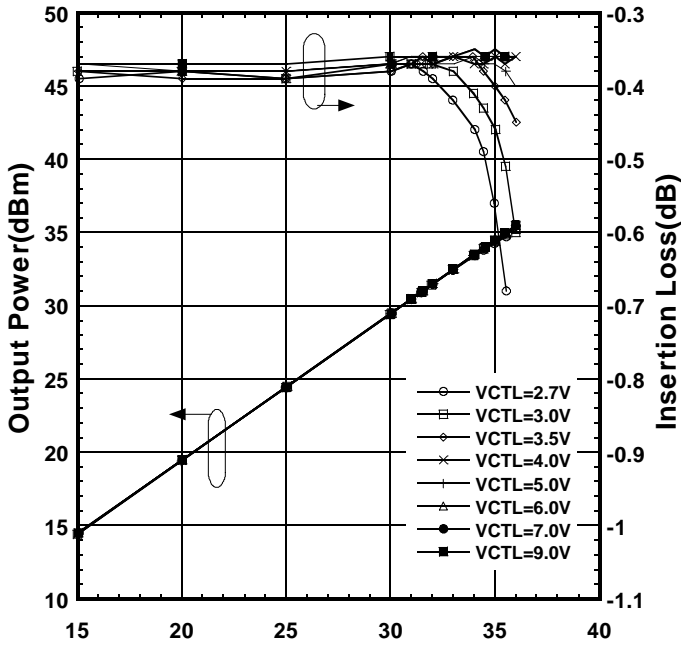
# NJG1516KC3

## ELECTRICAL CHARACTERISTICS

(f=0.8GHz, with application circuit 1 (Parts list 3), losses of PCB, DC blocking capacitor are excluded)

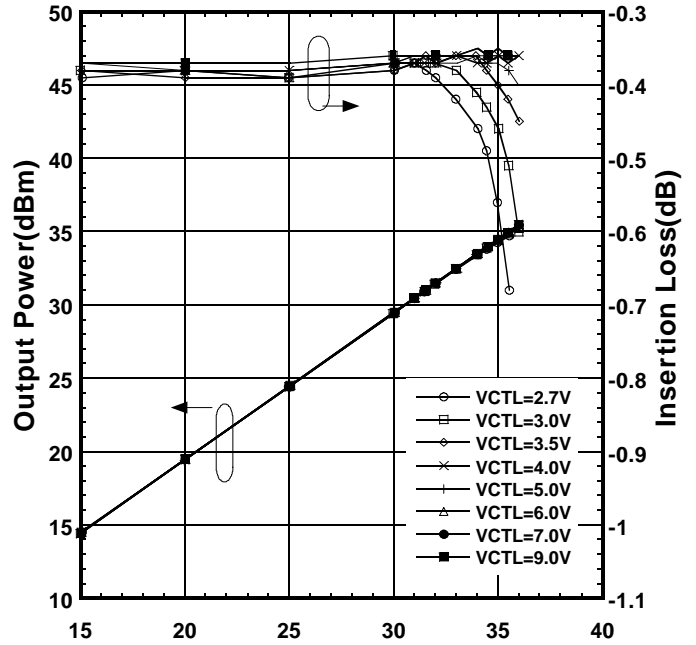
Output Power,Insertion Loss vs. Input power

(PC-P1,f=0.8GHz)



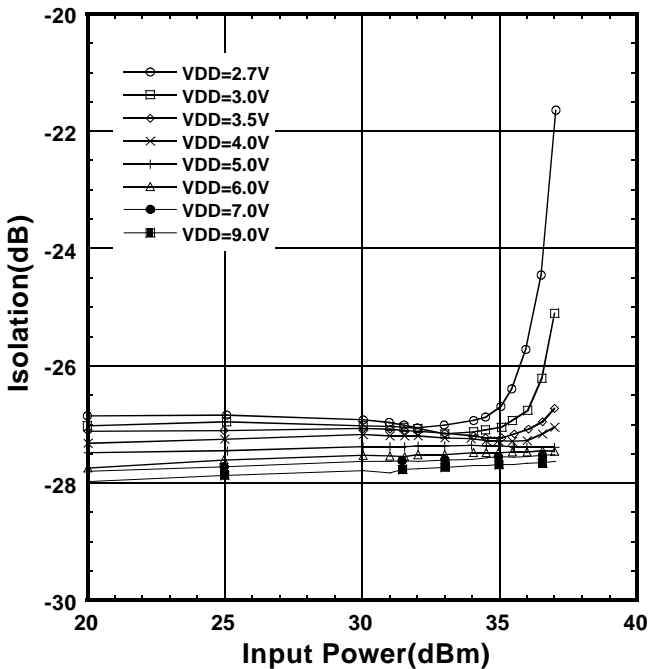
Output Power,Insertion Loss vs. Input power

(PC-P2,f=0.8GHz)



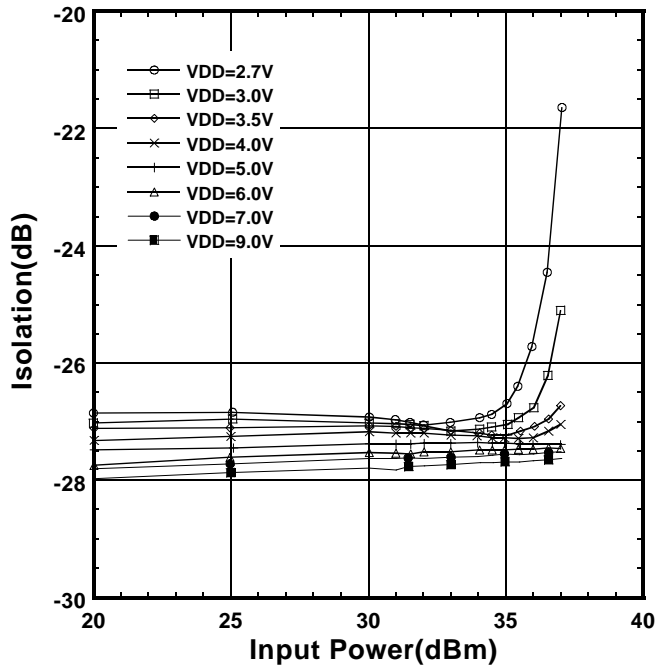
PC-P1 Isolation vs. Input Power

(PC-P1,f=0.8GHz)



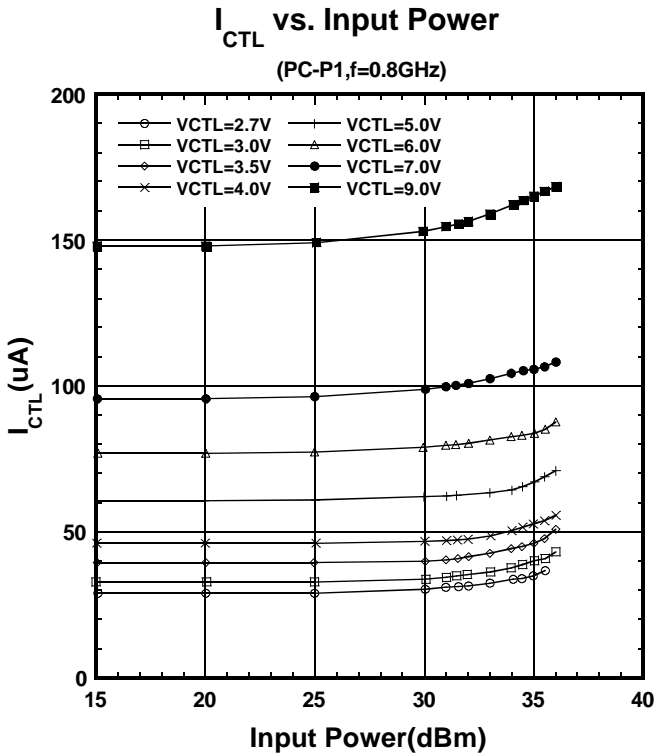
PC-P2 Isolation vs. Input Power

(PC-P2,f=0.8GHz)

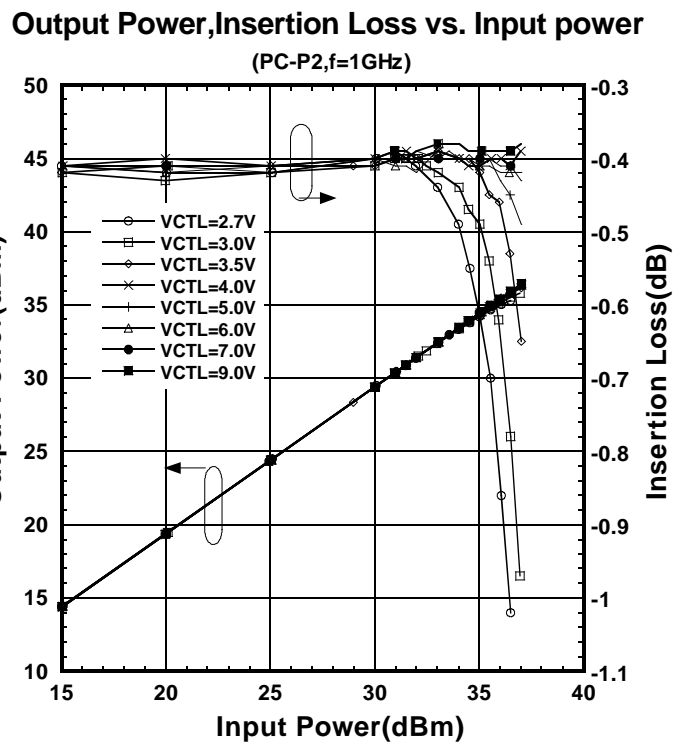
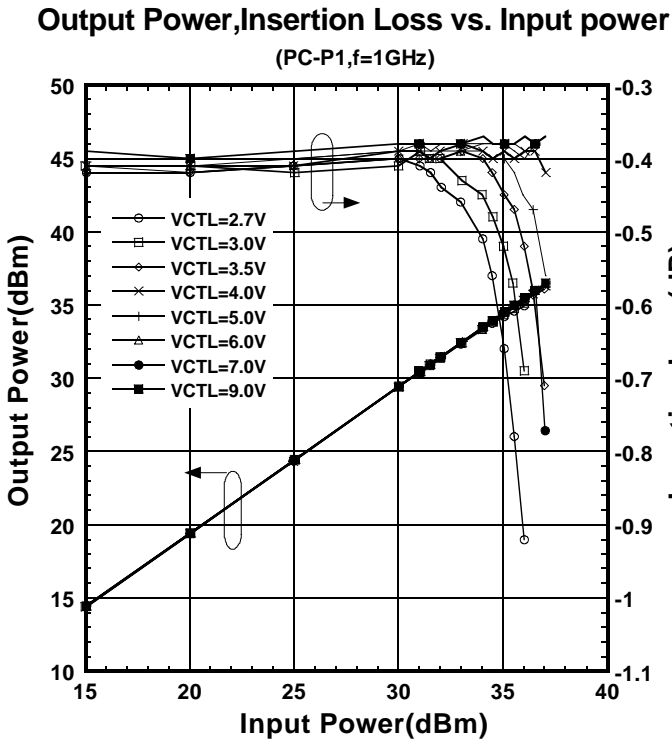


## ■ ELECTRICAL CHARACTERISTICS

(f=0.8GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)



(f=1.0GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)



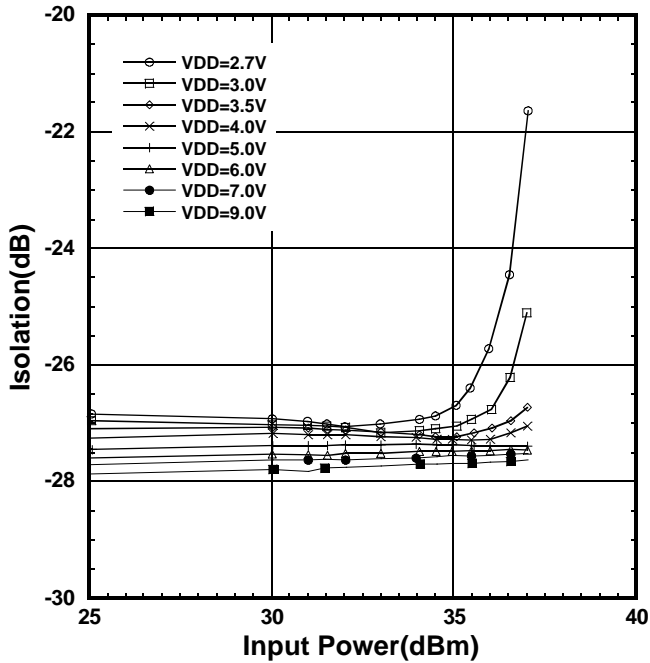
# NJG1516KC3

## ELECTRICAL CHARACTERISTICS

(f=1.0GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)

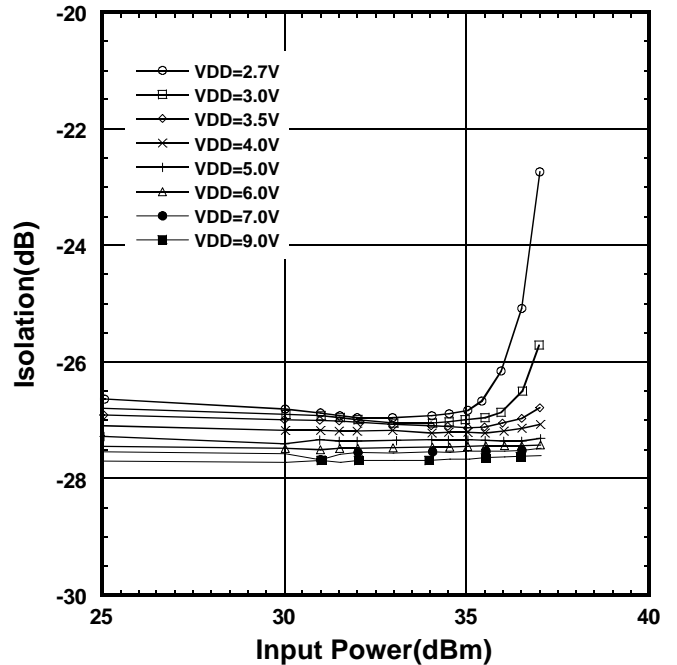
**PC-P1 Isolation vs. Input Power**

(PC-P1, f=1GHz)



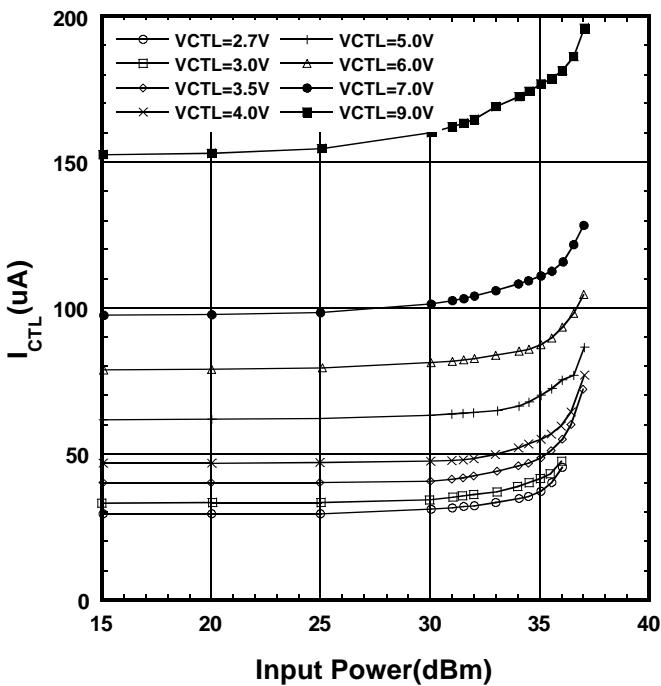
**PC-P2 Isolation vs. Input Power**

(PC-P2, f=1GHz)



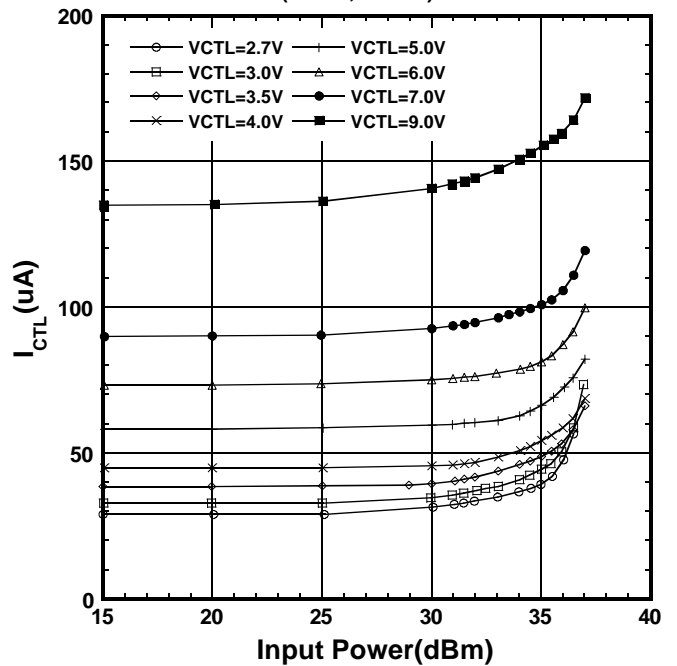
**I<sub>CTL</sub> vs. Input Power**

(PC-P1, f=1GHz)



**I<sub>CTL</sub> vs. Input Power**

(PC-P2, f=1GHz)



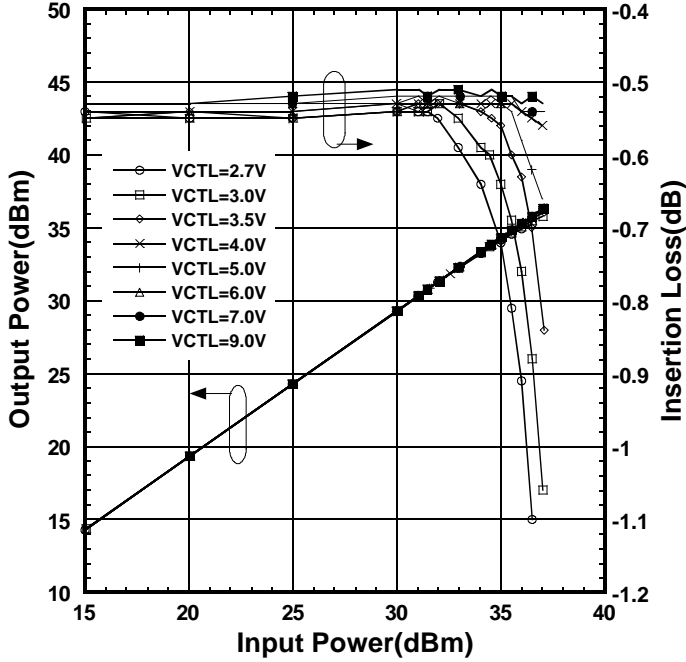


## ELECTRICAL CHARACTERISTICS

(f=1.5GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)

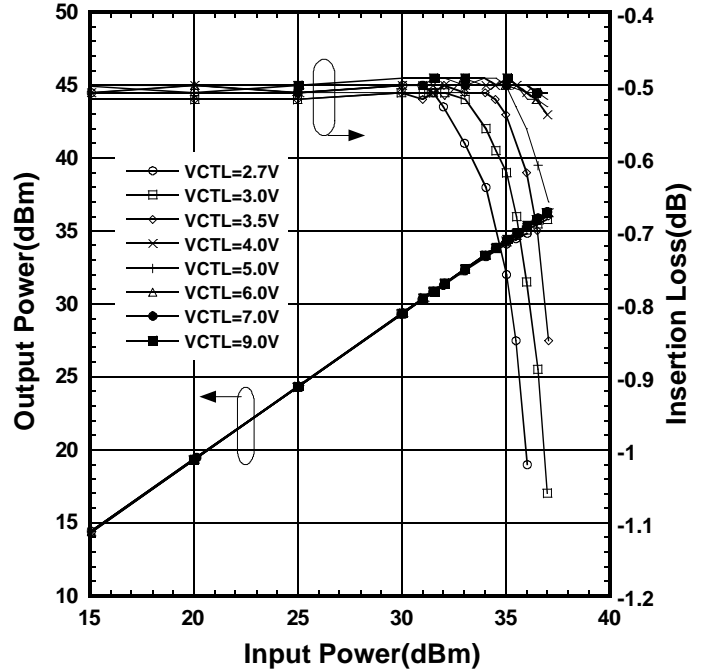
### Output Power, Insertion Loss vs. Input power

(PC-P1, f=1.5GHz)



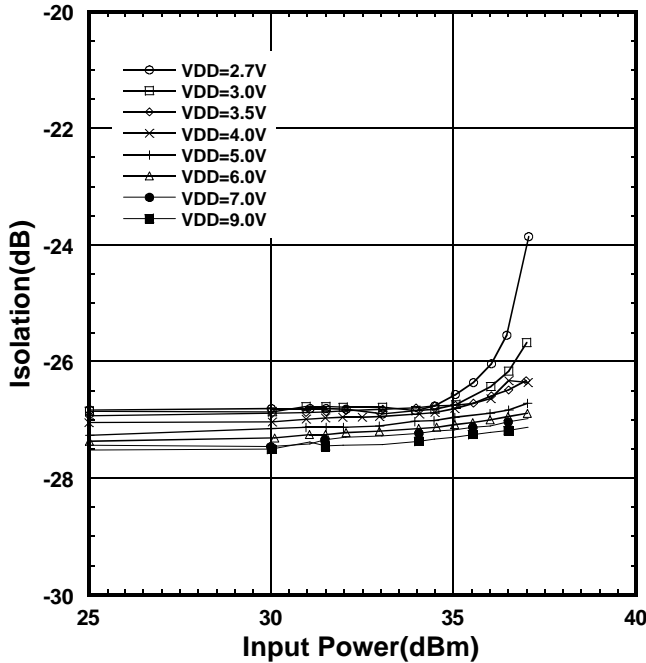
### Output Power, Insertion Loss vs. Input power

(PC-P2, f=1.5GHz)



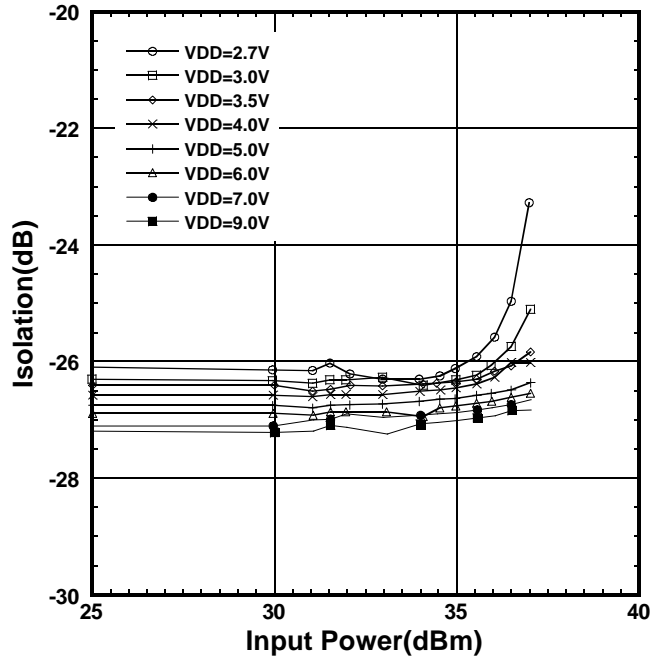
### PC-P1 Isolation vs. Input Power

(PC-P1, f=1.5GHz)



### PC-P2 Isolation vs. Input Power

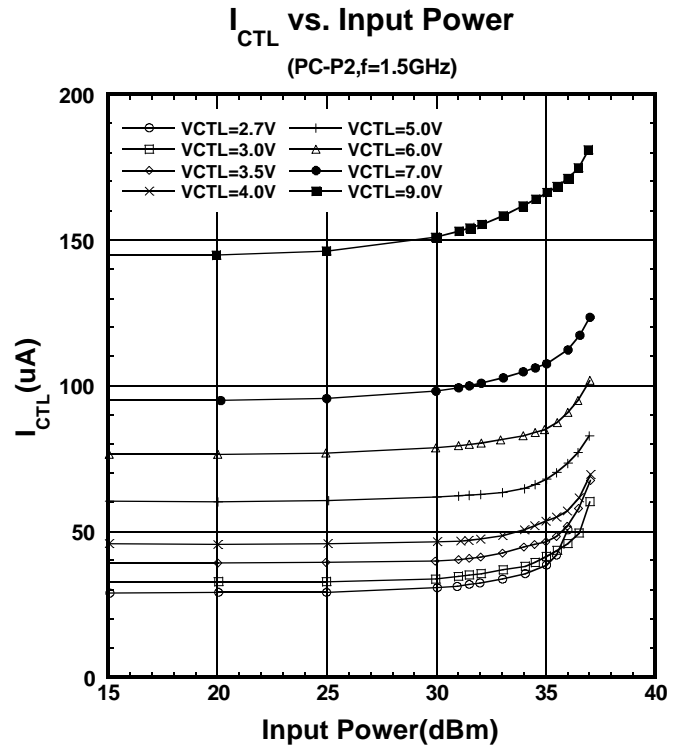
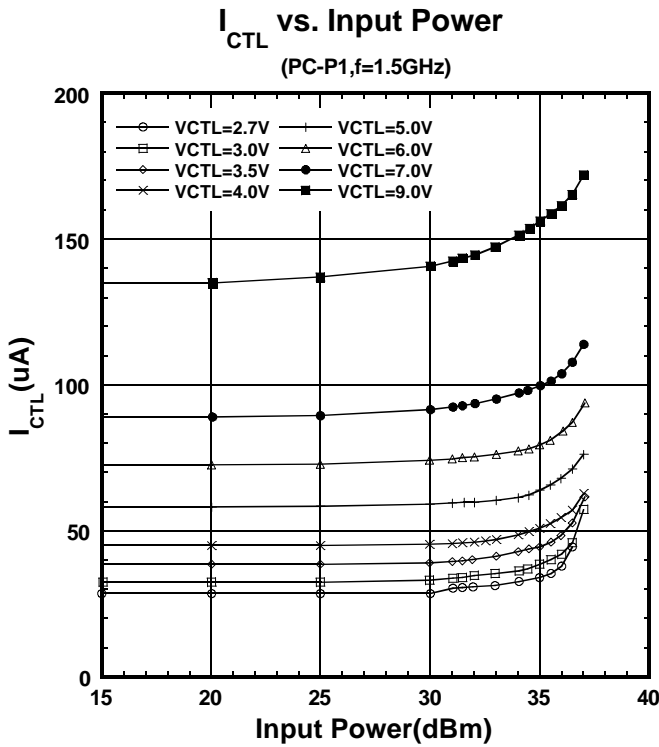
(PC-P2, f=1.5GHz)



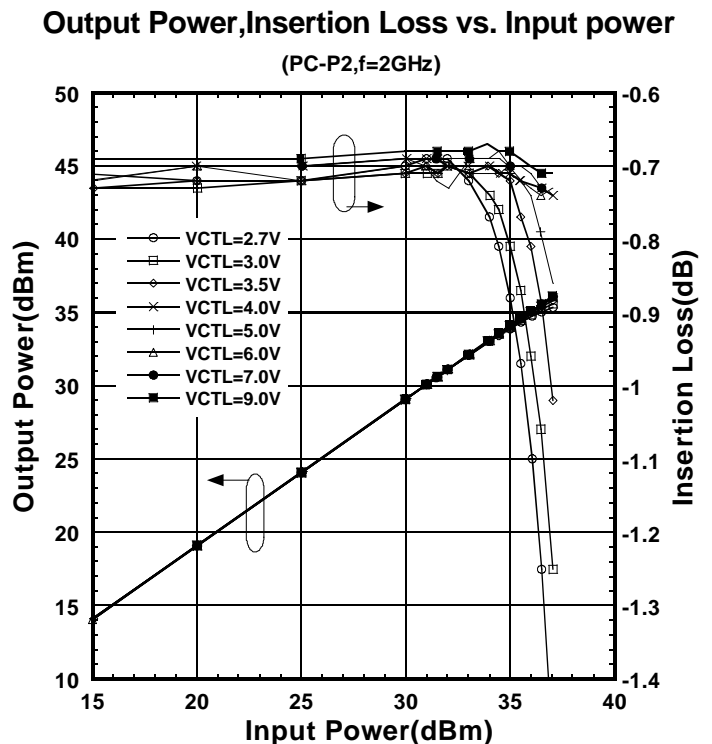
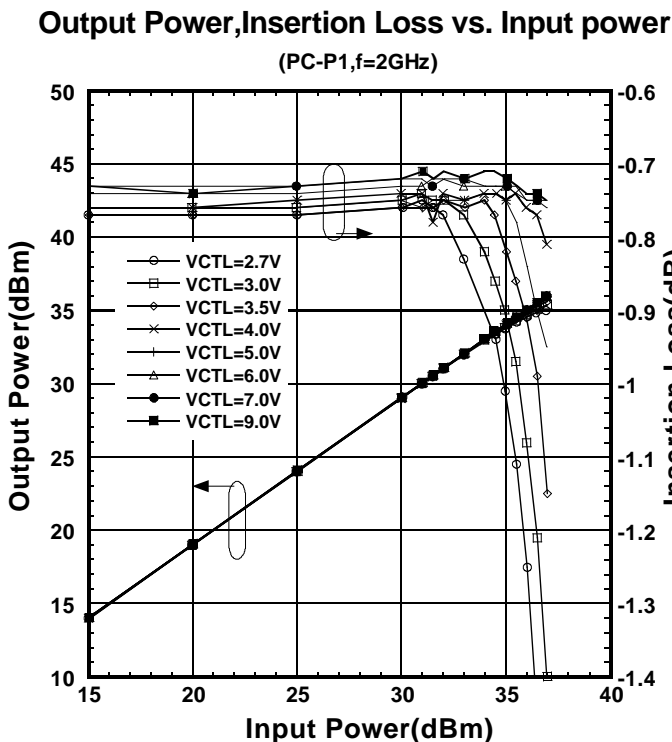
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## ELECTRICAL CHARACTERISTICS

(f=1.5GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)



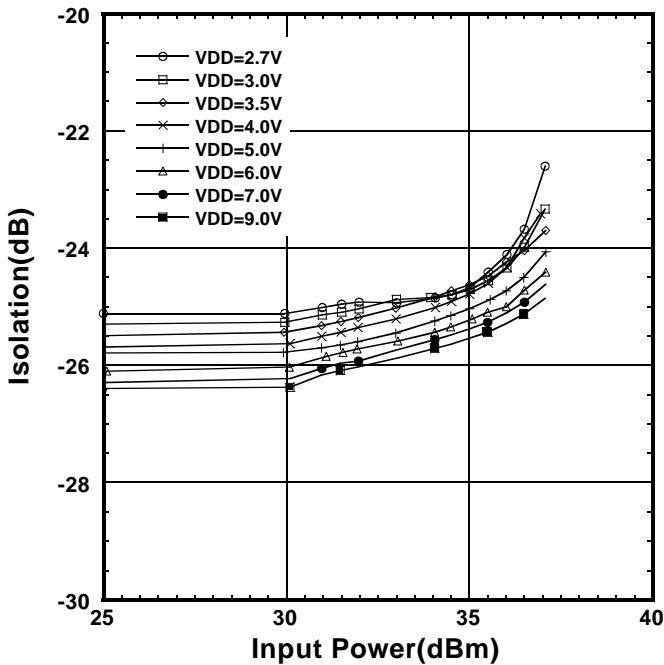
(f=2.0GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)



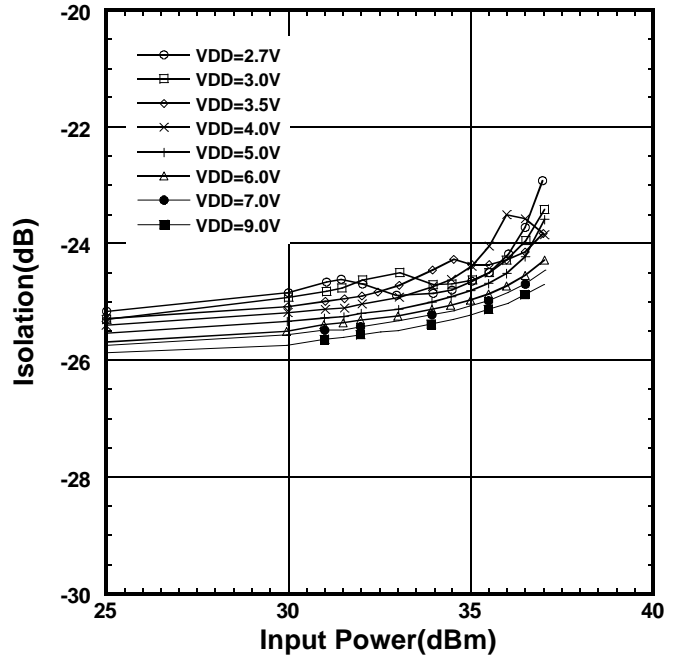
## ■ ELECTRICAL CHARACTERISTICS

(f=2.0GHz, with application circuit 1 (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)

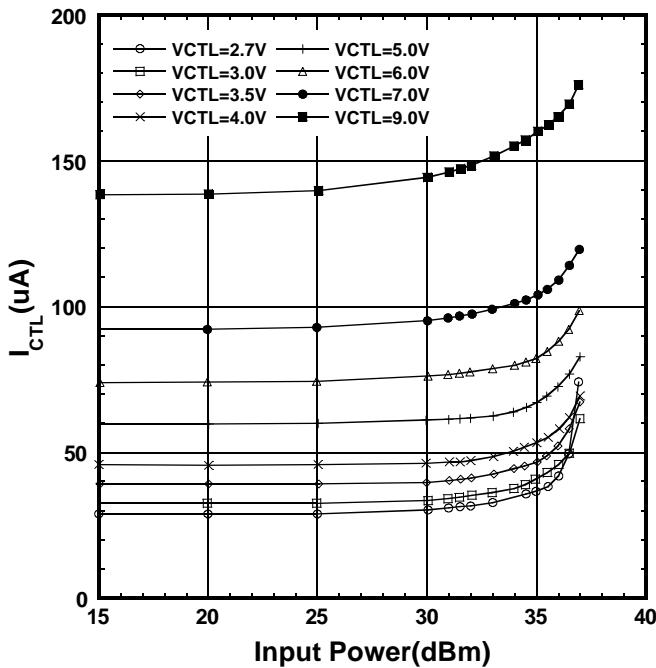
**PC-P1 Isolation vs. Input Power**  
(PC-P1, f=2GHz)



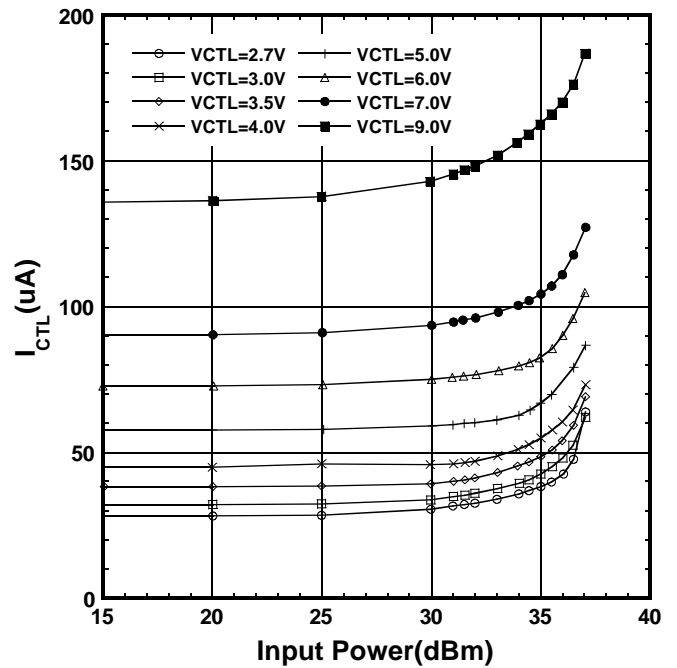
**PC-P2 Isolation vs. Input Power**  
(PC-P2, f=2GHz)



**$I_{CTL}$  vs. Input Power**  
(PC-P1, f=2GHz)

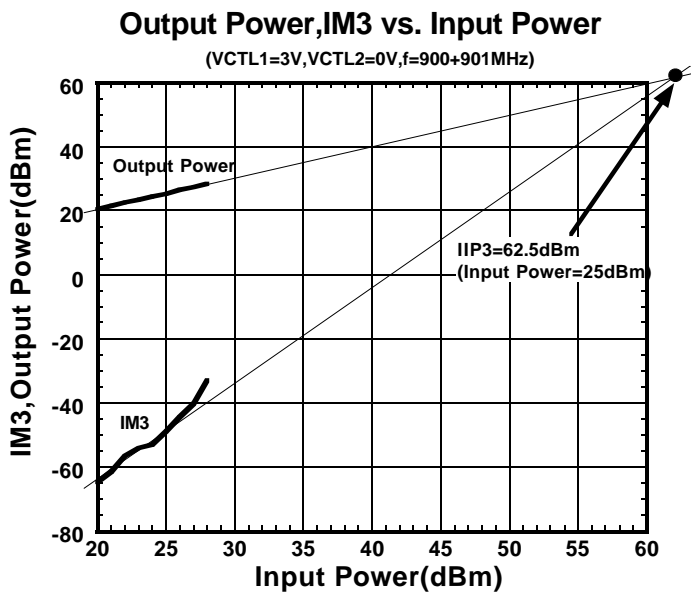
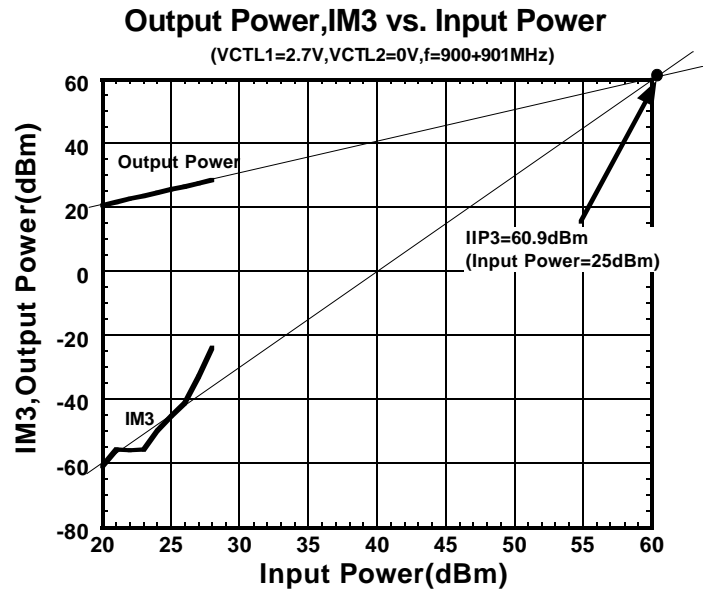
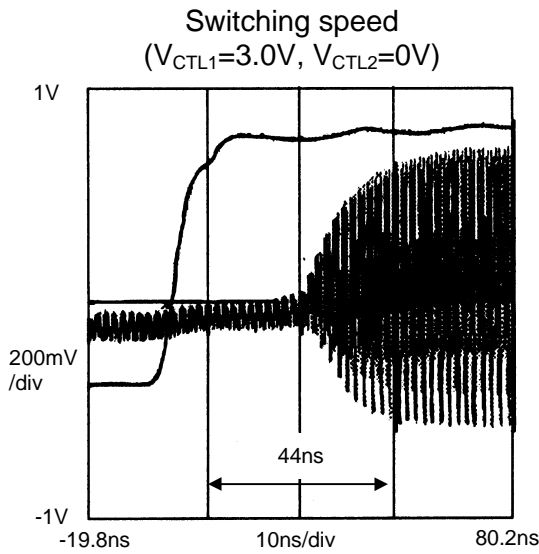


**$I_{CTL}$  vs. Input Power**  
(PC-P2, f=2GHz)



# NJG1516KC3

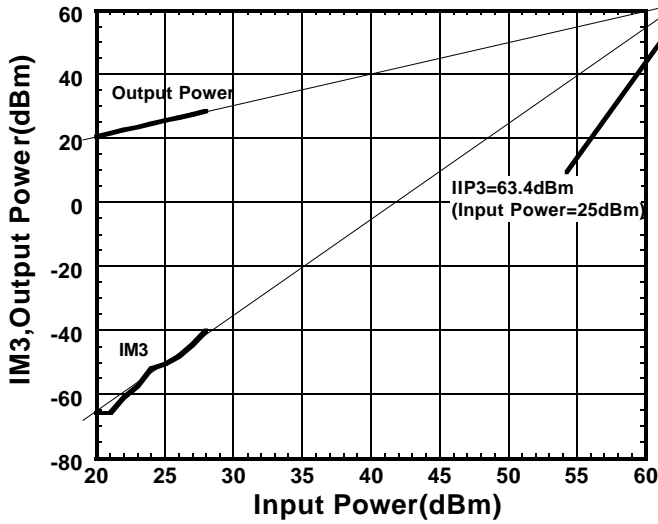
## ■ ELECTRICAL CHARACTERISTICS (with application circuit 1, Parts list 3)



**ELECTRICAL CHARACTERISTICS** (with application circuit 1, Parts list 3)

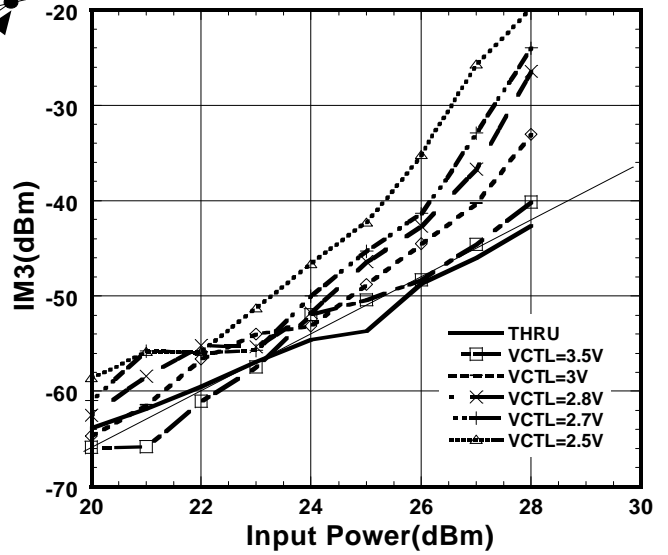
**Output Power, IM3 vs. Input Power**

(VCTL1=3.5V, VCTL2=0V, f=900+901MHz)



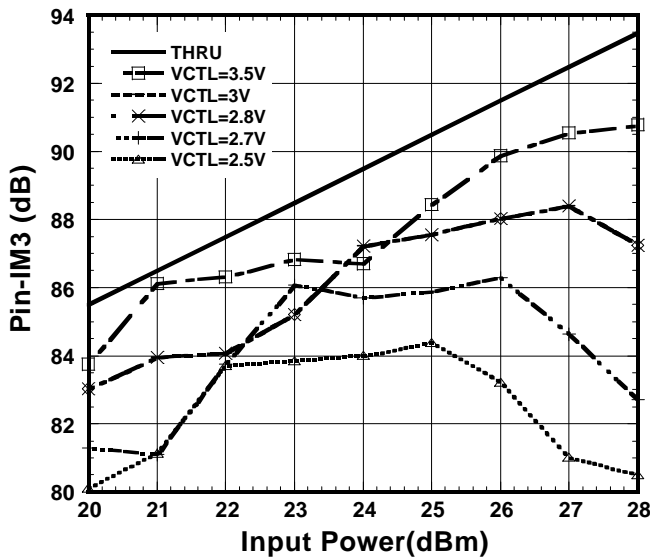
**IM3 vs. Input Power**

(f=900+901MHz)



**Pin-IM3 vs. Input Power**

(f=900+901MHz)

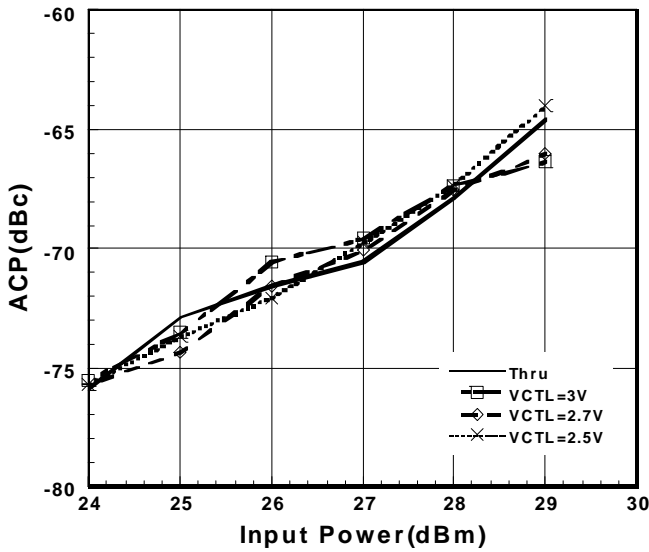


# NJG1516KC3

## ELECTRICAL CHARACTERISTICS (with application circuit 1, Parts list 3)

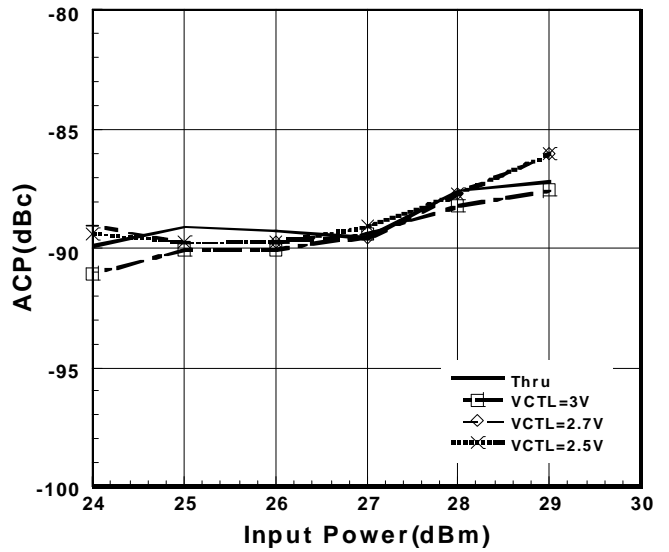
ACP vs. Input Power

(f=1GHz,offset=0.9MHz)



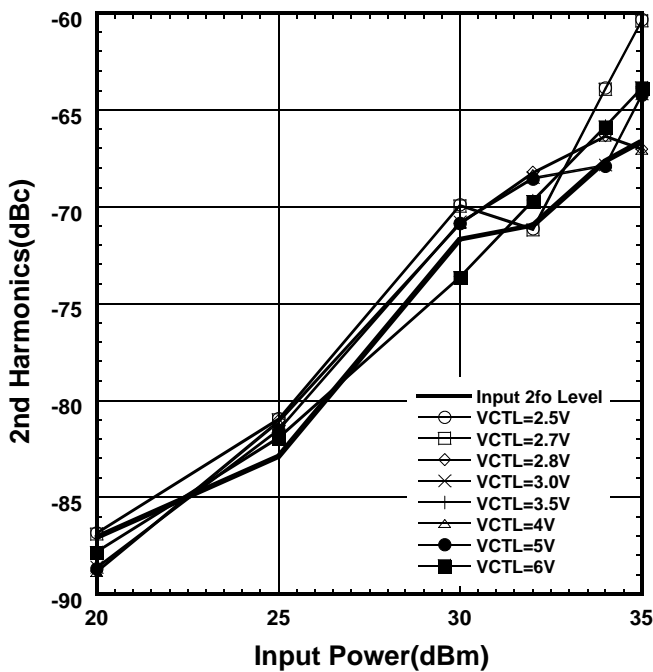
ACP vs. Input Power

(f=1GHz,offset=1.98MHz)



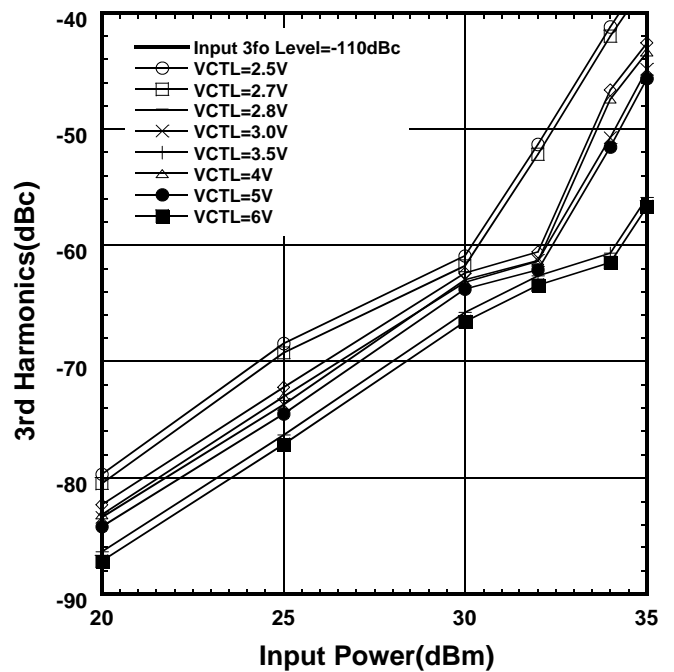
2nd Harmonics vs. Input Power

(f=900MHz)



3rd Harmonics vs. Input Power

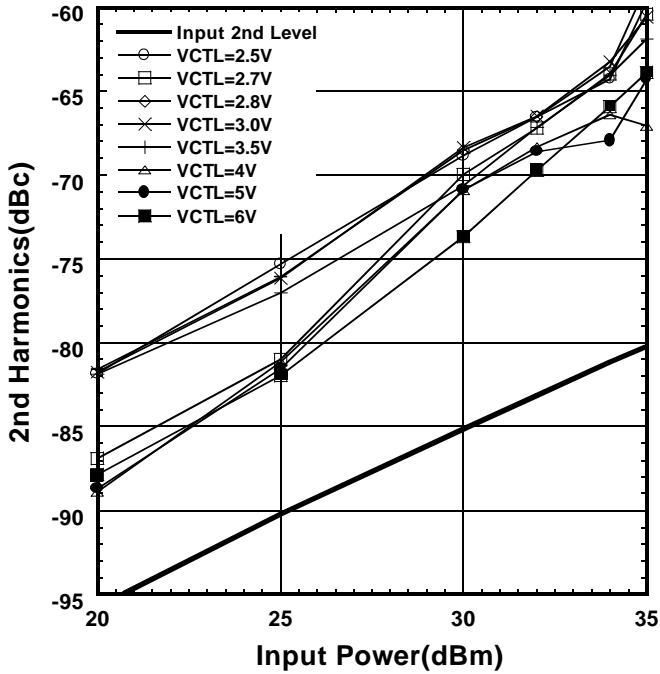
(f=900MHz)



## ■ ELECTRICAL CHARACTERISTICS (with application circuit 1, Parts list 3)

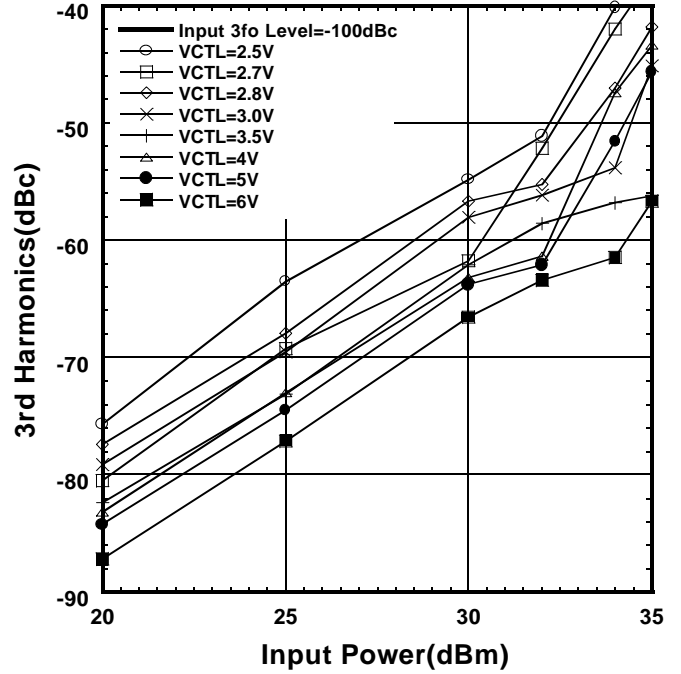
### 2nd Harmonics vs. Input Power

(f=1800MHz)



### 3rd Harmonics vs. Input Power

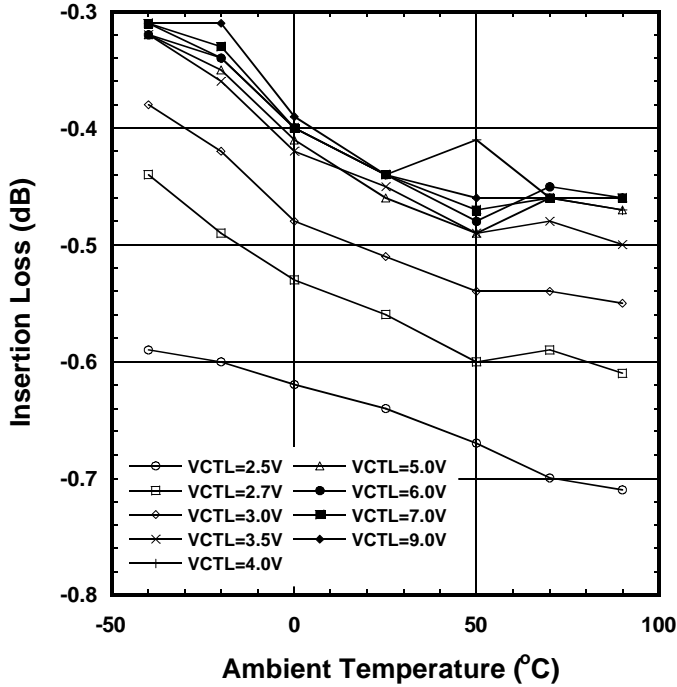
(f=1800MHz)



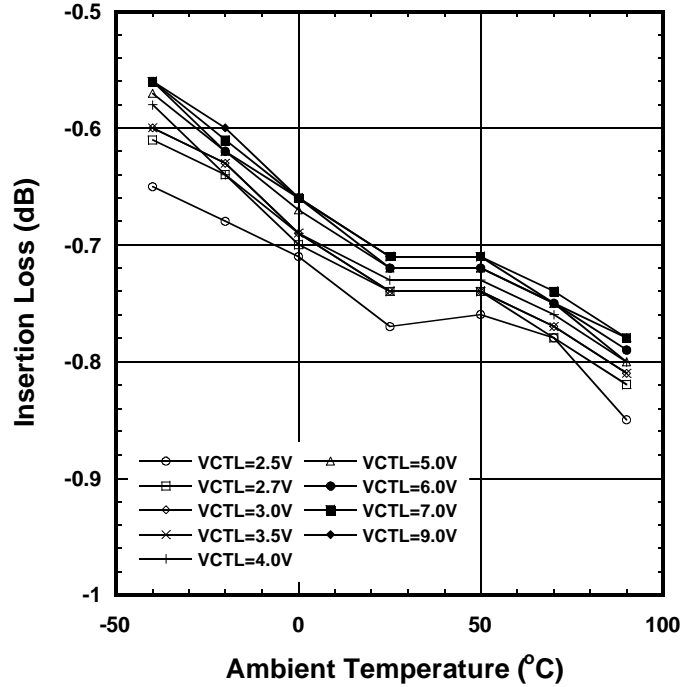
# NJG1516KC3

## TEMPERATURE CHARACTERISTICS (with application circuit 1, Parts list 3)

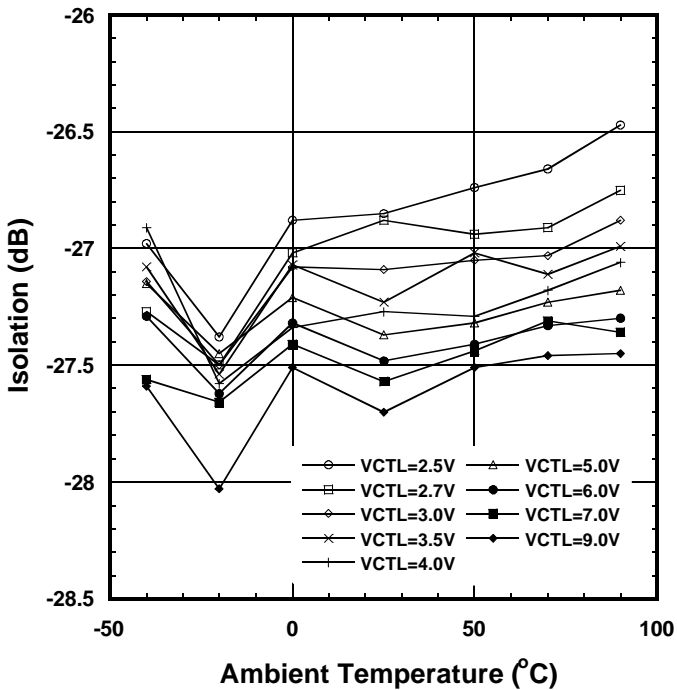
**Insertion Loss vs. Ambient Temperature**  
(PC-P1, f=1GHz, Input Power=34.5dBm)



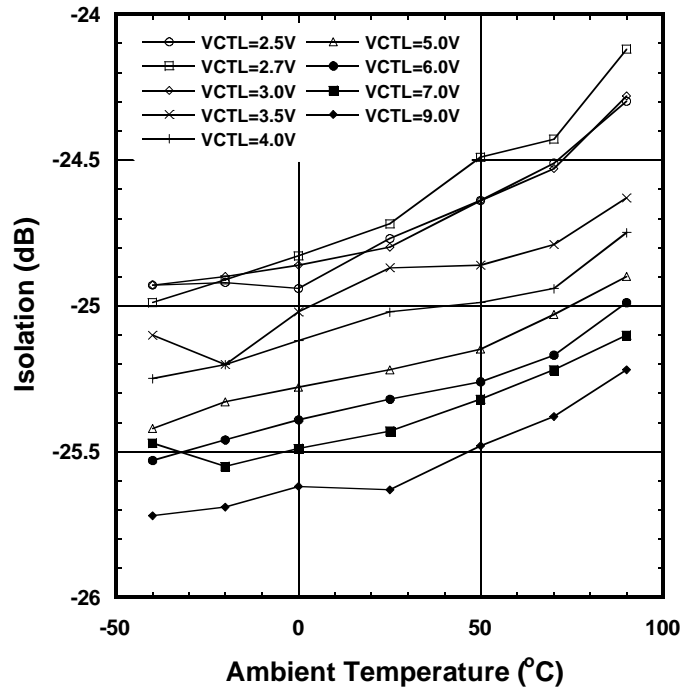
**Insertion Loss vs. Ambient Temperature**  
(PC-P1, f=2GHz, Input Power=31.5dBm)



**Isolation vs. Ambient Temperature**  
(PC-P1, f=1GHz, Input Power=34.5dBm)



**Isolation vs. Ambient Temperature**  
(PC-P1, f=2GHz, Input Power=31.5dBm)

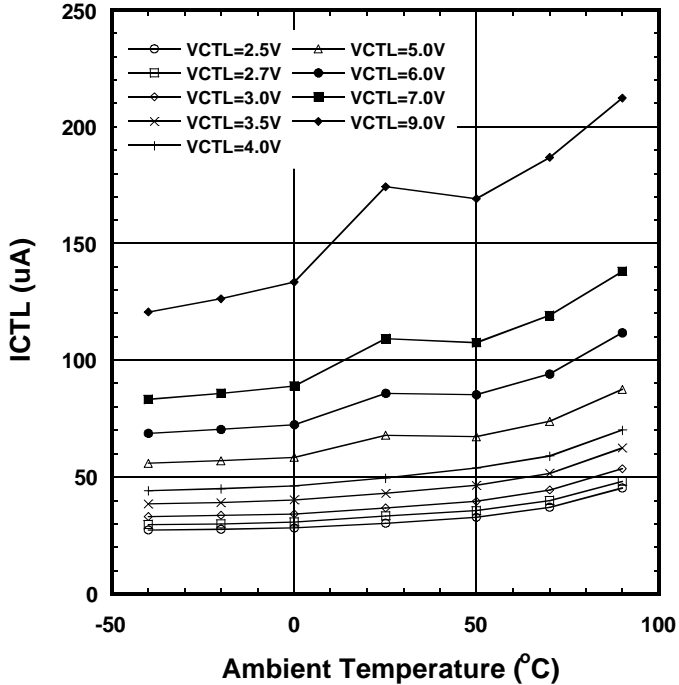




## TEMPERATURE CHARACTERISTICS (with application circuit 1, Parts list 3)

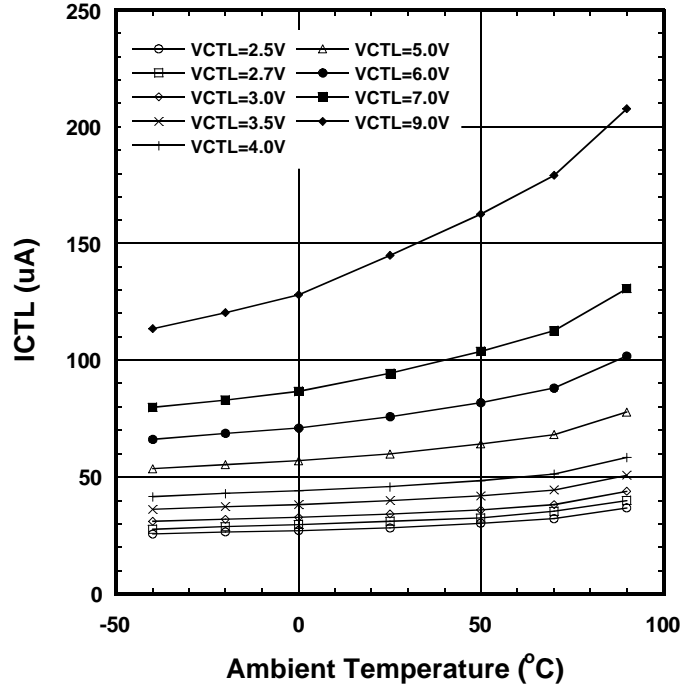
### ICTL vs. Ambient Temperature

(PC-P1, f=1GHz, Input Power=34.5dBm)



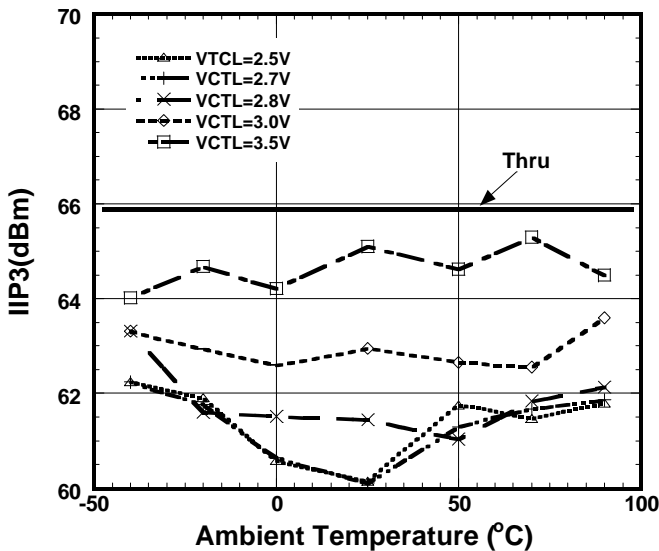
### ICTL vs. Ambient Temperature

(PC-P1, f=2GHz, Input Power=31.5dBm)



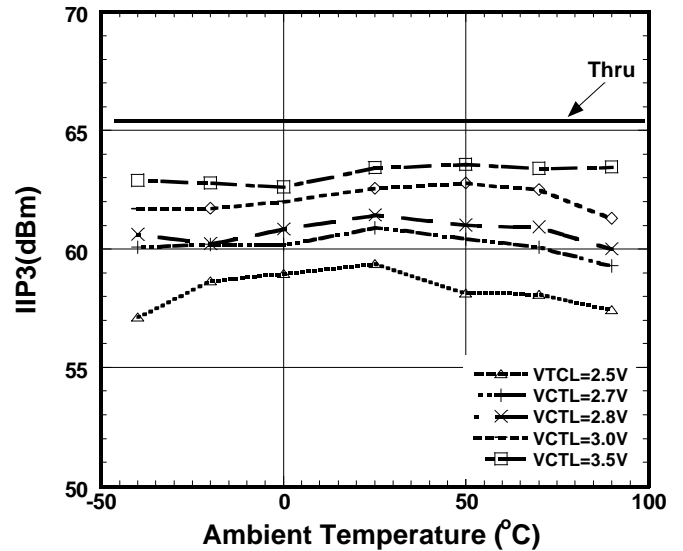
### IIP3 vs. Ambient Temperature

(PC-P1, f=900+901MHz, Input Power=21dBm)



### IIP3 vs. Ambient Temperature

(PC-P1, f=900+901MHz, Input Power=25dBm)

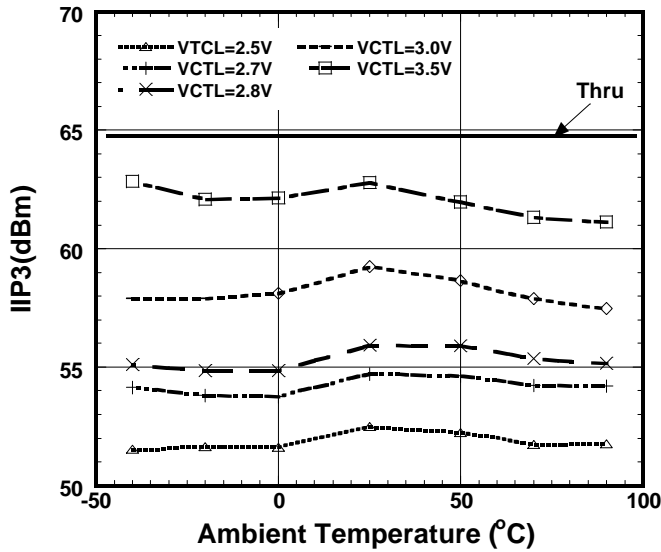


# NJG1516KC3

## TEMPERATURE CHARACTERISTICS (with application circuit 1, Parts list 3)

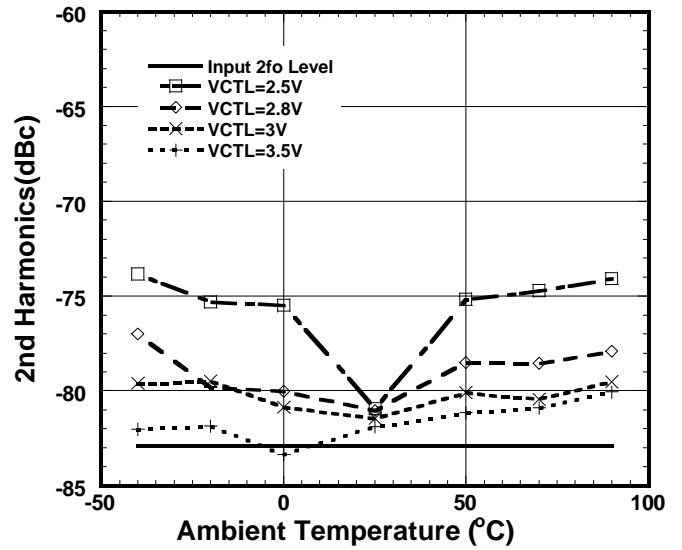
### IIP3 vs. Ambient Temperature

(PC-P1, f=900+901MHz, Input Power=28dBm)



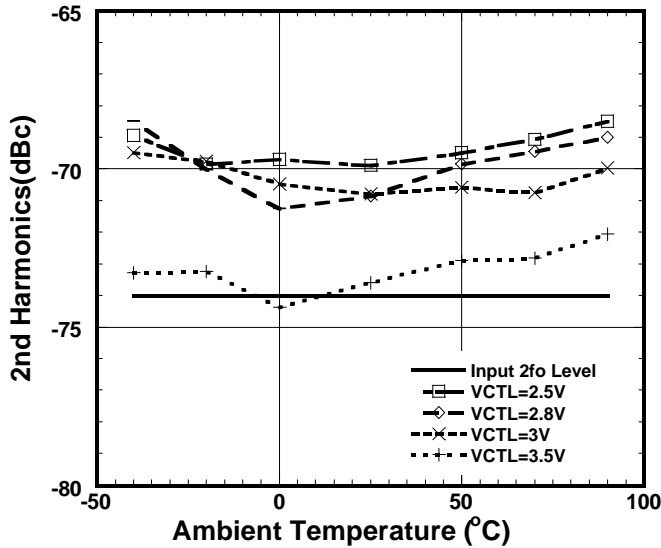
### 2nd Harmonics vs. Ambient Temperature

(f=900MHz, Input Power=25dBm)



### 2nd Harmonics vs. Ambient Temperature

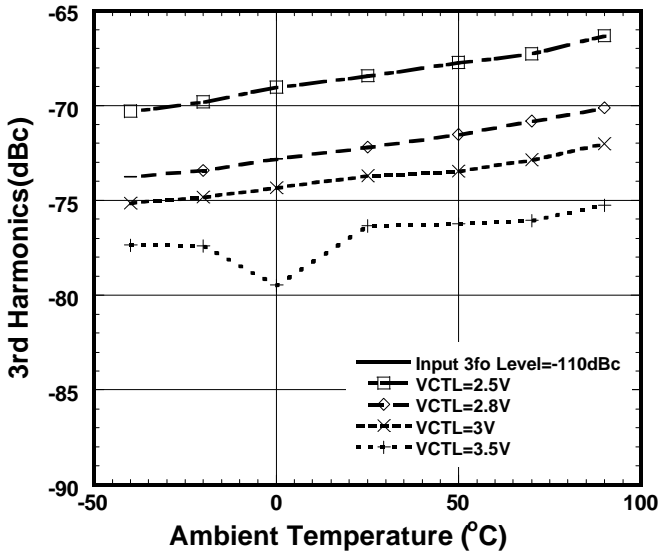
(f=900MHz, Input Power=30dBm)



## TEMPERATURE CHARACTERISTICS (with application circuit 1, Parts list 3)

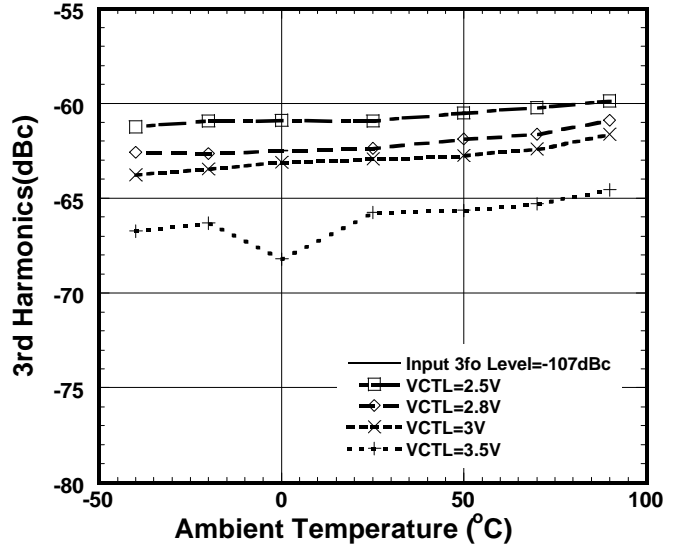
### 3rd Harmonics vs. Ambient Temperature

(f=900MHz, Input Power=25dBm)



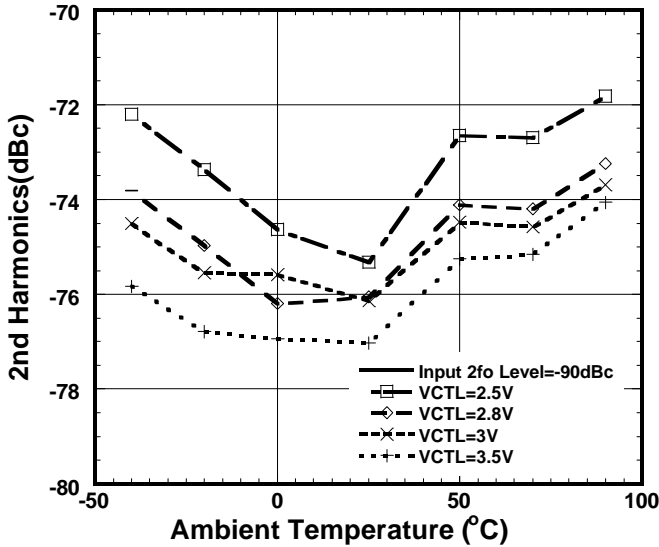
### 3rd Harmonics vs. Ambient Temperature

(f=900MHz, Input Power=30dBm)



### 2nd Harmonics vs. Ambient Temperature

(f=1800MHz, Input Power=25dBm)

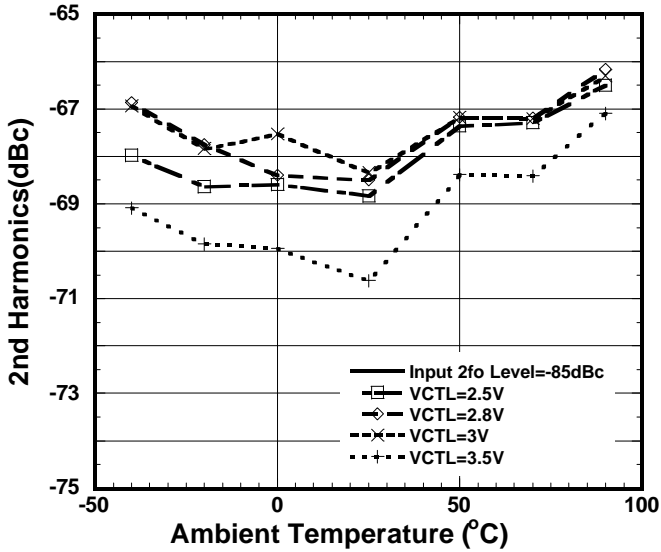


# NJG1516KC3

## TEMPERATURE CHARACTERISTICS (with application circuit 1, Parts list 3)

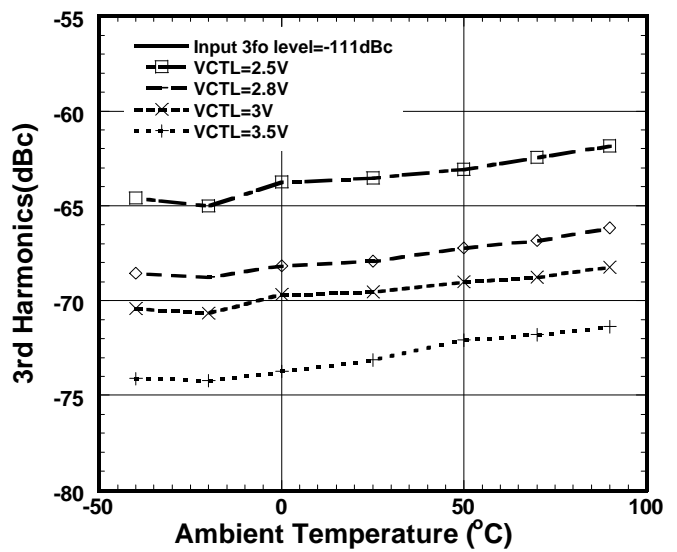
### 2nd Harmonics vs. Ambient Temperature

(f=1800MHz, Input Power=30dBm)



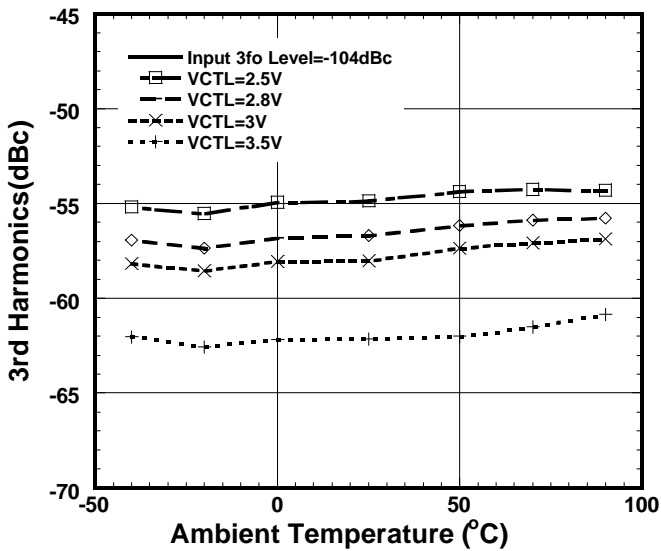
### 3rd Harmonics vs. Ambient Temperature

(f=1800MHz, Input Power=25dBm)



### 3rd Harmonics vs. Ambient Temperature

(f=1800MHz, Input Power=30dBm)

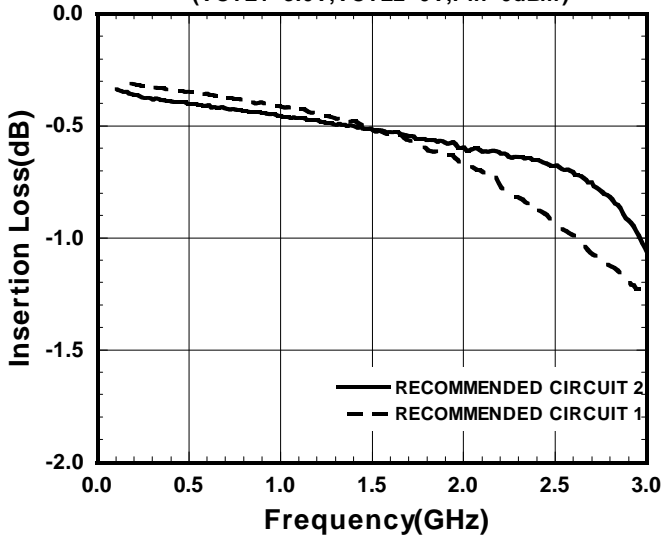


## ■ ELECTRICAL CHARACTERISTICS

(f=50MHz~3.0GHz, with application circuit 2, losses of PCB, connector and DC blocking capacitor are excluded)

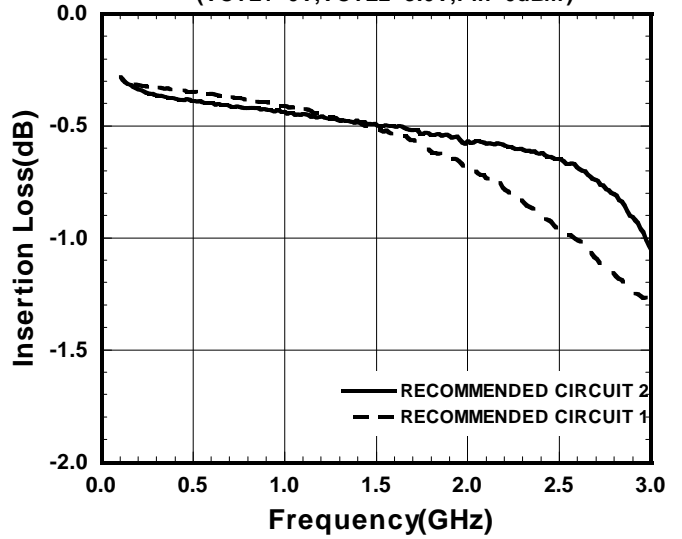
### PC-P1 Insertion Loss vs. Frequency

(VCTL1=3.0V, VCTL2=0V, Pin=0dBm)



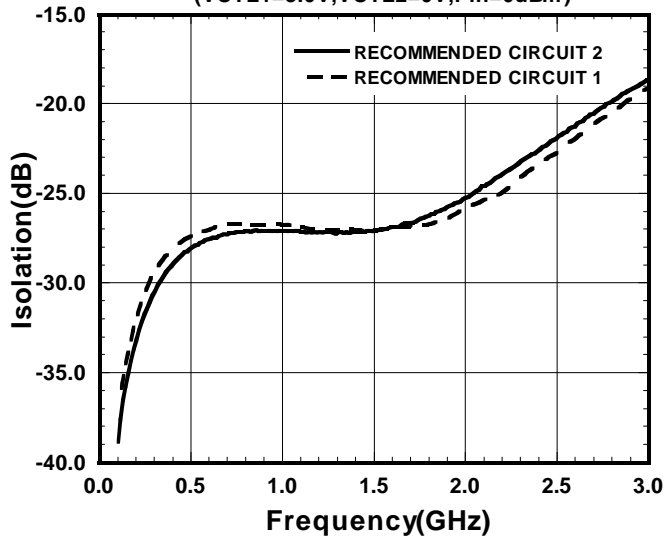
### PC-P2 Insertion Loss vs. Frequency

(VCTL1=0V, VCTL2=3.0V, Pin=0dBm)



### PC-P1 Isolation vs. Frequency

(VCTL1=3.0V, VCTL2=0V, Pin=0dBm)



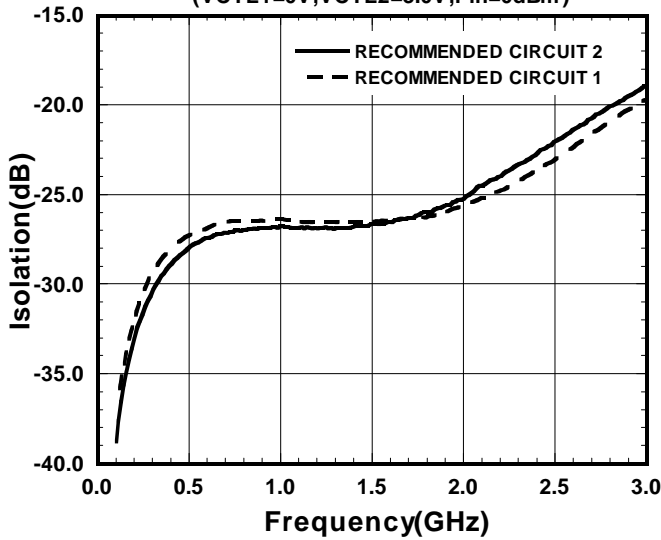
# NJG1516KC3

## ELECTRICAL CHARACTERISTICS

(f=50MHz~3.0GHz, with application circuit 2, losses of PCB, connector and DC blocking capacitor are excluded)

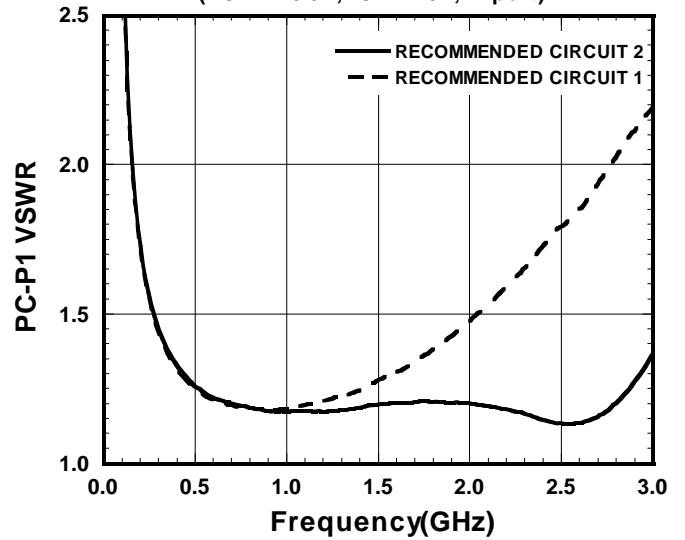
### PC-P2 Isolation vs. Frequency

(VCTL1=0V, VCTL2=3.0V, Pin=0dBm)



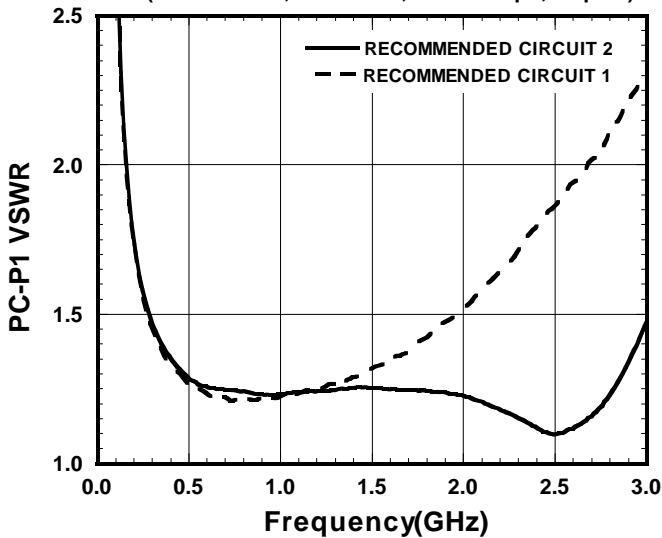
### PC-P1 VSWR vs. Frequency

(VCTL1=3.0V, VCTL2=0V, P1 port)

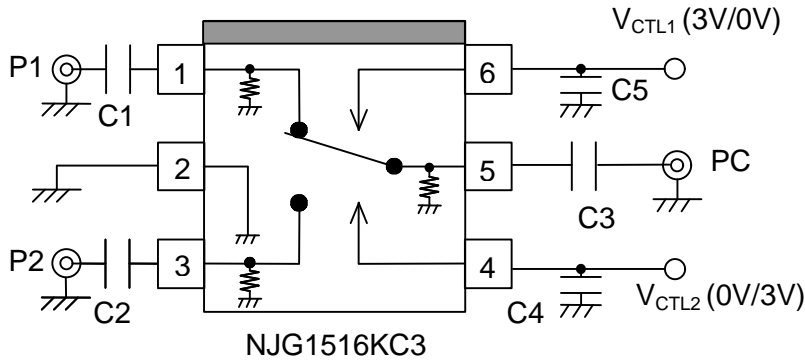


### PC-P1 VSWR vs. Frequency

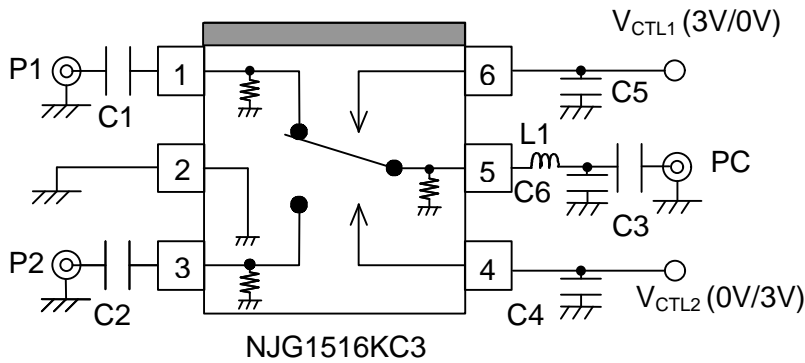
(VCTL1=3.0V, VCTL2=0V, DC cut=56pF, PC port)



## APPLICATION CIRCUIT 1 (Parts list 1~3)



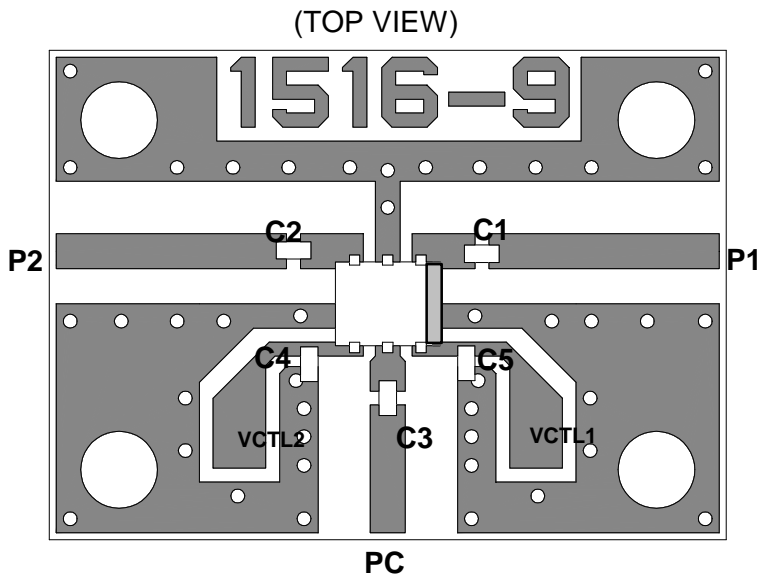
## APPLICATION CIRCUIT 2 (for 2GHz or above, Parts list 4)



| No.    | List 1                 | List 2                  | List 3                  | List 4                  |
|--------|------------------------|-------------------------|-------------------------|-------------------------|
|        | $f_{in}=50$<br>~100MHz | $f_{in}=0.1$<br>~0.5GHz | $f_{in}=0.5$<br>~2.0GHz | $f_{in}=2.0$<br>~2.5GHz |
| C1~C3  | 0.01uF                 | 1000pF                  | 56pF                    | 56pF                    |
| C4, C5 | 10pF                   | 10pF                    | 10pF                    | 10pF                    |
| C6     | -                      | -                       | -                       | 0.75pF                  |
| L1     | -                      | -                       | -                       | 2.2nH                   |

# NJG1516KC3

## RECOMMENDED PCB DESIGN



Circuit losses including losses of capacitors and connectors

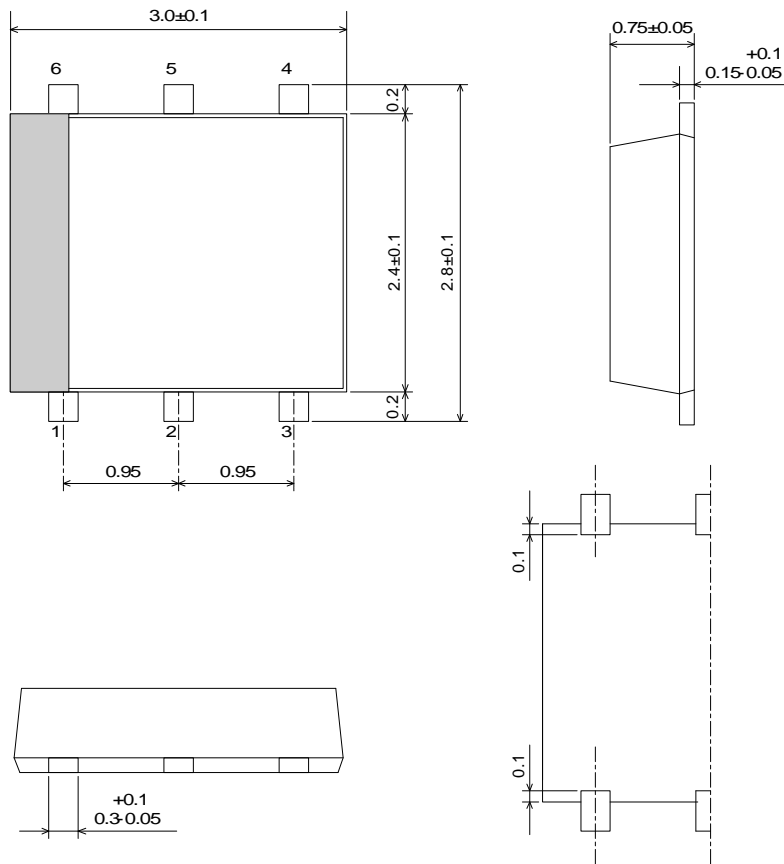
| freq[GHz] | LOSS[dB] |
|-----------|----------|
| 0.8       | 0.11     |
| 1.0       | 0.13     |
| 1.5       | 0.16     |
| 1.8       | 0.20     |
| 2.0       | 0.22     |
| 2.5       | 0.26     |

## PRECAUTIONS

- [1]The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC.
- [2]Bypass capacitors (C4, C5) should be placed close to terminals of V<sub>CTL1</sub>, V<sub>CTL2</sub> to reduce stripline influence of RF characteristics.
- [3]For good isolation, the GND terminal (2nd pin) must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.



## PACKAGE OUTLINE



Lead material : Copper  
 Lead surface finish : Solder plating  
 Molding material : Epoxy resin  
 UNIT : mm  
 Weight : 14mg

### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.