SPDT SWITCH GaAs MMIC

■GENERAL DESCRIPTION

NJG1517KB2 is a GaAs SPDT switch suited for RF receiving circuit of cellular phone handsets.

This switch features very low loss, high isolation and exhibits wide operating frequency range from 50MHz to 3.0GHz at low voltage of 2.5V.

The Ultra small & ultra thin FLP6 package is applied.

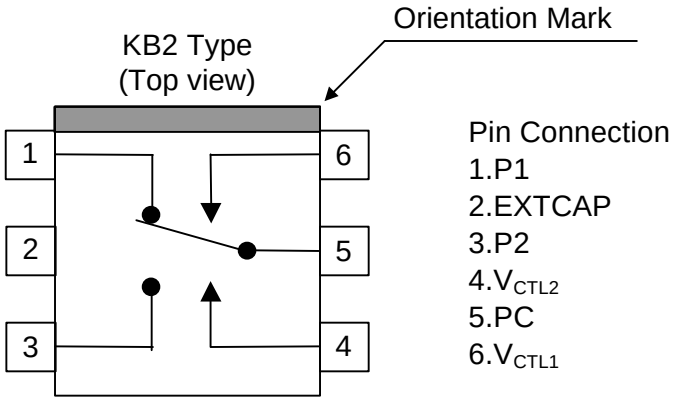
■PACKAGE OUTLINE

NJG1517KB2

■FEATURES

●Single low voltage control	+2.5~+6.5V
●Low insertion loss	0.3dB typ. @f=1GHz, P_{in}=0dBm
●High isolation	27dB typ. @f=1GHz, P_{in}=0dBm
●Handling power	20dBm max. @f=2GHz, V_{CTL}=2.7V
●Low current consumption	5uA typ. @f=2GHz, P_{in}=10dBm, R1=560kΩ
●Ultra small & ultra thin package	FLP6-B2 (Mount Size: 2.1x2.0x0.75mm)

■PIN CONFIGURATION



Pin Connection
1.P1
2.EXTCAP
3.P2
4.V_{CTL2}
5.PC
6.V_{CTL1}

■TRUTH TABLE

"H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$

V_{CTL1}	H	L	L	H
V_{CTL2}	L	H	L	H
P1-PC	ON	OFF	Insertion Loss=13dB P_1 Return Loss=-3dB	Insertion Loss=13dB P_1 Return Loss=-2dB
P2-PC	OFF	ON	Insertion Loss=13dB P_2 Return Loss=-3dB	Insertion Loss=13dB P_2 Return Loss=-2dB

NOTE: The values of insertion losses and return losses are typical values at 2.0GHz.

■ABSOLUTE MAXIMUM RATINGS

(T_a=25°C, Z_S=Z_I=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Input Power	P_{in}	$V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V	28	dBm
Control Voltage	V_{CTL}	$V_{CTL\ (H)}$ - $V_{CTL\ (L)}$	7.5	V
Power Dissipation	P_D	19.4x14.0x0.2mm FR4 Assembled Board, Tj=125°C	450	mW
Operating Temp.	T_{opr}		-30~+85	°C
Storage Temp.	T_{stg}		-55~+125	°C

■ELECTRICAL CHARACTERISTICS

($V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V, Z_S=Z_I=50Ω, R1=560KΩ, C6=10pF, T_a=25°C)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control voltage (Low)	$V_{CTL\ (L)}$		-0.2	0	0.2	V
Control voltage (High)	$V_{CTL\ (H)}$		2.5	2.7	6.5	V
Control current	I_{CTL}	f=2.0GHz, P_{in}=10dBm	-	5	6	uA
Insertion loss 1	LOSS1	f=1.0GHz, P_{in}=0dBm	-	0.3	0.6	dB
Insertion loss 2	LOSS2	f=2.0GHz, P_{in}=0dBm	-	0.5	0.8	dB
Isolation 1 (PC-P1, PC-P2, P1-P2)	ISL1	f=1.0GHz, P_{in}=0dBm	25	27	-	dB
Isolation 2 (PC-P1, PC-P2, P1-P2)	ISL2	f=2.0GHz, P_{in}=0dBm, C6=5pF	21	23	-	dB
Pin at 1dB compression point	P_{-1dB}	f=2.0GHz	20	23	-	dBm
VSWR (PC, P1, P2)	VSWR	f=0.05~2.5GHz, ON State	-	1.3	1.6	
Switching time	T_{SW}	f=0.05~2.5GHz	-	15	-	ns

* The control current ICTL depends on the resistance of R1. Smaller resistance of R1 make larger control current.

■TERMINAL INFORMATION

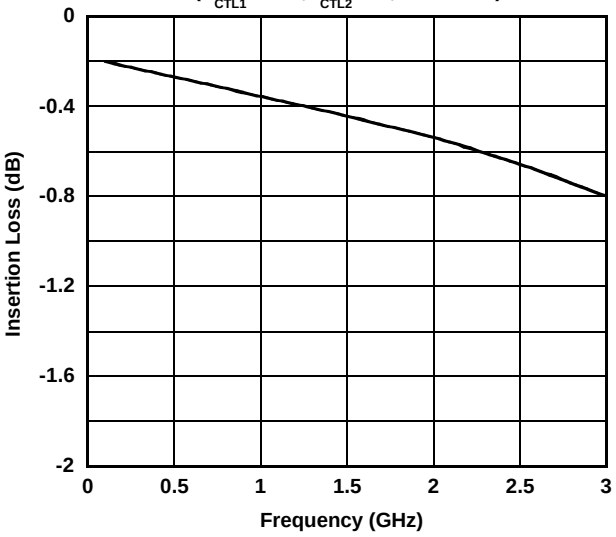
No.	SYMBOL	DESCRIPTIONS
1	P1	RF port. This port is connected with PC port by controlling 6th pin ($V_{CTL\ (H)}$) to 2.5~6.5V and 4th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01µF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
2	EXTCAP	External capacitor terminal. The isolation characteristics depends on the value of the capacitor which connected with GND. An external capacitor is required to block the DC bias voltage of internal circuit. (50MHz~1.7GHz: 10pF, 1.7~2.5GHz: 5pF)
3	P2	RF port. This port is connected with PC port by controlling 4th pin($V_{CTL(H)}$) to 2.5 – 6.5V and 6th pin($V_{CTL(L)}$) to -0.2~+0.2V. In order to block the DC bias voltage of internal circuit, an external capacitor is required. (50~100MHz: 0.01µF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
4	V_{CTL2}	Control port 2. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 6th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range.
5	PC	Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required. (50~100MHz: 0.01µF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
6	V_{CTL1}	Control port 1. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 4th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range.

■ELECTRICAL CHARACTERISTICS

(100MHz~3GHz, with application circuit, R1=560KΩ, C6=10pF, Losses of external circuit are excluded)

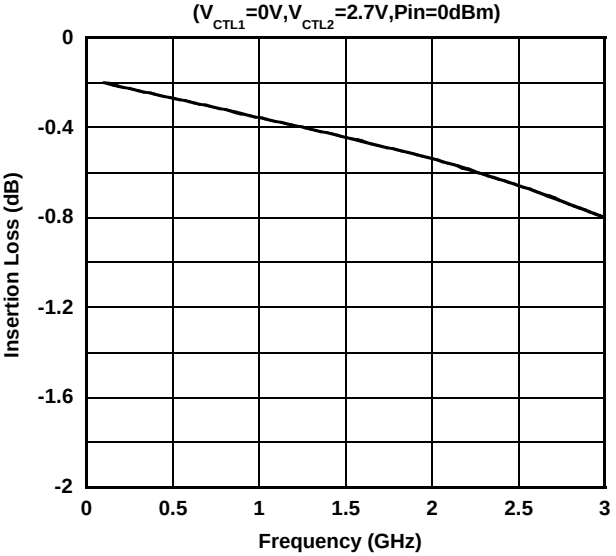
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



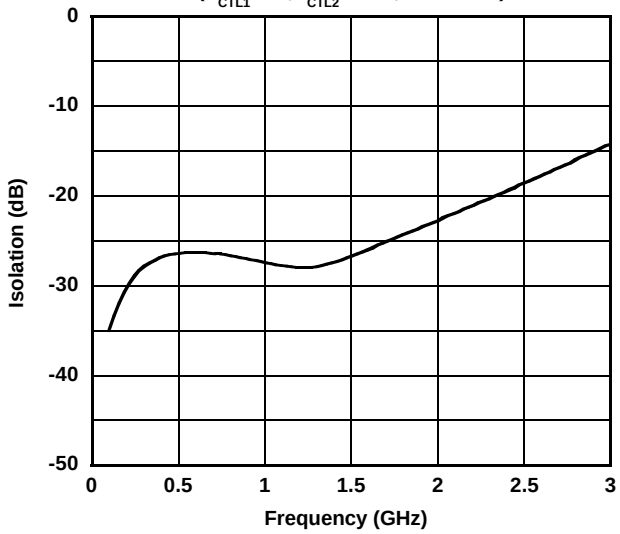
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



PC-P1 Isolation vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



PC-P2 Isolation vs. Frequency

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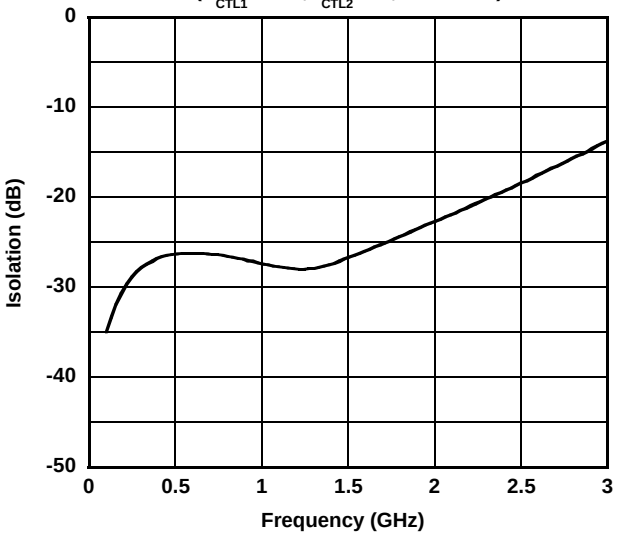
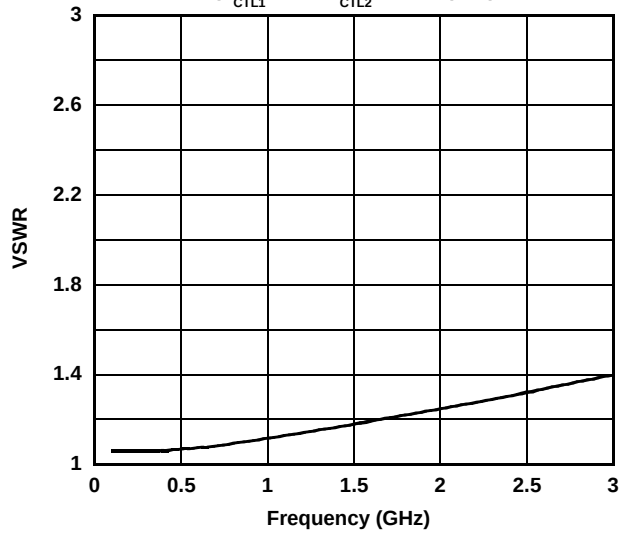


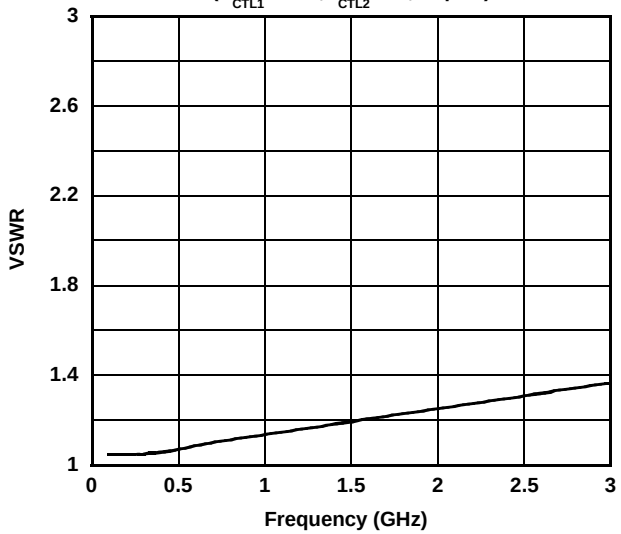
PC-P1 VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,PC port)



P1-PC VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,P1 port)

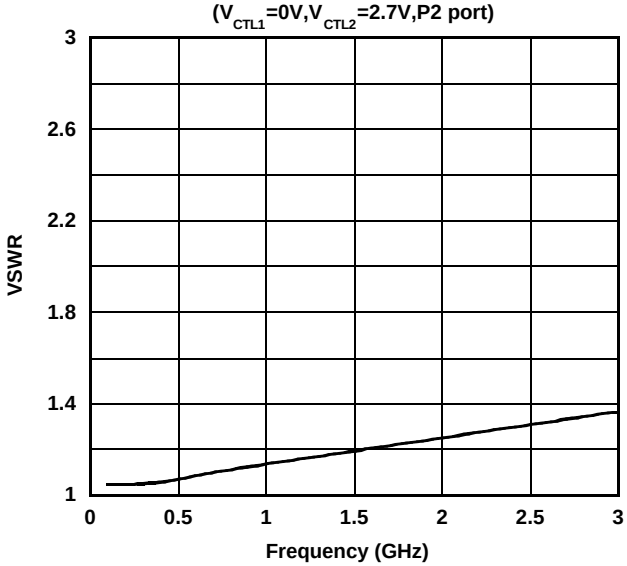


■ELECTRICAL CHARACTERISTICS

(with application circuit, without DC Blocking Capacitor, Losses of external circuit are excluded)

P2-PC VSWR vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,P2 port)



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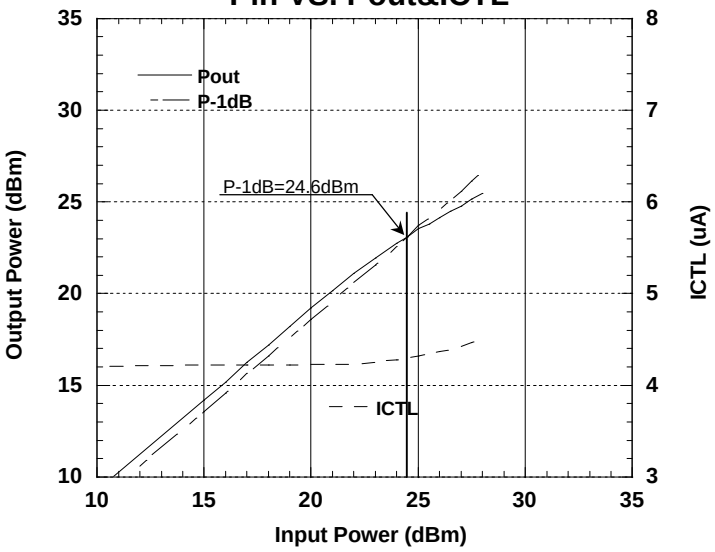
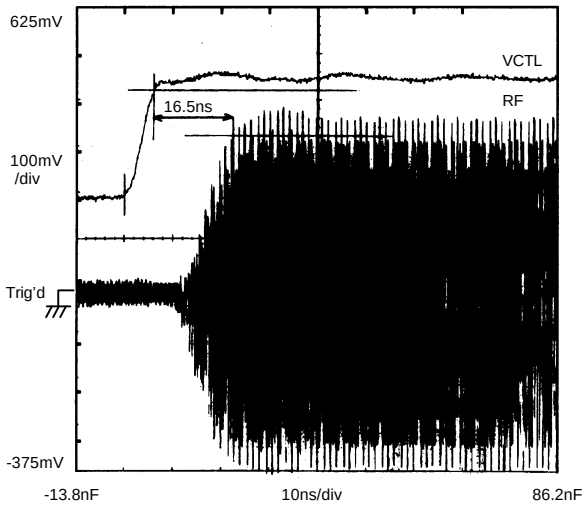
Pin VS. Pout&ICTL



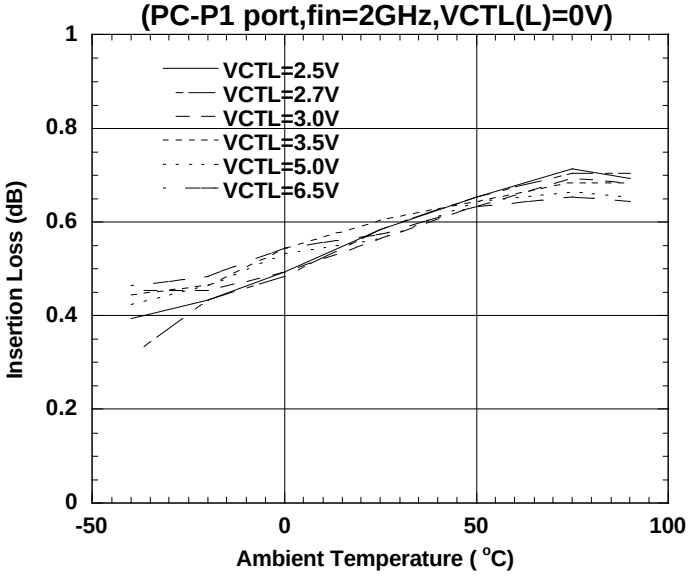
Switching Speed

($V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V)



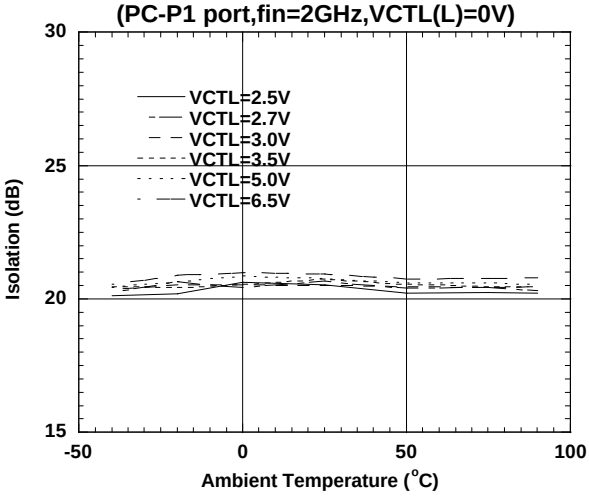
Insertion Loss vs. Ambient Temperature

(PC-P1 port,fin=2GHz,VCTL(L)=0V)



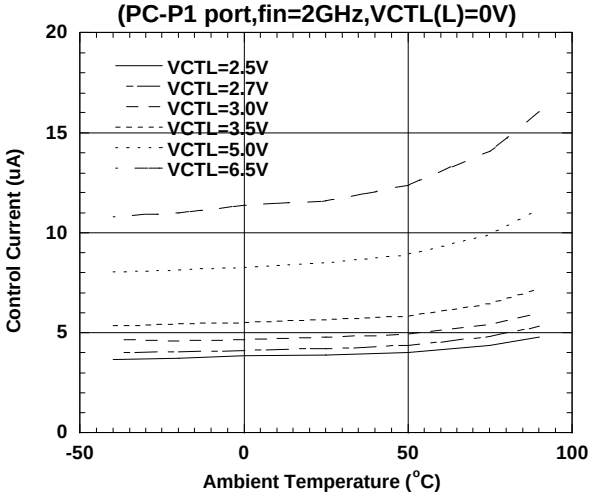
Isolation vs. Ambient Temperature

(PC-P1 port,fin=2GHz,VCTL(L)=0V)



ICTL vs. Ambient Temperature

(PC-P1 port,fin=2GHz,VCTL(L)=0V)

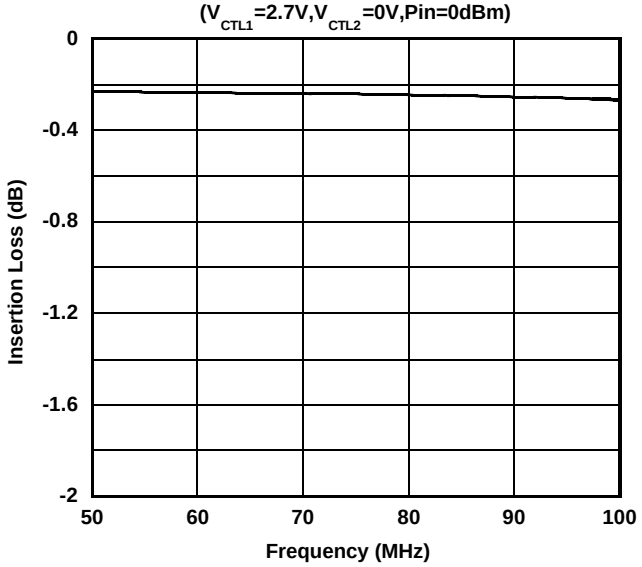


■ELECTRICAL CHARACTERISTICS

(50MHz~100MHz, with Application circuit (Parts list 1), Losses of PCB, connector and DC blocking capacitor are included)

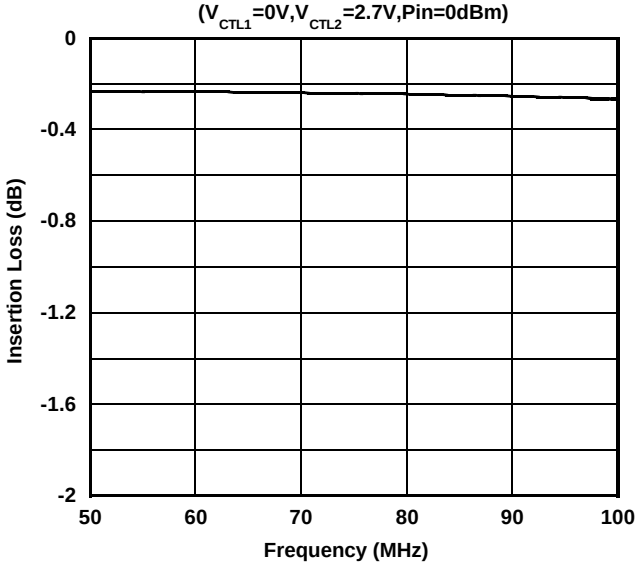
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



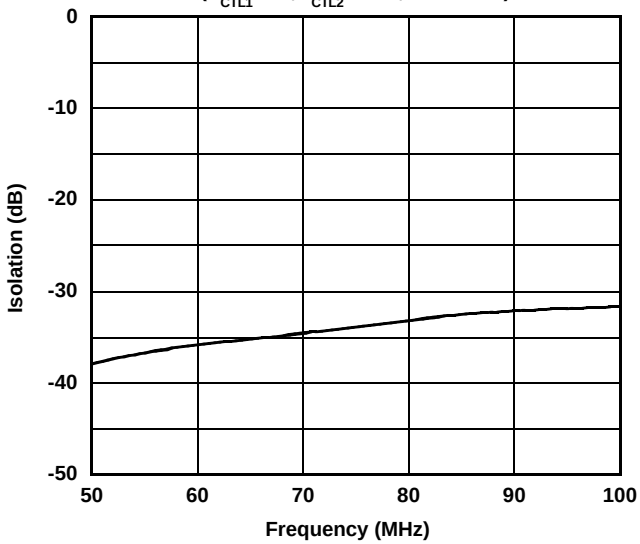
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



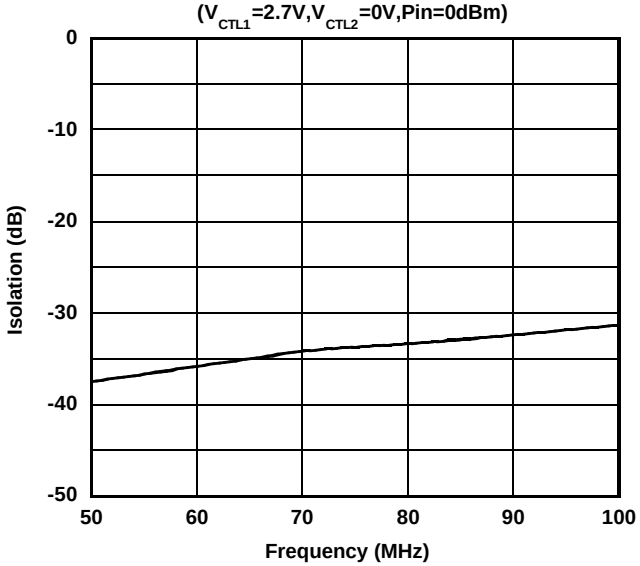
PC-P1 Isolation vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



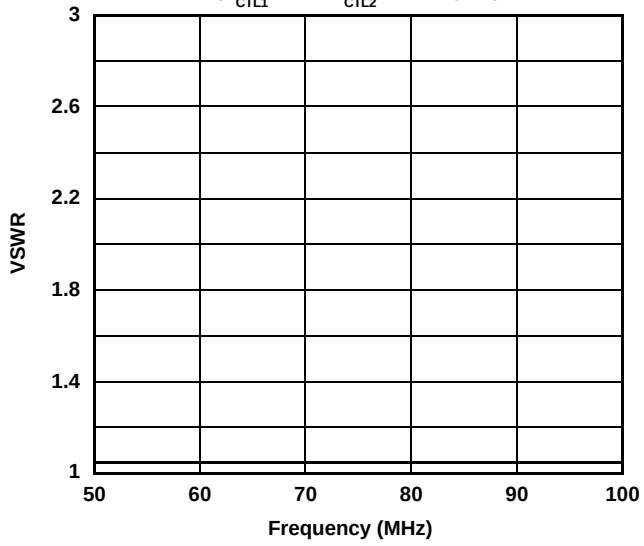
PC-P2 Isolation vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



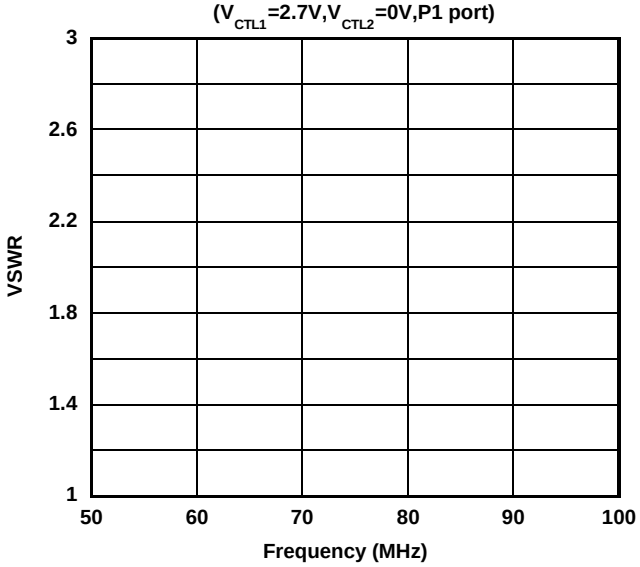
PC-P1 VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,PC port)



P1-PC,P2-PC VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,P1 port)

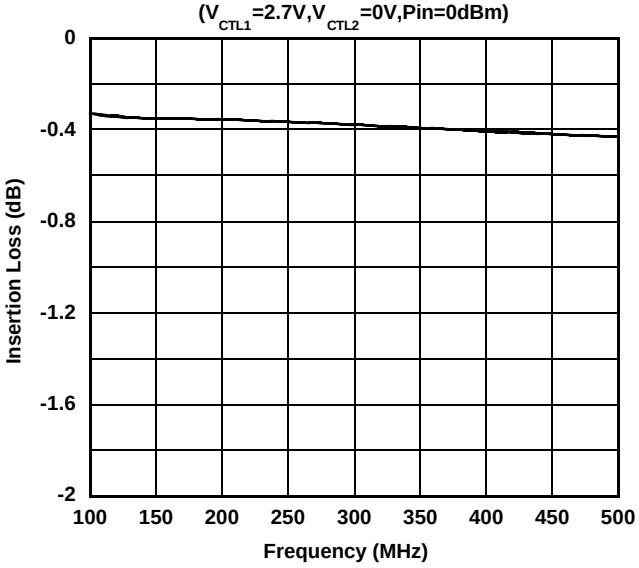


■ELECTRICAL CHARACTERISTICS

(100MHz~500MHz, with Application circuit (Parts list 2), Losses of PCB, connector and DC blocking capacitor are included)

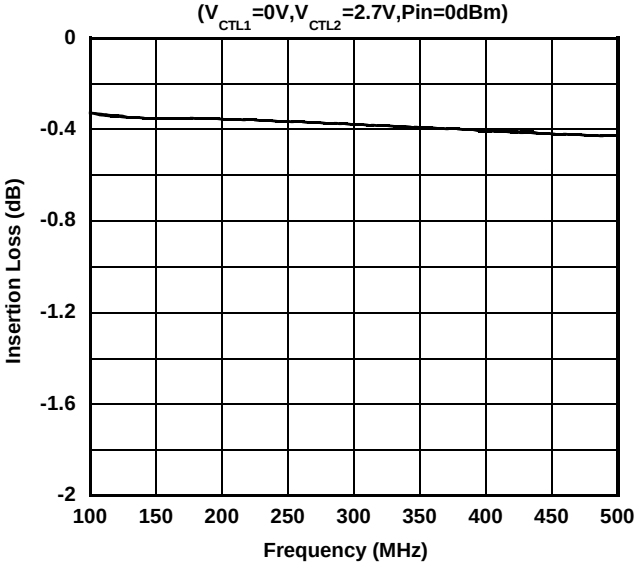
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



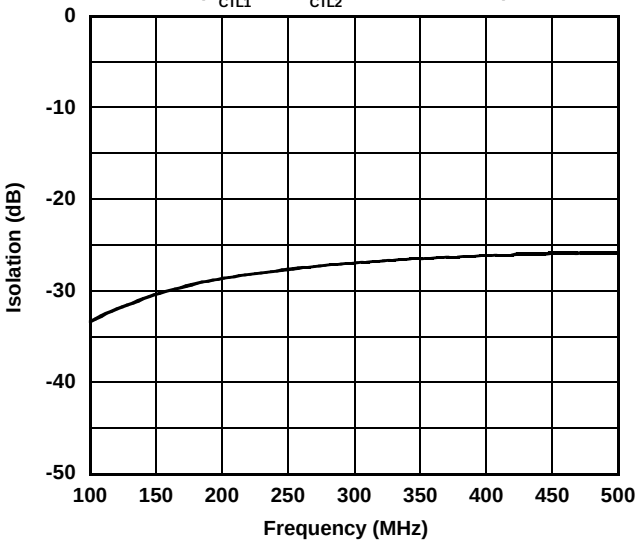
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



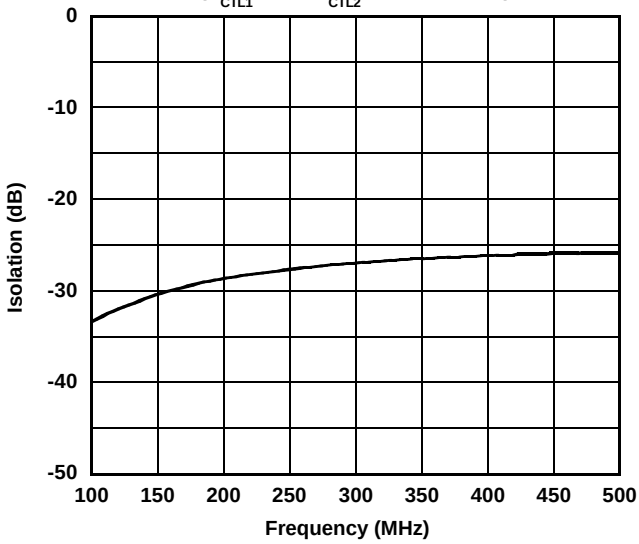
PC-P1 Isolation vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



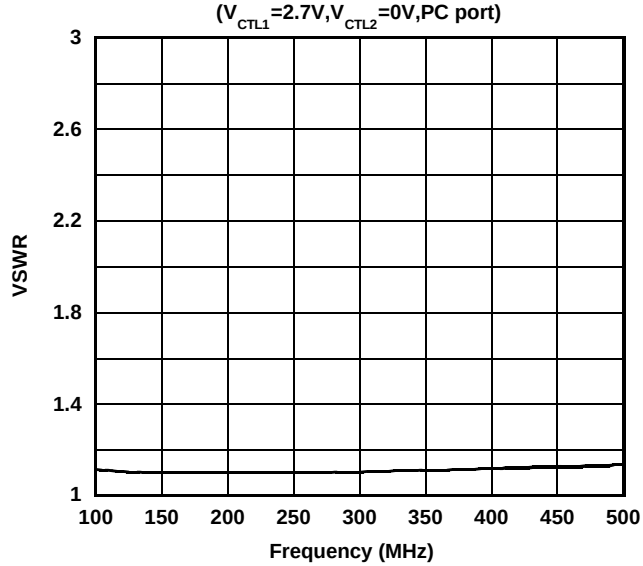
PC-P2 Isolation vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



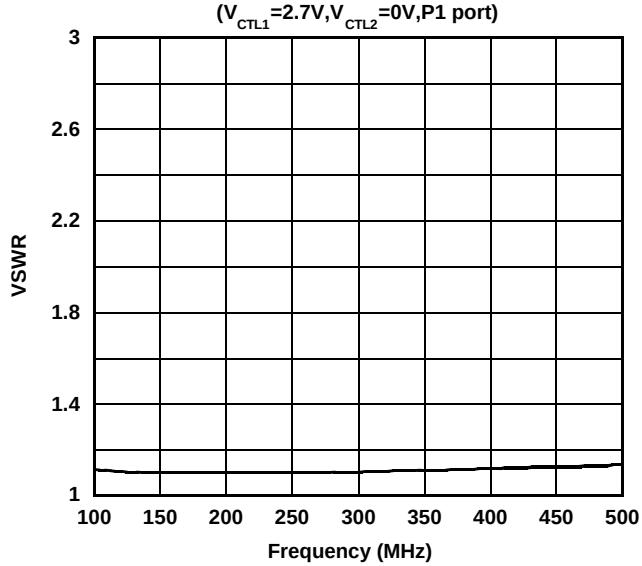
PC-P1 VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,PC port)



PC-P1,P2-PC VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,P1 port)

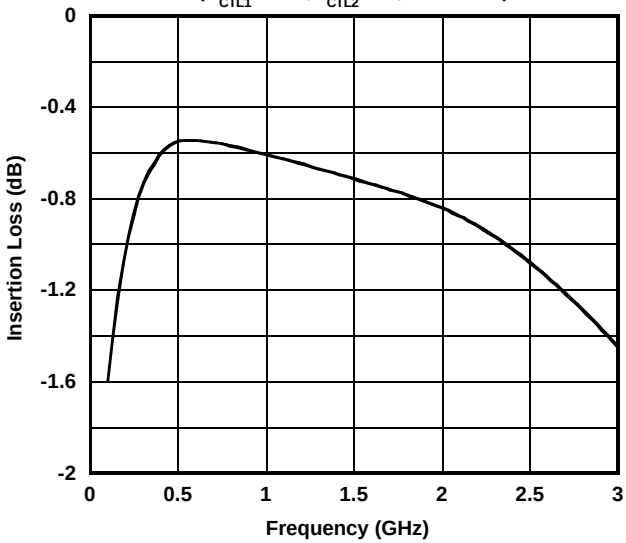


■ELECTRICAL CHARACTERISTICS

(0.1GHz~3GHz, with Application circuit (Parts list 3), Losses of PCB, connector and DC blocking capacitor are included)

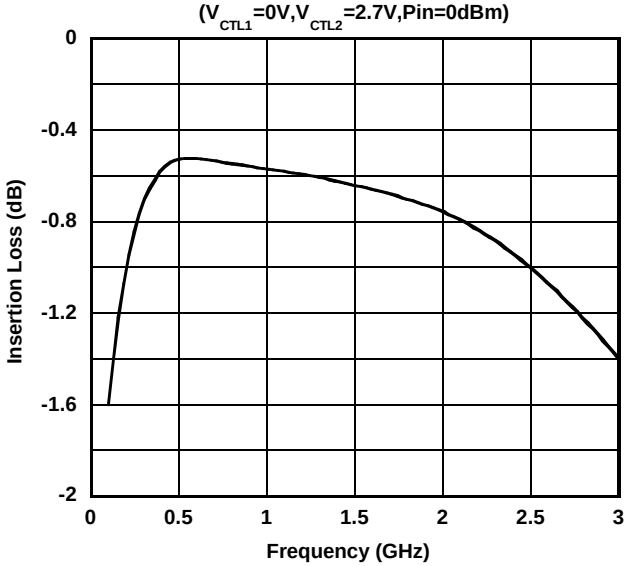
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



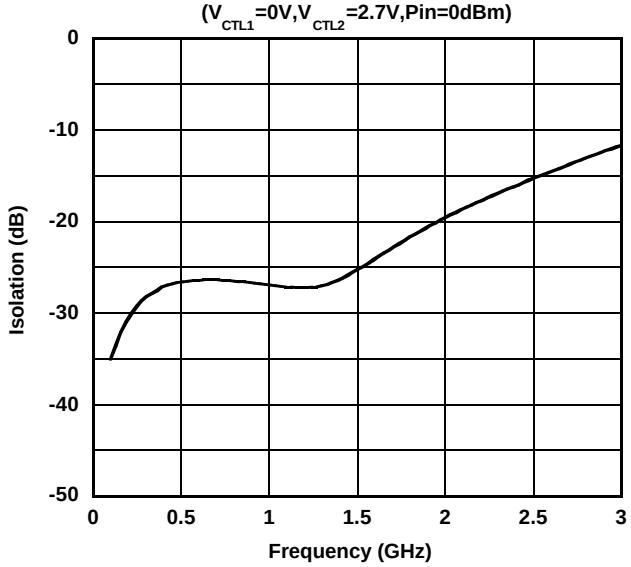
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



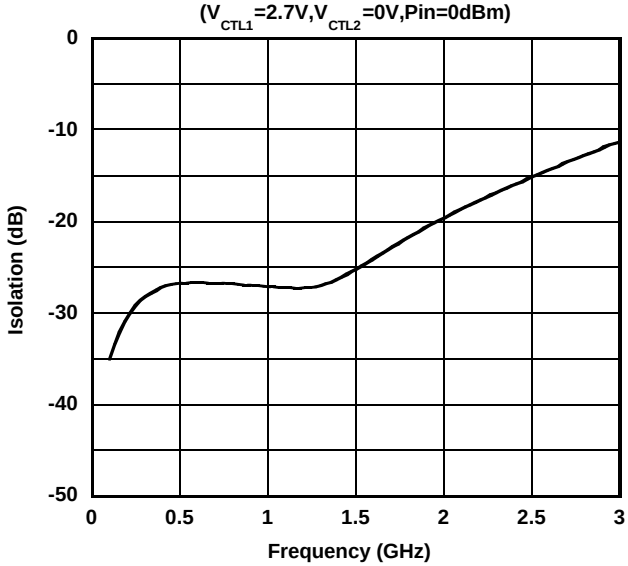
PC-P1 Isolation vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



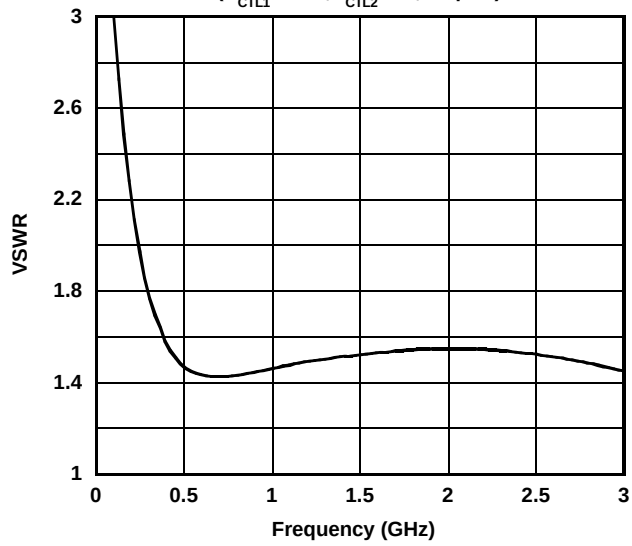
PC-P2 Isolation vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



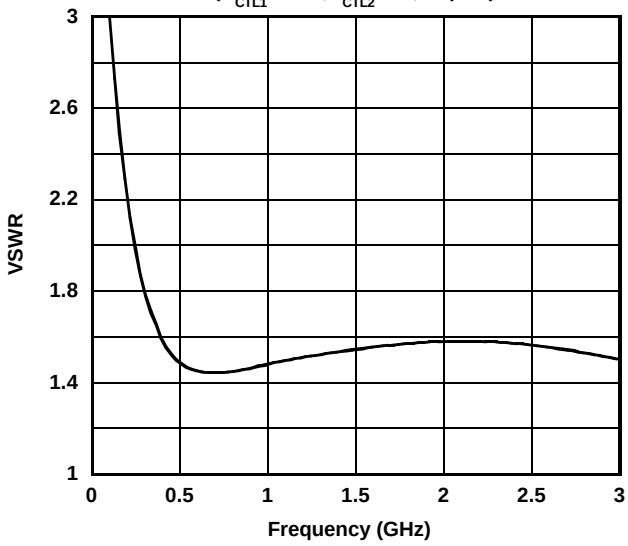
PC-P1 VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,PC port)



P1-PC,P2-PC VSWR vs. Frequency

(V_{CTL1}=2.7V,V_{CTL2}=0V,P1 port)

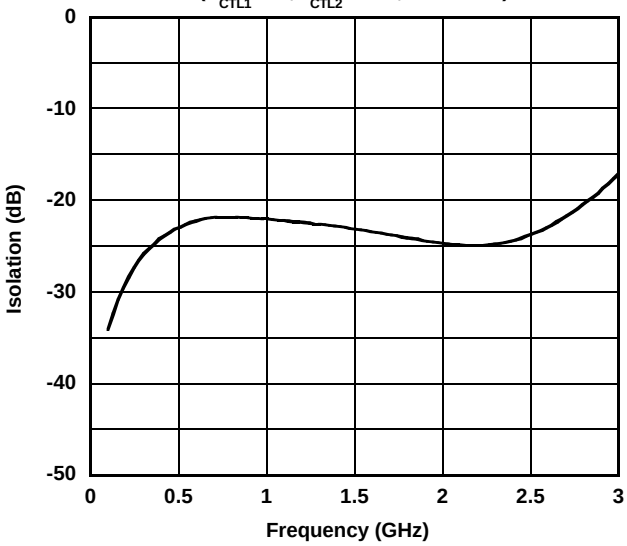


■ELECTRICAL CHARACTERISTICS

(0.1GHz~3GHz, with Application circuit (Parts list 4), Losses of PCB, connector and DC blocking capacitor are included)

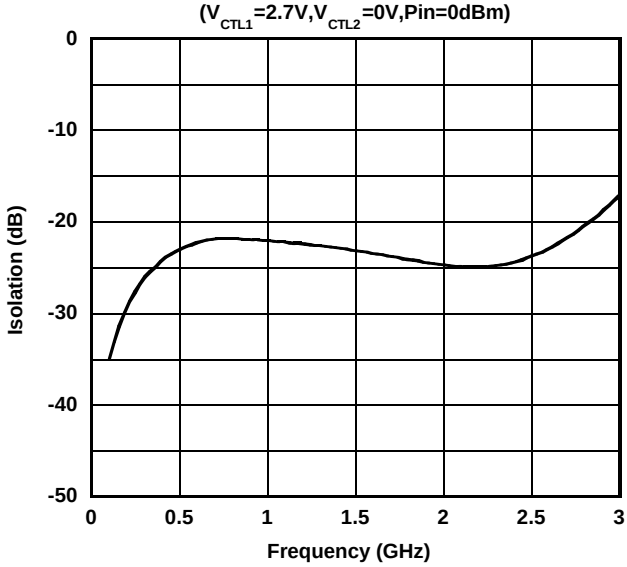
PC-P1 Isolation vs. Frequency

(V_{CTL1}=0V,V_{CTL2}=2.7V,Pin=0dBm)



PC-P2 Isolation vs. Frequency

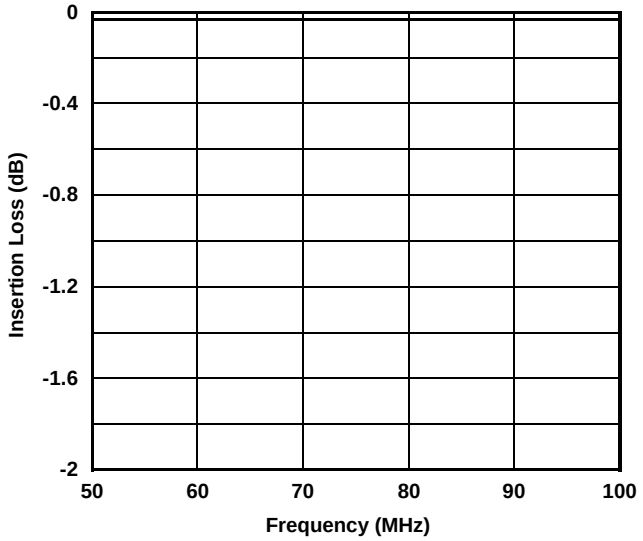
(V_{CTL1}=2.7V,V_{CTL2}=0V,Pin=0dBm)



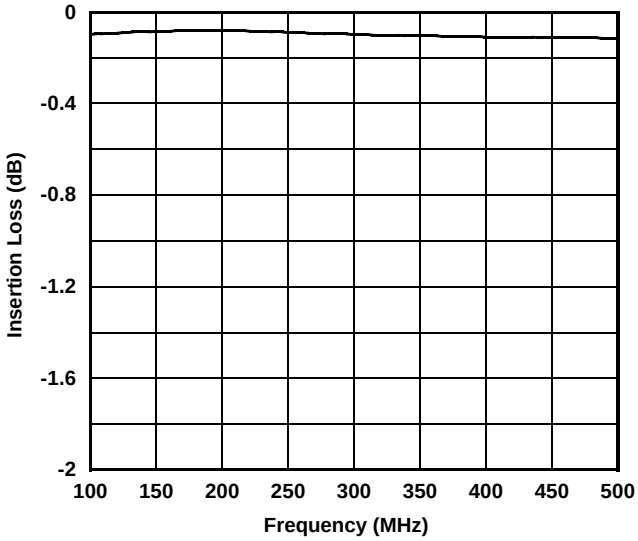
■ELECTRICAL CHARACTERISTICS

(Losses of PCB, connector and DC blocking capacitor at each frequency.)

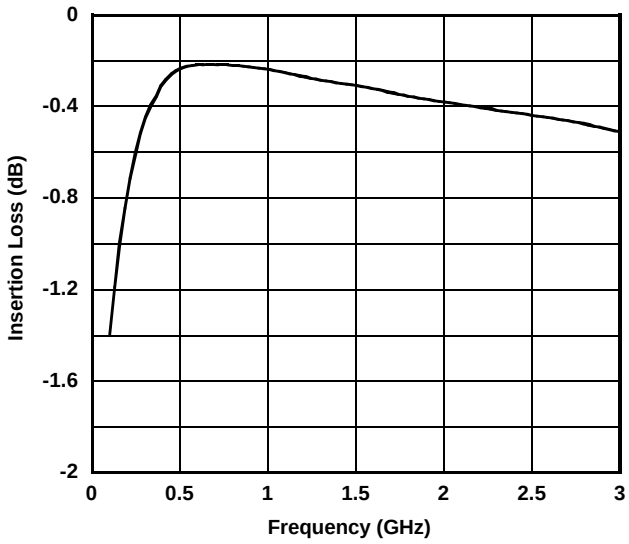
PCB Through Loss vs. Frequency
(Frequency:50MHz-100MHz)



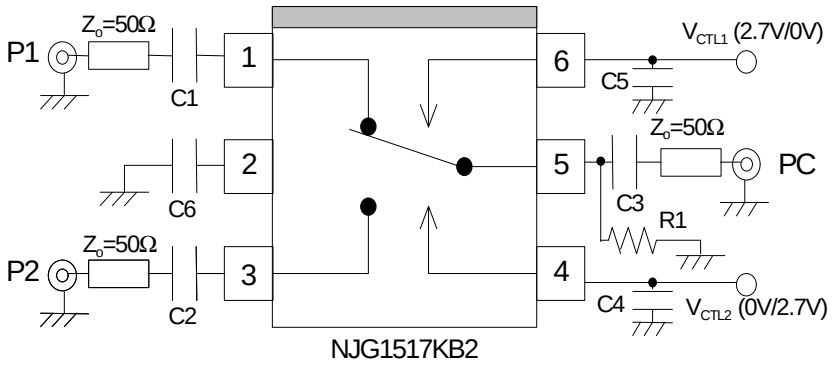
PCB Through Loss vs. Frequency
(Frequency:100MHz-500MHz)



PCB Through Loss vs. Frequency
(Frequency:100MHz-3GHz)



■APPLICATION CIRCUIT



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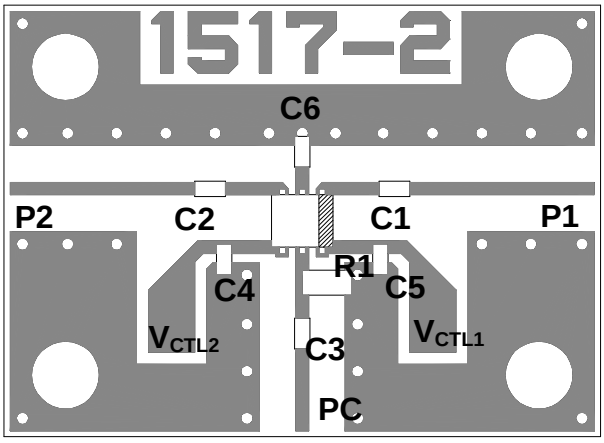
Parts List

Parts number	List 1	List 2	List 3	List 4
	fin=50~100MHz	fin=0.1~0.5GHz	fin=0.5~1.7GHz	fin=1.7~2.5GHz
C1~C3	0.01uF	1000pF	56pF	56pF
C4, C5	10pF	10pF	10pF	10pF
C6	10pF	10pF	10pF	5pF
R1	560KΩ	560KΩ	560KΩ	560KΩ

■RECOMMENDED PCB DESIGN

(TOP VIEW)



PCB SIZE=19.4x14mm
PCB: FR-4, t=0.2mm
CAPACITOR: size 1005
STRIPLINE WIDTH=0.4mm

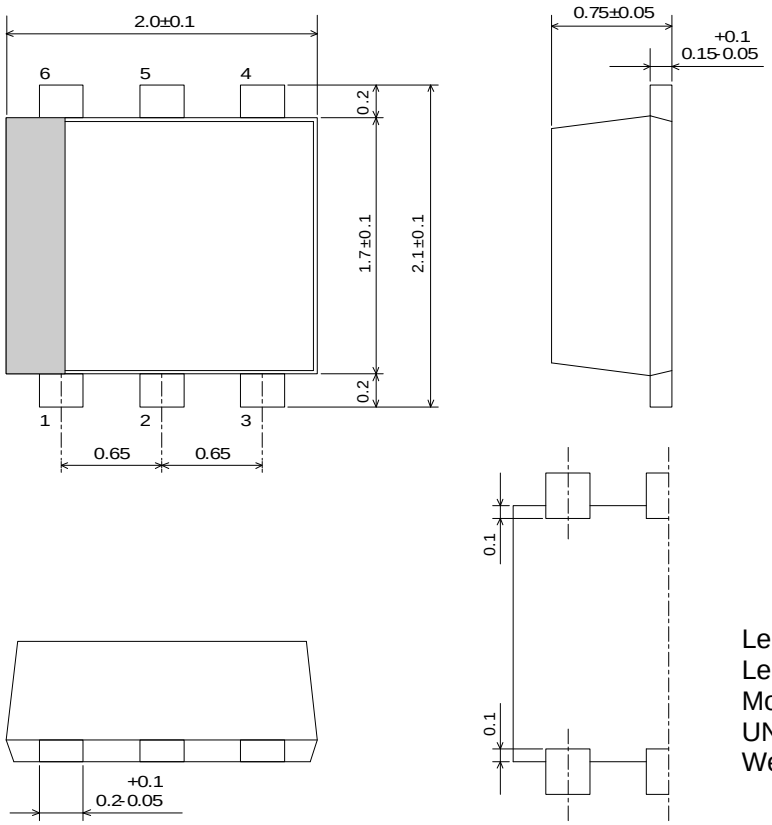
PRECAUTIONS

[1] The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC. Please choose appropriate capacitance values to the application frequency.

[2] To reduce stripline influence on RF characteristics, please locate bypass capacitors (C4, C5) close to each terminals.

[3] For good isolation, the EXTCAP terminal (2nd pin) must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.

■PACKAGE OUTLINE (FLP6-B2)



Lead material : Copper
Lead surface finish: Solder plating
Molding material : Epoxy resin
UNIT : mm
Weight : 6.5mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.