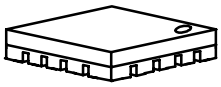
SP3T SWITCH GaAs MMIC

■GENERAL DESCRIPTION

NJG1548PC1 is a GaAs high power SP3T switch MMIC for antenna switch of tri-mode cellular phone applications such as CDMA, AMPS and PCS. This switch features low loss, high isolation, low operation current and low distortion at high input power. The SP3T switch MMIC is controlled by internal Si C-MOS decoder IC that has 2bit input signal ports.

The ultra small & ultra thin FFP16-C1 package is applied.

■PACKAGE OUTLINE



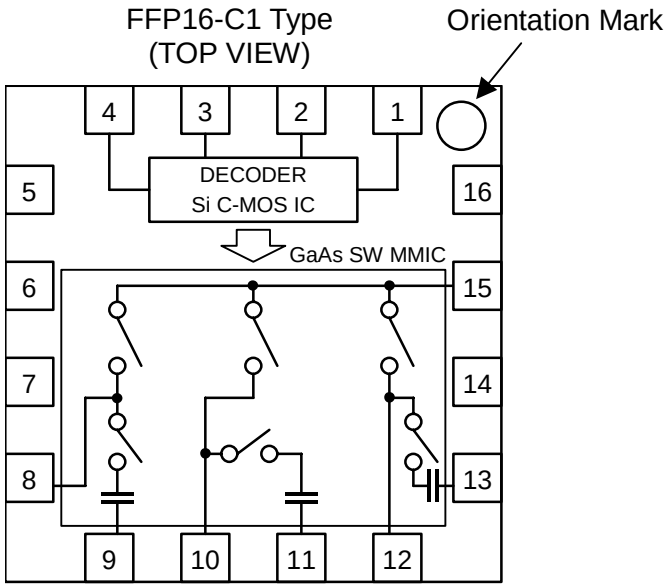
NJG1548PC1

■FEATURES

●Low voltage operation	V_{DD}=2.5V min, $V_{CTL(H)}$=1.5V min
●Pin at 0.2dB compression point	35dBm typ. @f=0.9GHz, V_{DD}=2.7V
●Low insertion loss	0.40dB typ. @f=0.9GHz, P_{IN}=25dBm, V_{DD}=2.7V
	0.50dB typ. @f=1.9GHz, P_{IN}=25dBm, V_{DD}=2.7V
●High isolation	30dB typ. @f=0.9GHz, P_{IN}=25dBm, V_{DD}=2.7V
	30dB typ. @f=1.9GHz, P_{IN}=25dBm,V_{DD}=2.7V
●Low operation current	5μA typ. @P_{IN}=25dBm, V_{DD}=2.7V
●Ultra small & ultra thin package	FFP16-C1 (Package size: 2.5 x 2.5 x 0.85mm)

■PIN CONFIGURATION

FFP16-C1 Type
(TOP VIEW)



Pin Connection

1.	GND	9.	GND
2.	CTL2	10.	RF2
3.	CTL1	11.	GND
4.	VDD	12.	RF1
5.	GND	13.	GND
6.	GND	14.	GND
7.	GND	15.	ANT
8.	RF3	16.	GND

■TRUTH TABLE

CTL1	CTL2	Path
H	L	ANT-RF1
L	H	ANT-RF2
H	H	ANT-RF3

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

NOTE: Please note that any information on this catalog is subject to change.

■ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD}=2.7V	36	dBm
Supply Voltage	V_{DD}	VDD Terminal	6.0	V
Control Voltage	V_{CTL}	CTL1 and CTL2 Terminals	6.0	V
Power Dissipation	P_D	At on PCB board	400	mW
Operating Temperature	T_{opr}		-40~+85	°C
Storage Temperature	T_{stg}		-55~+150	°C

■ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operation Voltage	V_{DD}		2.5	2.7	5.0	V
Operating Current	I_{DD}	P_{IN}=25dBm	-	5.0	30	μA
Control Voltage (Low)	$V_{CTL\ (L)}$		0	-	0.4	V
Control Voltage (High)	$V_{CTL\ (H)}$		1.5	2.7	V_{DD}	V
Control Current	I_{CTL}		-1.0	-	1.0	μA
Insertion Loss 1	LOSS1	f=0.9GHz, P_{IN}=25dBm	-	0.40	0.55	dB
Insertion Loss 2	LOSS2	f=1.9GHz, P_{IN}=25dBm	-	0.50	0.65	dB
Isolation 1	ISL1	f=0.9GHz, P_{IN}=25dBm	25	30	-	dB
Isolation 2	ISL2	f=1.9GHz, P_{IN}=25dBm	25	30	-	dB
Pin at 0.2dB Compression Point1	$P_{-0.2dB}$(1)	f=0.9GHz	32.5	35	-	dBm
Pin at 0.2dB Compression Point2	$P_{-0.2dB}$(2)	f=1.9GHz	32.5	35	-	dBm
2nd Harmonics 1	2fo(1)	f=0.9GHz, P_{IN}=25dBm	-	-71	-60	dBc
2nd Harmonics 2	2fo(2)	f=1.9GHz, P_{IN}=25dBm	-	-75	-60	dBc
3rd Harmonics 1	3fo(1)	f=0.9GHz, P_{IN}=25dBm	-	-75	-60	dBc
3rd Harmonics 2	3fo(2)	f=1.9GHz, P_{IN}=25dBm	-	-75	-60	dBc
Input 3rd order Intercept Point 1	IIP3(1)	f=0.9+0.901GHz, Pin=25dBm *1	+55	+60	-	dBm
Input 3rd order Intercept Point 2	IIP3(2)	f=1.9+1.901GHz, Pin=25dBm *1	+55	+60	-	dBm
VSWR	$VSWR_i$	on-state ports, f=1.9GHz	-	1.2	1.4	
Switching Time	T_{SW}		-	0.35	-	μs

*1: The input IP3 is defined as following equation.
IIP3=(3 x Pout - IM3) / 2 + LOSS

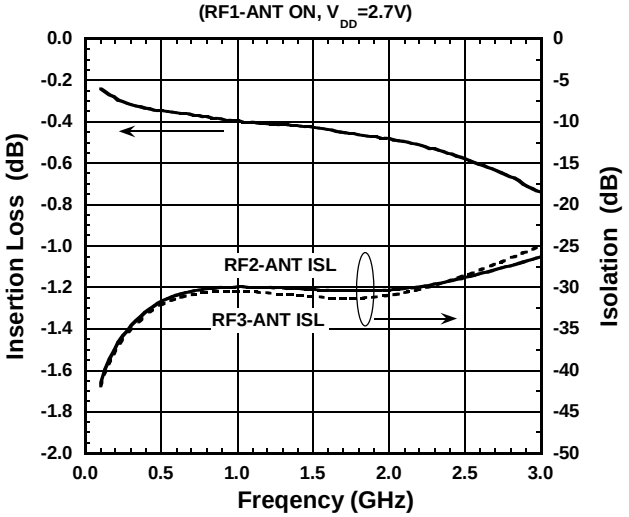
■TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1, 4, 5, 6 7, 9, 11, 13, 14,16	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
15	ANT	RF port for Tx/Rx signal. An external capacitor is required to block the DC bias voltage (V_{DD}).
2	CTL2	Control signal input terminal of high impedance C-MOS. High level: +1.5V~VDD, Low level: 0~0.4V. Please connect this terminal to GND or VDD portion by 100kΩ resistor if the voltage level of this terminal is undefined.
3	CTL1	Control signal input terminal of high impedance C-MOS. High level: +1.5V~VDD, Low level: 0~0.4V. Please connect this terminal to GND or VDD portion by 100kΩ resistor if the voltage level of this terminal is undefined.
4	VDD	Positive power supply terminal. The positive voltage (+2.5~+5.0V) has to be supplied with or before other DC voltage supply terminal to avoid latch up effect.
8	RF3	RF port. To block the DC bias voltage of internal circuit, an external capacitor is required.
10	RF2	RF port. To block the DC bias voltage of internal circuit, an external capacitor is required.
12	RF1	RF port. To block the DC bias voltage of internal circuit, an external capacitor is required.

■ **ELECTRICAL CHARACTERISTICS** (with application circuit, Losses of external circuit are excluded)

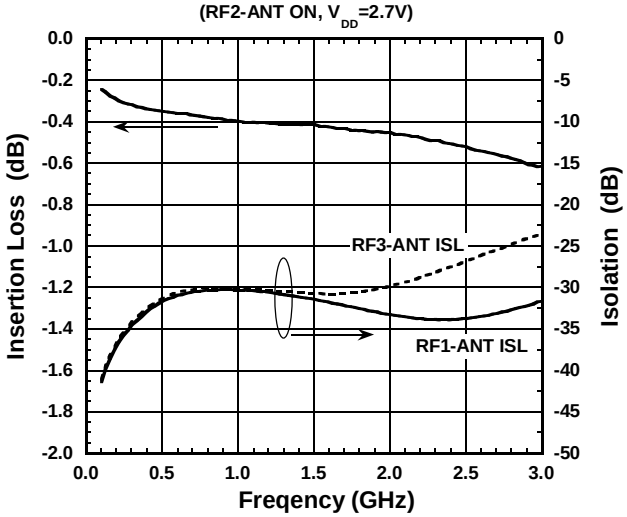
Loss, ISL vs. Frequency

(RF1-ANT ON, V_{DD}=2.7V)



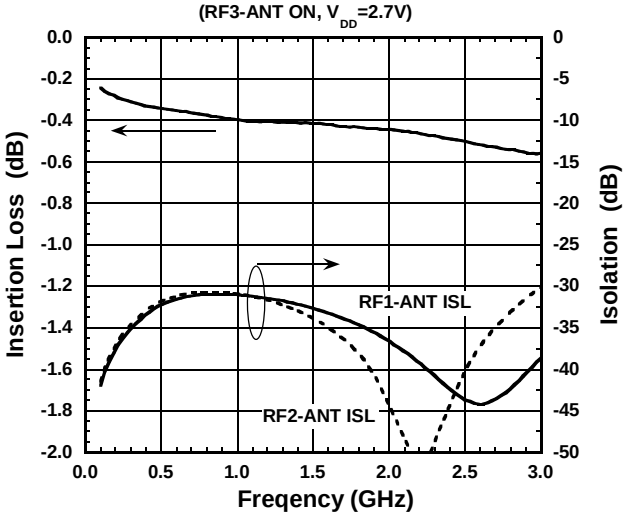
Loss, ISL vs. Frequency

(RF2-ANT ON, V_{DD}=2.7V)



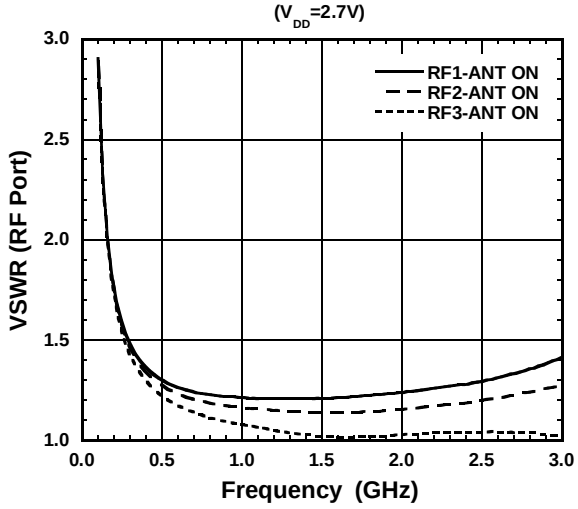
Loss, ISL vs. Frequency

(RF3-ANT ON, V_{DD}=2.7V)



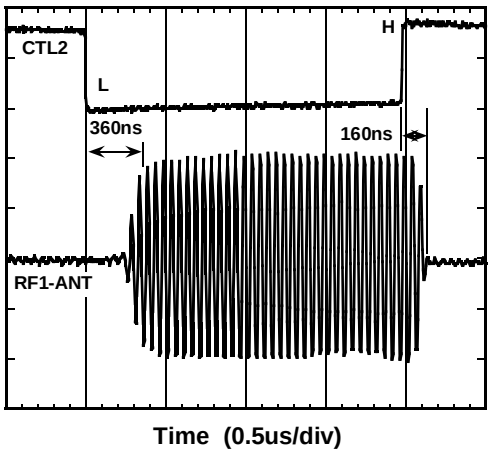
VSWR vs Frequency

(V_{DD}=2.7V)



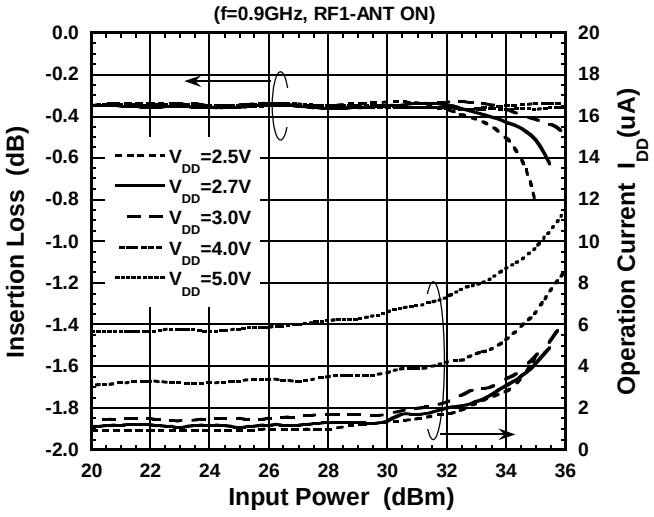
Switching Time

(V_{DD}=2.7V, CTL1=2.7V)

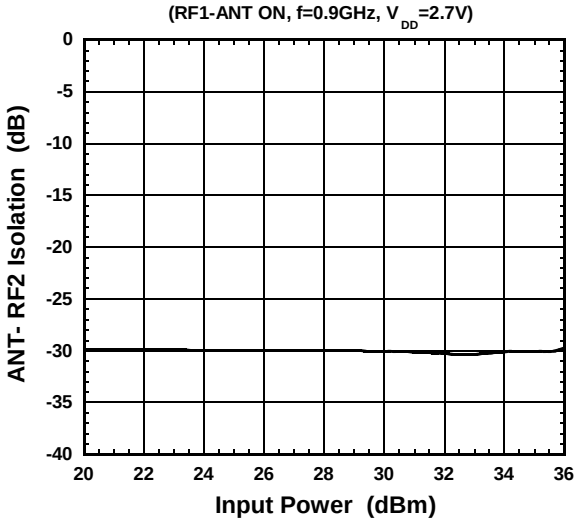


■ **ELECTRICAL CHARACTERISTICS** (with application circuit, Losses of external circuit are excluded)

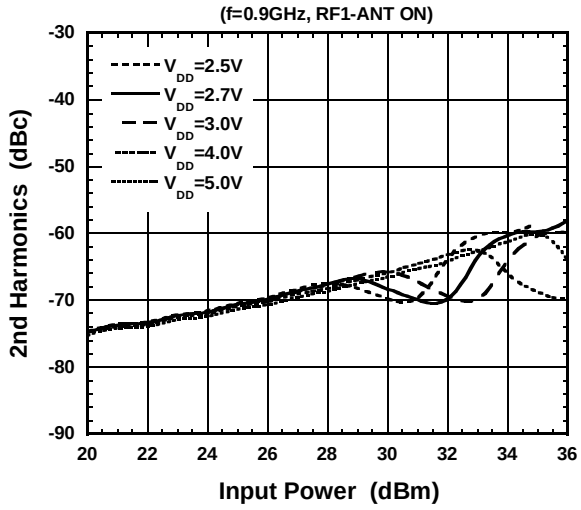
Loss, I_{DD} vs Input Power



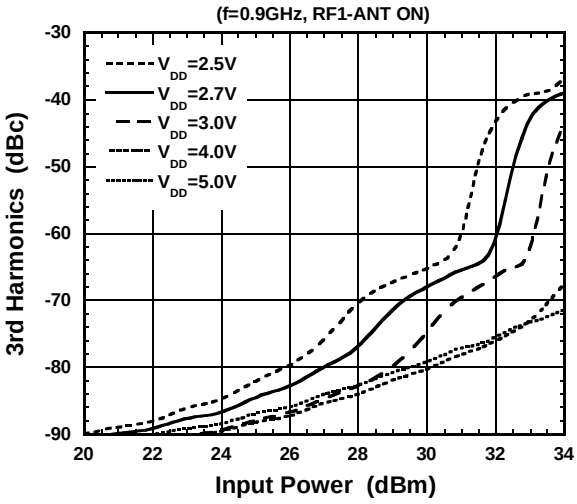
Isolation vs Input Power



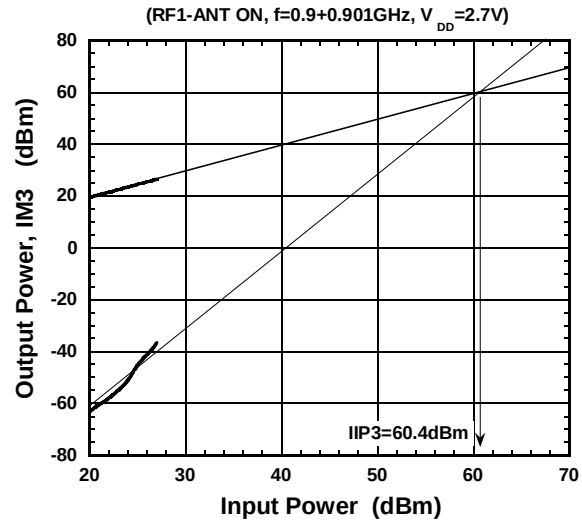
2nd Harmonics vs Input Power



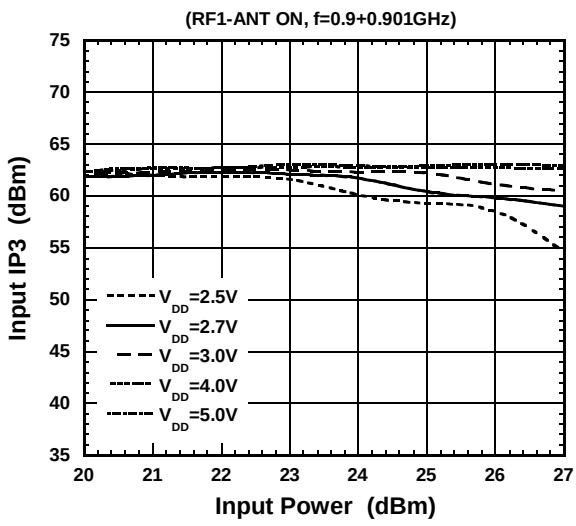
3rd Harmonics vs Input Power



Output Power, IM3 vs Input Power



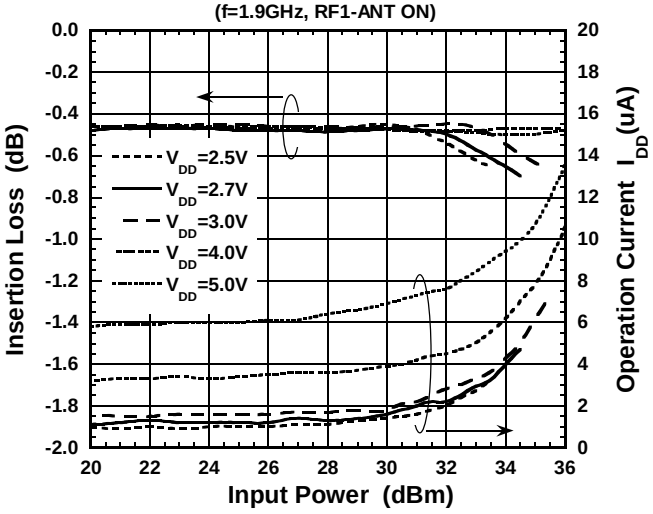
IIP3 vs Input Power



■ **ELECTRICAL CHARACTERISTICS** (with application circuit, Losses of external circuit are excluded)

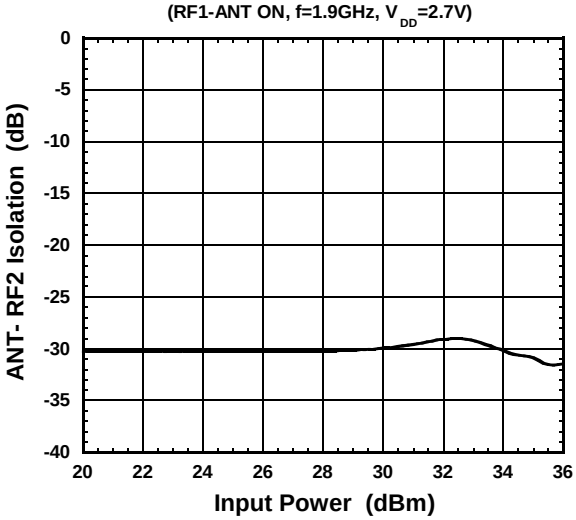
Loss, I_{DD} vs Input Power

(f=1.9GHz, RF1-ANT ON)



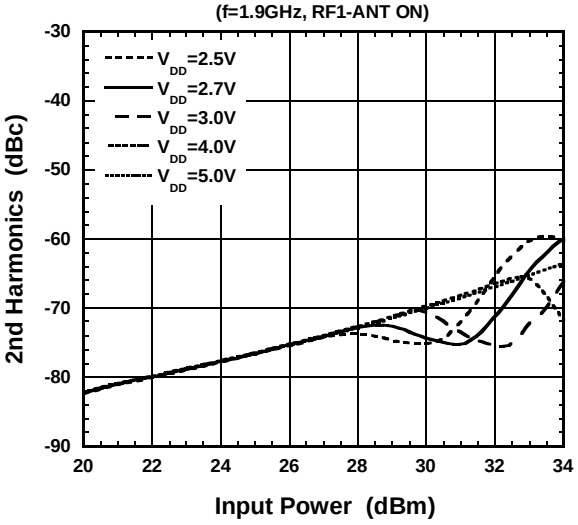
Isolation vs Input Power

(RF1-ANT ON, f=1.9GHz, V_{DD}=2.7V)



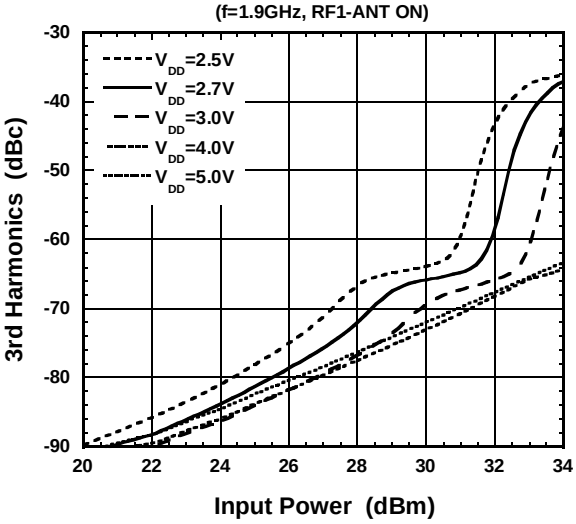
2nd Harmonics vs Input Power

(f=1.9GHz, RF1-ANT ON)



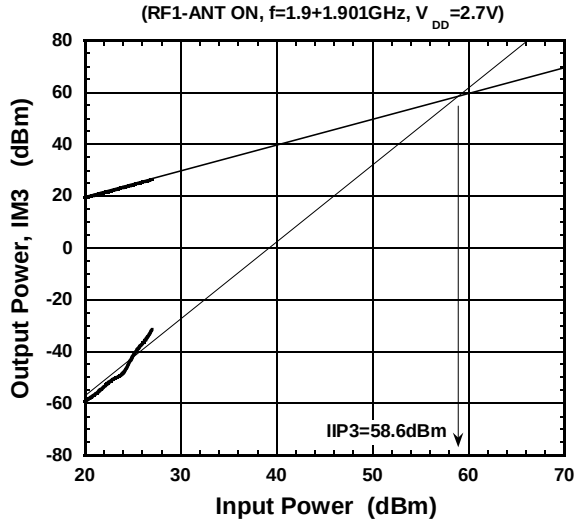
3rd Harmonics vs Input Power

(f=1.9GHz, RF1-ANT ON)



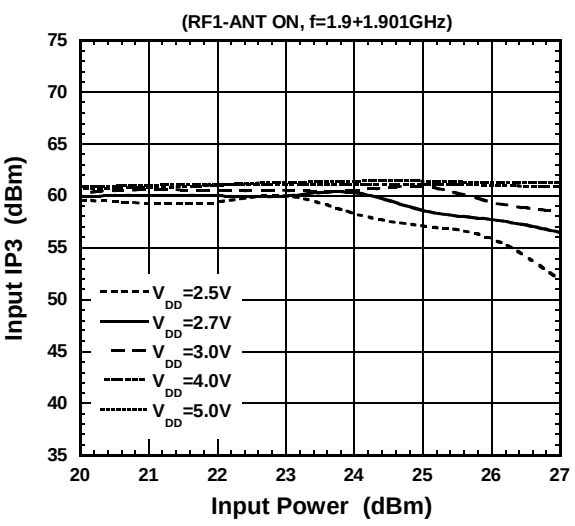
Output Power, IM3 vs Input Power

(RF1-ANT ON, f=1.9+1.901GHz, V_{DD}=2.7V)



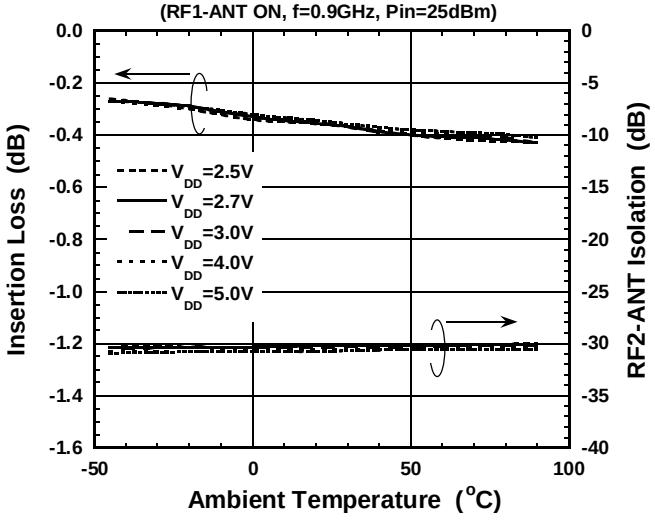
IIP3 vs Input Power

(RF1-ANT ON, f=1.9+1.901GHz)

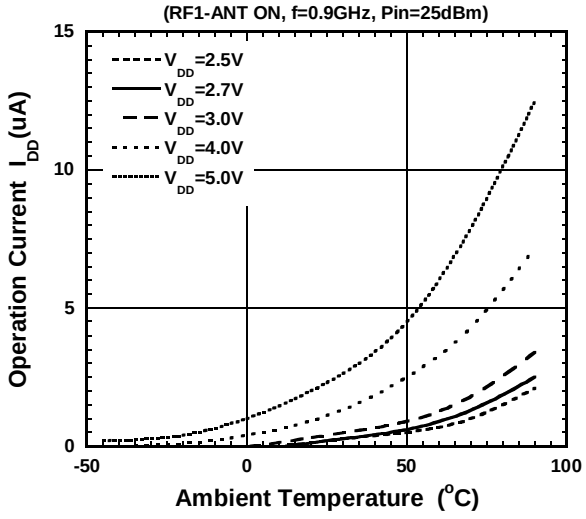


■ **ELECTRICAL CHARACTERISTICS** (with application circuit, Losses of external circuit are excluded)

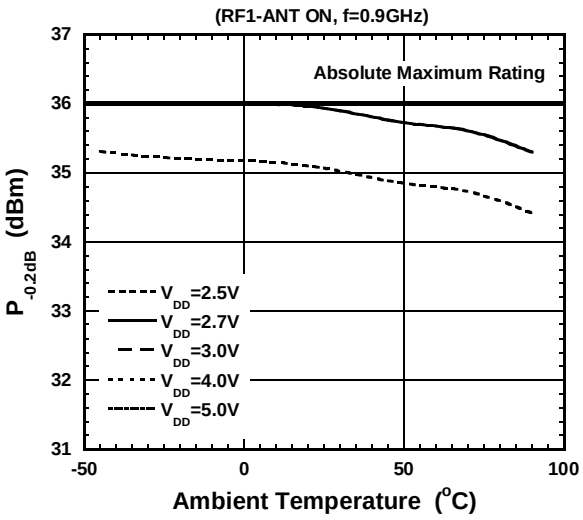
Loss, ISL vs Ambient Temperature



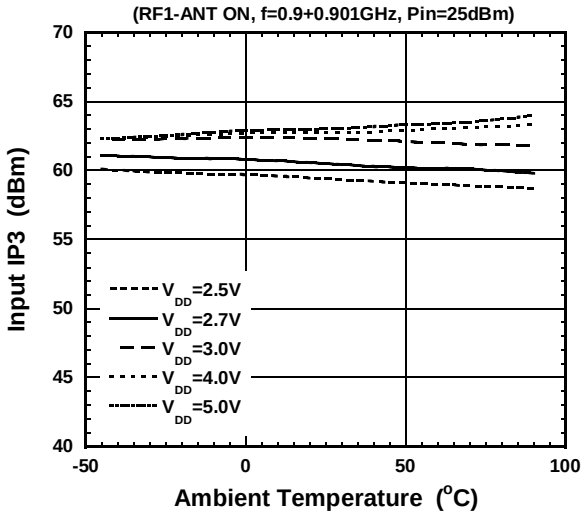
I_{DD} vs Ambient Temperature



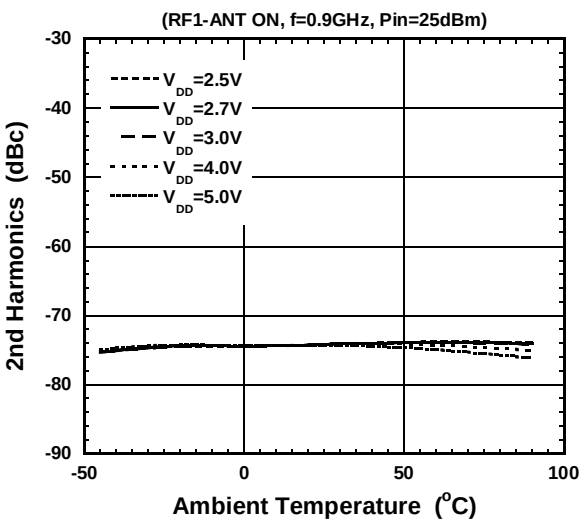
$P_{-0.2dB}$ vs Ambient Temperature



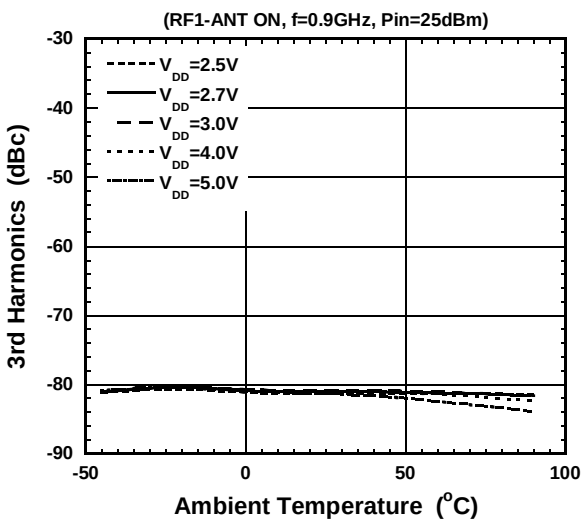
IIP3 vs Ambient Temperature



$2f_0$ vs Ambient Temperature

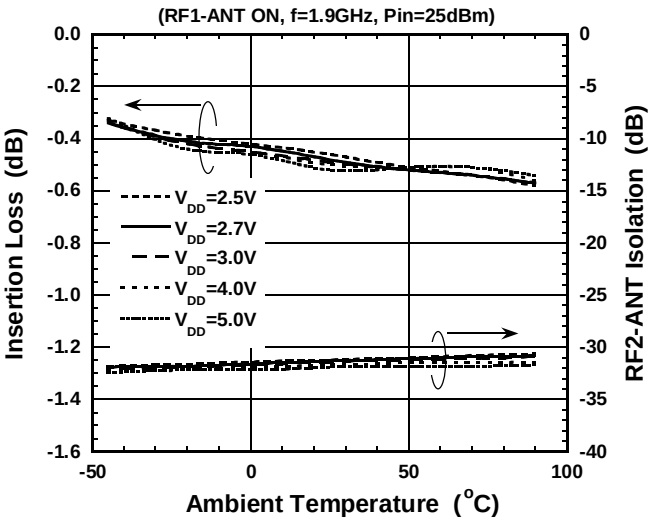


$3f_0$ vs Ambient Temperature

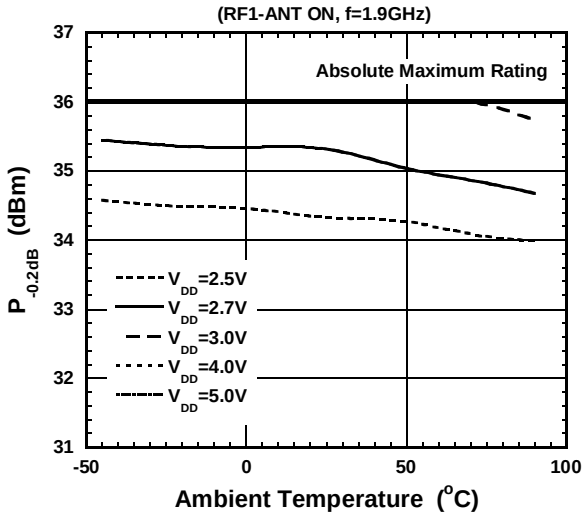


■ **ELECTRICAL CHARACTERISTICS** (with application circuit, Losses of external circuit are excluded)

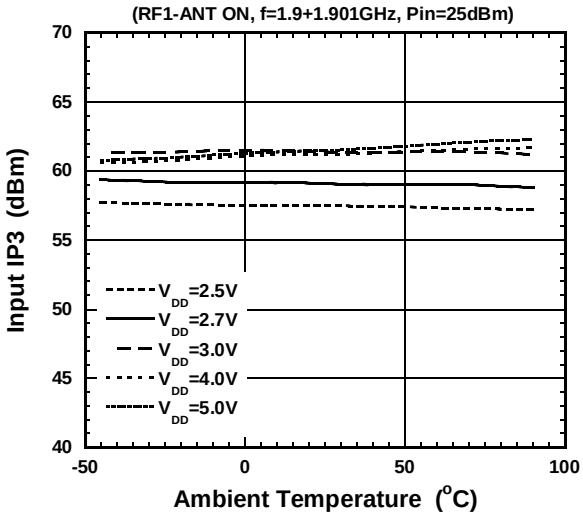
Loss, ISL vs Ambient Temperature



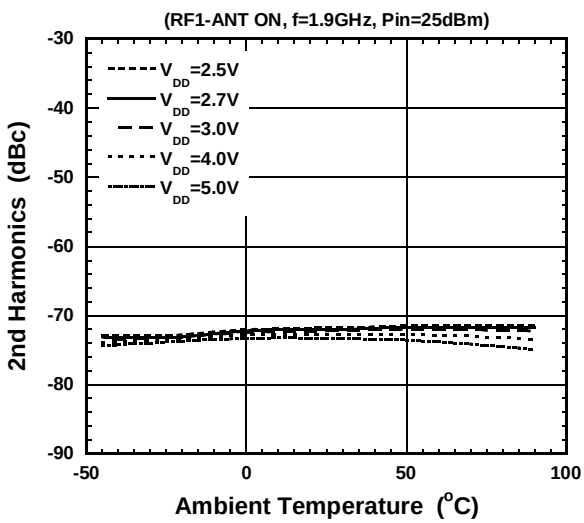
$P_{-0.2dB}$ vs Ambient Temperature



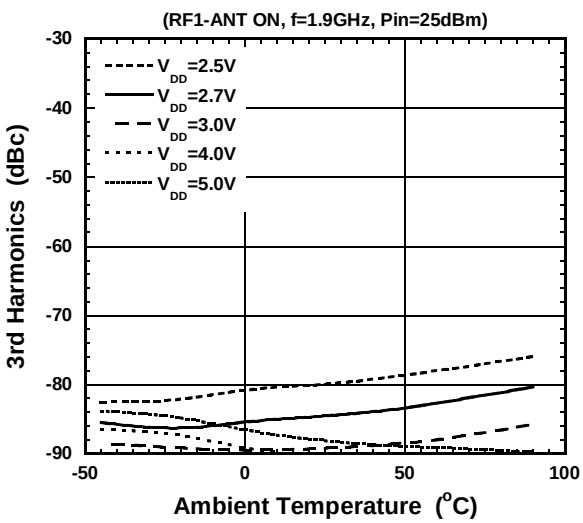
IIP3 vs Ambient Temperature



$2f_0$ vs Ambient Temperature

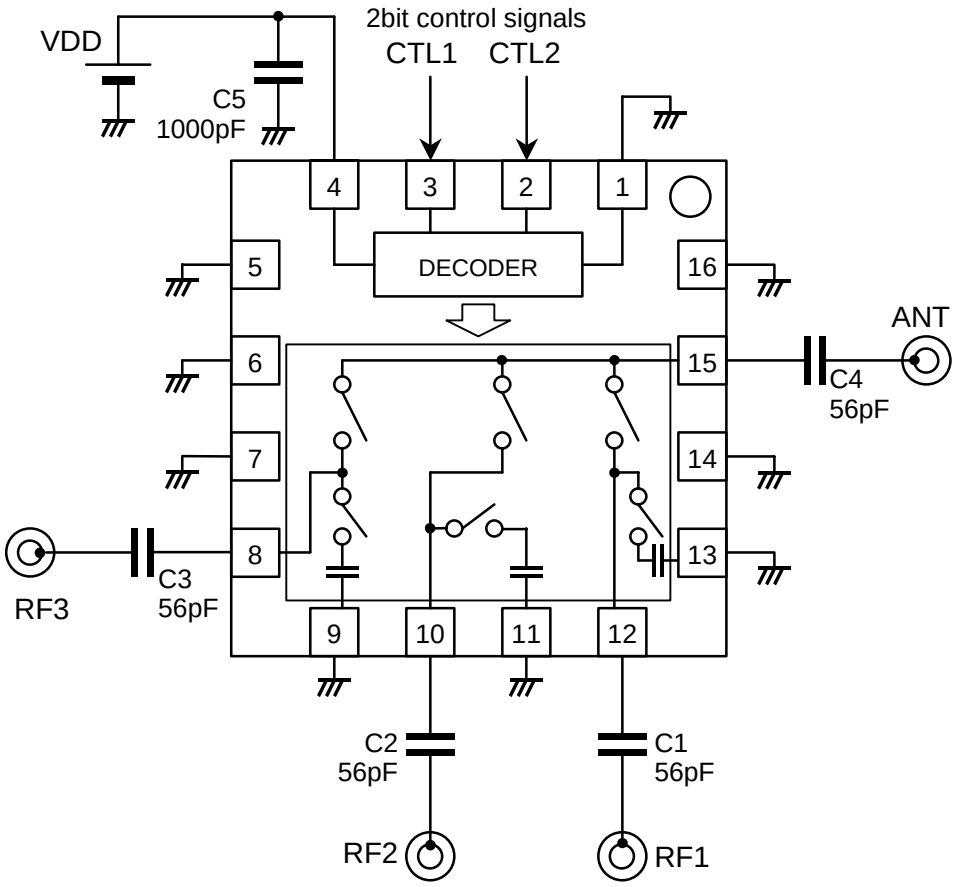


$3f_0$ vs Ambient Temperature

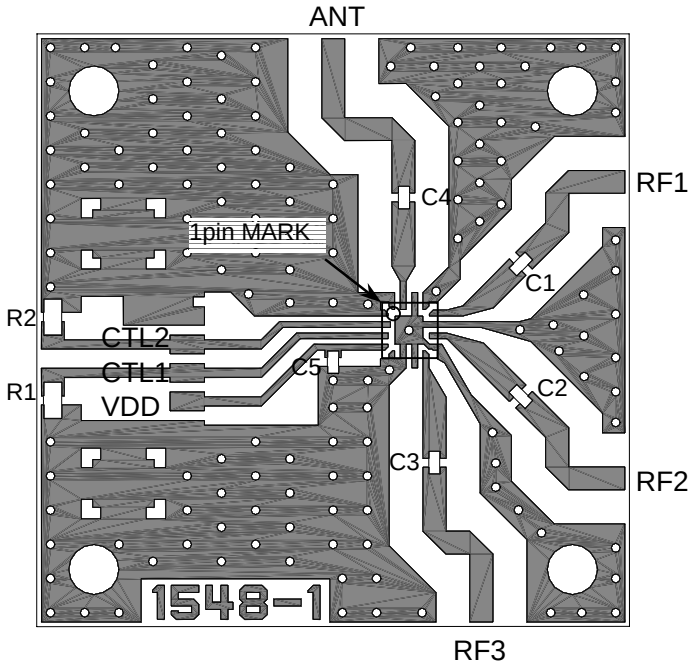


■ APPLICATION CIRCUIT

(TOP VIEW)



■ RECOMMENDED PCB DESIGN



PCB SIZE = 26 x 26 mm
PCB: FR4, t=0.5mm
CAPACITOR: size 1005
STRIP LINE WIDTH = 1mm(Z_o=50Ω)

■ PARTS LIST

Parts	Value	Notes
C1~C4	56pF	MURATA (GRM15)
C5	1000pF	
R1, R2 (*1)	100kΩ	

(*1) If the voltage level of CTL1/CTL2 is unstable, please connect R1, R2 with GND or VDD respectively.

■ BOARD TOTAL LOSS

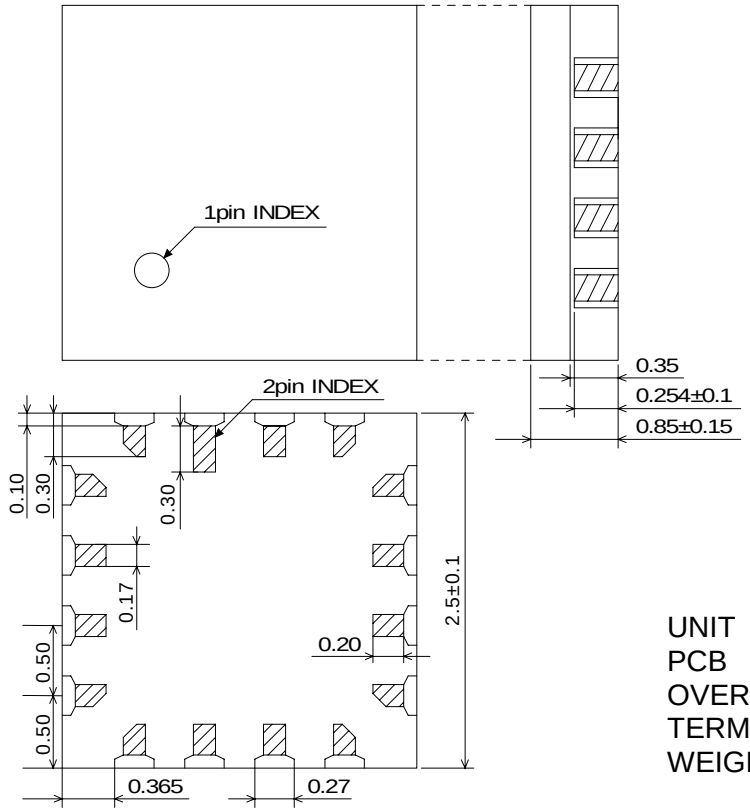
(DC blocking capacitor, Connector and PCB)

Pass	0.9GHz	1.9GHz
RF1-ANT RF2-ANT RF3-ANT	0.18dB	0.27dB

■ PRECAUTIONS

[1] DC blocking capacitors have to be placed at ANT, RF1, RF2 and RF3 terminals.
[2] To reduce strip line influence on RF characteristics, please locate bypass capacitor (C5) close to VDD terminal.
[3] To avoid degradation of isolation or high power characteristics, please GND terminals (1, 5, 6, 7, 9, 11, 13, 14, 15) must be placed close to grand plane of substrate and through holes for GND should be placed near by the pin connection.

■PACKAGE OUTLINE (FFP16-C1)



UNIT	: mm
PCB	: Ceramic
OVER COAT	: Epoxy resin
TERMINAL TREAT	: Au
WEIGHT	: 15mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.